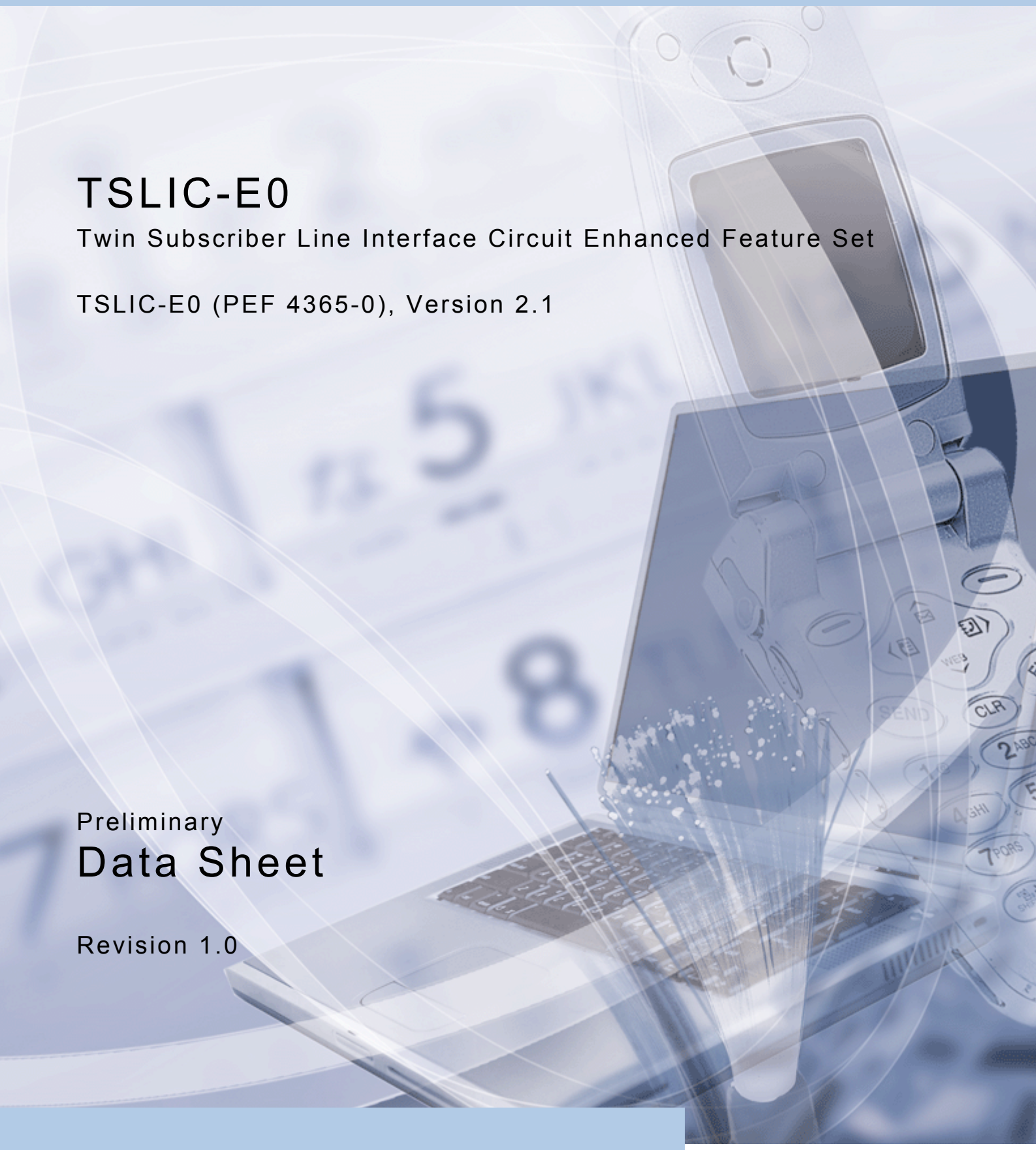
February 2007

TSLIC-E0

Twin Subscriber Line Interface Circuit Enhanced Feature Set

TSLIC-E0 (PEF 4365-0), Version 2.1



Preliminary

Data Sheet

Revision 1.0

Communication Solutions

Never stop thinking

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PEF 4365-0, Twin Subscriber Line Interface Circuit Enhanced Feature Set

Revision History: 2007-02-13, Revision 1.0

Previous Version: none

Page	Subjects (major changes since last revision)

Trademarks

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1 General Description

Infineon Technologies' new dual-channel high voltage ringing Subscriber Line Interface Circuit TSLIC-E0 (PEF 4365-0) **V2.1** is the latest out of the well-known and broadly used SLIC-E family. It has been designed not only to cover all previous TSLIC-E0 applications, but also for particular "ADSL friendliness" and thus it enables the realization of highly cost optimized integrated voice data (IVD) systems. Special effort has been put on minimizing the influence of line voltage transients and distortions caused by mode transitions and the associated unavoidable impedance changes.

TSLIC-E0 V2.1 can be operated with all codec devices of the DuSLIC® or VINETIC® chip sets. The highly flexible device offers 3.3 V compatibility and integrated balanced ringing up to 85 V_{rms}, utilizing a positive auxiliary supply voltage. With TSLIC-E0, an additional integrated supply switch allows the choice between two negative battery voltages.

A power-down mode helps to minimize the average system power dissipation: the transmission part is switched off completely and off-hook supervision is provided by activating a simple line current sensor with negligible power consumption.

TSLIC-E0 V2.1 is available in a PG-DSO-36-15 package (heat-slug down).

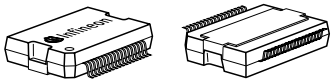
1.1 Version 2.1: Summary of Changes

Compared with the previous version (V1.2) of TSLIC-E0, the new version V2.1 is characterized by the following changes:

- Improved high-frequency noise and distortion performance
- Optimized mode transitions to minimize influence on ADSL data in IVD systems
- Compatible with both 3.3 and 5 V VDD supplies
- High impedance DC inputs
- Fully differential receive path - VCMS pin not required
- Fast current limitation for improved overvoltage behaviour
- Application circuit:
  - 100 nF / 50 V capacitor at CEXT
  - Per channel series diode in VBATL supply mandatory (no shared diodes)

Version 2.1

1.2 Features



PG-DSO-36-15

- Dual-channel “ADSL-friendly” high voltage SLIC with integrated ringing
- Compatible with both 3.3 and 5 V systems
- High-voltage line feed (long loop driving capability)
- Sensing of transversal and longitudinal line currents
- Two negative Battery voltages
- Positive ring supply voltage up to +85 V
- Total supply voltage up to 150 V
- Integrated balanced ringing up to 85 V_{rms}
- Integrated test mode (ACTH-R)
- Power-saving active mode (ACTL) with reduced battery voltage
- Power Down mode with negligible power consumption
- PG-DSO-36-15 package
- Reliable Smart Power Technology (SPT170)

Product Name	Product Type	Package
TSLIC-E0	PEF 4365-0 T	PG-DSO-36-15

1.3 Logic Symbol

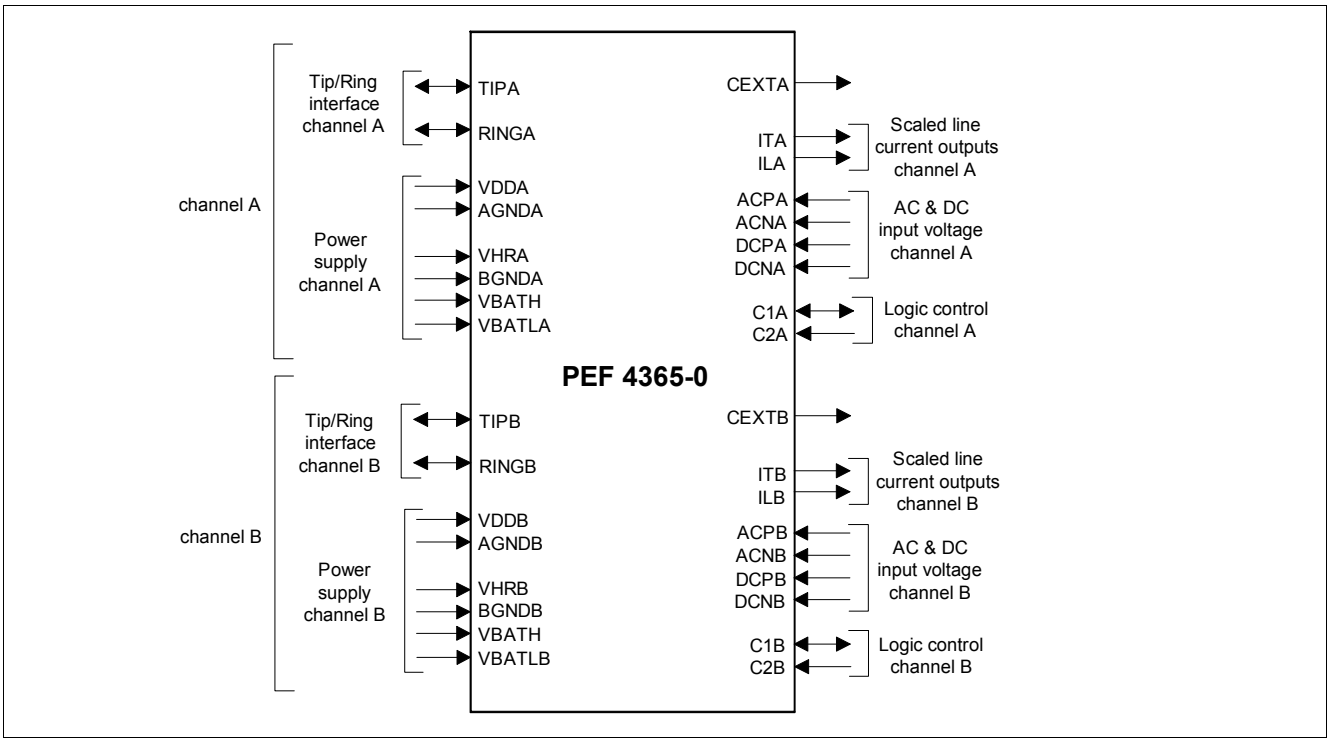


Figure 1 Logic Symbol TSLIC-E0 (PEF 4365-0)

1.4 Pin Configuration

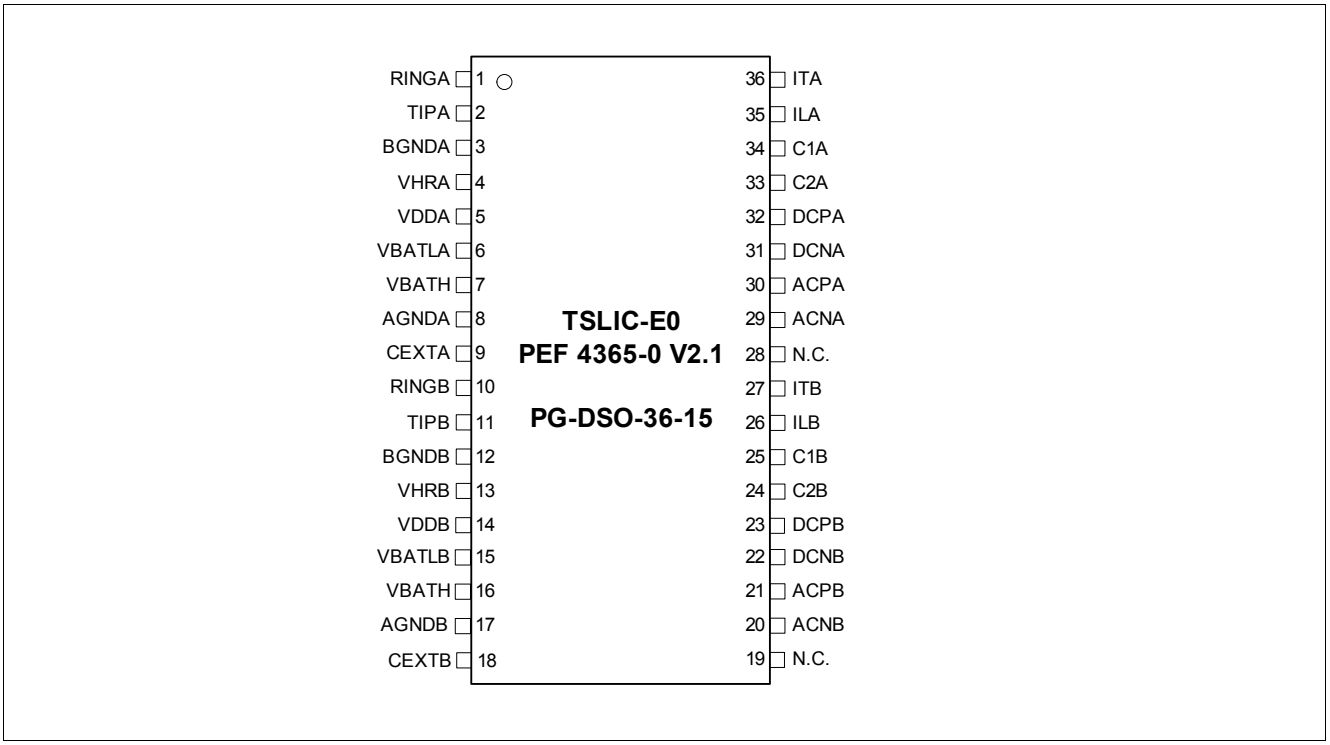


Figure 2 Pin Configuration TSLIC-E0

1.5 Pin Definitions and Functions

Table 1 Pin Definitions and Functions TSLIC-E0

Pin No. TSLIC-E0	Name	Pin Type	Function
1 10	RINGA RINGB	I/O	Subscriber loop connection RING (Channel A) Subscriber loop connection RING (Channel B)
2 11	TIPA TIPB	I/O	Subscriber loop connection TIP
3 12	BGNDA BGNDB	GND	Battery ground: reference for TIP, RING, VBATH, VBATL and VHR
4 13	VHRA VHRB	PWR	Auxiliary positive battery supply voltage used in ringing mode (5 V ≤ V_{HR} ≤ 85 V)
5 14	VDDA VDDB	PWR	Positive supply voltage (+3.3 or +5 V), referred to AGND
6 15	VBATLA VBATLB	PWR	Second negative battery supply voltage (–15 V ≥ V_{BATL} ≥ V_{BATH})
7, 16	VBATH	PWR	Most negative battery supply voltage; chip substrate potential (–20 V ≥ V_{BATH} ≥ –85 V)
8 17	AGNDA AGNDB	GND	Analog ground: reference for VDD and all signal and control pins except TIP and RING
9 18	CEXTA CEXTB	O	Common mode line potential with high output resistance (160 kΩ); an external capacitance allows supply voltage filtering
29, 30 20, 21	ACNA, ACPA ACNB, ACPB	I	ACP - ACN: differential two-wire AC input voltage; at TIP/RING amplified by -6
31, 32 22, 23	DCNA, DCPA DCNB, DCPB	I	DCP - DCN: differential DC or ring input voltage; at TIP/RING amplified by -30 (ACTL, ACTH) and -60 (ACTR mode), resp.
33 24	C2A C2B	I	Ternary logic input, controlling the operation mode
34 25	C1A C1B	I/O	Ternary logic input, controlling the operation mode; in case of thermal overload (chip temperature exceeding 165 °C), this pin sinks a current of typically 150 µA.
35 26	ILA ILB	O	Current output: longitudinal line current scaled down by a factor of 100
36 27	ITA ITB	O	Current output: transversal line current scaled down by a factor of 50
19, 28	N.C.		Not connected

1.6 Functional Block Diagrams

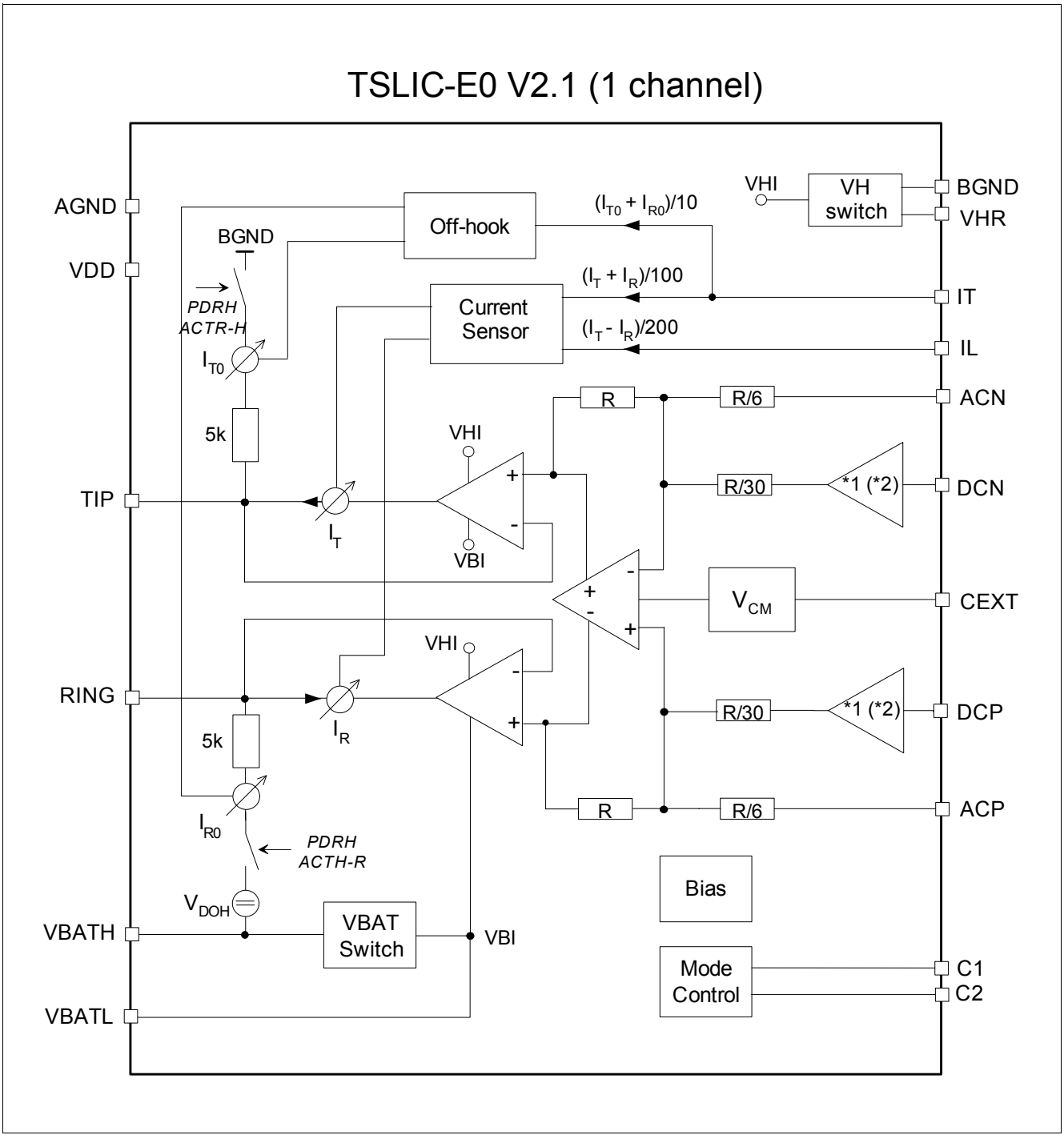


Figure 3 Block Diagram TSLIC-E0 (one channel)

*Note: As both channels "A" and "B" are identical, channel independent pin names (e.g. "TIP" instead of "TIPA / TIPB") are used throughout this document (with the exception of **Table 1**)*

2 Functional Description

Functional block diagram is shown in **Figure 3**.

TSLIC-E0 V2.1 supports AC and DC control loops based on feeding a voltage V_{TR} to the line and sensing the transversal line current I_{Trans} and the longitudinal current I_{Long}.

In receive direction, DC and AC voltages are handled separately with different gains. Both are applied differentially via the codec interface pins DCP / DCN and ACP / ACN, respectively, defining the transversal line voltage V_{TR} through

$V_{TR} = V_{TIP} - V_{RING} = V_{ab} =$

$= 30 * (V_{DCP} - V_{DCN}) + 6 * (V_{ACP} - V_{ACN})$ for modes ACTL and ACTH

$= 60 * (V_{DCP} - V_{DCN}) + 6 * (V_{ACP} - V_{ACN})$ for mode ACTR

As the ring signal is processed in the DC path, the DC gain is doubled in the ring mode ACTR to enable the full output voltage swing.

The common mode line voltage is always equal to the mean supply voltage, $V_{CM} = (V_{HI} + V_{BI}) / 2$, leading to symmetrical line potentials with respect to the supplies. Depending on the operation mode, V_{HI} is switched either to V_{HR} or to BGND via the VH switch. V_{BI} is connected either to V_{BATH} via the VBAT switch or to V_{BATL} via an external diode.

A reversed polarity of V_{TR} is easily obtained by changing the polarity of $(V_{DCP} - V_{DCN})$.

In transmit direction, the transversal and longitudinal line currents I_{Trans} and I_{Long} (**Figure 4**) are measured, and scaled images are provided at the IT and IL pins, respectively:

$I_{IT} = (I_T + I_R) / 100 = I_{Trans} / 50$

$I_{Trans} = (I_T + I_R) / 2$

$I_{IL} = (I_T - I_R) / 200 = I_{Long} / 100$

$I_{Long} = (I_T - I_R) / 2$

For off-hook detection in PDRH mode, 5 kΩ resistors are connected from TIP to BGND and from RING to VBATH, respectively. The currents through these resistors, I_{T0} and I_{R0}, are sensed, scaled and provided at IT:

$I_{IT0} = (I_{T0} + I_{R0}) / 10 = I_{TRANS0} / 5$

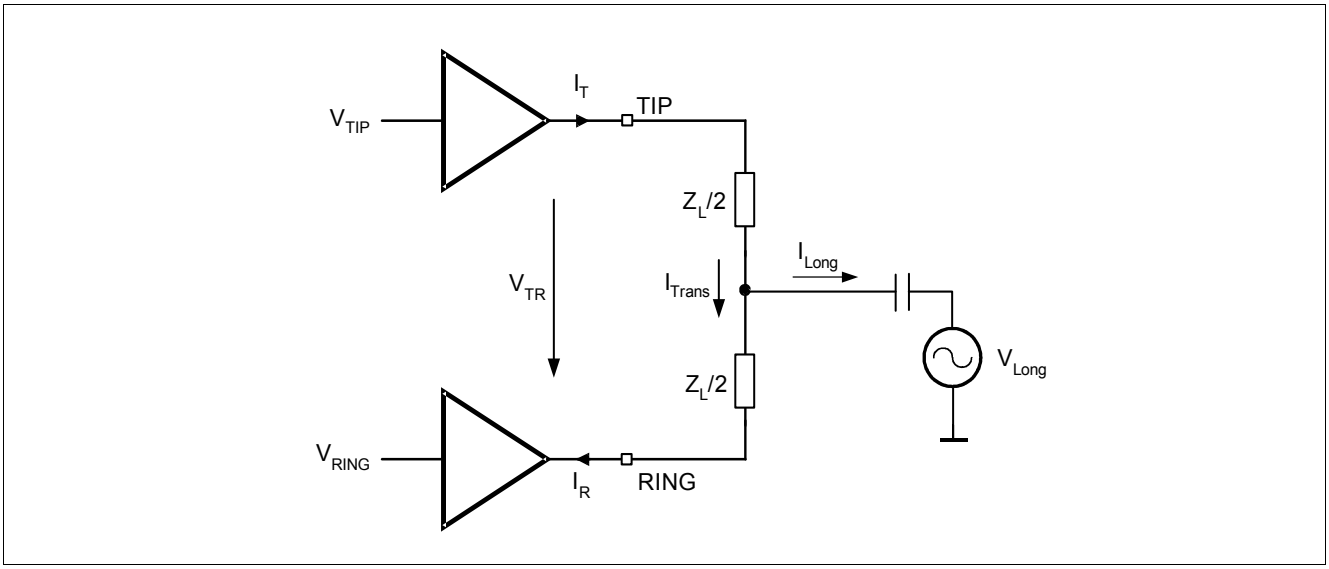


Figure 4 Transversal and Longitudinal Line Currents

2.1 Operating Modes

Each channel of TSLIC-E0 V2.1 operates in one of the following modes controlled by ternary logic signals at the respective C1 and C2 input pins

Table 2 TSLIC-E0 Mode Table

		C2		
		L	**M**	**H**
C1	**L**[1)]	HIRT	PDRHL	PDRH
	M	ACTL	ACTH	ACTR
	H	ACTH-R	HIT	HIR

1) No ‘Overtemp’ signaling possible via pin C1 if C1 is low.

The operating modes of channels A and B can be chosen completely independent. Any combination is allowed; thermal restrictions, however, have to be obeyed (e.g. max. chip temperature).

Table 3 TSLIC-E0 Modes and Supplies

Mode	Mode Description	Internal Supply Voltages V_{BI}, V_{HI}
PDRH	Power Down Resistive High	VBATH, VH switch open
PDRHL	Power Down Resistive High Load	VBATH, VH switch open
ACTL	Active Low	VBATL, BGND
ACTH	Active High	VBATH, BGND
ACTH-R	Active High Resistive	VBATH, BGND
ACTR	Active Ring	VBATH, VHR
HIRT	High Impedance on RING and TIP	VBATH, VHR
HIT	High Impedance on TIP	VBATH, VHR
HIR	High Impedance on RING	VBATH, VHR

Power Down Resistive High (PDRH)

Power consumption is reduced to a minimum by switching completely off all voice transmission functions. To allow off-hook detection, PDRH provides a connection of 5 kΩ each from TIP to BGND and RING to VBATH, respectively, while the output buffers show high impedance (see **Figure 3**). The current through these resistors is sensed, scaled by 1/5 and transferred to the IT pin for off-hook supervision.

Power Down Resistive High Load (PDRHL)

PDRHL is used as a transition state from Power Down to Active modes (automatically initiated during a mode change). It causes fast preloading of CEXT in order to suppress line voltage transients.

Active Low (ACTL), Active High (ACTH)

These are the regular transmission modes for voiceband. The line-driving section is operated between BGND and VBATL (ACTL) or VBATH (ACTH).

Active High Resistive (ACTH-R)

The SLIC is operated in Active High state together with the 5 kΩ resistors from TIP to BGND and from RING to VBATH. This mode is intended to be used for line testing.

Active Ring (ACTR)

Utilizing an additional positive battery voltage V_{HR}, this mode allows balanced ringing of up to 85 Vrms or feeding of very long telephone lines. In ACTR mode the DC voltage gain is doubled to 60.

High Impedance (HIR, HIT, HIRT)

In these modes each of the line outputs can be programmed to show high impedance. HIT switches off the TIP buffer, while HIR switches off the RING buffer. The current through the active buffer is still sensed. In the HIRT mode both buffers show high impedance. The current sensor remains active thus allowing sensor offset calibration (for test purposes).

2.2 Current Limitation / Overtemperature Protection

In any operating mode the total current delivered by the output drivers is limited to typically 85 mA.

If, however, the junction temperature exceeds 165 °C, the current limit is further reduced to keep the junction temperature constant.

Simultaneously, pin C1 sinks a signalling current I_{therm}.

3 Typical Application Circuit

Figure 5 shows one channel of an application circuit including TSLIC-E0 V2.1, together with a VINETIC® codec (for latest information please refer to the VINETIC® Data Sheets).

In **Table 4** the recommended external components for a dual channel system and their typical values are listed.

Table 4 External Components VINETIC® for 2 Channels

No.	Symbol	Value	Unit	Relat. Tol.	Rating
2	R_{IT1}	510	Ω	1 %	–
2	R_{IT2}	680	Ω	1 %	–
2	R_{IL}	1.6	kΩ	1 %	–
4	R_{STAB}	30	Ω	1 %[1)]	–
4	C_{STAB}	15 (POTS) 22 (IVD)	nF nF	10 % 10 %	100 V 100 V
2	C_{DC}[2)]	220	nF	10 %	10 V
2	C_{ITAC}	1	µF	10 %	10 V
2	C_{PRE}	18	nF	5 %	10 V
1	C_{REF}	68	nF	20 %	10 V
2	C_{EXT}	100	nF	20 %	50 V
13	C_1	100	nF	10 %	10 V
6	C_2	100	nF	10 %	100 V
2	D_1	BAS 21	–	–	–
2	D_2	BAS 21	–	–	–
2	D_3[3)]	BAS 21	–	–	–
2	OVP[4)]	Overvoltage Protection (e.g. thyristor)	–	–	–
4	OCP[4)]	Overcurrent Protection (e.g. LFR, fuse, PTC)	–	–	–

1) Matching tolerance depends on longitudinal balance requirements (for details see **[2]**).

2) With VINETIC®-2CPE this capacitance is substituted by 100 nF between DCN and DCP.

3) Due to the changed battery switch concept (see **Figure 3**), the VBATL series diode must not be shared between different channels; one diode per channel is mandatory (also for applications with TSLIC).

4) See **[1]**

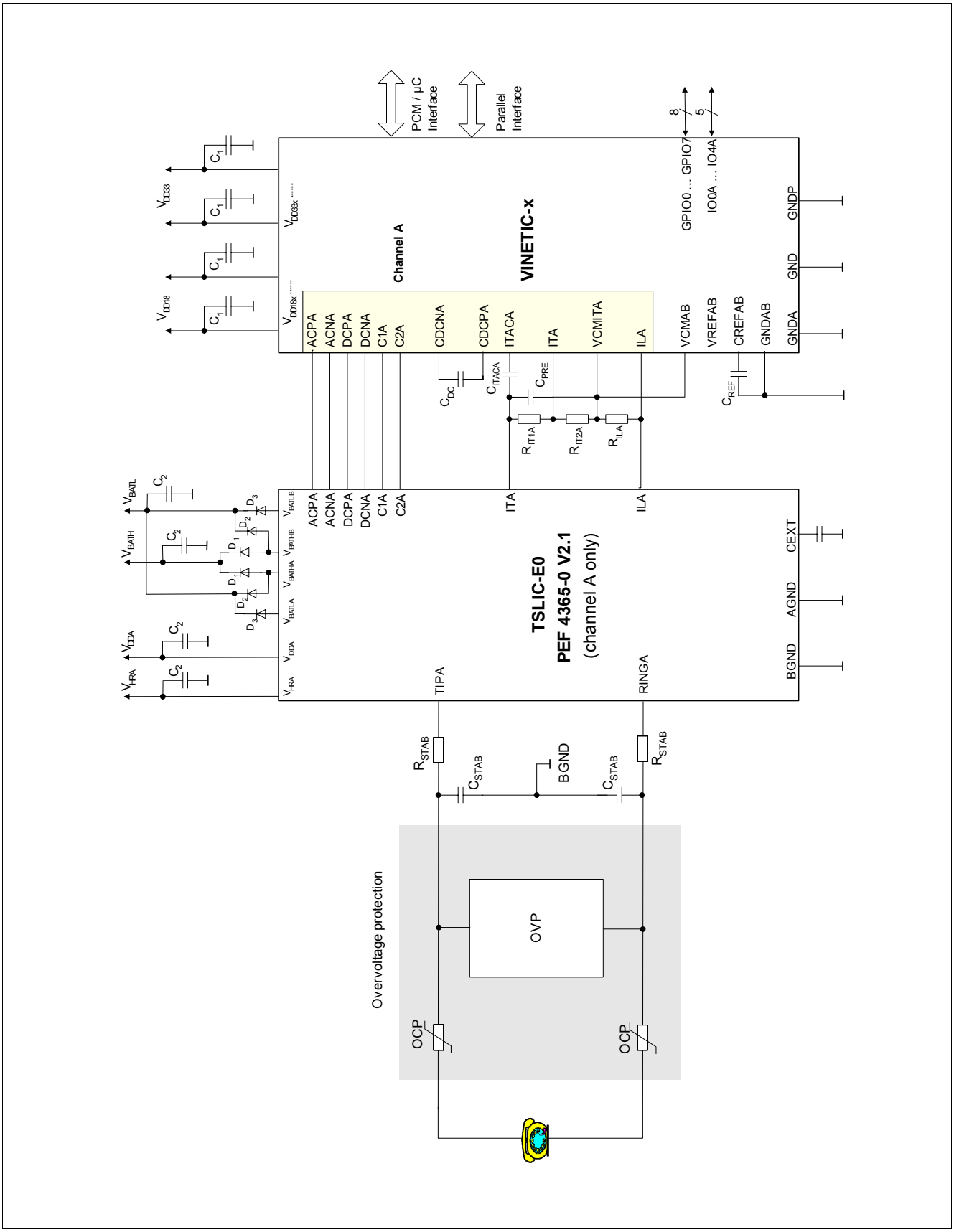


Figure 5 Application Circuit TSLIC-E0

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 5 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Battery voltage low	V_{BATL}	–85	–	0.4	V	Referred to BGND
Battery voltage high	V_{BATH}	–90	–	0.4	V	Referred to BGND
Battery voltage difference	$V_{BATL} - V_{BATH}$	–0.4	–	–	V	–
Auxiliary supply voltage	V_{HR}	–0.4	–	90	V	Referred to BGND
Total battery supply voltage, continuous	$V_{HR} - V_{BATH}$	–0.4	–	160	V	–
V_{DD} supply voltage	V_{DD}	–0.4	–	7	V	Referred to AGND
Ground voltage difference	$V_{BGND} - V_{AGND}$	–0.4	–	0.4	V	–
Input voltages	V_{DCP}, V_{DCN}, V_{ACP}, V_{ACN}, V_{C1}, V_{C2}	–0.4	–	V_{DD} + 0.4	V	Referred to AGND
Junction temperature	T_j	–	–	150	°C	–
ESD voltage, all pins	–	–	–	1	kV	SDM (Socketed Device Model)[1)]
	–	–	–	1	kV	HBM (Human Body Model)[1)]

1) EOS/ESD Assn. Standard DS5.3-1993.

Attention: Stresses exceeding the max. values listed above may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4.2 Foreign Line Voltages

External voltages applied at the line outputs may cause large currents in the SLIC. The resulting on-chip power dissipation has to be limited to avoid thermal destruction, if the overtemperature protection cannot react sufficiently fast due to high local power density. The safe power dissipation values are strongly dependent on duration. They can be expressed in terms of voltage and current limits directly at the TIP and RING pins (see **Table 6** and **Table 7**).

Table 6 Voltage Limits on Output Pins

Voltage Duration	Pins	Min. Voltage [V]	Max. Voltage [V]
Continuous	TIP, RING	V_{BATH} – 0.4	V_{HR} + 5
< 10 ms	TIP, RING	V_{BATH} – 5	V_{HR} + 10
< 100 µs	TIP, RING	V_{BATH} – 10	V_{HR} + 20
< 1 µs	TIP, RING	V_{BATH} – 15	V_{HR} + 40

Table 7 Current Limits on Output Pins

Current Duration	Pins	Min. current [A]	Max. current [A]
Continuous	TIP, RING	– 0.1	0.1
< 10 ms	TIP, RING	– 0.5	0.5
< 100 µs	TIP, RING	– 1.0	1.0
< 1 µs	TIP, RING	– 1.5	1.5

The above limitations have to be regarded as typical. They are valid simultaneously. Together with external circuitry they determine protection requirements (see **[1]**).

4.3 Operating Range

Table 8 Operating Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Battery voltage L	V_{BATL}	–80	–	–15	V	Referred to BGND
Battery voltage H	V_{BATH}	–85	–	–20	V	Referred to BGND
Auxiliary supply voltage	V_{HR}	V_{DD}	–	85	V	Referred to BGND
Total battery supply voltage	$V_{HR} - V_{BATH}$	–	–	150	V	–
V_{DD} supply voltage	V_{DD}	3.15	–	5.5	V	Referred to AGND
Ground voltage difference	$V_{BGND} - V_{AGND}$	–0.4	–	0.4	V	–
Voltage at pins IT, IL	V_{IT}, V_{IL}	–0.4	–	V_{DD} - 0.6	V	Referred to AGND
Input range V_{DCP}, V_{DCN}, V_{ACP}, V_{ACN}		0	–	3.3	V	Referred to AGND
Ambient temperature	T_{amb}	–40	–	85	°C	–
Junction temperature	T_J	–	–	125[1)]	°C	–

1) Operation up to T_J = 150 °C possible. However, a permanent junction temperature exceeding 125 °C could degrade device reliability.

4.4 Thermal Resistances

Table 9 Thermal Resistances

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Junction to case	$R_{th, jC}$	–	2	–	K/W	
Junction to ambient	$R_{th, jA}$	–	50	–	K/W	PG-DSO-36-15, without additional heatsink
		–	20	–	K/W	PG-DSO-36-15, 4-layer JEDEC PCB with vias, die pad soldered to PCB (footprint see **Chapter 6.1.1**)

The allowed total power dissipation can be calculated as:

$P_{max} = P_A + P_B = (T_{j, max} - T_{amb}) / R_{th, jA}$

P_A ... Power Dissipation Channel A

P_B ... Power Dissipation Channel B

4.5 Electrical Parameters

Unless otherwise stated, minimum and maximum values are valid within the full operating range.

Testing is performed according to the specific test figures at V_{BATH} = –48 V, V_{BATL} = –24 V, V_{HR} = +32 V and V_{DD} = +3.3 V.

Functionality and performance is guaranteed for T_A = 0 to 70 °C by production testing. Extended temperature range operation at –40 °C < T_A < 85 °C is guaranteed by design, characterization and periodically sampling and testing production devices at the temperature extremes.

4.5.1 Supply Currents and Power Dissipation

Table 10 Supply Currents, Power Dissipation (I_R = I_T = 0; V_{TR} = 0; one channel)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power Down High Impedance, Power Down Resistive High						
V_{DD} current	I_{DD}	–	250	350	µA	–
V_{BATH} current	I_{BATH}	–	40	80	µA	–
V_{BATL} current	I_{BATL}	–	0	10	µA	–
V_{HR} current	I_{HR}	–	0	10	µA	–
Active Low						
V_{DD} current	I_{DD}	–	2.2	2.8	mA	–
V_{BATH} current	I_{BATH}	–	40	80	µA	–
V_{BATL} current[1)]	I_{BATL}	–	3.3	4	mA	-
V_{HR} current	I_{HR}	–	0	10	µA	–
Active High						
V_{DD} current	I_{DD}	–	2.6	3.2	mA	–
V_{BATH} current[2)]	I_{BATH}	–	3.8	4.5	mA	–
V_{BATL} current	I_{BATL}	–	0	10	µA	–
V_{HR} current	I_{HR}	–	0	10	µA	–
Active Ring						
V_{DD} current	I_{DD}	–	1.5	2	mA	–
V_{BATH} current[3)]	I_{BATH}	–	3.5	4.3	mA	–
V_{BATL} current	I_{BATL}	–	0	10	µA	–
V_{HR} current[4)]	I_{HR}	–	1.8	2.3	mA	–
High Impedance on TIP or RING (HIR, HIT)						
V_{DD} current	I_{DD}	–	1.5	2	mA	–
V_{BATH} current	I_{BATH}	–	2.9	3.6	mA	–
V_{BATL} current	I_{BATL}	–	0	10	µA	–
V_{HR} current	I_{HR}	–	1.3	1.7	mA	–
High Impedance on TIP and RING (HIRT)						
V_{DD} current	I_{DD}	–	1.4	1.8	mA	–
V_{BATH} current	I_{BATH}		2.2	2.8	mA	–

Table 10 Supply Currents, Power Dissipation (I_R = I_T = 0; V_{TR} = 0; one channel) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
V_{BATL} current	I_{BATL}	–	0	10	µA	–
V_{HR} current	I_{HR}	–	0.8	1.1	mA	–

1) Current depending on supply voltage: I_{BATL} (V_{BATH}) = I_{BATL} (-24 V) + (-V_{BATL} - 24) / 40 kΩ
2) Current depending on supply voltage: I_{BATH} (V_{BATH}) = I_{BATH} (-48 V) + (-V_{BATH} - 48) / 40 kΩ
3) Current depending on line voltage: I_{BATH} (V_{TR}) = I_{BATH} (0) + |V_{TR}| / 40 kΩ
4) Current depending on line voltage: I_{HR} (V_{TR}) = I_{HR} (0) + |V_{TR}| / 60 kΩ

The total power dissipated in each SLIC consists of the quiescent power P_Q due to the supply currents and the output stage power P_O caused by any line current I_{Trans} (see **Table 11**).

$P_{tot} = P_Q + P_O$

with $P_Q = V_{DD} * I_{DD} + |V_{BATH}| * I_{BATH} + |V_{BATL}| * I_{BATL} + V_{HR} * I_{HR}$

Table 11 Output Stage Power Dissipation

Operating Mode	Equation for P_O Calculation	Comment
ACTL	$P_O = (1.05 * \|V_{BATL}\| - V_{TR}) * I_{Trans}$	–
ACTH	$P_O = (1.05 * \|V_{BATH}\| - V_{TR}) * I_{Trans}$	–
ACTR	$P_O = (1.02 * V_{HR} + 1.05 * \|V_{BATH}\| - V_{TR}) * I_{Trans}$ $P_O = [4 * (V_H + \|V_{BATH}\|) - \pi * V_P * \cos\varphi] * V_P / (2 * \pi * Z_L)$	Ohmic load complex load Z = $Z_L e^{i\varphi}$, V_P ... peak ring voltage

The power values of both channels have to be added to yield the TSLIC's total power dissipation.

4.5.2 DC Characteristics

Table 12 DC Characteristics (V_{ACP} = V_{ACN} = 1.5 V)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line Termination TIP, RING						
Differential DC line voltage	$V_{TR, DC}$	–0.4	0	0.4	V	V_{DCP} = V_{DCN} = 1.5 V Modes: ACTx
		23.5	24	24.5	V	V_{DCP} – V_{DCN} = 0.8 V
		–24.5	–24	–23.5	V	V_{DCP} – V_{DCN} = –0.8 V
Common mode DC line voltage	$V_{TIP, DC}$ =	–13	–12	–11	V	Mode: ACTL
	= $V_{RING, DC}$	–25	–24	–23	V	Mode: ACTH
		–10	–9	–8	V	Mode: ACTR
DC line voltage drop (see **Figure 6**)	– V_{BATH}– $V_{TR, max}$	–	2.5	3	V	$I_{Trans,DC}$ = 20 mA V_{DCP} – V_{DCN} = 2.5 V Temp = 25°C[1)] Mode: ACTH
Output current limit (see **Figure 11**)	$\|I_{R, max}\|$, $\|I_{T, max}\|$	70 80	85 100	100 120	mA	V_T,V_R = 0 (sinking) V_T,V_R = V_{BATx} (sourcing) Temp = 25°C[2)]
Open loop resistance TIP to V_{BGND} (see **Figure 12**)	R_{TG}	4.2	5	5.8	kΩ	Temp = 25°C[3)] Mode: PDRH
Open loop resistance RING to V_{BATH} (see **Figure 12**)	R_{RB}	4.2	5	5.8	kΩ	Temp = 25°C[3)] Mode: PDRH
Power down open loop line voltage	$V_{TR,PD}$ = = – V_{BATH} – V_{DOH}	42	44	47	V	Mode: PDRH
Power down output leakage current	$I_{Leak,R}$	–10	–	10	µA	Mode: PDH
	$I_{Leak,T}$	–10	–	10	µA	V_{BATH} < $V_{T/R}$ < 0
High impedance output leakage current	$I_{Leak,R}$	–10	–	10	µA	Mode: HIR, HIRT V_{BATH} < V_R < V_{HR}
	$I_{Leak,T}$	–10	–	10	µA	Mode: HIT, HIRT V_{BATH} < V_T < V_{HR}
Inputs DCP, DCN, ACP, ACN, Output C_{EXT}						
Input current DCP, DCN	I_{DC}	–	0.1	–	µA	–
Differential AC input resistance ACP, ACN	R_{AC}	–	20	–	kΩ	–
Output resistance on C_{EXT}	–	–	100	–	kΩ	–
Current Outputs IT, IL						
IT output current	I_{IT}	–15	0	15	µA	I_R = I_T = 0 mA
IT output current normal polarity	I_{IT}	380	400	420	µA	I_R = I_T = 20 mA
IT output current reverse polarity[4)]	I_{IT}	–420	–400	–380	µA	I_R = I_T = –20 mA

Table 12 DC Characteristics (V_{ACP} = V_{ACN} = 1.5 V) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Transversal current ratio (see Figure 14)[5]	$1/G_{IT,DC}$	49.5	50	50.5	–	I_R = I_T = 20 mA, I_R = I_T = –20 mA
Off-hook output current on IT	–	800	950	1100	µA	TIP/RING shorted, Temp = 25 °C[6] Mode: PDRH
IL output current (see Figure 14)	I_{IL}	–20	0	20	µA	I_R = I_T = 20 mA
		30	50	70	µA	I_R = 15 mA, I_T = 25 mA
		–160	–125	–90	µA	I_R = 50mA, I_T = 25mA
Control Inputs C1, C2						
H-input voltage	V_{IH}	2.7	–	V_{DD} + 0.3	V	–
M-input voltage	V_{IM}	1.2	–	2.1	V	–
L-input voltage	V_{IL}	–0.3	–	0.6	V	–
Input pull down current	I_{in}	0	2	10	µA	–
Thermal overload current C1	I_{therm}	120	150	250	µA	V_{C1} = 1.20 V
Thermal overload threshold temperature	T_{jLIM}	–	165	–	°C	Mode: ACTx, HIx

1) The systematic temperature dependence is appr. + 7 mV / °C
2) The systematic temperature dependence is appr. -0.3 % / °C
3) The systematic temperature dependence is appr. +0.1 %/ °C
4) With **VDD = 3.3 V**, the IT output current **in reverse polarity** is limited to typically 700 uA; thus, the DC current regulation loop operates correctly only up to the corresponding line current value of 35 mA. In all other cases, IT is linear within the full line current range
5) The offset (I_R = I_T = 0 mA) has to be taken into account.
6) The systematic temperature dependence is appr. -0.1 %/ °C

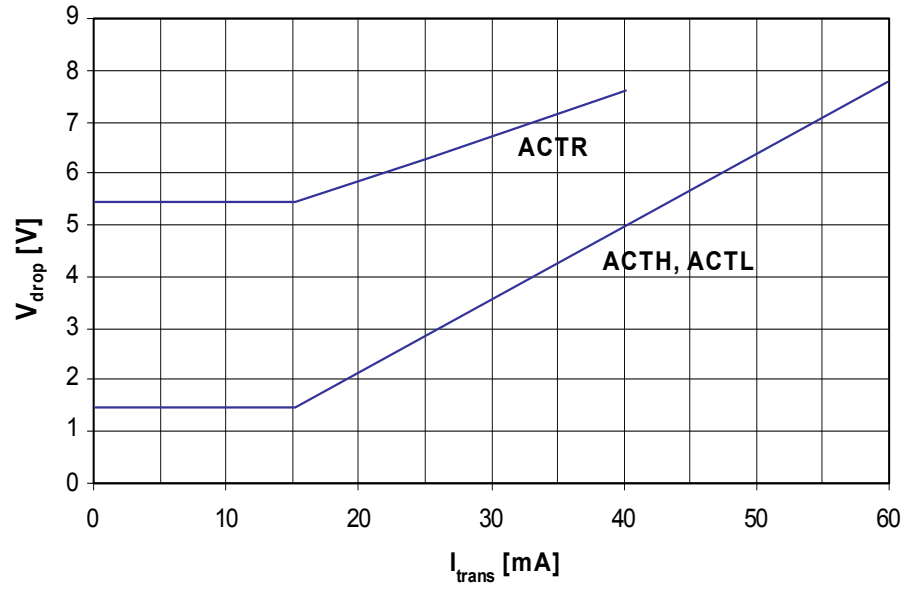


Figure 6 Typical Buffer Voltage Drop in Operating Modes ACTL, ACTH, ACTR

4.5.3 AC Characteristics

If not otherwise stated, AC characteristics are tested at a DC line current of 25 mA and –25 mA, respectively; they are valid in all active modes.

Table 13 AC Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line Termination TIP, RING						
Receive gain (see **Figure 14**)	G_r	5.925	6.0	6.075	–	$V_{ACP} - V_{ACN}$ = 640 mV_{rms}, f = 1015 Hz
Total harmonic distortion V_{TR} (see **Figure 14**)	THD	–	0.01		%	$V_{ACP} - V_{ACN}$ = 640 mV_{rms}, f = 1015 Hz
Teletax distortion	$THDTTX$	–	0.1		%	$V_{TR,AC}$ = 5 V_{rms}, f = 16 kHz, R_L = 200 Ω
		–	0.2		%	$V_{TR,AC}$ = 5 V_{rms}, f = 16 kHz, R_L = 200 Ω, $I_{Trans,DC}$ = 0 mA
Psophometric noise (see **Figure 14**)	N_{pVTR}	–	–82	–78	dBmp	–
Longitudinal to transversal rejection ratio V_{long}/V_{TR} (see **Figure 15**)	$LTRR$	–	80	–	dB	V_{long} = 3 V_{rms}, 300 Hz < f < 3.4 kHz
Longitudinal to transversal rejection ratio V_{long}/V_{TR} (loop) PEF 4365-0 (see **Figure 15**)	$LTRR_{loop}$	54 52	58 56	– –	dB dB	300 Hz < f < 1kHz f = 3.4 kHz V_{long} = 3 V_{rms}
Transversal to longitudinal rejection ratio V_{TR}/V_{long} (see **Figure 17**)	$TLRR$	48	60	–	dB	$V_{ACP} - V_{ACN}$ = 1920 mV_{rms}, 300 Hz < f < 3.4 kHz
Power supply rejection ratio (see **Figure 7**, **Figure 8**, **Figure 10**, **Figure 10**)	$PSRR$					$V_{SupplyAC}$ = 100 mV_p, 300 Hz < f < 3.4 kHz
V_{BATL}/V_{TR}		40	60	–	dB	
V_{BATH}/V_{TR}		40	60	–	dB	
V_{HR}/V_{TR}		33	50	–	dB	
V_{DD}/V_{TR}		33	50	–	dB	
Interchannel crosstalk			-80		dB	300 Hz < f < 3.4 kHz both channels active
			-80		dB	One channel active, one channel power down
Ringing amplitude TIP/RING	V_{RNG0}	–	85	–	Vrms	$V_{DCP} - V_{DCN}$ = 0.15 V (DC) + 1.42 V_{rms} (sine wave, 20 Hz) R_R = 450 Ω, C_R = 3.4 µF, Mode: ACTR
Ringing distortion (see **Figure 18**)	RD	–	0.1		%	

Table 13 AC Characteristics (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Transversal Current IT[1)]						
Transversal current ratio (see **Figure 14**)	$1/G_{it}$	49.5	50	50.5		$V_{ACP} - V_{ACN}$ = 640 mV_{rms}, f = 1015 Hz $I_{Trans,DC}$ = 25 mA
		49	50	51		$I_{Trans,DC}$ = –25 mA
Total harmonic distortion V_{IT}	THD_{IT}	–	0.02	0.3	%	$V_{ACP} - V_{ACN}$ = 640 mV_{rms}, f = 1015 Hz
Psophometric noise (see **Figure 14**)	N_{pVIT}	–	–110	–105	dBmp	–
Longitudinal to transversal current output rejection ratio V_{long}/V_{IT} (see **Figure 15**)	$LITRR$	–	85	–	dB	V_{long} = 3 V_{rms}, 300 Hz < f < 3.4 kHz
Power supply rejection ratio	$PSRR$					$V_{SupplyAC}$ = 100 mV_p, 300 Hz < f < 3.4 kHz
V_{BATL}/V_{IT}		50	70	–	dB	
V_{BATH}/V_{IT}		50	70	–	dB	
V_{HR}/V_{IT}		50	70	–	dB	
V_{DD}/V_{IT}		50	70	–	dB	

1) Unless otherwise specified, characteristics are valid for both DC line current directions (normal and reverse polarity)

4.5.3.1 Frequency Dependence of PSRR

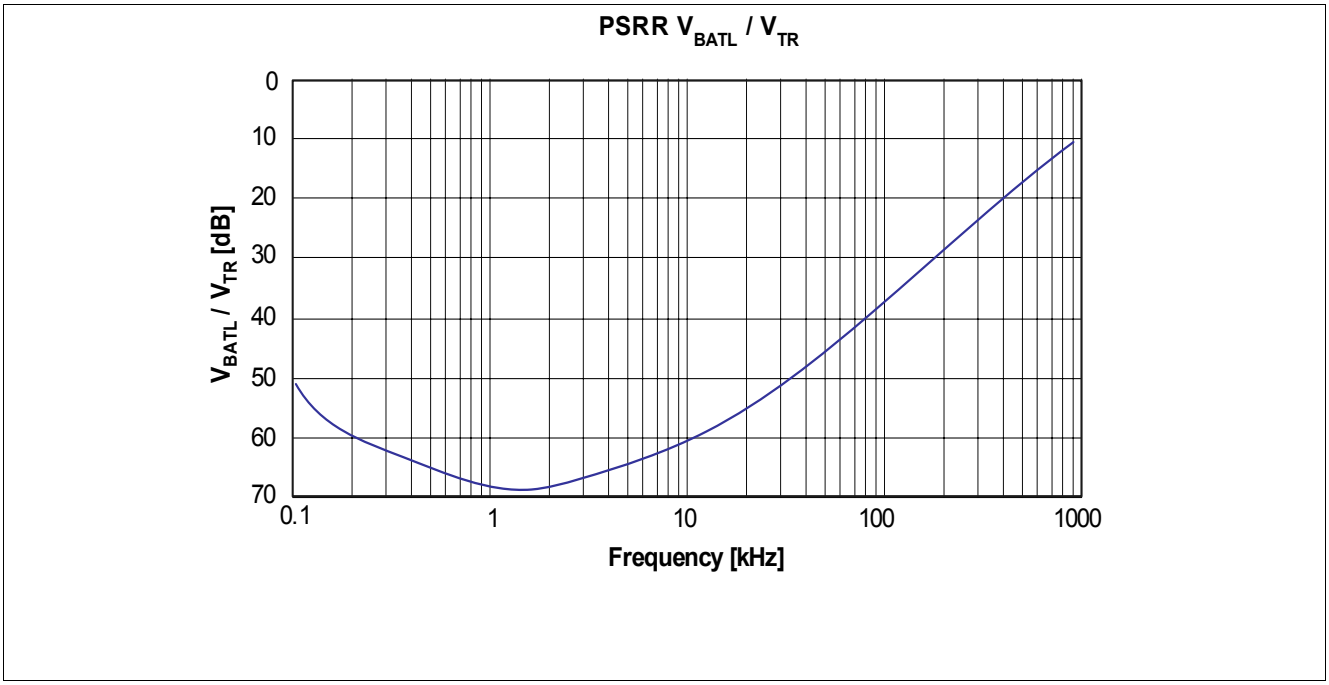


Figure 7 Typical Frequency Dependence of PSRR VBATL/VTR

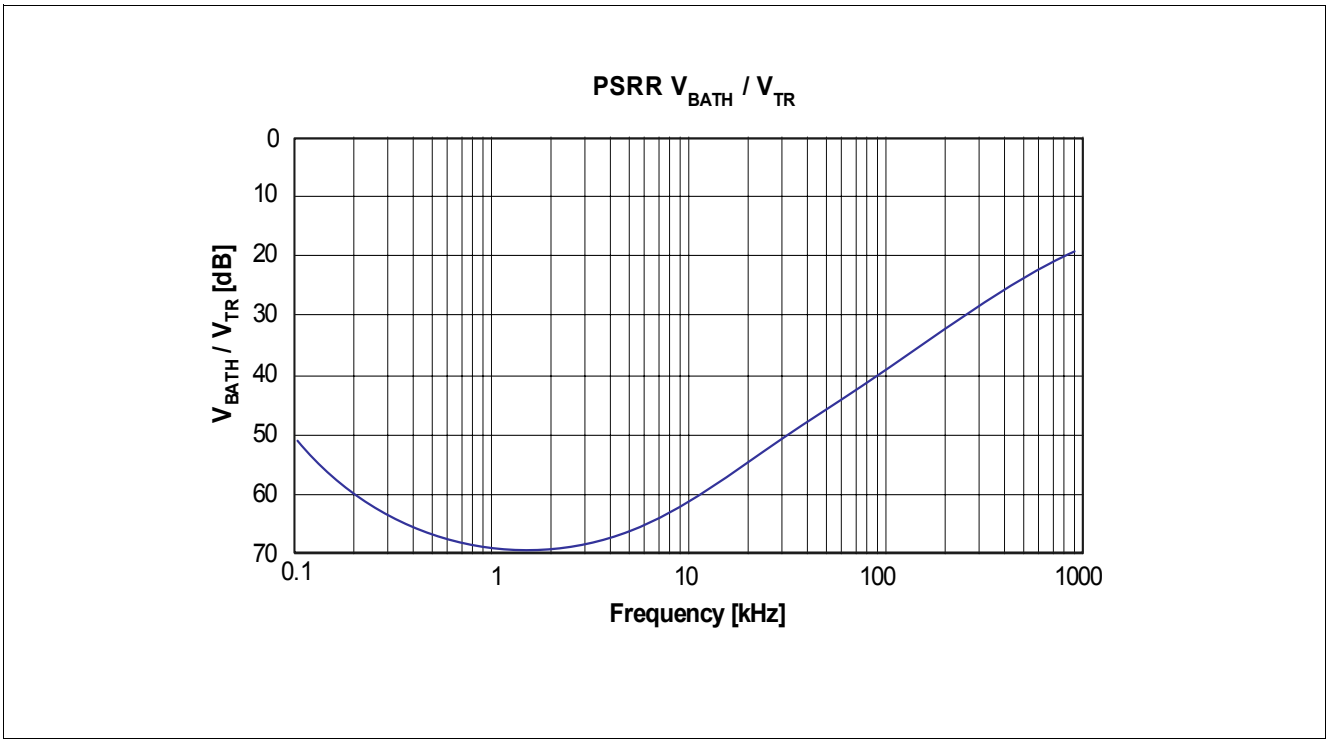


Figure 8 Typical Frequency Dependence of PSRR VBATH/VTR

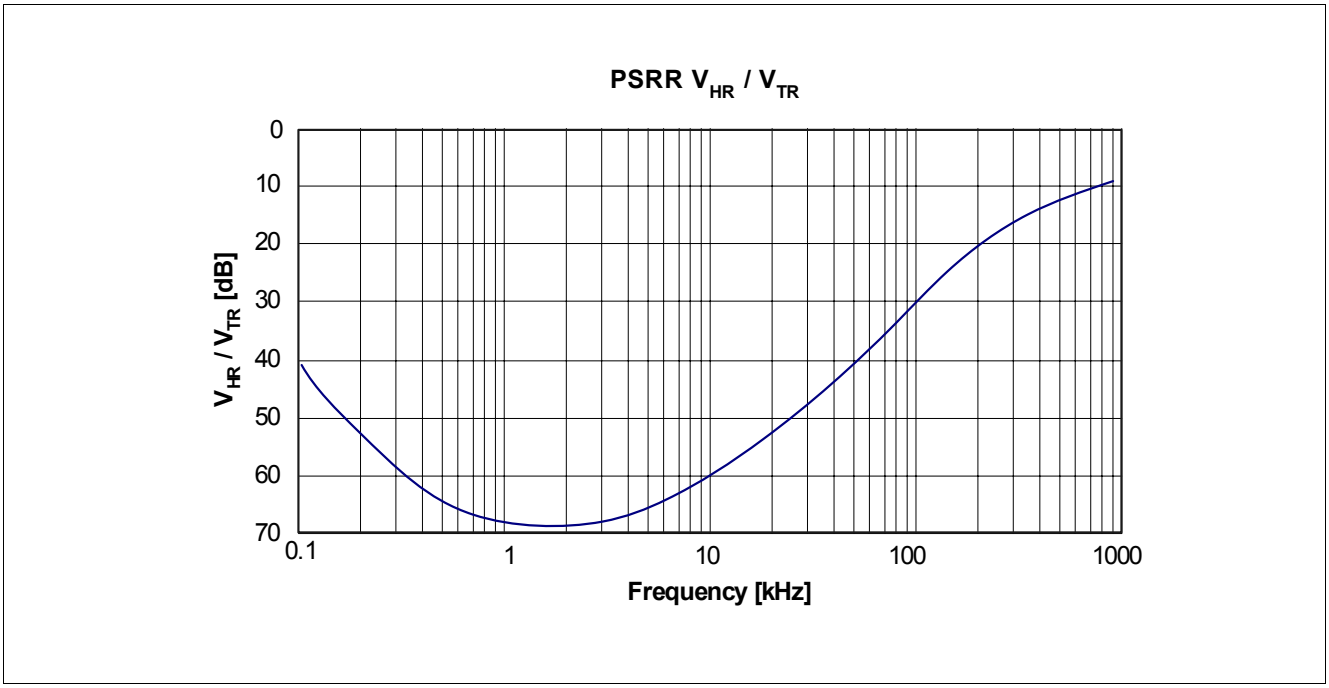


Figure 9 Typical Frequency Dependence of PSRR VHR/VTR

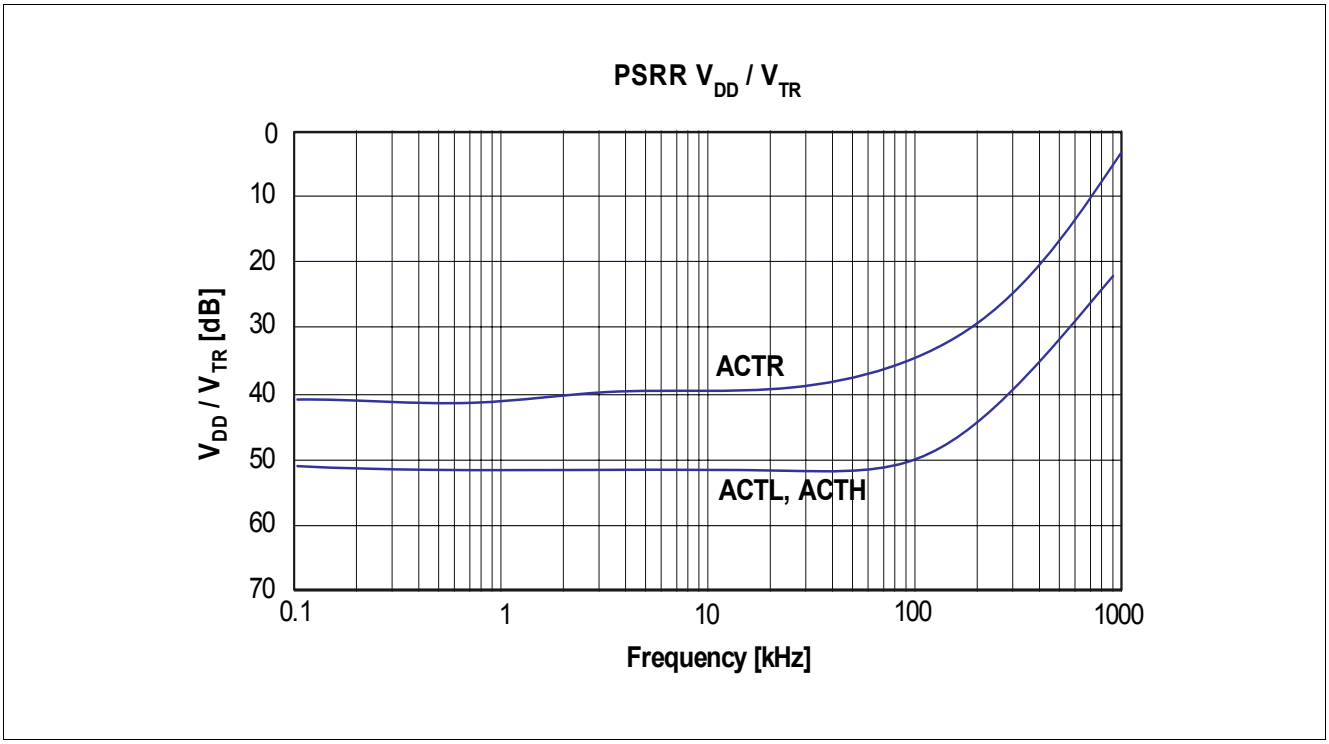


Figure 10 Typical Frequency Dependence of PSRR VDD/VTR

5 Test Figures

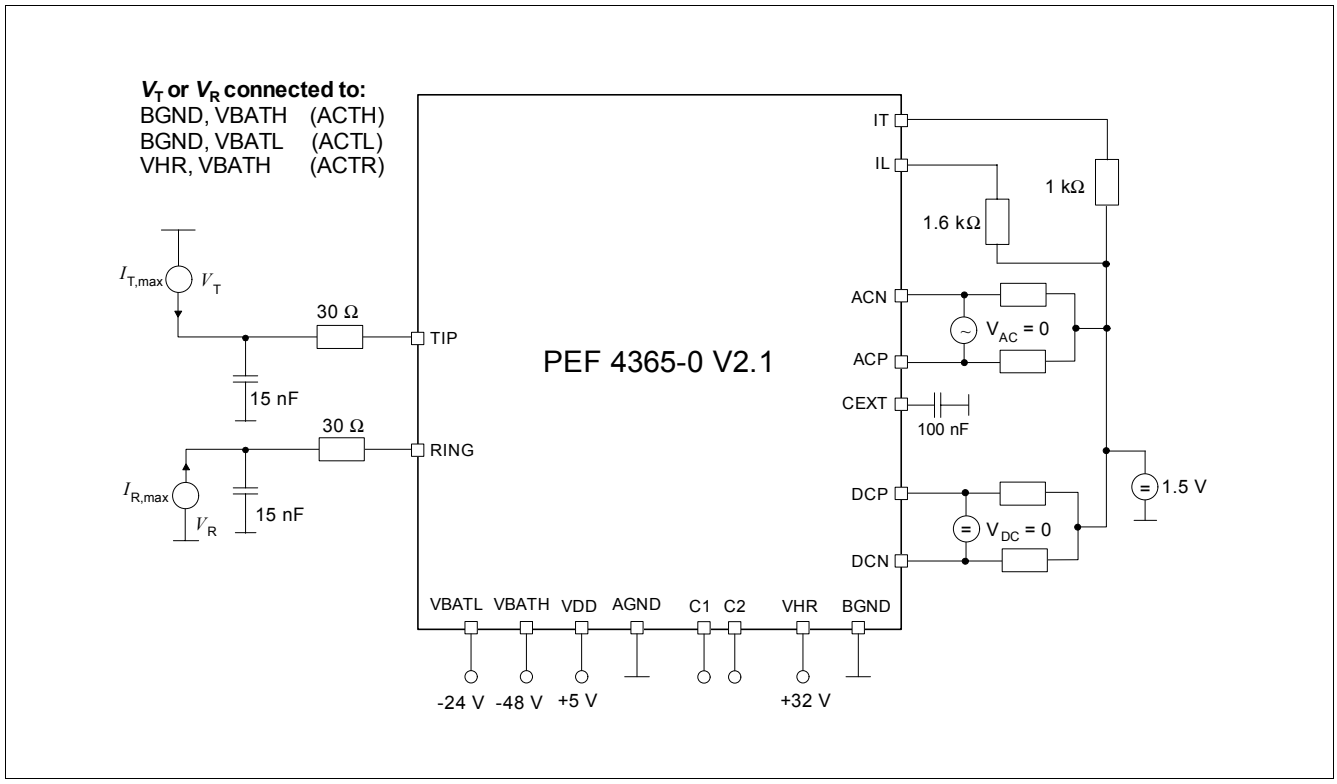


Figure 11 Output Current Limit

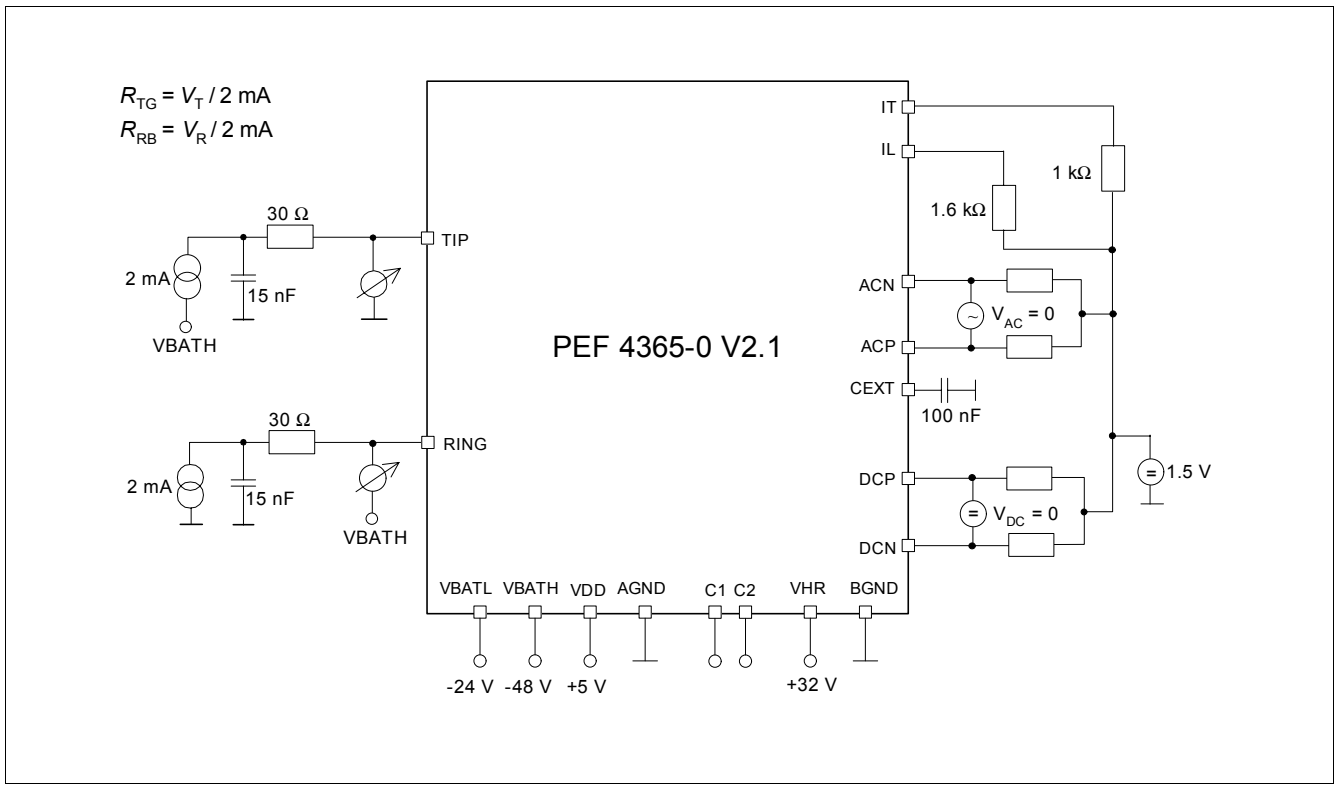


Figure 12 Output Resistance PDRH, PDRHL

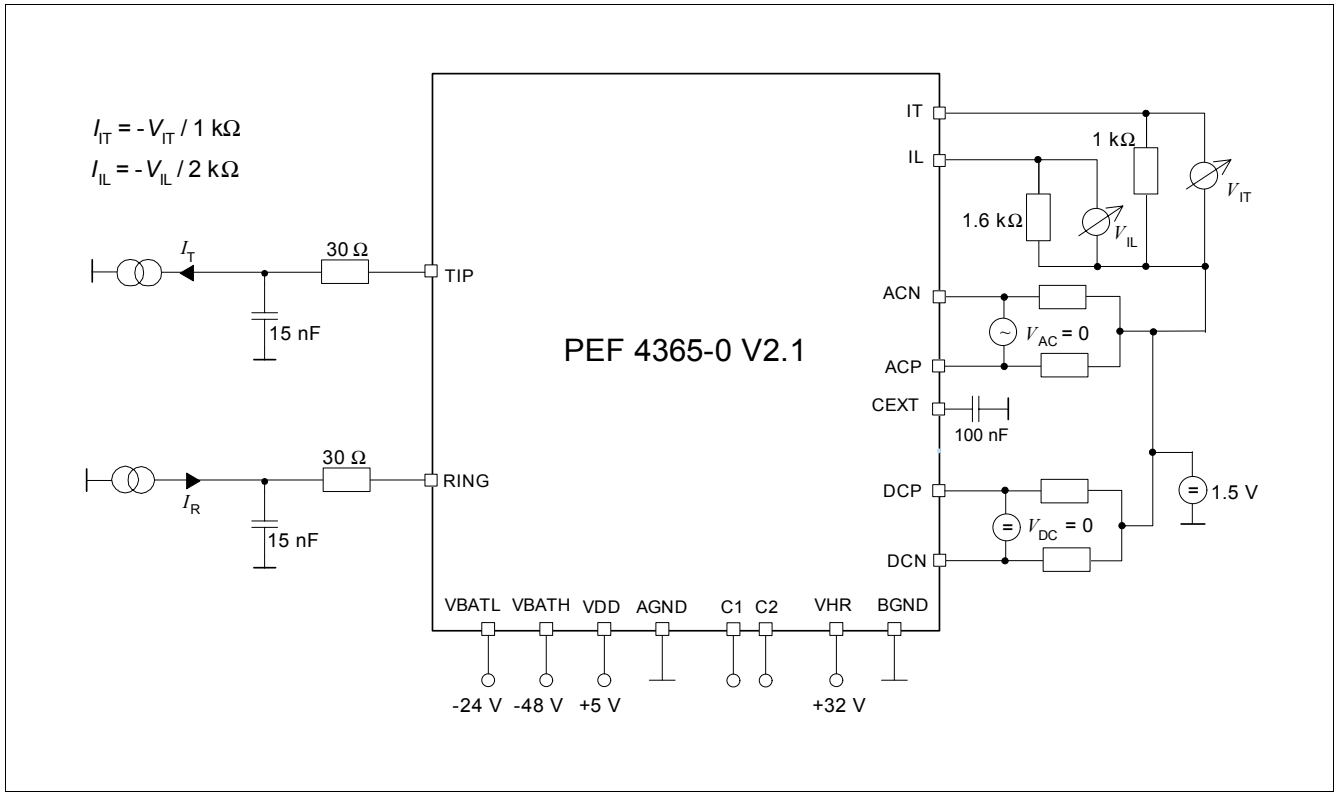


Figure 13 Current Outputs IT, IL

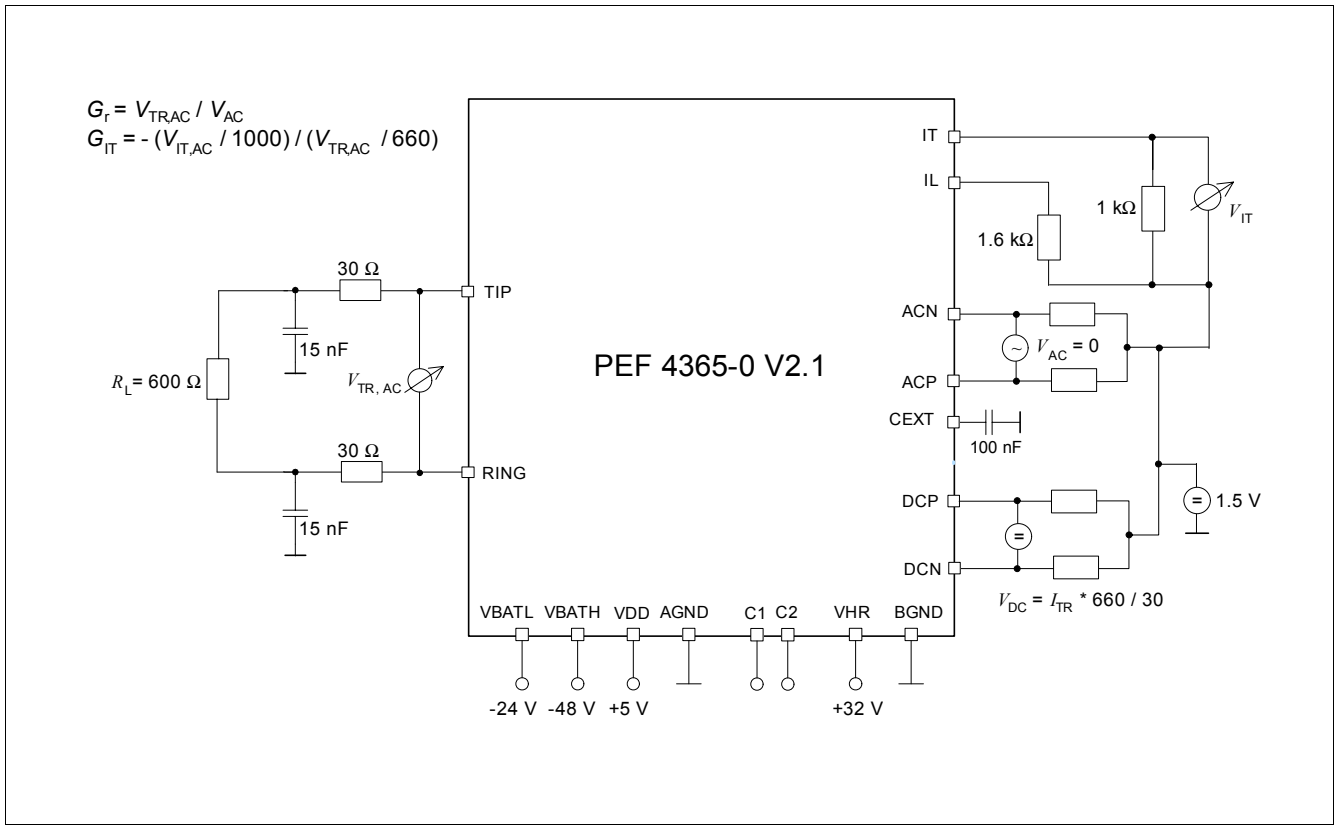


Figure 14 Transmission Characteristics

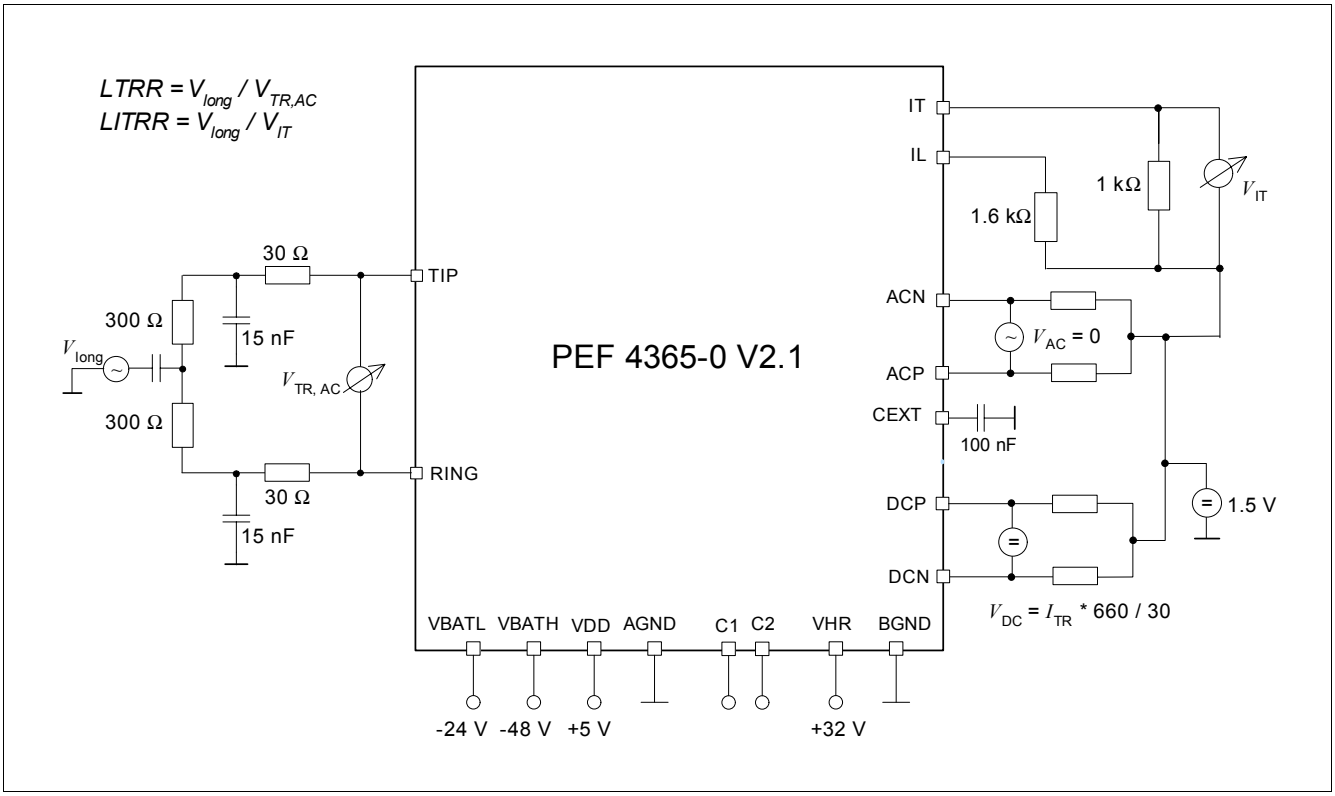


Figure 15 Longitudinal to Transversal Rejection

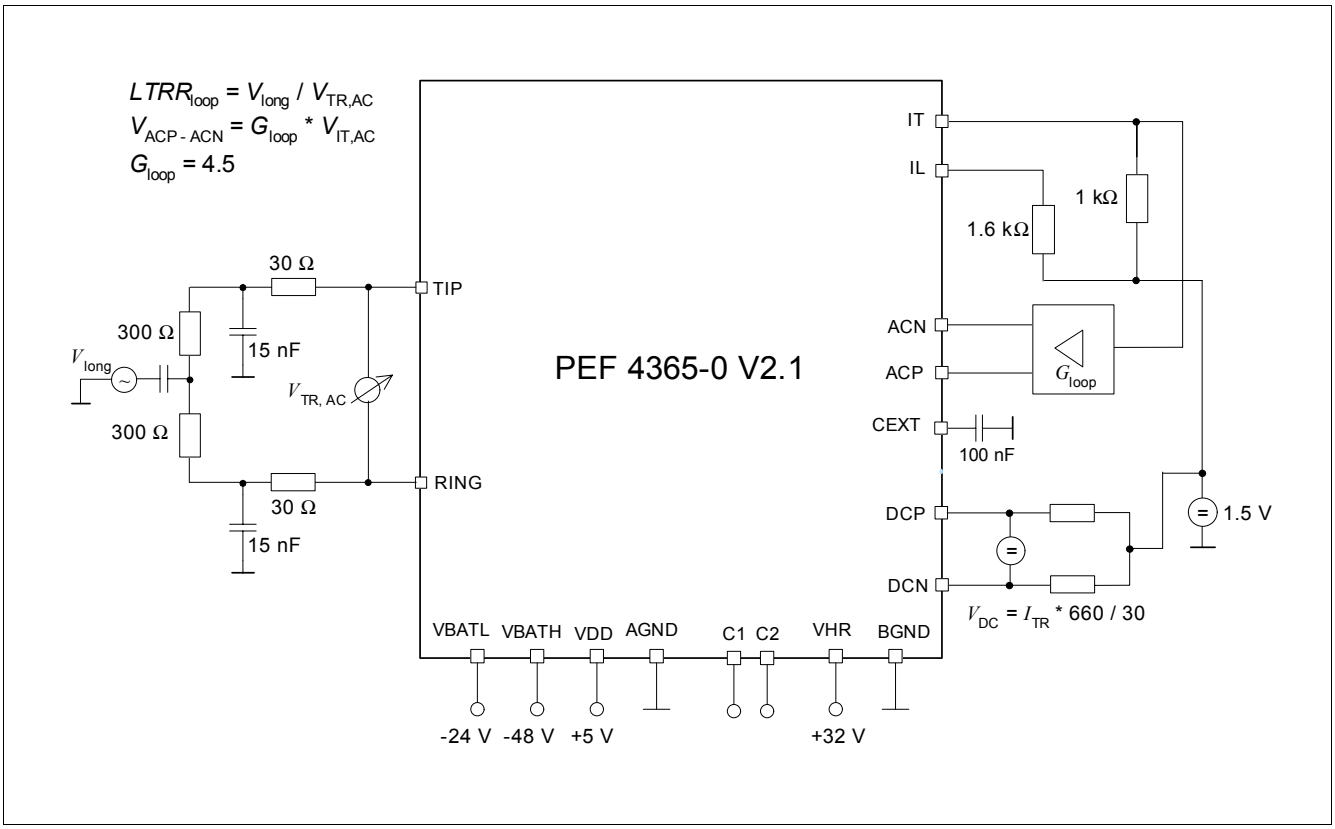


Figure 16 Longitudinal to Transversal Rejection Loop

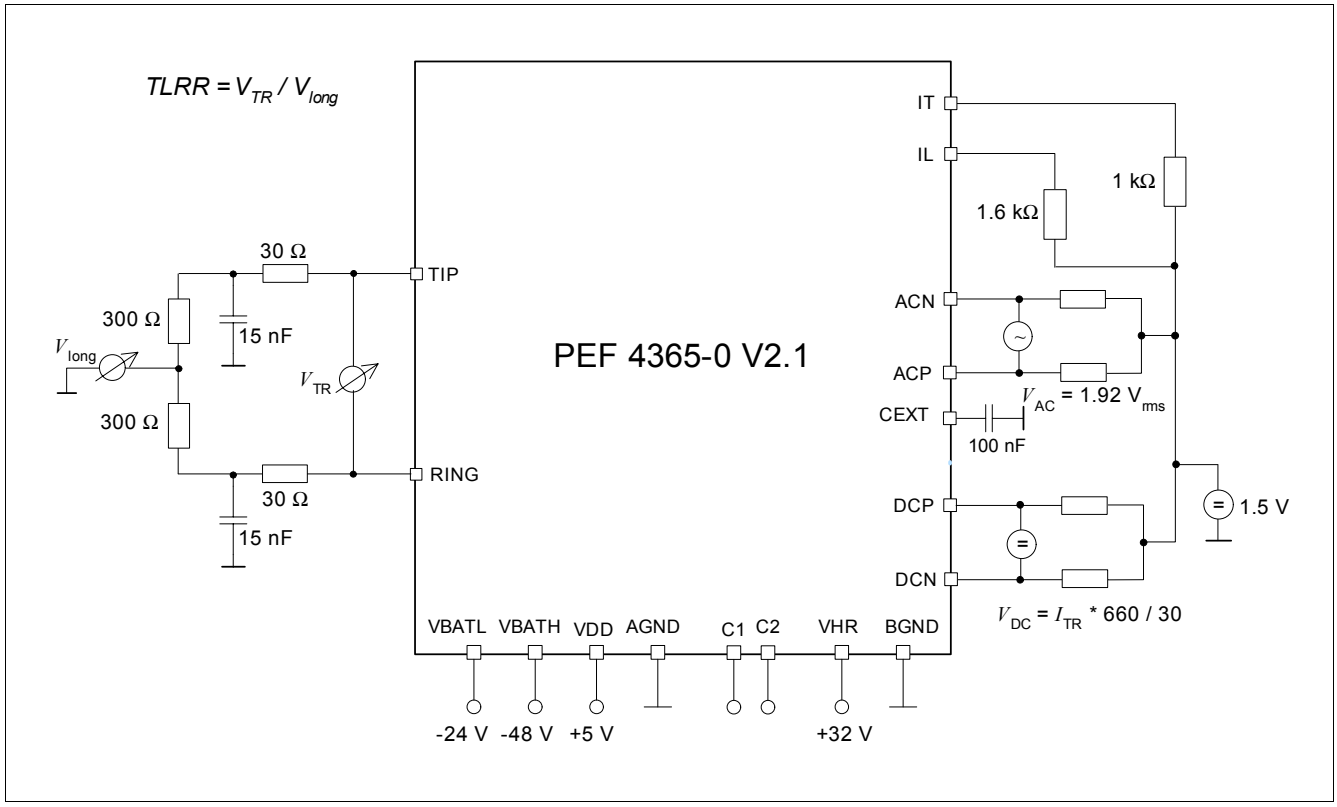


Figure 17 Transversal to Longitudinal Rejection

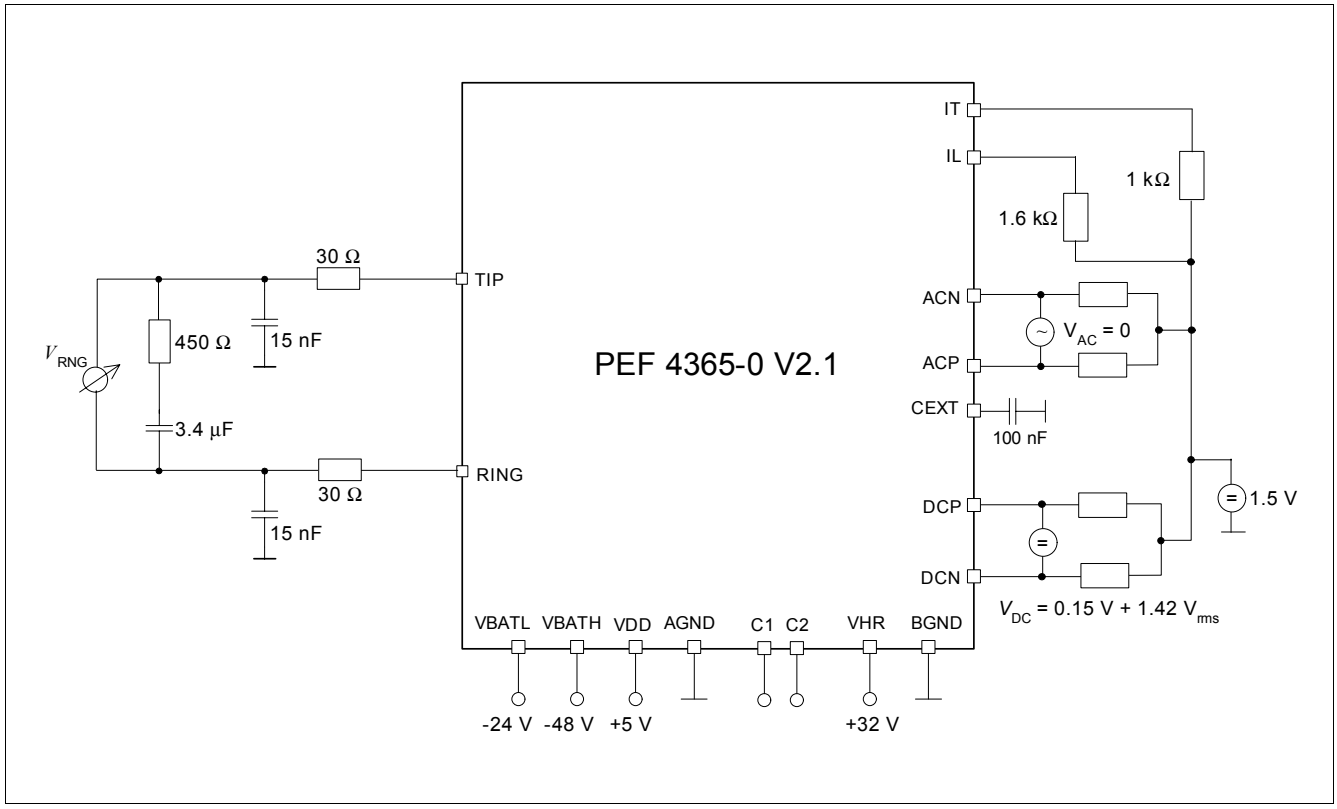


Figure 18 Ring Amplitude

6 Package Outlines

6.1 PG-DSO-36-15 Package

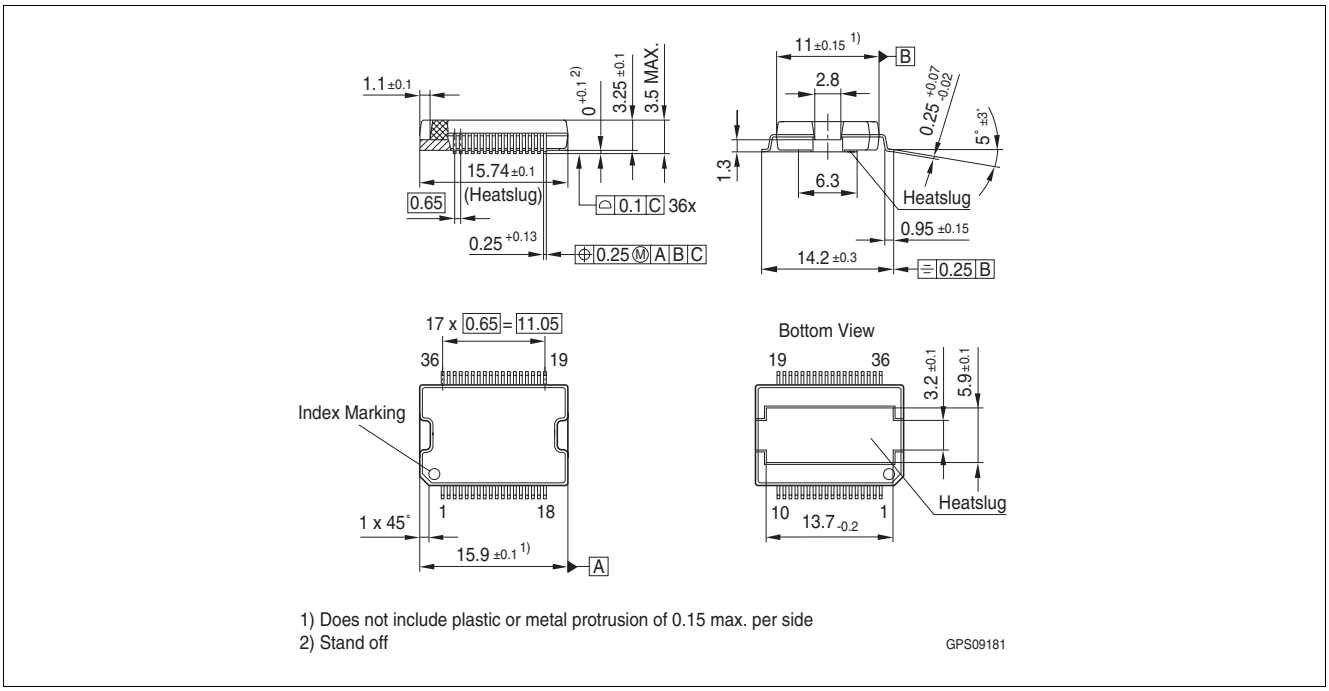


Figure 19 Package Outline for PG-DSO-36-15 (Plastic Green Dual Small Outline)

Notes

1. *Heatslug down version - pin counting counterclockwise (top view)*
2. *Dimensions in mm*

Attention: The heatslug is connected to VBATH via the chip substrate. Due to the high voltage of up to 150 V between VHR and VBATH, touching of the heatsink or any attached conducting part can be hazardous.

6.1.1 Recommended PCB Foot Print Pattern for PG-DSO-36-15 Package

The heatslug is soldered to the PCB according to **Figure 6.1.1**. For improved thermal behaviour the utilization of another PCB metal layer as an additional cooling area is recommended. These copper areas should be both electrically separated from each other and floating, i. e. they must not be connected with any other metallic part on the PCB.

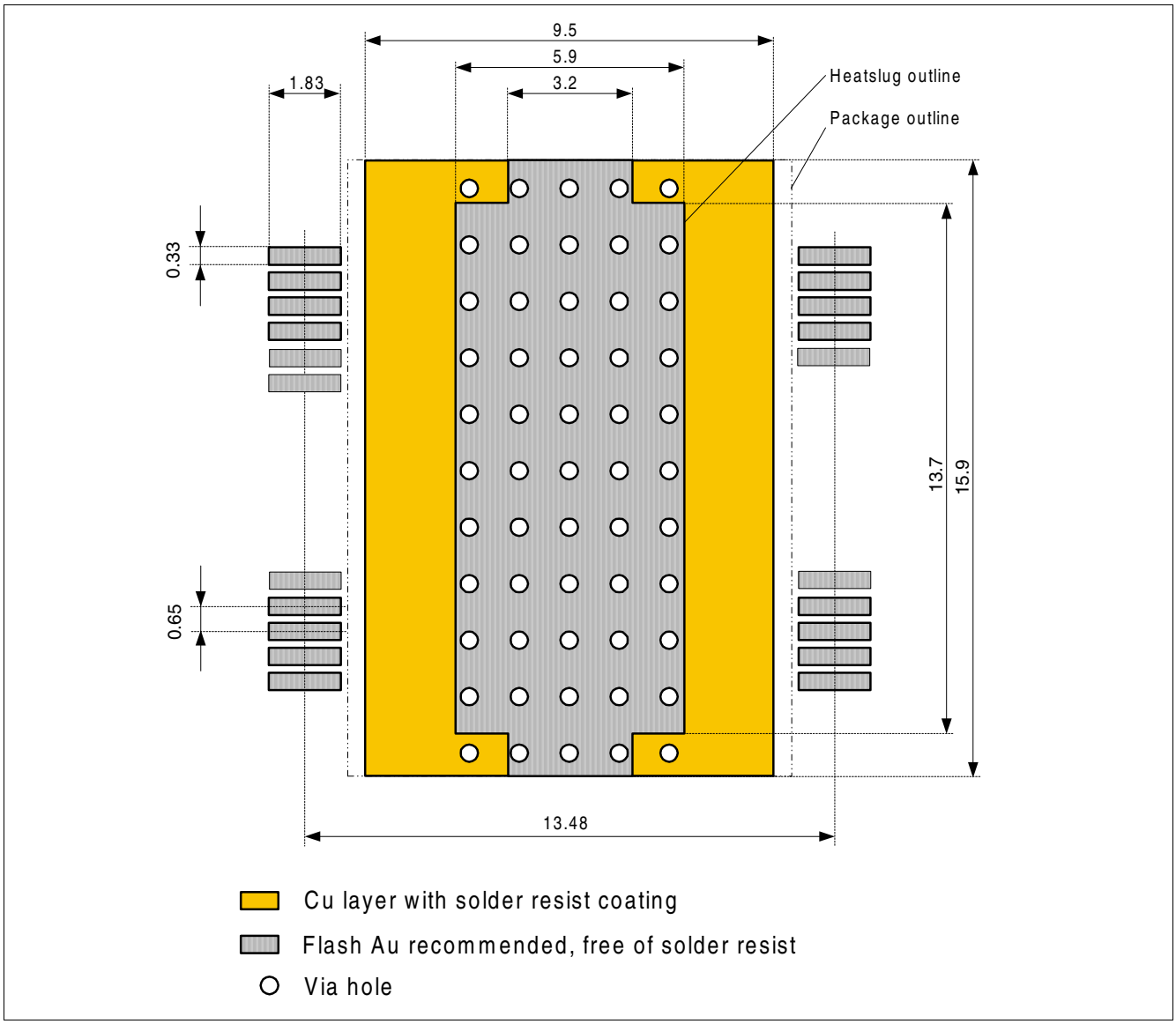


Figure 20 Footprint for PG-DSO-36-15

References

[1] SLIC-E/-E2 / TSLIC-E (PEF 4265/-2 / PEF 4365) Application Note “Protection for SLIC-E/-E2 against Overvoltages and Overcurrents according to ITU-T K.20/K.21/K.45” Rev. 1.0, 2004-06-29

[2] VINETIC® Version 1.4 Prel. Application Note External Components Rev. 2.0, 2005-09-06

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