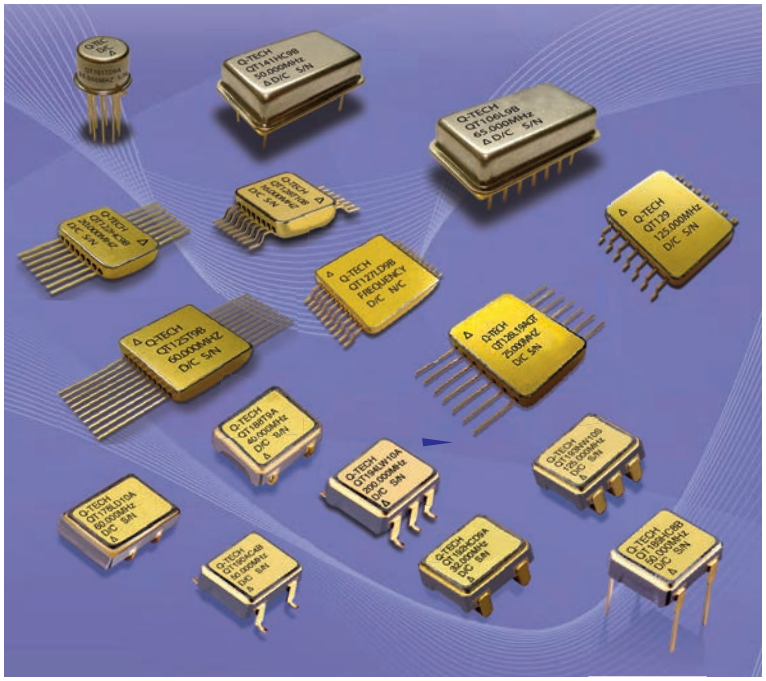
Q-TECH CORPORATION

CLASS B+ PRODUCTS

HIGH RELIABILITY HYBRID CRYSTAL CLOCK OSCILLATORS

2.5 to 5.0Vdc - 15kHz to 350MHz



Features

- Made in the USA
- ECCN: EAR99
- DFARS 252-225-7014 Compliant
  Electronic Component Exemption
- Broad frequency range from 15kHz to 350MHz
- Rugged 4-point mount (SMD ceramic) or 3 point mount (others) shock resistant
- ACMOS, LVCMOS, TTL, LVDS, LVPECL
- Tristate Output option (-D) except for LVDS and LVPECL standard
- Hermetically sealed package
- Fundamental and 3rd Overtone design
- Swept Quartz Crystal or Cultured Quartz Crystal
- Low phase noise and jitter
- Q-Tech does not use pure lead or pure tin in its products
- Custom screening and QCI available with MCM part number
- MIL-PRF-55310/9, /16, /21, /26, /27, /28, /30, /33, /34, /35, /37, /38, /39 equivalent

Ordering Information

(Sample part number)

QT188ACD10S-100.000MHz

Q	T	1	88	AC	D	10	S	-	100.000MHz

Lead Finish:

T	= Standard (*)
S	= Solder Dip (**)

Materials Level

1	= Rad Tolerant Die, Swept Quartz Crystal
2	= Rad Tolerant Die, Cultured Quartz Crystal
3	= Class B Die, Swept Quartz Crystal

Package:
See Pages 5, 25, 26, 27

Logic & Supply Voltage:

(All B+ Packages)		
AC	= ACMOS (****)	5.0V
HC	= HCMOS	5.0V
L	= LVCMOS	3.3V
T	= TTL	5.0V
N	= LVCMOS	2.5V
(QT122, QT128, QT125, QT127, QT193 & QT194 Only)		
LW	= LVDS	3.3V
NW	= LVDS	2.5V
LP	= LVPCL	3.3V
NP	= LVPECL	2.5V

Tristate Option:
(Standard offering in LW & NW)

Blank	= No Tristate
D	= Tristate

Output Frequency

Screening Option:

S	= Per MIL-PRF-38534, Class K (modified)
A	= Per MIL-PRF-55310, Level S
C	= Per MIL-PRF-55310, Level S (modified)
B	= Per MIL-PRF-55310, Level B (modified)
N	= Per NASA EEE-INST-002, Level 1
E	= Engineering Model

Frequency vs. Temperature Code (***):

2	=	± 65ppm at -55ºC to +125ºC
6	=	± 50ppm at -55ºC to +105ºC
7	=	± 75ppm at -55ºC to +125ºC
9	=	± 50ppm at -55ºC to +125ºC
10	=	±100ppm at -55ºC to +125ºC
11	=	± 50ppm at -40ºC to +85ºC
12	=	±100ppm at -40ºC to +85ºC
19	=	± 15ppm at 23ºC ± 1ºC ± 50ppm at -55ºC to +125ºC reference to F at 23ºC

(*) Gold Plated: 50µ ~ 80µ inches typ.
(**) Hot Solder Dip Sn60/Pb40 per MIL-PRF 55310 is optional for an additional cost
(***) Frequency stability vs. temperature codes may not be available in all frequencies
(****) HCMOS & TTL compatible

For Non-Standard requirements, contact Q-Tech Corporation at Sales@Q-Tech.com

GENERAL SPECIFICATION

1 SCOPE

1.1 Scope. This specification establishes the general quality and reliability requirements for a family of hybrid, hermetically sealed square wave, B+ crystal oscillators.

1.2 Part Number. The part number shall be as specified in the detail specification.

2 APPLICABLE DOCUMENTS

2.1 Specifications and Standards. Unless otherwise specified, the following documents shall be applicable to this specification to the extent specified herein.

SPECIFICATIONS

MIL-PRF-55310 Crystal Oscillators, General Specification For

MIL-PRF-38534 Hybrid Microcircuits, General Specification For

NASA EEE-INST-002 Instructions for EEE Parts Sections, Screenings, Qualifications and Ratings

STANDARDS

MIL-STD-202 Test Methods for Electronic and Electrical Component Parts

MIL-STD-883 Test Methods and Procedures for Microelectronics

2.2 Conflicting Requirements. In the event of conflict between requirements of this specification and other requirements of the applicable detail drawing, the precedence in which requirements shall govern, in descending order, is as follows:

a) Applicable Customer purchase order.

b) Applicable Customer detail drawing.

c) This specification.

d) Other specifications or standards referenced in 2.1 herein.

2.3 Customer Purchase Order Special Requirements. Additional special requirements shall be specified in the applicable Customer purchase order when additional requirements or modifications specified herein are needed for compliance to special program or product line requirements

3 REQUIREMENTS

3.1 Item Requirements. The individual item requirements shall be as specified herein and the detail specification.

3.2 Case Outline. The case outline shall be as specified in the detail specification. (See pages 25 to 27)

3.2.1 Terminal Connections. The terminal connections shall be as shown on page 25.

3.2.2 Lead Material and Finish. Lead material and finish shall be as shown on page 29.

3.2.3 Hot Solder Dip. Terminals can be solder dipped Sn60/Pb40 per MIL-PRF-55310 at additional cost. Prefix designated with an "S". See sample part number in the "Ordering Information" table.

3.2.4 Solderability. Leads shall meet the requirements of MIL-PRF-55310/38534 when tested.

3.3 Maximum Ratings. Unless otherwise specified, the maximum ratings shall as specified in the detail specification.

3.4 Electrical Performance Requirements. The electrical performance requirements shall be as specified herein and the applicable detail specification.

3.5 Design and Construction. The design and construction of the crystal oscillator shall be as specified herein. As a minimum, the oscillators shall meet the design and construction requirements of MIL-PRF-55310.

GENERAL SPECIFICATION (Cont'd)

3.5.1 Construction Technology. The device shall be constructed as a class 2-Type 1 hybrid oscillator of MIL-PRF-55310.

3.5.2 Workmanship. The device workmanship shall meet the requirements of MIL-PRF-55310.

3.5.3 Element Derating. All active and passive elements shall be derated in accordance with the applicable hybrid microcircuit element requirements of MIL-STD-975. Elements shall not operate in excess of derated values.

3.5.4 Active Elements. The active component shall be derived from lots that meet the Element Evaluation requirements of MIL-PRF-38534, Class K (for QT100 and QT200), and MIL-PRF-55310, Level B (QT300).

3.5.5 Quartz Crystal. Unless otherwise specified by the detail specification, the quartz crystal material for the QT100 and QT300 shall be swept synthetic, grade 2.2 or better and cultured quartz crystal for QT200.

3.5.6 Passive Elements. Element Evaluation shall be as a minimum in accordance with MIL-PRF-55310, Level S for QT100 and Level B for QT200 And QT300.

3.5.7 Crystal Mounting. The crystal element shall be three-point minimum mounted in such a manner as to assure adequate crystal performance when the oscillator is subjected to the environmental conditions specified herein.

3.5.8 Maximum Allowable Leak Rate. The maximum allowable leakage rate shall be as specified by MIL-STD-883, method 1014 based on the internal cavity volume. The hermetic seal (fine and gross leak) tests shall be in accordance with MIL-STD-883, Method 1014.

3.5.9 Weight. The maximum weight of the crystal oscillator shall be defined on page 29.

3.5.10 Delta Criteria. The crystal oscillator shall meet the parameter delta criteria post burn-in called out in the detail specification. The change in the parameter (delta) shall be calculated between the initial measurement and the present (interim or final) measurement.

3.5.11 Marking. Each unit shall be permanently marked with the manufacturer's name or symbol, part number, frequency, lot date code number, and serial number. The unit shall be marked with the outline of an equilateral triangle near pin 1 to show that it contains devices which are sensitive to electrostatic discharge.

3.5.12 Traceability. Material, element and process traceability requirements shall be as specified by MIL-PRF-55310.

3.5.13 Rework Provisions. Rework shall be in accordance with the provisions of MIL-PRF-55310.

4 QUALITY ASSURANCE PROVISIONS

4.1 Responsibility for Inspection. Unless otherwise specified in the contract or purchase order, the supplier shall be responsible for the performance of all inspection requirements as specified. Customer reserves the right to perform any of the inspections set forth in the specification where such inspections are deemed necessary to assure supplies and services conform to prescribed requirements, and to return any product failing to meet the specified requirements.

4.2 Screening. Hybrid crystal oscillators shall have been subjected to and successfully passed all the screening tests as applicable in Tables I, II, III, IV, V, VI.

4.2.1 Nondestructive Bondpull. 100% Non-destructive bondpull applicable to screening S, A, C, N.

4.2.2 Percent Defective Allowable (PDA). The percent defective allowable shall be 2% (Screening Option S, A, C) or 5% (Screening Option N) 10% (Screening Option B) or one device, whichever is greater. PDA accountability shall be based on failures occurring during the second half of burn-in only. PDA shall be applicable to the +25 ºC static parameters as specified in the delta criteria.

4.3 Quality Conformance Inspection (QCI). Shall be as outlined in the QCI section for each screening option here-in. All records shall be traceable to the lot number and unit serial number. Samples used for Group A that pass all tests may be delivered on contract prior to QCI completion.

GENERAL SPECIFICATION (Cont'd)

4.4 Customer Source Inspection. Provisions for periodic in-process source inspection by Customer shall be included in the supplier's manufacturing plan. Q-Tech will notify customer when the deliverable devices are ready for an in-process source inspection. The inspection points shall, as a minimum, be:

a) Pre crystal mount visual inspection. (Optional, applicable to all B+ ceramic packages)

b) Pre cap visual inspection.

c) Prior to shipment inspection.

4.5 Retention of Records. All records pertaining to the design, processes, incoming receiving, in-process inspections, screening and quality conformance inspection, product lot identification, product traceability, failure reports and analyses etc., shall be retained by the vendor for a period of seven years from the date of product shipment.

5 PREPARATION FOR DELIVERY

5.1 Packaging. The requirements for packaging shall be in accordance with MIL-PRF-55310.

5.2 Electrostatic Discharge Sensitivity. Meet MIL-STD-883, Method 3015, Class 1C HBM 1,999V

6 NOTES

6.1 Ordering Data. The contract or purchase order should specify the following:

a) Customer or Q-Tech part number.

b) Quality Conformance Inspection requirements.

c) Requirements for special technical documentation.

d) Test data requirements.

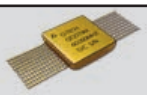
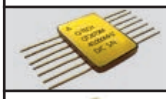
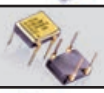
e) Special packaging.

f) Requirement for source inspection and notification.

6.2 Handling. The devices used must be handled with certain precautions to avoid damage due to electrostatic discharge.

6.3 Certificate of Conformance. Deliverables include a certificate of conformance to this specification, signed by an authorized representative of the manufacturer.

CLASS B+ PRODUCT OFFERINGS

Photo	Product QT	Package	Output Logic	Vdd (V)	Frequency Range	Outline	Pin Connection
	QT101 QT201 QT301	Transistor Outline (TO-5) 8 Pin	CMOS TTL	3.3Vdc, 5.0Vdc	450kHz to 85MHz	Page 25	Page 28
	QT106 QT206 QT306	Dual In-Line (DIP-14) 14 Pin	CMOS TTL	2.5Vdc, 3.3Vdc, 5.0Vdc	15kHz to 200MHz		
	QT141 QT241 QT341	Dual In-Line (DIP-14) 4 Pin	CMOS TTL	2.5Vdc, 3.3Vdc, 5.0Vdc	15kHz to 200MHz		
	QT142 QT242 QT342	Dual In-Line (DIP-14) 4 Pin	CMOS TTL	2.5Vdc, 3.3Vdc 5.0Vdc	15kHz to 200MHz		
	QT122 QT222 QT322	Flat Pack (FP) 16 Pin	CMOS TTL LVDS LVPECL	2.5Vdc, 3.3Vdc, 5.0Vdc	450kHz to 350MHz	Page 26	
	QT128 QT228 QT328	Flat Pack (FP) 16 Pin Formed Lead	CMOS TTL LVDS LVPECL	2.5Vdc, 3.3Vdc, 5.0Vdc	450kHz to 350MHz		
	QT125 QT225 QT325	Flat Pack (FP) 20 Pin	CMOS TTL LVDS LVPECL	2.5Vdc, 3.3Vdc, 5.0Vdc	15kHz to 350MHz		
	QT127 QT227 QT327	Flat Pack (FP) 20 Pin Formed Lead	CMOS TTL LVDS LVPECL	2.5Vdc, 3.3Vdc, 5.0Vdc	15kHz to 350MHz		
	QT126 QT226 QT326	Flat Pack (FP) 14 Pin	CMOS TTL LVDS	2.5Vdc, 3.3Vdc, 5.0Vdc	15kHz to 350MHz		
	QT129 QT229 QT329	Flat Pack (FP) 14 Pin Formed Lead	CMOS TTL LVDS	2.5Vdc, 3.3Vdc, 5.0Vdc	15kHz to 350MHz		
	QT178 QT278 QT378	Surface Mount (SMD) 4 Pin J-Lead	CMOS TTL	2.5Vdc, 3.3Vdc, 5.0Vdc	15kHz to 160MHz	Page 27	
	QT188 QT288 QT388	Surface Mount (SMD) 4 Pin J-Lead	CMOS TTL	2.5Vdc, 3.3Vdc, 5.0Vdc	450kHz to 160 MHz		
	QT189 QT289 QT389	Surface Mount (SMD) 4 Pin Thru-hole	CMOS TTL	2.5Vdc, 3.3Vdc, 5.0Vdc	450kHz to 160 MHz		
	QT190 QT290 QT390	Surface Mount (SMD) 4 Pin Gull Wing	CMOS TTL	2.5Vdc, 3.3Vdc, 5.0Vdc	450kHz to 160 MHz		
	QT192 QT292 QT392	Surface Mount (SMD) 4 Pin Formed Lead	CMOS TTL	2.5Vdc, 3.3Vdc, 5.0Vdc	450kHz to 160 MHz		
	QT193 QT293 QT393	Surface Mount (SMD) 6 Pin Formed Lead	CMOS TTL LVDS LVPECL	2.5Vdc, 3.3Vdc, 5.0Vdc	450kHz to 350 MHz		
	QT194 QT294 QT394	Surface Mount (SMD) 6 Pin Gull Wing	CMOS TTL LVDS LVPECL	2.5Vdc, 3.3Vdc, 5.0Vdc	450kHz to 350 MHz		

SCREENING OPTIONS SUMMARY

(Click on appropriate column to view screening details)

Test Description	Screening S Modified MIL-PRF-38534 Class K See Details in Table I (Pages 7- 8)	Screening A MIL-PRF-55310 Level S See Details in Table II (Page 9-10)	Screening C Modified MIL-PRF-55310 Level S See Details in Table III (Page 11-12)	Screening N NASA EEE-INST-002 Level 1 See Details in Table IV (Page 13-14)	Screening B Modified MIL-PRF-55310 Level B See Details in Table V (Page 15)	Screening E Engineering Model See Details in Table VI (Page 16)
Non Destructive Bond Pull	✓	✓	✓	✓	N/A	N/A
Internal Visual	✓	✓	✓	✓	✓	✓
Stabilization Bake	✓	✓	✓	✓	✓	✓
Thermal Shock	N/A	✓	✓	✓	N/A	N/A
Temperature Cycling	✓	✓	✓	✓	✓	N/A
Constant Acceleration	✓	✓	✓	✓	✓	N/A
Particle Impact Noise Detection (PIND)	✓	✓	✓	✓	✓	N/A
Pre Burn-In Electrical	✓	✓	✓	✓	✓	N/A
Burn-In # 1	✓ (160 Hrs at +125ºC)	✓ (240 Hrs at +125ºC)	✓ (240 Hrs at +125ºC)	✓ (240 Hrs at +125ºC)	✓ (160 Hrs at +125ºC)	N/A
Interim Electrical	✓	N/A	N/A	N/A	N/A	N/A
Burn-In # 2	✓ (160 Hrs at +125ºC)	N/A	N/A	N/A	N/A	N/A
Final Electrical	✓	✓	✓	✓	✓	✓
Percent Defective Allowance (PDA)	✓	✓	✓	✓	✓	N/A
Seal Fine Leak	✓	✓	✓	✓	✓	✓
Seal Gross Leak	✓	✓	✓	✓	✓	✓
Radiographic Inspection	✓	✓	N/A	N/A	N/A	N/A
Frequency Aging 30 days	✓	100% Group B Tested	N/A	✓	(QCI Group B)	N/A
External Visual	✓	✓	✓	✓	✓	✓

Group A Inspection (QCI)	✓ See Details in Table I-c	✓ MIL-PRF-55310 Level S	✓ MIL-PRF-55310 Level S	N/A	N/A	N/A
Group B Inspection (Aging)	N/A (in screening)	✓ MIL-PRF-55310 Level S	N/A	N/A (in screening)	N/A (optional in Group B)	N/A

Screening - Option S (Modified MIL-PRF-38534, Class K)

(Example: QT178LD10S-50.000MHz)

Table I

Test Description	MIL Standard	Method	Condition	Qty	Comments
Non Destructive Bond Pull	883	2023		100%	Completed During Assembly
Internal Visual	883	2017	Class K	100%	
Stabilization Bake	883	1008	C 48 hours at +150°C	100%	
Temperature Cycling	883	1010	C	100%	10 cycles
Constant Acceleration	883	2001	A	100%	Y1 direction only (5,000g's)
Particle Impact Noise Detection (PIND)	883	2020	B	100%	5 passes minimum (See Note 1)
Pre Burn-In Electrical	Refer to Table I-b and Detail Specification			100%	
Burn-In # 1	883	1015	+125°C for 160 hours	100%	With load and nominal supply voltage
Interim Electrical	Refer to Table I-b and Detail Specification			100%	
Burn-In # 2	883	1015	+125°C for 160 hours	100%	With load and nominal supply voltage
Final Electrical	Refer to Table I-a, I-b and Detail Specification			100%	
Percent Defective Allowance (PDA)	38534		Refer to table I-a below		PDA=2% (Supply Current only)
Seal Fine Leak	883	1014	A1 or B1	100%	(See Note 3)
Seal Gross Leak	883	1014	C or B2	100%	(See Note 3)
Radiographic Inspection	883	2012	Class S	100%	
Frequency Aging 30 days	55310		+70°C±3°C Refer to Table I-a below	100%	±1.5ppm max. for F≤150MHz ±2ppm max. for >150MHz < F ≤ 200MHz ±2.5ppm max. for F > 200MHz (See Note 2)
External Visual	883	2009		100%	

NOTES:

1. PIND testing shall be performed using five (5) independent passes and all failures found at the end of each pass are rejected. The survivors of the last pass are acceptable.
2. Normally frequency aging is up 30 days. However, aging may be ceased if value at 15 days is half than the limit of 30-day aging value, or continued up to 90 days if value exeeds 30 day aging limit.
3. Unless otherwise specificed info, Q-Tech uses conditions A1 and C for Fine and Gross Leak

Table I-a
Delta Limits

Tests	Parameters	Symbol	Delta Limits
Burn-In # 2	Supply current	Icc	±10% of initial reading
Life Test after 1,000 hours at +125°C	Supply current	Icc (Life)	±10% of initial reading
Frequency Aging after 30 days at +70°C	Output Frequency	Fo	Refer to detail spec.

Option S - Continued

Back To Summary

Screening - Option S (Continued)

Table I-b
Electrical Test - Measurement Requirements

Parameters	Pre BI at 25°C	Pre BI Low Temp	Pre BI High Temp	Interim BI at 25°C	Post BI at 25°C	Post BI Low Temp	Post BI High Temp
Output Frequency	✓	✓	✓	✓	✓	✓	✓
Frequency/Temperature Stability	✓	✓	✓	✓	✓	✓	✓
Frequency/Voltage Stability	✓				✓	✓	✓
Input Current	✓			✓	✓	✓	✓
Output Voltage	✓	✓	✓	✓	✓	✓	✓
Waveform	✓	✓	✓	✓	✓	✓	✓
Duty Cycle	✓	✓	✓	✓	✓	✓	✓
Rise and Fall Times	✓			✓	✓	✓	✓
Start-up Time	✓			✓	✓	✓	✓
Tristate Function	✓				✓	✓	✓

NOTE: Frequency Stability code 19, measure frequency parameter at +23°C ± 1°C.

Table I-c
Group A Inspection (100%)

Test Description	Condition
Supply Current	25°C and temperature extremes
Initial Accuracy at Reference Temperature	25°C and temperature extremes
Frequency - Temperature Stability	Over specified operating temperature range, measure output frequency at minimum ten equispaced points of the temperature extremes.
Frequency - Voltage Tolerance	25°C and temperature extremes
Output Voltages	
Duty Cycle (output waveform symmetry)	
Output Rise and Fall Times	
Start-up Time	
Tristate Function	

NOTE: Frequency Stability code 19, measure frequency parameter at +23°C ± 1°C.

QCI Options (per MIL-PRF-55310, level S)

- Group C Inspection per MIL-PRF-55310, Level S *(See details on Table X)*

QCI (per MIL-PRF-38534, Class K-Modified) (To be specified on Purchase Order)

- Group B Inspection per MIL-PRF-38534, Class K-Modified *(See details on Table VII)*
- Group C Inspection per MIL-PRF-38534, Class K-Modified (Delta Limits per Table I-a) *(See details on Table VIII)*
- Group D Inspection per MIL-PRF-38534, Class K-Modified *(See details on Table IX)*

Option S - Back
Back To Summary

Screening Option A (MIL-PRF-55310, Level S)

(Example: QT188ACD10A-40.000MHz)

Table II

Test Description	MIL Standard	Method	Condition	Qty	Comments
Non Destructive Bond Pull	883	2023		100%	Completed During Assembly
Internal Visual	883	2017 2032	Class K	100%	
Stabilization Bake	883	1008	C 48 hours at +150°C	100%	
Thermal Shock	883	1011	A	100%	
Temperature Cycling	883	1010	B	100%	10 cycles
Constant Acceleration	883	2001	A	100%	Y1 direction only (5,000g's)
Seal Fine and Gross Leak	883	1014	A1 or B1 C or B2	100%	See Note 2
Particle Impact Noise Detection (PIND)	883	2020	B	100%	
Pre Burn-In Electrical	Refer to Table II-a and Detail Specification			100%	
Burn-In	883	1015	+125°C for 240 hours minimum	100%	With load and nominal supply voltage
Final Electrical	Refer to Table II-a and Detail Specification			100%	
Percent Defective Allowance (PDA)	55310		Level S		PDA=2% (Supply Current only)
Radiographic Inspection	883	2012	Class S	100%	
External Visual	883	2009		100%	

NOTES:

1. 100% QCI Group A and Group B (Aging) Inspections are performed. See Table II-b
2. Unless otherwise specificed info, Q-Tech uses conditions A1 and C for Fine and Gross Leak

Table II-a
Electrical Test – Measurement Requirements

Parameters	Pre BI at 25°C	Pre BI Low Temp	Pre BI High Temp	Post BI at 25°C	Post BI Low Temp	Post BI High Temp
Output Frequency	✓	✓	✓	✓	✓	✓
Frequency/Temperature Stability	✓	✓	✓	✓	✓	✓
Frequency/Voltage Stability	✓			✓		
Input current	✓			✓	✓	✓
Output Voltage	✓	✓	✓	✓	✓	✓
Waveform	✓	✓	✓	✓	✓	✓
Duty cycle	✓	✓	✓	✓	✓	✓
Rise and Fall Times	✓			✓	✓	✓
Start-up Time	✓			✓	✓	✓
Tristate Function (if applicable)	✓			✓	✓	✓

NOTE: Frequency Stability code 19, measure frequency parameter at +23°C ± 1°C.

Option A - Continued

Back To Summary

Screening - Option A (Continued)

Table II-b
Group A Inspection (100%)

Test Description	Condition
Supply Current	25°C and temperature extremes
Initial Accuracy at Reference Temperature	25°C and temperature extremes
Frequency - Temperature Stability	Over specified operating temperature range, measure output frequency at minimum ten equispaced points of the temperature extremes.
Frequency - Voltage Tolerance	25°C and temperature extremes
Output Voltages	
Duty Cycle (output waveform symmetry)	
Output Rise and Fall Times	
Start-up Time	
Tristate Function	

NOTE: Frequency Stability code 19, measure frequency parameter at +23ºC ± 1ºC.

QCI (per MIL-PRF-55310, Level S) (To be specified on Purchase Order)

- Group C Inspection per MIL-PRF-55310, Level S *(See details on Table X)*

QCI (per MIL-PRF-38534, Class K-Modified) (To be specified on Purchase Order)

- Group B Inspection per MIL-PRF-38534, Class K-Modified *(See details on Table VII)*
- Group C Inspection per MIL-PRF-38534, Class K-Modified (Delta Limits per Table I-a) *(See details on Table VIII)*
- Group D Inspection per MIL-PRF-38534, Class K-Modified *(See details on Table IX)*

Option A - Back
Back To Summary

Screening Option C (Modified MIL-PRF-55310, Level S)

(Example: QT188ACD10C-40.000MHz)

Table III

Test Description	MIL Standard	Method	Condition	Qty	Comments
Non Destructive Bond Pull	883	2023		100%	Completed During Assembly
Internal Visual	883	2017 2032	Class K	100%	
Stabilization Bake	883	1008	C 48 hours at +150°C	100%	
Thermal Shock	883	1011	A	100%	
Temperature Cycling	883	1010	B	100%	10 cycles
Constant Acceleration	883	2001	A	100%	Y1 direction only (5,000g's)
Seal Fine and Gross Leak	883	1014	A1 or B1 C or B2	100%	See Note 2
Particle Impact Noise Detection (PIND)	883	2020	B	100%	
Pre Burn-In Electrical	Refer to Table III-a and Detail Specification			100%	
Burn-In	883	1015	+125°C for 240 hours minimum	100%	With load and nominal supply voltage
Final Electrical	Refer to Table III-a and Detail Specification			100%	
Percent Defective Allowance (PDA)	55310		Level S		PDA=2% (Supply Current only)
External Visual	883	2009		100%	

NOTES:

1. 100% QCI Group A Inspections is performed. See Table III-b
2. Unless otherwise specificed info, Q-Tech uses conditions A1 and C for Fine and Gross Leak

Table III-a
Electrical Test – Measurement Requirements

Parameters	Pre BI at 25ºC	Pre BI Low Temp	Pre BI High Temp	Post BI at 25ºC	Post BI Low Temp	Post BI High Temp
Output Frequency	✓	✓	✓	✓	✓	✓
Frequency/Temperature Stability	✓	✓	✓	✓	✓	✓
Frequency/Voltage Stability	✓			✓		
Input current	✓			✓	✓	✓
Output Voltage	✓	✓	✓	✓	✓	✓
Waveform	✓	✓	✓	✓	✓	✓
Duty cycle	✓	✓	✓	✓	✓	✓
Rise and Fall Times	✓			✓	✓	✓
Start-up Time	✓			✓	✓	✓
Tristate Function (if applicable)	✓			✓	✓	✓

NOTE: Frequency Stability code 19, measure frequency parameter at +23ºC ± 1ºC.

Option C - Continued

Back To Summary

Screening - Option C (Continued)

Table III-b
Group A Inspection (100%)

Test Description	Condition
Supply Current	25°C and temperature extremes
Initial Accuracy at Reference Temperature	25°C and temperature extremes
Frequency - Temperature Stability	Over specified operating temperature range, measure output frequency at minimum ten equispaced points of the temperature extremes.
Frequency - Voltage Tolerance	25°C and temperature extremes
Output Voltages	
Duty Cycle (output waveform symmetry)	
Output Rise and Fall Times	
Start-up Time	
Tristate Function	

NOTE: Frequency Stability code 19, measure frequency parameter at +23ºC ± 1ºC.

QCI (per MIL-PRF-55310, Level S) (To be specified on Purchase Order)

- Group C Inspection per MIL-PRF-55310, Level S *(See details on Table X)*

QCI (per MIL-PRF-38534, Class K-Modified) (To be specified on Purchase Order)

- Group B Inspection per MIL-PRF-38534, Class K-Modified *(See details on Table VII)*
- Group C Inspection per MIL-PRF-38534, Class K-Modified (Delta Limits per Table I-a) *(See details on Table VIII)*
- Group D Inspection per MIL-PRF-38534, Class K-Modified *(See details on Table IX)*

Option C - Back
Back To Summary

Screening Option N (NASA EEE-INST-002)

(Example: QT188ND10A-40.000MHz)

Table IV

Test Description	MIL Standard	Method	Condition	Qty	Comments
Non Destructive Bond Pull	883	2023		100%	Completed During Assembly
Internal Visual	883	2017 2032	Class K	100%	
Stabilization Bake	883	1008	C 48 hours at +150°C	100%	
Thermal Shock	883	1011	A	100%	
Temperature Cycling	883	1010	B	100%	10 cycles
Constant Acceleration	883	2001	A	100%	Y1 direction only (5,000g's)
Particle Impact Noise Detection (PIND)	883	2020	B	100%	
Pre Burn-In Electrical	Refer to Table IV-a and Detail Specification			100%	
Burn-In	883	1015	+125°C for 240 hours minimum	100%	With load and nominal supply voltage
Final Electrical	Refer to Table IV-a and Detail Specification			100%	
Frequency Aging	55310		70°C± 3°C	100%	30 Days
Percent Defective Allowance (PDA)	55310		Level S		PDA=5% (Supply Current only Frequency Aging)
Radiographic Inspection	883	2012	Class S	100%	
Seal Fine and Gross Leak	883	1014	A1 or B1 C or B2	100%	See Note 2
External Visual	883	2009		100%	

NOTES:

1. 100% QCI Group A and Group B (Aging) Inspections are performed. See Table II-b
2. Unless otherwise specificed info, Q-Tech uses conditions A1 and C for Fine and Gross Leak

Table IV-a
Electrical Test – Measurement Requirements

Parameters	Pre BI at 25°C	Pre BI Low Temp	Pre BI High Temp	Post BI at 25°C	Post BI Low Temp	Post BI High Temp
Output Frequency	✓	✓	✓	✓	✓	✓
Frequency/Temperature Stability	✓	✓	✓	✓	✓	✓
Frequency/Voltage Stability	✓			✓		
Input current	✓			✓	✓	✓
Output Voltage	✓	✓	✓	✓	✓	✓
Waveform	✓	✓	✓	✓	✓	✓
Duty cycle	✓	✓	✓	✓	✓	✓
Rise and Fall Times	✓			✓	✓	✓
Start-up Time	✓			✓	✓	✓
Tristate Function (if applicable)	✓			✓	✓	✓

Option A - Continued

Back To Summary

Screening - Option N (Continued)

Table IV-b
Additional Electrical Measurements

Test Description	Condition
Osscillator Supply Voltage	Measure voltage magnitude, tolerance, polarity, regulation, peak to peak ripple, repple frequency and noise across oscillator input terminals with specified load
Initial Accuracy at Reference Temperature	Apply over voltage 20% above maximum specified supply voltage for 1 minute with no performance degradation
Frequency - Temperature Stability	25°C and temperature extremes

NOTE: Frequency Stability code 19, measure frequency parameter at +23ºC ± 1ºC.

Table IV-c
Additional Electrical Measurements

Test Description	Test Methods and Conditions	Quantity
GROUP 1 Frequency Aging	MIL-PRF-55310, par. 4.8.35	8(0)
GROUP 2 Vibration Sine Mechanical Shock	MIL-STD 202, Method 204 and MIL-PRF-55310, par. 4.8.39.1 MIL-STD-202, Method 213 and MIL-PRF-55310, par 4..8.41	8(0)
GROUP 3 Thermal Shock	MIL-STD-202, Method 107 and MIL-PRF-55310, par. 4.8.45	4(0)
GROUP 4 Resistance to Soldering Heat Moisture Resistance Terminal Strength Solderability Resistance to Solvents	MIL-STD 202, Method 210 and MIL-PRF-55310, par. 4.8.49 MIL-STD 202, Method 106 and MIL-PRF-55310, par. 4.8.50 MIL-STD 202, Method 211 and MIL-PRF-55310, par 4.8.52 MIL-STD 202, Method 208, each lead MIL-STD 202, Method 215	2(0)
GROUP 5 Interval Water Vapor Content	MIL-STD 883, Method 1018, 5000ppm at 100°C	3(0) or 5(1)

NOTE: 1) Sample units shall have previously met all requirements of the previous test of Table IV-a.
2) Sample for this group came from Group 1 samples

Option A - Back
Back To Summary

Screening - Option B (Modified MIL-PRF-55310, Level B)

(Example: QT178LD10B-50.000MHz)

Table V

Test Description	MIL Standard	Method	Condition	Qty	Comments
Internal Visual	883	2017	Class H	100%	Completed During Assembly
Stabilization Bake	883	1008	C 48 hours at +150°C	100%	
Temperature Cycling	883	1010	B	100%	10 cycles
Constant Acceleration	883	2001	A	100%	Y1 direction only (5,000g's)
Particle Impact Noise Detection (PIND)	883	2020	B	100%	
Pre Burn-In Electrical	Refer to Table V-a and Detail Specification			100%	
Burn-In	883	1015	+125°C for 160 hours	100%	With load and nominal supply voltage
Final Electrical	Refer to Table V-a and Detail Specification			100%	
Percent Defective Allowance (PDA)	38534				PDA=10% (Supply Current only)
Seal Fine Leak	883	1014	A1	100%	
Seal Gross Leak	883	1014	C	100%	
External Visual	883	2009		100%	

NOTES:
1. 100% Group A QCI test per MIL-PRF-55310

Table V-a
Electrical Test - Measurement Requirements

Parameters	Pre BI at 25°C	Pre BI Low Temp	Pre BI High Temp	Post BI at 25°C	Post BI Low Temp	Post BI High Temp
Output frequency	✓	✓	✓	✓	✓	✓
Frequency/temperature stability	✓	✓	✓	✓	✓	✓
Frequency/voltage stability	✓			✓		
Input current	✓			✓	✓	✓
Output voltage	✓	✓	✓	✓	✓	✓
Waveform	✓	✓	✓	✓	✓	✓
Duty cycle	✓	✓	✓	✓	✓	✓
Rise and fall times	✓			✓	✓	✓
Start up time	✓			✓	✓	✓
Tristate Function (if applicable)	✓			✓	✓	✓

NOTE: Frequency Stability code 19, measure frequency parameter at +23°C ± 1°C.

QCI (per MIL-PRF-55310, Level B or S) (To be specified on Purchase Order)

- Group B (AgingTest)
- Group C *(See details on Table X)*

QCI Options (per MIL-PRF-38534, Class K-Modified)

- Group B Inspection per MIL-PRF-38534, Class K-Modified *(See details on Table VII)*
- Group C Inspection per MIL-PRF-38534, Class K-Modified (Delta Limits per Table II) *(See details on Table VIII)*
- Group D Inspection per MIL-PRF-38534, Class K-Modified *(See details on Table IX)*

Back To Summary

Screening Option E (Engineering Model)

(Example: QT122ACD9E-16.000MHz)

Table VI

Test Description	MIL Standard	Method	Condition	Qty	Comments
Internal Visual	883	2017	Class H	100%	Completed During Assembly
Stabilization Bake	883	1008	C 48 hours at +150°C	100%	
Seal Fine and Gross Leak	883	1014	A1, C	100%	
Final Electrical	Refer to Table V-a and Detail Specification			100%	
Frequency vs. Temperature Stability	55310	Measure output frequency at 10 equispaced points minimum of the specified operating temperature range		100%	
External Visual	883	2009		100%	

Table VI-a
Electrical Test – Measurement Requirements

Parameters	Final at 25°C	Final Low Temp	Final High Temp
Output frequency	✓	✓	✓
Frequency/temperature stability	✓	✓	✓
Frequency/voltage stability	✓	✓	✓
Input current	✓	✓	✓
Output voltage	✓	✓	✓
Waveform	✓	✓	✓
Duty cycle	✓	✓	✓
Rise and fall times	✓	✓	✓
Start up time	✓	✓	✓
Tristate Function (if applicable)	✓	✓	✓

NOTE: Frequency Stability code 19, measure frequency parameter at +23ºC ± 1ºC.

Engineering model oscillators will have the same design and manufacturing processes as to the flight units. Finished units will be tested over the operating temperature range. No screening test and/or QCI are required.

Back To Summary

Electrical Performance Characteristics 15kHz to 85MHz

Maximum Ratings

(For FACT +5Vdc and +3.3Vdc CMOS Outputs Using 54ACT3301NSC)

Parameters	Symbol	Min.	Max.	Units
Supply Voltage	Vdd	-0.5	+7	V
Operating Temperature	Top.	-55	+125	°C
Storage Temperature	Tstg	-62	+125	°C
Lead Solder Temperature			260/10	°C/seconds
Package Thermal Resistance	ΘJc		50	°C/W
Junction Temperature			+175	ºC

Recommended Operating Conditions

Electrical Parameter	Test Conditions	Limits				Notes
		Min.	Nom.	Max.	Units	
Frequency Range	+3.3Vdc	.015 .450		80 70	MHz MHz	DIP, FPack Other Packages
	+5.0Vdc	.015 .450		85 85	MHz MHz	DIP, FPack Other Packages
Frequency/Temperature Stability	See temperature codes	-55	+25	+125	°C	(See Note 1)
Supply Voltage		2.97 4.5	3.3 5.0	3.63 5.5	Vdc Vdc	
Input Current at 3.63Vdc	Measured without load at maximum Vdd			3 6 10 20 30	mA	15k-<500kHz 500k-<16MHz 16M-<32MHz 32M-<60MHz 60M-80MHz
Input Current at 5.5Vdc	Measured without load at maximum Vdd			20 25 35 45	mA	15k-<16MHz 16M-<32MHz 32M-<60MHz 60M-85MHz
Output Voltage VOL				Vdd x 0.1 0.4 (TTL)	Vdc	(See Note 4)
Output Voltage VOH		Vdd x 0.9 2.4 (TTL)			Vdc	(See Note 4)
Output Waveform		Square Wave			N/A	
Rise and Fall Time	10% to 90% (0.8V to 2.0V for TTL)			6 3	ns ns	15k-<36MHz 36M-85MHz (See Note 4)
Duty Cycle	50% of output (1.4Vdc for TTL)	45 40	50	55 60	% %	15k-<16MHz 16M-85MHz (See Note 4 & 5)
Load		15pF//10kΩ (CMOS) 6TTL to 10TTL (TTL)				Per MIL-PRF-55310 loads (See Note 4)
Frequency Aging after 30 days	70°C±3°C			±1.5	ppm	(See Note 2)
Frequency Aging/Year	70°C±3°C			±5	ppm	(See Note 3)
Start-up Time	100µs ramp			10	ms	
Output Enable VIH		2.2			Vdc	
Output Disable VIL				0.8	Vdc	Output High Impedance
Frequency Voltage Tolerance	over ±10% change in supply voltage	-2 -4		+2 +4	ppm	TO, DIP, FP All Ceramic Packages

NOTES:

1. Frequency stability compared to nominal frequency including initial accuracy at 25°C, load, and supply variations ±10%. Frequency Stability code 19, measure frequency parameter at +23ºC ± 1ºC.
2. Normally frequency aging is up 30 days. However, aging may be ceased if value at 15 days is half than the limit of 30-day aging value, or continued up to 90 days if value exeeds 30 day aging limit for screening options "S".
3. Aging is ±5ppm after first year and ±2ppm/year thereafter.
4. AC logic (+5Vdc) is HCMOS & TTL compatible.
5. For ACMOS, Duty Cycle is set at 50% output waveform level.

Electrical Performance Characteristics 40MHz to 200MHz CMOS

(For BiCMOS +2.5Vdc, +3.3Vdc CMOS Ouputs)

Maximum Ratings

Parameters	Symbol	Min.	Max.	Units
Supply Voltage	Vdd	-0.5	+5	V
Operating Temperature	Top.	-55	+125	°C
Storage Temperature	Tstg	-62	+125	°C
Lead Solder Temperature			260/10	°C/seconds
Package Thermal Resistance	ΘJc		50	°C/W
Junction Temperature			+150	ºC

Recommended Operating Conditions

Electrical Parameter	Test Conditions	Limits				Notes
		Min.	Nom.	Max.	Units	
Frequency Range	+2.5Vdc	40		133	MHz	DIP, FP20
		70		133		DIP, FP16, FP20
	+3.3Vdc	70		165		All Ceramic Packages
		70		200		DIP, FP16, FP20
Frequency/Temperature Stability	See temperature codes	-55	+25	+125	°C	(See Note 1)
Supply Voltage		2.97	3.3	3.63	Vdc	
Input Current	Measured without load at maximum Vdd			30 40 50	mA	40M-<100MHz 100M-<130MHz 130M-200MHz
Output Voltage VOL				Vdd x 0.1	Vdc	
Output Voltage VOH		Vdd x 0.9			Vdc	
Output Waveform		Square Wave			N/A	
Rise and Fall Time	10% to 90%			3	ns	
Duty Cycle	50% of output	40		60	%	
Load		15pF//10kΩ				
Frequency Aging after 30 days	70°C±3°C			±1.5 ±2	ppm ppm	40M-150MHz >150M-200MHz (See Note 2)
Frequency Aging/Year	70°C±3°C			±5	ppm	(See Note 3)
Start-up Time	100µs ramp			10	ms	
Output Enable VIH		2.2			Vdc	
Output Disable VIL				0.8	Vdc	Output High Impedance
Frequency Voltage Tolerance	over ±10% change in supply voltage	-2		+2	ppm	DIP, FP16, FP20
		-4		+4		All Ceramic Packages

NOTES:

1. Frequency stability compared to nominal frequency including initial accuracy at 25°C, load, and supply variations ±10%. Frequency Stability code 19, measure frequency parameter at +23ºC ± 1ºC.
2. Normally frequency aging is up 30 days. However, aging may be ceased if value at 15 days is half than the limit of 30-day aging value, or continued up to 90 days if value exeeds 30 day aging limit for screening option “S”.
3. Aging is ±5ppm after first year and ±2ppm/year thereafter.

Electrical Performance Characteristics 40MHz to 350MHz LVDS

(For BiCMOS +2.5Vdc and +3.3Vdc LVDS Ouputs)

Maximum Ratings

Parameters	Symbol	Min.	Max.	Units
Supply Voltage	Vdd	-0.5	+5	V
Operating Temperature	Top.	-55	+125	°C
Storage Temperature	Tstg	-62	+125	°C
Lead Solder Temperature			260/10	°C/seconds
Package Thermal Resistance	ΘJc		50	°C/W
Junction Temperature			+150	ºC

Recommended Operating Conditions

Electrical Parameter	Test Conditions	Limits				Notes
		Min.	Nom.	Max.	Units	
Frequency Range	+2.5Vdc	80		250	MHz	FP16, FP20, QT93, QT94
	+3.3Vdc	40		350		
Frequency/Temperature Stability	See temperature codes	-55	+25	+125	°C	(See Note 1)
Supply Voltage		3.135 2.375	3.3 2.5	3.465 2.625	Vdc Vdc	
Input Current	Measured without load at maximum Vdd			66	mA	
Output Voltage VOL		0.90	1.1		Vdc	
Output Voltage VOH			1.45	1.65	Vdc	
Differential Output Voltage (VOD)		247	330	454	mv	
Offset Voltage (VOS)		1.125	1.125	1.375	V	
Output Waveform		Square Wave			N/A	
Rise and Fall Time	20% to 80%			600	ps	
Duty Cycle	50% of output	45	50	55	%	
Load		100Ω (Connected between Q & QNOT)			Ω	
Frequency Aging after 30 days	70°C±3°C			±1.5 ±2 ±3	ppm ppm ppm	40M-150MHz >150M-<200MHz 200M-350MHz (See Note 2)
Frequency Aging/Year	70°C±3°C			±5	ppm	(See Note 3)
Start-up Time	100µs ramp			10	ms	
Output Enable VIH		0.7xVcc			Vdc	
Output Disable VIL				0.3xVcc	Vdc	Output High Impedance

NOTES:

1. Frequency stability compared to nominal frequency including initial accuracy at 25°C, load, and supply variations ±5%. Frequency Stability code 19, measure frequency parameter at +23ºC ± 1ºC.
2. Normally frequency aging is up 30 days. However, aging may be ceased if value at 15 days is half than the limit of 30-day aging value, or continued up to 90 days if value exeeds 30 day aging limit.
3. Aging is ±5ppm after first year and ±2ppm/year thereafter.

Electrical Performance Characteristics 80MHz to 250MHz LVPECL

(For BiCMOS +2.5Vdc and +3.3Vdc LVPECL Ouputs)

Maximum Ratings

Parameters	Symbol	Min.	Max.	Units
Supply Voltage	Vdd	-0.5	+5	V
Operating Temperature	Top.	-55	+125	°C
Storage Temperature	Tstg	-62	+125	°C
Lead Solder Temperature			260/10	°C/seconds
Package Thermal Resistance	ΘJc		50	°C/W
Junction Temperature			+150	ºC

Recommended Operating Conditions

Electrical Parameter	Test Conditions	Limits				Notes
		Min.	Nom.	Max.	Units	
Frequency Range	+2.5Vdc	80		200	MHz	FP16, FP20, QT93, QT94
	+3.3Vdc	80		250		
Frequency/Temperature Stability	See temperature codes	-55	+25	+125	°C	(See Note 1)
Supply Voltage		3.135 2.375	3.3 2.5	3.465 2.625	Vdc Vdc	
Input Current	Measured without load at maximum Vdd		60	88	mA	
Output Voltage VOL	3.3V	1.470	1.600	1.745	Vdc	
	2.5V	1.415	1.495	1.620	Vdc	
Output Voltage VOH	3.3V	2.215	2.295	2.420	Vdc	
	2.5V	0.670	0.800	1.195	Vdc	
Output Waveform		Square Wave			N/A	
Rise and Fall Time	20% to 80%		300	700	ps	
Duty Cycle	50% of output	45	50	55	%	
Load		50Ω to Vcc-2V			Ω	or Thevenin equivalent
Output Swing Vopp	3.3V peak to peak of single output waveform	0.4			V	
	2.5V peak to peak of single output waveform	0.2			V	
Frequency Aging after 30 days	70°C±3°C			±1.5 ±2 ±3	ppm ppm ppm	80M-150MHz >150M-<200MHz 200M-250MHz (See Note 2)
Frequency Aging/Year	70°C±3°C			±5	ppm	(See Note 3)
Start-up Time	100µs ramp			10	ms	
Output Enable VIH		0.7xVcc			Vdc	
Output Disable VIL				0.3xVcc	Vdc	Output High Impedance

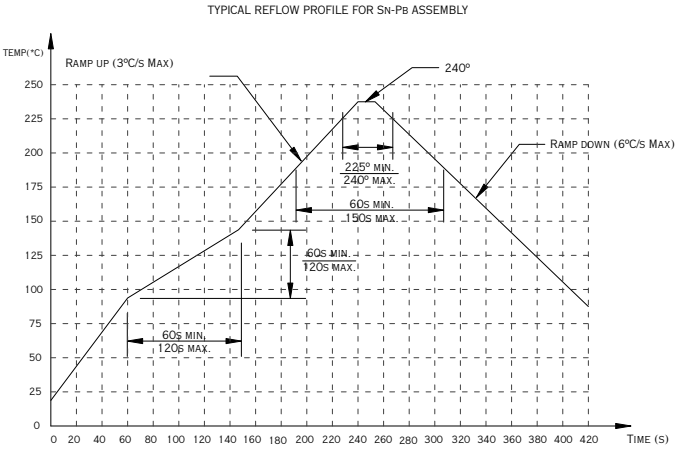
NOTES:

1. Frequency stability compared to nominal frequency including initial accuracy at 25°C, load, and supply variations ±5%. Frequency Stability code 19, measure frequency parameter at +23ºC ± 1ºC.
2. Normally frequency aging is up 30 days. However, aging may be ceased if value at 15 days is half than the limit of 30-day aging value, or continued up to 90 days if value exeeds 30 day aging limit for screening options “S” only.
3. Aging is ±5ppm after first year and ±2ppm/year thereafter.

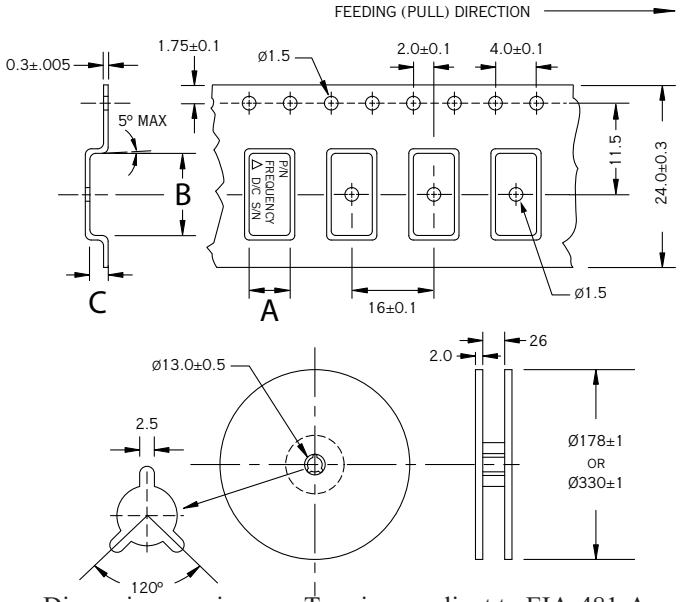
Reflow Profile

The five transition periods for the typical reflow process are:

- Preheat
- Flux activation
- Thermal equalization
- Reflow
- Cool down



Embossed Tape and Reel Information



Dimensions are in mm. Tape is compliant to EIA-481-A.

QT	A	B	C
QT178	10.01 ±0.1	14.53 ±0.1	4.80 ±0.1
QT190	9.470 ±0.1	11.92 ±0.1	6.16 ±0.1
QT188, QT192, QT193	7.747 ±0.1	9.271 ±0.1	4.699 ±0.1

Reel size vs. quantity:

Reel size (Diameter in mm)	Qty per reel (pcs)	
	QT178	QT188,QT190,QT192, QT193
178	250	150
330	1000	800

Environmental Specifications

Q-Tech Standard Screening/QCI (MIL-PRF-38534 or MIL-PRF55310) is available for all of our B+ Products. Q-Tech can also customize screening and test procedures to meet your specific requirements. The B+ product is designed and processed to exceed the following test conditions:

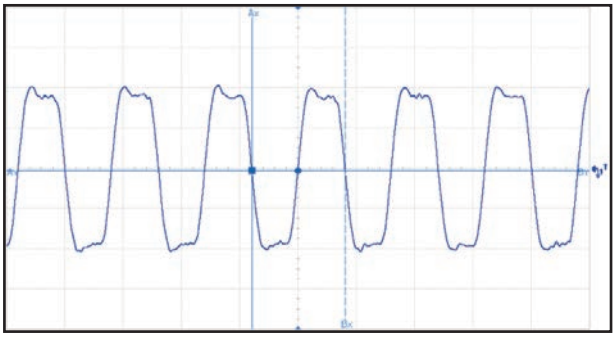
Environmental Test	Test Conditions
Temperature cycling	MIL-STD-883, Method 1010, Cond. B or Cond. C
Constant acceleration	MIL-STD-883, Method 2001, Cond. A, Y1
Seal: Fine and Gross Leak	MIL-STD-883, Method 1014, Cond. A and C
Burn-in	160 hours, 125°C with load
Aging	30 days, 70°C, ±1.5ppm max
Vibration sinusoidal	MIL-STD-202, Method 204, Cond. D
Shock, non operating	MIL-STD-202, Method 213, Cond. I (See Note 1)
Thermal shock, non operating	MIL-STD-202, Method 107, Cond. B
Ambient pressure, non operating	MIL-STD-202, 105, Cond. C, 5 minutes dwell time minimum
Resistance to solder heat	MIL-STD-202, Method 210, Cond. B
Moisture resistance	MIL-STD-202, Method 106
Terminal strength	MIL-STD-202, Method 211, Cond. C
Resistance to solvents	MIL-STD-202, Method 215
Solderability	MIL-STD-202, Method 208
ESD Classification	MIL-STD-883, Method 3015, Class 1C HBM 1,999V
Moisture Sensitivity Level	J-STD-020, MSL=1

Note 1: Additional shock results successfully passed on 16MHz, 40MHz, and 80MHz

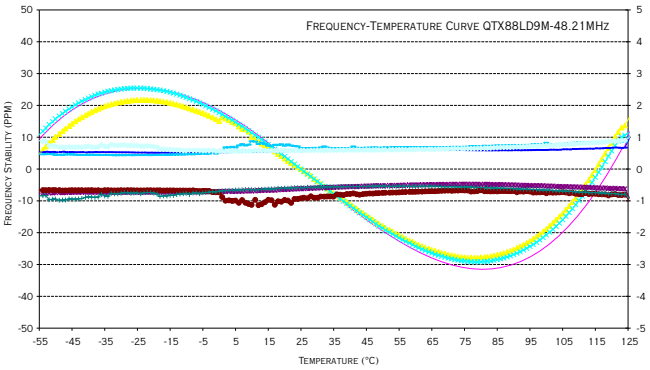
- Shock 850g peak, half-sine, 1 ms duration (MIL-STD-202, Method 213, Cond. D modified)
- Shock 1,500g peak, half-sine, 0.5ms duration (MIL-STD-883, Method 2002, Cond. B)
- Shock 36,000g peak, half-sine, 0.12 ms duration (QT188, QT190 & QT192, QT193)

Please contact Q-Tech for higher shock requirements

Differential Output of a QT93NW10M-312.500MHz



Frequency vs. Temperature Curve



Thermal Characteristics

The heat transfer model in a hybrid package is described in figure 1.

Heat spreading occurs when heat flows into a material layer of increased cross-sectional area. It is adequate to assume that spreading occurs at a 45° angle.

The total thermal resistance is calculated by summing the thermal resistances of each material in the thermal path between the device and hybrid case.

$$RT = R1 + R2 + R3 + R4 + R5$$

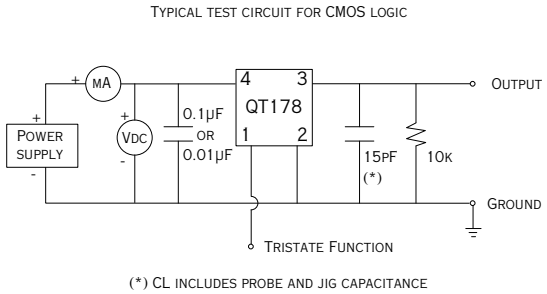
The total thermal resistance RT (see figure 2) between the heat source (die) to the hybrid case is the Theta Junction to Case (Theta JC) in°C/W.

- Theta junction to case (Theta JC) for this product is 30°C/W.
- Theta case to ambient (Theta CA) for this part is 100°C/W.
- Theta Junction to ambient (Theta JA) is 130°C/W.

Maximum power dissipation PD for this package at 25°C is:

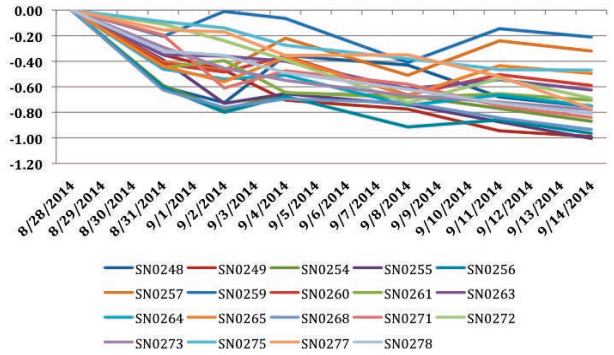
- PD(max) = (TJ (max) – TA)/Theta JA
- With TJ = 175°C (Maximum junction temperature of die)
- PD(max) = (175 – 25)/130 = 1.15W

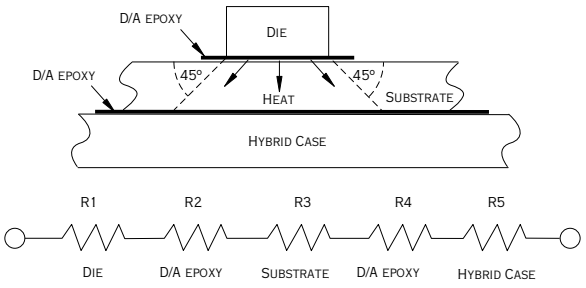
Test Circuit



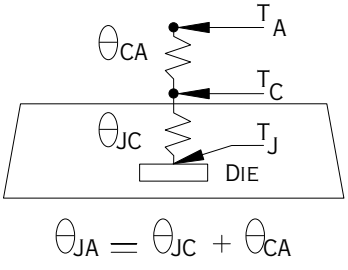
The Tristate function on pin 1 has a built-in pull-up resistor typical 50kΩ, so it can be left floating or tied to Vdd without deteriorating the electrical performance.

15-Day Aging of a QT122L10S-200MHz





(Figure 1)



(Figure 2)

Jitter And Phase Noise

As data rate increases, effect of jitter becomes critical with its budget tighter. Jitter is the deviation of a timing event of a signal from its ideal position. Jitter is complex and is composed of both random jitter (RJ) and deterministic jitter (DJ) components.
Random Jitter (RJ) is theoretically unbounded and Gaussian in distribution, while Deterministic Jitter (DJ) is bounded and does not follow any predictable distribution.

Q-Tech utilizes the EZJIT Plus jitter analysis software with Noise reduction software that supports Agilent Infinium real-time oscilloscope. Measure at its maximum sampling rate 40Gs/s and memory depth, we can separate the signal's aggregate total jitter into Random Jitter (RJ) and Deterministic Jitter (DJ).

Since Random Jitter is unbounded and Gaussian in style, the Total Jitter is a function of Bit Error Rate (BER).

TJ = RJ + DJ

Where:

RJ = RJ(rms) x 2α + DJ(p-p)

BER	α
10E-3	3.1
10E-6	4.75
10E-9	6
10E-12	7.0

Typical Jitter at BER=10E-12

Frequency	DJ (p-p) ps	RJ (rms) ps	TJ (ps)
22.118MHz	31	3.36	78.9
100MHz	1.61	1.99	21.1
125MHz	1.34	1.23	18.9
200MHz	1.53	2.04	30.7

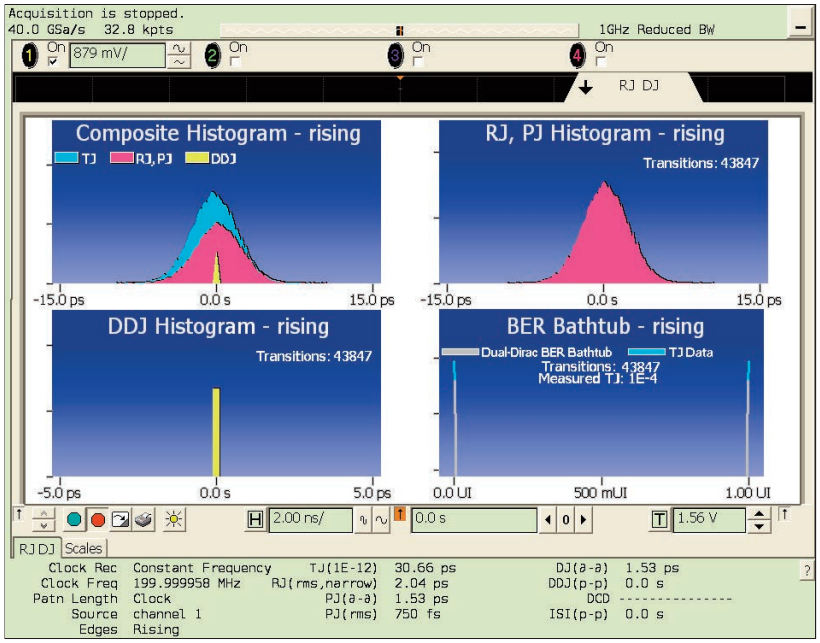


Figure 1: Jitter Analysis of a QT128L10S-200MHz

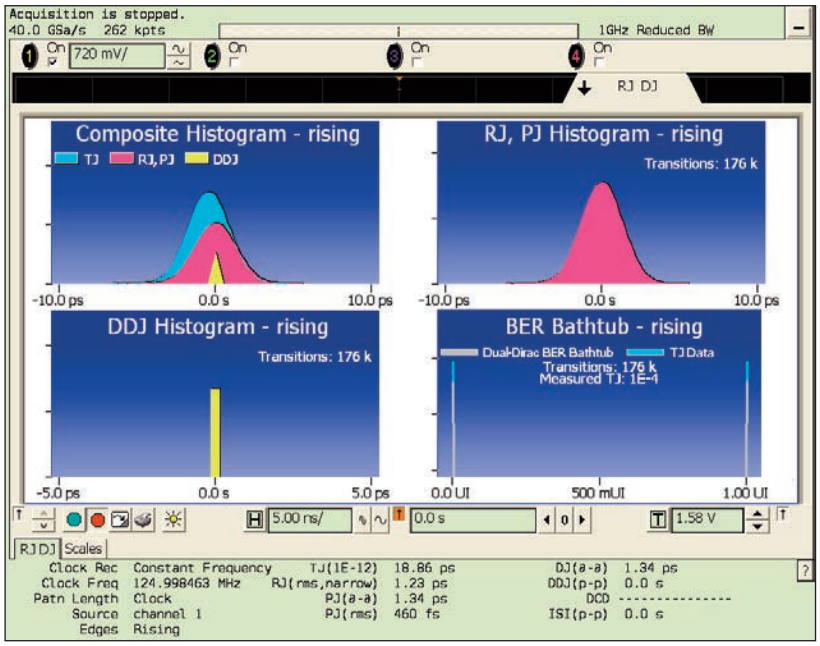


Figure 2: Jitter Analysis of a QT192LD9S-125MHz

Typical Phase Noise

Frequency	10Hz	100Hz	1kHz	10kHz	100kHz	1MHz	Phase Jitter (ps) *
22.118MHz	-90	-125	-150	-157	-162	-162	0.151
100MHz	-76	-101	-128	-140	-143	-149	0.120
125MHz	-74	-101	-131	-143	-145	-150	0.118
200MHz	-73	-99	-124	-134	-145	-148	0.121

(*) Integrated from 1kHz to 20MHz

Phase Noise and Phase Jitter Integration

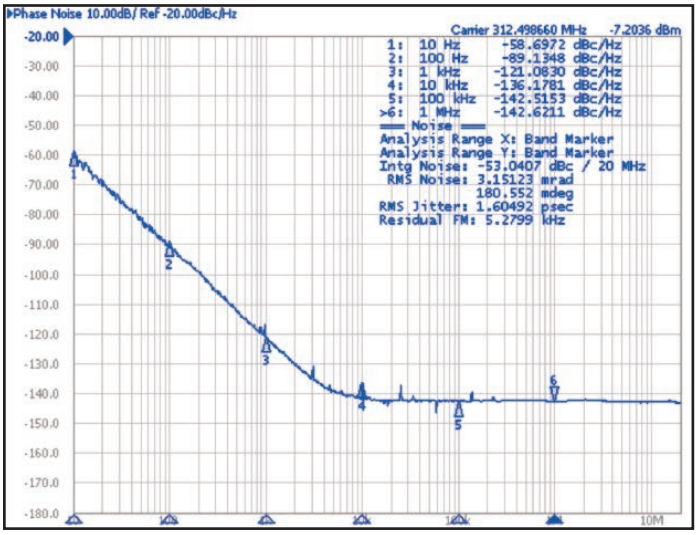
Phase noise is measured in the frequency domain, and is expressed as a ratio of signal power to noise power measured in a 1Hz bandwidth at an offset frequency from the carrier, e.g. 10Hz, 100Hz, 1kHz, 10kHz, 100kHz, etc. Phase noise measurement is made with an Agilent E5052A Signal Source Analyzer (SSA) with built-in outstanding low-noise DC power supply source. The DC source is floated from the ground and isolated from external noise to ensure accuracy and repeatability.

In order to determine the total noise power over a certain frequency range (bandwidth), the time domain must be analyzed in the frequency domain, and then reconstructed in the time domain into an rms value with the unwanted frequencies excluded. This may be done by converting L(f) back to Sφ(f) over the bandwidth of interest, integrating and performing some calculations.

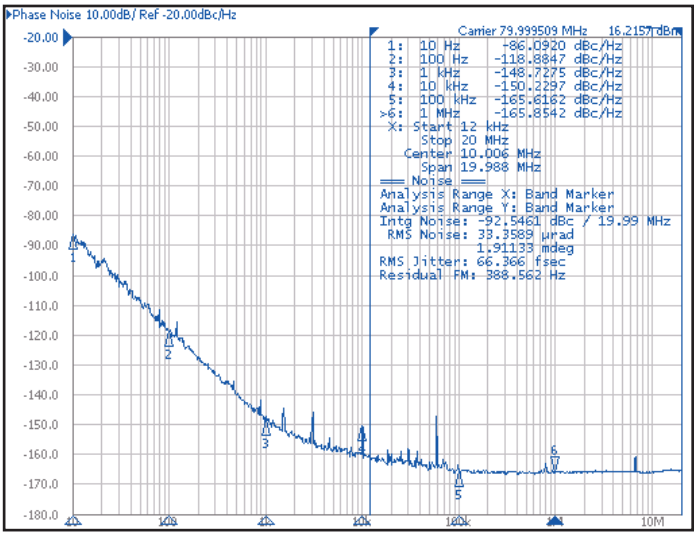
Symbol	Definition
$\int \mathcal{L}(f)$	Integrated single side band phase noise (dBc)
$S\varphi(f)=(180/\Pi)x\sqrt{2\int \mathcal{L}(f)df}$	Spectral density of phase modulation, also known as RMS phase error (in degrees)
RMS jitter = Sφ (f)/(fosc.360°)	Jitter(in seconds) due to phase noise. Note Sφ (f) in degrees.

The value of RMS jitter over the bandwidth of interest, e.g. 10kHz to 20MHz, 10Hz to 20MHz, represents 1 standard deviation of phase jitter contributed by the noise in that defined bandwidth.

Figure below shows a typical Phase Noise/Phase jitter of a QT193NW10M, 2.5Vdc, 312MHz and QT178AC9A, 5.0Vdc, 80MHz clock at offset frequencies 10Hz to 1MHz, and phase jitter integrated over the bandwidth of 12kHz to 1MHz.



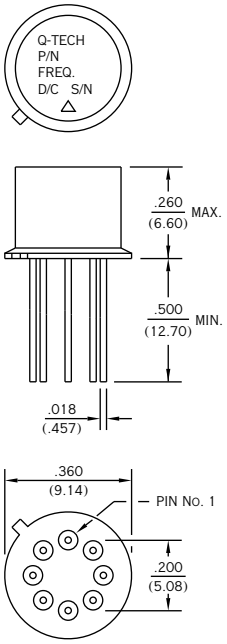
QT193NW10M, 2.5Vdc, 312MHz



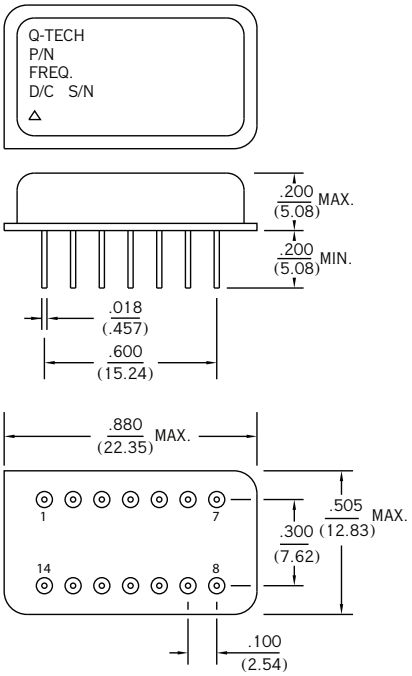
QT178AC9A, 5.0Vdc, 80MHz

Package Outline - Dimensions are in inches (mm)

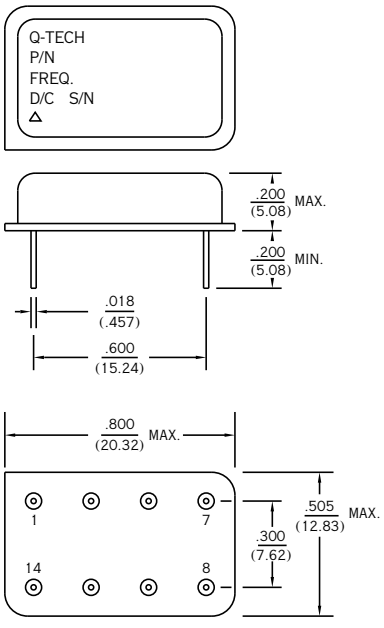
QT101



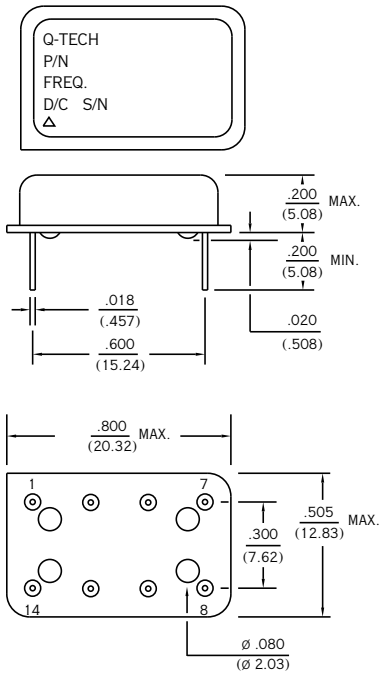
QT106



QT141

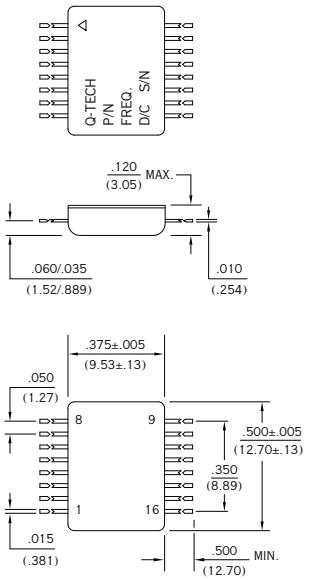


QT142

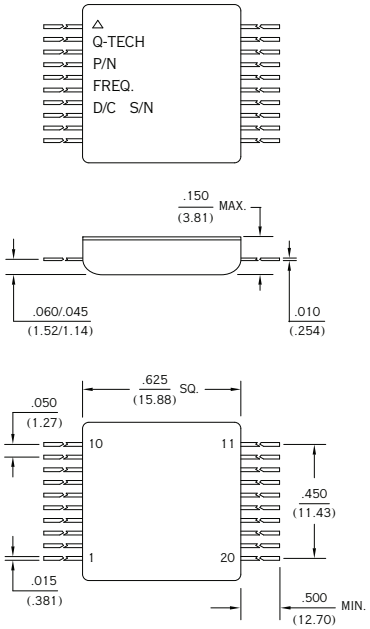


Package Outline - Dimensions are in inches (mm) (Continued)

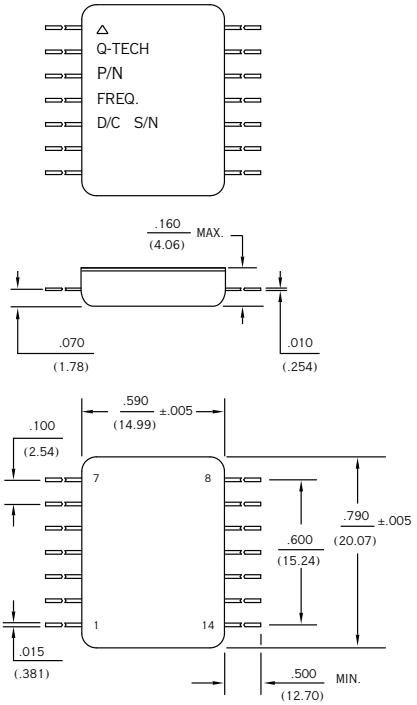
QT122



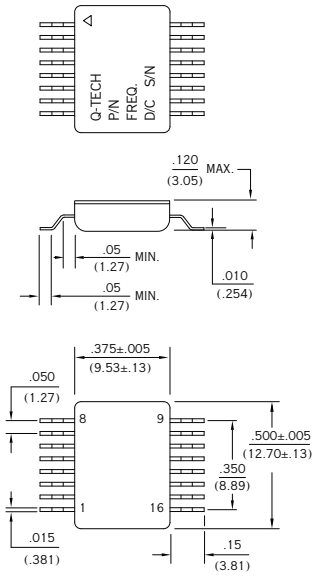
QT125



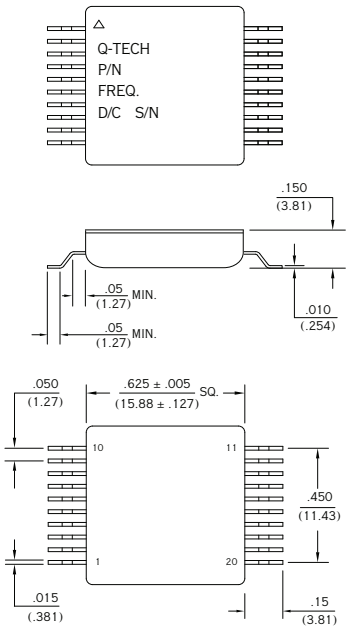
QT126



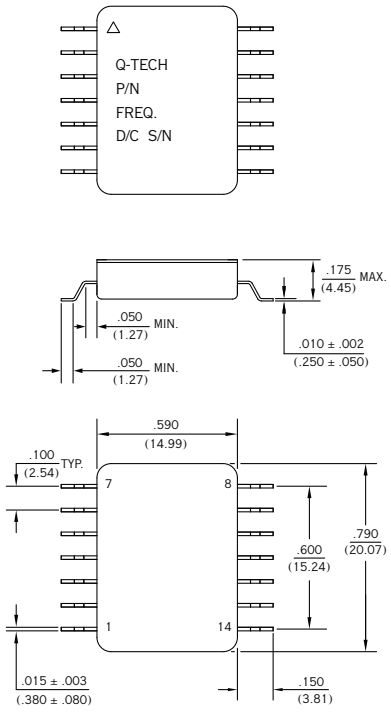
QT128



QT127

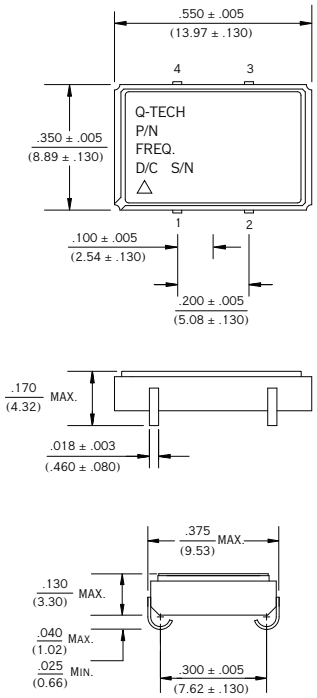


QT129

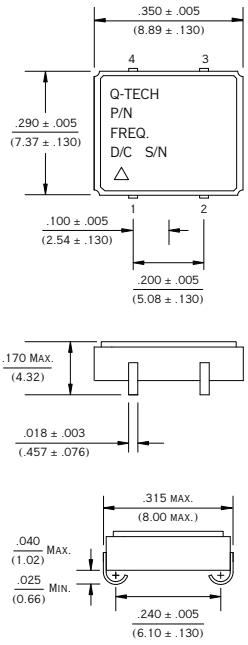


Package Outline - Dimensions are in inches (mm)
(Continued)

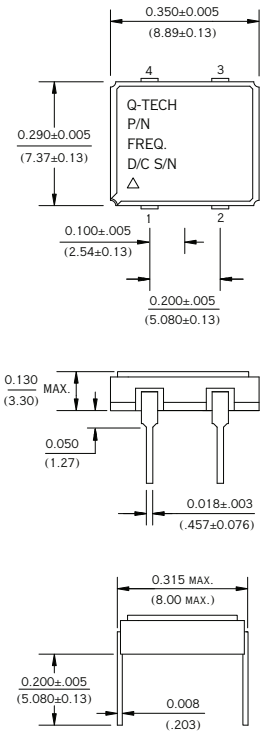
QT178



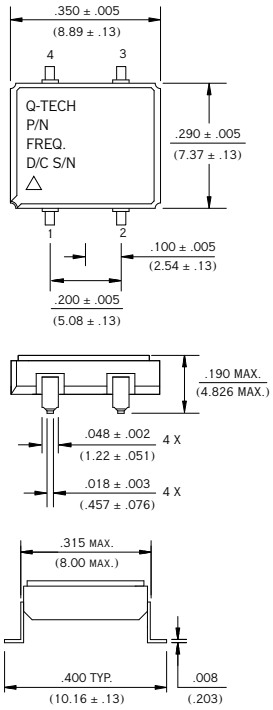
QT188



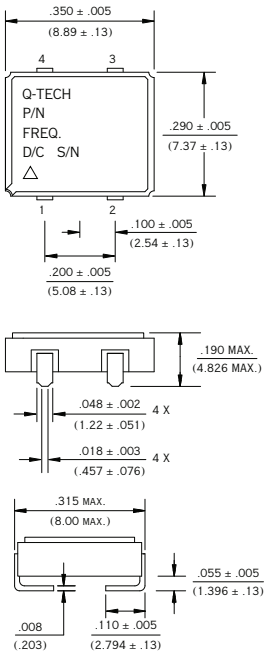
QT189



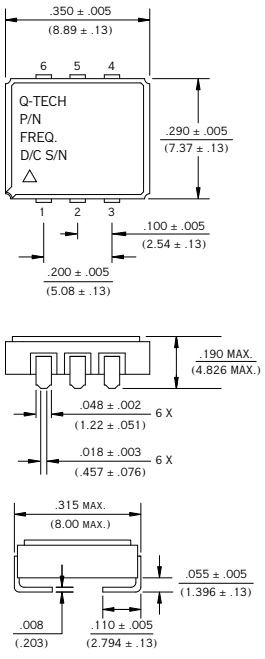
QT190



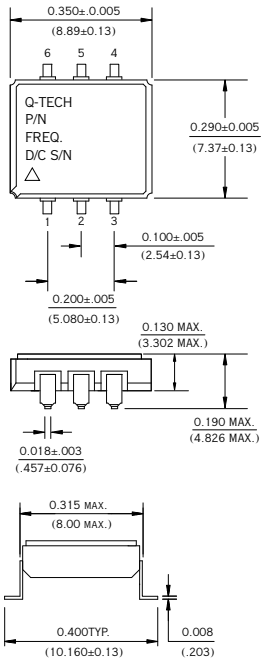
QT192



QT193



QT194



Pin Connections

QT#	Vcc	GND	Case	Output	E/D or N/C	Equivalent MIL-PRF-55310 Configuration
 QT101	8	4	4	5	2	/9 = QT1T
 QT106	14	7	7	8	1	/16 = QT6T /26A = QT6HC
 QT141	14	7	7	8	1	/26B = QT41HC
 QT142	14	7	7	8	1	N/A
 QT122	8	9	9	10 (CMOS, TTL) 10 & 11 (LVDS) 10 & 11 (LVPECL)	7	N/A
 QT128	8	9	9	10 (CMOS, TTL) 10 & 11 (LVDS) 10 & 11 (LVPECL)	7	N/A
 QT125	13	10	10	11 (CMOS TTL) 11 & 12 (LVDS) 11 & 12 (LVPECL)	12 8	/21 = QT25T
 QT127	13	10	10	11 (CMOS TTL) 11 & 12 (LVDS) 11 & 12 (LVPECL)	12 8	N/A
 QT126	14	7	7	8	6	N/A
 QT129	14	7	7	8	6	N/A
 QT178	4	2	2	3	1	/27 = QT78HCD /28 = QT78TD /30 = QT78LD
 QT188	4	2	2	3	1	/33 = QT88HCD /34 = QT88LD /35 = QT88ND
 QT189	4	2	2	3	1	N/A
 QT190	4	2	2	3	1	N/A
 QT192	4	2	2	3	1	/37 = QT92HCD /38 = QT92LD /39 = QT92ND
 QT193	6	3	3	4 (CMOS, TTL) 4 & 5 (LVDS)	1	N/A
 QT194	6	3	3	4 (CMOS, TTL) 4 & 5 (LVDS) 4 & 5 (LVPECL)	1	N/A

Package Information

QT101
- Package material (header and leads): Kovar
- Lead finish: Gold Plated – 50µ ~ 80µ inches
  Nickel Underplate – 100µ ~ 250µ inches
- Cover: Pure Nickel Grade A
- Package to lid attachment: Resistance weld
- Weight: 2.0g typ., 4.96g max.

QT106, QT141, QT142
- Package material (header and leads): Kovar
- Lead finish: Gold Plated – 50µ ~ 80µ inches
  Nickel Underplate – 100µ ~ 250µ inches
- Package to lid attachment: Resistance weld
- Cover: (DIP-14): Pure Nickel Grade A
- Weight: (DIP-14): 3.4g typ.,14.2g max.

QT122, QT125, QT126, QT127, QT128, QT129:
- Package material (Header and Leads): Kovar
- Lead finish: Gold Plated – 50µ ~ 80µ inches
  Nickel Underplate – 100µ ~ 250µ inches
- Cover: Kovar, Gold Plated – 50µ ~ 100µ inches
  Nickel Underplate – 70µ ~ 90µ inches
- Package to lid attachment: Seam weld
- Weight: 2.0g typ., 4.0g max.

QT178, QT188, QT189, QT190, QT192, QT193, QT194
- Package material: 90% AL2O3
- Lead material: Kovar
- Lead finish: Gold Plated: 50µ ~ 80µ inches
  Nickel Underplate: 100µ ~ 250µ inches
- Weight: QT178: 1.1g typ., 3.0g max.
  QT188, QT189, QT190, QT192, QT193, QT194: .6g typ., 3.0g max.

Packaging Options

QT101, QT106, QT141, QT142
- Standard packaging in black foam

QT122, QT125, QT126, QT127, QT128, QT129
- Standard packaging in a locked anti-static cardboard

QT178, QT188, QT189, QT190, QT192, QT193, QT194
- Standard packaging in anti-static plastic tube (60pcs/tube)
- Tape and Reel is available for an additional charge.

Specifications subject to change without prior notice.

QCI Per MIL-PRF-38534, CLASS K (Modified)

Table VII
Group B Inspection (Note 1)

Subgroup	Test Description	MIL-STD-883		Quantity / (Accept No.)
		Method	Condition	
1	Physical Dimensions	2016	-	2 (0)
2	Particle Impact Noise Detection (Note 2)	2020	B	15 (0)
3	Resistance to Solvents	2015	-	4 (0)
4	Internal Visual and Mechanical	2014	-	1 (0)
5	Bond Strength (Note 3)	2011	C or D	2 (0)
6	Die Shear Strength (Note 4)	2019	-	2 (0)
7	Solderability (Note 5)	2003	Solder Temperature: 245 ±5º C	1 (0)
8	Seal; Fine Leak and Gross Leak (Note 6)	1014	A_1 & C	4 (0)
9	ESD Classification (Note 7)	3015	-	4 (0)

NOTES:
1. Non catastrophic screening test rejects may be used for Group B.
2. To be omitted. Being performed during screening, see Table I.
3. Subgroup 5 shall be performed in accordance with the Group B bond strength requirements of MIL-PRF-38534. This test may be performed in-process anytime prior to cover seal.
4. Die shear test samples shall not be the same units as subjected to bond pull. Die shear specimens shall not be exposed to the 300ºC preconditioning used for the bond strength test.
5. Solder temperature shall be 245 ±5ºC.
6. Subgroup 8, the fine and gross leak tests are being done during screening, see Table I.
7. Subgroup 9, the ESD classification test, is not required. The hybrid has been classified as ESDS Class 1C (i.e., Electrostatic voltage = 1999V) and shall be marked accordingly.

Table VIII
Group C Inspection

Subgroup	Test Description	MIL-STD-883		Quantity / (Accept No.)
		Method	Condition	
1	External Visual	2009		5 (0) (Note 1,2,3)
	Temperature Cycling	1010	C, 20 Cycles	
	Constant Acceleration	2001	A, Y_1 Axis	
	Seal (fine & gross leak)	1014	A_1 & C	
	Radiographic Inspection	2012		
	Visual Examination			
	End Point Electricals			
2	End Point Electricals Steady State Life End Point Electricals	1005	1000 hours at 125ºC	5 (0) (Note 2,3)
3	Internal Water Vapor Content	1018		3 (0) or 5 (1)

NOTES:
1. Five units shall be used for Group C inspection based on limited usage acquisition requirements of MIL-PRF-38534.
2. End point electrical shall be as specified in the detail specification.
3. Subgroup 1 specimens shall be used for subgroup 3 testing, but not recommended for subgroup 2 testing.

QCI Per MIL-PRF-38534, CLASS K (Modified)
(continued)

Table IX
Group D Inspection

Subgroup	Test Description	MIL-STD-883		Quantity / (Accept No.)
		Method	Condition	
1	Thermal Shock	1011	C	5 (0)
	Stabilization Bake	1008	1 hour at 150ºC	5 (0)
	Lead Integrity	2004 2028	B2 (lead fatigue) (LCC) Rigid Leads	1 (0)
	Seal (fine and gross leak)	1014	A_1 & C	5 (0)

QCI Per MIL-PRF-55310, LEVEL S

Table X
Group C Inspection

Subgroup	Test Description	Quantity/ (Accept No.)
1 all sample units	Vibration Shock	4 (0)
2 1/2 of all sample units	Thermal Shock Ambient Pressure Storage Temperature	2 (0)
3 1/4 of all sample units	Resistance to Solder Heat Moisture Resistance Salt Atmosphere	1 (0)
4 1/4 of all sample units	Terminal Strength Resistance to Solvents	1 (0)

1. A minimum of four (4) sample units shall be selected from inspection lots which have passed quality conformance inspection unless otherwise specified by the qualifying activity.
2. All test conditions are in accordance with MIL-PRF-55310, Level S.

Revision History

ECO	REV	REVISION SUMMARY	PAGE	DATE
10380	K	Change Frequency: Was: 450kHz -350MHz Is: 250kHz -350MHz	Applicable Pages	3/22/2012
		Add QT189 package	Applicable Pages	
		Remove USML Registration	1	
		Add tolerance code 2 & 7 to Freq vs. Temp Code	1	
		Add General Specification	2 - 4	
		Add Class B+ Logic Offerings	5	
		Add Group B Inspection (100% Aging) to Screening Option A	6	
		Add tolerance to dimensions (QT122 & QT128)	19	
10625	K w/amendment 1	Add document number on footer of all pages	All	7/16/2012
10703	K w/amendment 2	Add Group B, C, D, Inspection tables	21 & 22	10/26/2012
10851	L	Add QT101, QT106, QT125, QT127, QT141, QT142, QT194	Applicable Pages	5/21/2013
		Update frequency range from 250kHz - 350MHz to 15kHz - 350MHz		
		Add Supply Voltage 2.5V to ordering information table for CMOS	1	
10925	M	Add QT26 & QT29	Applicable Pages	1/17/2014
		Add Logic AC for ACMOS	Applicable Pages	
		Add code 19 to Ordering Info Table (Freq vs. Temp)	1	
		Modified Par. 4.2.1 & 4.2.2	3	
		Non Destructive Bond Pull: for all packages (Table I & II)	7 & 9	
		Internal Visual: Change Condition to Class K (Table I & II)	7 & 9	
		Add Option C Screening	1, 6, 11, 12	
		Modified Table IIb	10	
		Modified Rise & Fall time under “Notes” column (Change 30M to 36M)	15	
		Change E/D pin on QT101 from 3 to 2	25	
11510	N	Add screening options “N” per NASA EEE-INST-002, Level 1	6	6/5/2015
		Add LVPECL logic	20	
		Define Fine and Gross Level Test Methods	9, 11, 13, 16	
		Renumbering Pages		