

54F198 Shift Register

8-Bit Bidirectional Universal Shift Register

Military FAST Products

Product Specification

FEATURES

- Buffered clock and control inputs
- Shift right, shift left, and parallel load capability
- Asynchronous Master Reset

DESCRIPTION

The 54F198, Bidirectional Universal Shift Register is designed to incorporate virtually all of the features a system designer may want in a shift register. This circuit features parallel inputs and outputs, shift

right and shift left serial inputs, operating mode select inputs, and a direct overriding master reset input. The register has four distinct modes of operation:

- Parallel (broadside) load
- Shift right (in the direction Q_0 toward Q_7)
- Shift left (in the direction Q_7 toward Q_0)
- Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the 8 bits of data and taking both mode control inputs, S_0 and S_1 ,

High. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

ORDERING INFORMATION

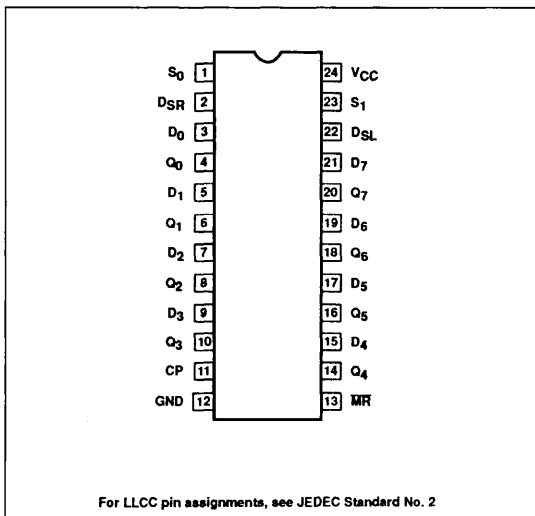
| DESCRIPTION | ORDER CODE |
|-------------------------|------------|
| 24-Pin Ceramic DIP | 54F198/BLA |
| 24-Pin Ceramic FlatPack | 54F198/BKA |
| 28-Pin Ceramic LLCC | 54F198/B3A |

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

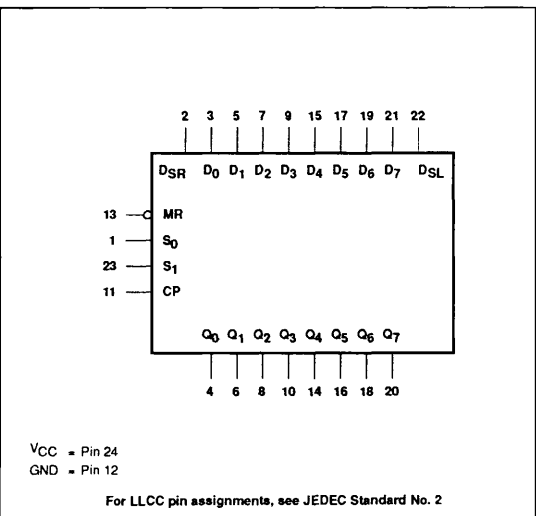
| PINS | DESCRIPTION | 54F(U.L.) HIGH/LOW | LOAD VALUE HIGH/LOW |
|-------------|--|--------------------|---------------------|
| $D_0 - D_7$ | Parallel data inputs | 1.0/1.0 | 20 μ A/0.6mA |
| D_{SR} | Serial data input (Shift Right) | 1.0/1.0 | 20 μ A/0.6mA |
| D_{SL} | Serial data input (Shift Left) | 1.0/1.0 | 20 μ A/0.6mA |
| S_0, S_1 | Mode Select inputs | 1.0/1.0 | 20 μ A/0.6mA |
| C_P | Clock pulse input (Active rising edge) | 1.0/1.0 | 20 μ A/0.6mA |
| M_R | Master reset input (Active Low) | 1.0/1.0 | 20 μ A/0.6mA |
| $Q_0 - Q_7$ | Data outputs | 50/33 | 1.0mA/20mA |

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20 μ A in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



LOGIC SYMBOL



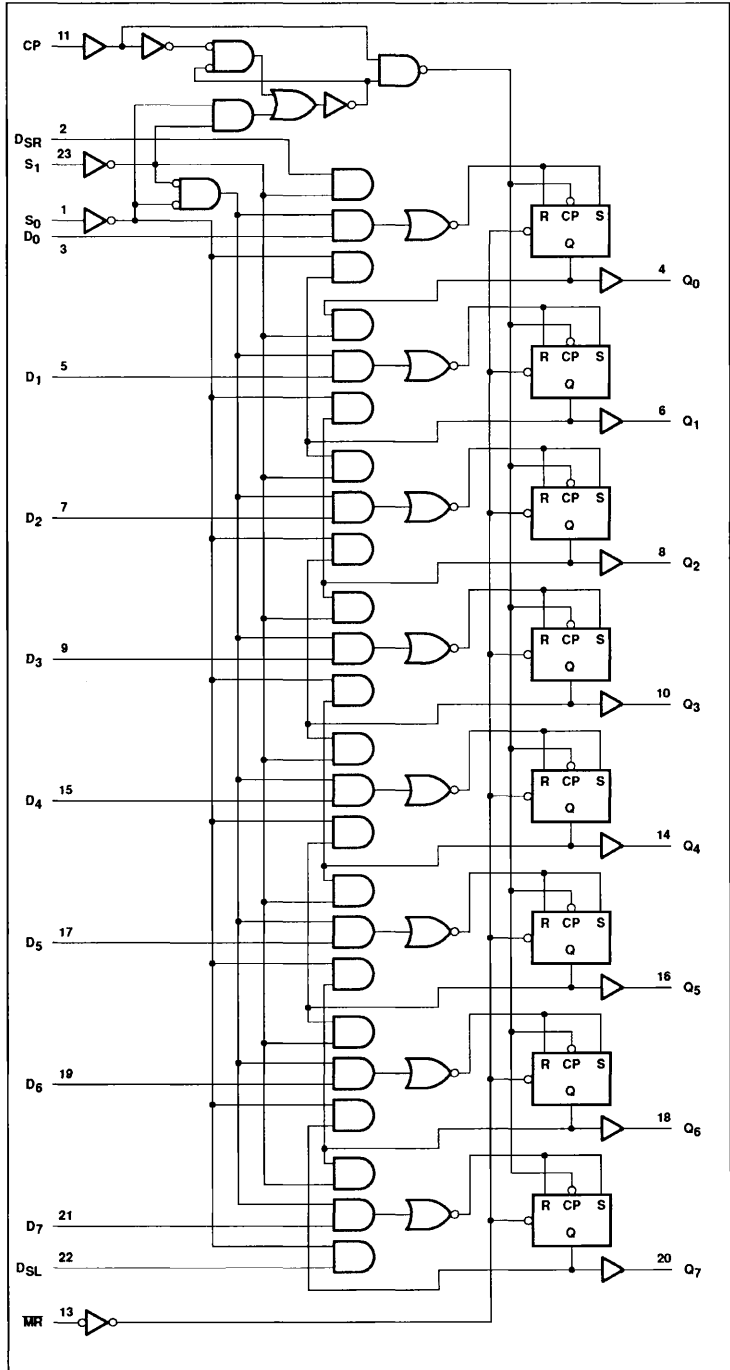
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Shift right is accomplished synchronously, with the rising edge of the clock pulse when S_0 is High and S_1 is Low. Serial data for this mode is entered at the right data input (D_{SR}). When S_0 is Low and S_1 is High, data shifts left synchronously and new data is entered at the shift-left serial input (D_{SL}).

Clocking of the flip-flops is inhibited when both mode control inputs are Low.

LOGIC DIAGRAM



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FUNCTION TABLE

| MR | INPUTS | | | | | | OUTPUTS | | | | |
|----|----------------|----------------|----|--------|-------|-------------------|-----------------|-----------------|-----|-----------------|-----------------|
| | Mode | | CP | Serial | | Parallel 0...7 | Q ₀ | Q ₁ | ... | Q ₆ | Q ₇ |
| | S ₀ | S ₁ | | Left | Right | | | | | | |
| L | X | X | X | X | X | X | L | L | | L | L |
| H | X | X | L | X | X | X | Q ₀₀ | Q ₁₀ | | Q ₆₀ | Q ₇₀ |
| H | H | H | ↑ | X | X | 0...7 | 0 | 1 | | 6 | 7 |
| H | H | L | ↑ | X | H | X | H | Q _{0n} | | Q _{5n} | Q _{6n} |
| H | H | L | ↑ | X | L | X | L | Q _{0n} | | Q _{5n} | Q _{6n} |
| H | L | H | ↑ | H | X | X | Q _{1n} | Q _{2n} | | Q _{7n} | H |
| H | L | H | ↑ | L | X | X | Q _{1n} | Q _{2n} | | Q _{7n} | L |
| H | L | L | X | X | X | X | Q ₀₀ | Q ₁₀ | | Q ₆₀ | Q ₇₀ |

H = High voltage level

L = Low voltage level

X = Don't care

↑ = Low-to-High transition of designated input

0...7 = The level of steady input at inputs 0 through 7, respectively

Q₀₀, Q₁₀, Q₆₀, Q₇₀ = The level of Q₀, Q₁, Q₆, Q₇, respectively, before the indicated steady state input conditions were established.Q_{0n}, Q_{1n}, Q_{6n}, Q_{7n} = The level of Q₀, Q₁, Q₆, Q₇, respectively, before the most recent Low-to-High clock transition.

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

| SYMBOL | PARAMETER | RATING | UNIT |
|------------------|--|--------------------------|------|
| V _{CC} | Supply voltage range | -0.5 to +7.0 | V |
| V _I | Input voltage range | -0.5 to +7.0 | V |
| I _I | Input current range | -30 to +5 | mA |
| V _O | Voltage applied to output in High output state range | -0.5 to +V _{CC} | V |
| I _O | Current applied to output in Low output state | 40 | mA |
| T _{STG} | Storage temperature range | -65 to +150 | °C |

RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|-----------------|--------------------------------------|--------|-----|------|------|
| | | Min | Nom | Max | |
| V _{CC} | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| V _{IH} | High-level input voltage | 2.0 | | | V |
| V _{IL} | Low-level input voltage | | | 0.8 | V |
| I _{IK} | Input clamp current | | | -18 | mA |
| I _{OH} | High-level output current | | | -1 | mA |
| I _{OL} | Low-level output current | | | 20 | mA |
| T _A | Operating free-air temperature range | -55 | | +125 | °C |

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

| SYMBOL | PARAMETER | TEST CONDITIONS ¹ | LIMITS | | | UNIT | |
|------------------|---|--|-----------------------|------------------|------|------|----|
| | | | Min | Typ ² | Max | | |
| V _{OH} | High-level output voltage | V _{CC} = Min, V _{IL} = Max, I _{OH} = Max, V _{IH} = Min | 2.5 | | | V | |
| V _{OL} | Low-level output voltage | V _{CC} = Min, V _{IL} = Max, I _{OL} = Max, V _{IH} = Min | | 0.35 | 0.50 | V | |
| V _{IK} | Input clamp voltage | V _{CC} = Min, I _I = I _{IK} | | -0.73 | -1.2 | V | |
| I _{IH2} | Input current at maximum input voltage | V _{CC} = Max, V _I = 7.0V | | | 100 | μA | |
| I _{IH1} | High-level input current | V _{CC} = Max, V _I = 2.7V | | | 20 | μA | |
| I _{IL} | Low-level input current | V _{CC} = Max, V _I = 0.5V | | | -0.6 | mA | |
| I _{OS} | Short-circuit output current ³ | V _{CC} = Max | -60 | | -150 | mA | |
| I _{CC} | Supply current (total) | I _{CCH} I _{CCL} | V _{CC} = Max | | 70 | 100 | mA |
| | | | | | 75 | 110 | mA |

AC ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | | | UNIT |
|------------------|---|-----------------|---|------|------|---|------|------|
| | | | T _A = +25°C, V _{CC} = +5.0V C _L = 50pF R _L = 500Ω | | | T _A = -55°C to +125°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω | | |
| | | | Min | Type | Max | Min | Max | |
| f _{MAX} | Maximum clock frequency | Waveform 1 | 80 | 95 | | 70 ⁴ | | MHz |
| t _{PLH} | Propagation delay CP input to Q _n | Waveform 1 | 5.0 | 7.5 | 10.0 | 4.5 | 12.0 | ns |
| t _{PHL} | | | 6.0 | 8.5 | 11.0 | 5.5 | 13.0 | ns |
| t _{PHL} | Propagation delay | Waveform 3 | 5.0 | 7.5 | 10.0 | 4.5 | 13.0 | ns |

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AC SETUP REQUIREMENTS

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | | UNIT |
|--|--|-----------------|---|------|----------------------------------|-------------|----------|
| | | | T _A = +25°C, V _{CC} = +5.0V | | T _A = -55°C to +125°C | | |
| | | | Min | Type | Max | Min | |
| t _s (H) t _s (L) | Setup time, High or Low D _n to CP | Waveform 2 | 0.0 3.0 | | | 1.0 3.5 | ns ns |
| t _h (H) t _h (L) | Hold time, High or Low D _n to CP | Waveform 2 | 0.0 3.5 | | | 2.5 5.0 | ns ns |
| t _s (H) t _s (L) | Setup time, High or Low D _{SR} , D _{SL} to CP | Waveform 2 | 0.0 3.0 | | | 1.5 3.5 | ns ns |
| t _h (H) t _h (L) | Hold time, High or Low D _{SR} , D _{SL} to CP | Waveform 2 | 0.0 2.5 | | | 1.5 3.5 | ns ns |
| t _s (H) t _s (L) | Setup time, High or Low S _n to CP | Waveform 2 | 9.0 6.0 | | | 11.0 7.5 | ns ns |
| t _h (H) t _h (L) | Hold time, High or Low S _n to CP | Waveform 2 | 0.0 0.0 | | | 0.0 0.0 | ns ns |
| t _w (H) t _w (L) | CP Pulse width High or Low | Waveform 1 | 5.0 5.0 | | | 6.0 6.0 | ns ns |
| t _w (L) | MR Pulse width, Low | Waveform 3 | 5.0 | | | 6.0 | ns |
| t _{rec} | Recovery time MR to CP | Waveform 3 | 5.0 | | | 6.5 | ns |

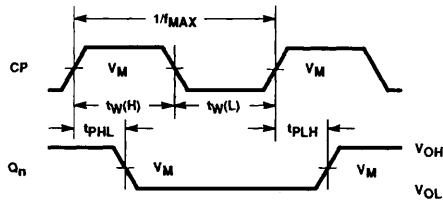
NOTES:

- For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
- These parameters are guaranteed, but not tested.

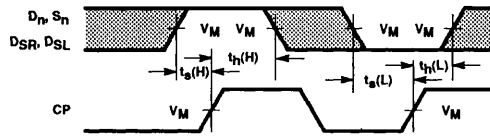
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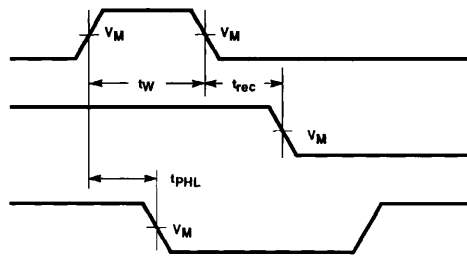
AC WAVEFORMS



Waveform 1. Propagation Delay, Clock Input to Output, Clock Widths, and Maximum Clock Frequency



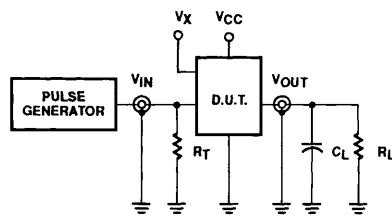
Waveform 2. Setup and Hold Times



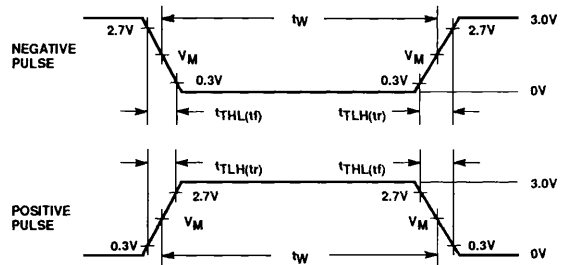
Waveform 3. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

NOTE: For all waveforms, $V_M = 1.5V$
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS:

- R_L = Load Resistor; see AC Characteristics for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
- V_X = Unlocked pins must be held at: $\leq 0.8V$; $\geq 2.7V$ or open per Function Table.

| INPUT PULSE CHARACTERISTICS | | | | |
|-----------------------------|-----------|-------------|--------------|--------------|
| Family | Rep. Rate | Pulse Width | t_{TLH} | t_{THL} |
| 54F | 1MHz | 500ns | $\leq 2.5ns$ | $\leq 2.5ns$ |