AT&T

DATA SHEET

41KW Loop Divider

FEATURES

- 2-bit and 8-bit counters
- Either 1.544 MHz or 3.152 MHz square-wave clock output
- 32 kHz clock output
- Standard LSTTL-compatible inputs and outputs

DESCRIPTION

The 41KW Loop Divider integrated circuit is an LSTTL-compatible gate array used in a phase-lock loop (PLL) to derive, from a system clock, the 1.544 MHz or 3.152 MHz square-wave clock signal for the DS1 or DS1C chip set. The divisor is set by logic for either DS1 or DS1C operation. A 32 kHz clock output provides the required PLL signal. The loop divider requires a single 5 V supply and is available in a 16-pin plastic DIP.

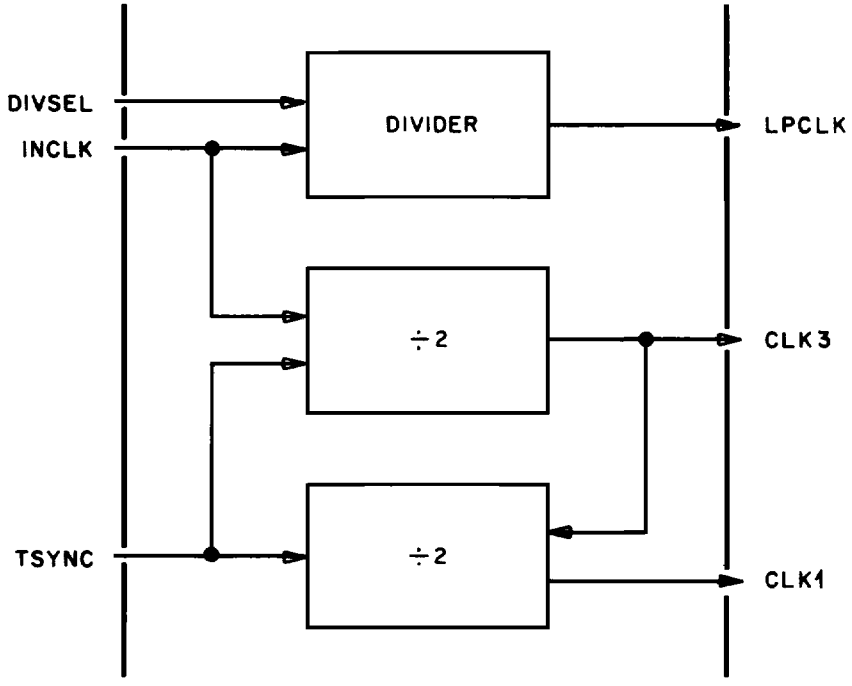
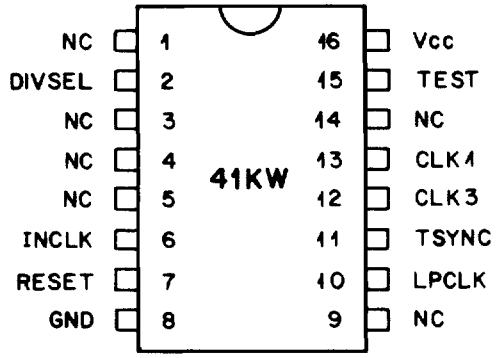


Figure 1. 41KW Loop Divider Block Diagram

December 1986

USER INFORMATION

Pin Descriptions



Symbol	Pin(s)	Symbol	Pin(s)
CLK1	13	RESET	7
CLK2	12	TEST	15
DIVSEL	2	TSYNC	11
INCLK	6	Vcc	16
LPCLK	10	GND	8
NC	1, 3—5 9, 14		

Figure 2. 41KW Pin Function Diagram and Alphabetical Listing of Symbols

Table 1. 41KW Pin Descriptions

Pin	Symbol	Type	Name/Function
1	NC	—	**No Connect.**
2	DIVSEL	I	**Divide Select.** When logic 0, the divisor is 193 for DS1 operation. When logic 1, the divisor is 197 for DS1C operation.
3	NC	—	**No Connect.**
4	NC	—	**No Connect.**
5	NC	—	**No Connect.**
6	INCLK	I	**Input Clock.** 6.176 MHz clock for DS1 operation; 6.304 MHz clock for DS1C operation.
7	RESET	I	**Reset Input.** Logic 1 during normal system operations.
8	GND	—	**Ground.**
9	NC	—	**No Connect.**
10	LPCLK	O	**Loop Clock.** 32 kHz clock signal used in PLL.
11	TSYNC	I	**Transmit Sync.** 8 kHz sync pulse.
12	CLK3	O	**Clock 3.** Divide-by-two output.
13	CLK1	O	**Clock 1.** Divide-by-four output.
14	NC	—	**No Connect.**
15	TEST	O	**Test.** Manufacturing test pin. Not connected during normal operation.
16	Vcc	—	**5 V Supply.**

Operation

The 41KW Loop Divider is a gate array IC used in conjunction with a 129EC Timing Generator to provide the interface between a DS1 or DS1C chip set and a PBX or host computer.

For DS1 operation, system clock input, INCLK, is 6.176 MHz; for DS1C operation, it is 6.304 MHz. INCLK is divided by 193 for DS1 operation, or by 197 for DS1C operation, to provide the PLL with a 32 kHz clock.

A 2-bit counter is used to derive the required clocks from INCLK. The 1.544 MHz clock is obtained by dividing INCLK (6.176 MHz) by four and synchronizing it to the 8 kHz transmit sync pulse during DS1 operation. The 3.152 MHz clock for DS1C operation is obtained by dividing INCLK (6.304 MHz) by two and synchronizing it to the 8 kHz transmit sync pulse.

DIVSEL determines if operation is DS1 or DS1C. When DIVSEL is low (logic 0), INCLK is divided by 193 (DS1 operation); when it is high (logic 1), INCLK is divided by 197 (DS1C operation).

Input and output timing relationships are shown on the timing diagram. All outputs change on the rising edge of INCLK. Note that the rising edges of INCLK, CLK1, CLK3, and LPCLK align during the middle of the TSYNC pulse.

CHARACTERISTICS

Clocks

System Clocks: 6.176 MHz (DS1)
6.304 MHz (DS1C)
8 kHz, 244 ns pulse duration

Electrical Characteristics

T_A = 0 to 85 °C, V_{CC} = 5 ± 0.5 V

Parameter	Symbol	Min	Max	Unit	Test Conditions
Supply Current	I_{CC}	–	90	mA	V_{CC} = 5.5 V
Input Voltages					
High Level (Logic 1)	V_{IH}	2	–	V	–
Low Level (Logic 0)	V_{IL}	–	0.7	V	–
Output Voltages					
High Level (Logic 1)	V_{OH}	2.5	–	V	V_{CC} = 4.5 V, I_{OH} = −400 μA
Low Level (Logic 0)	V_{OL}	–	0.5	V	V_{CC} = 4.5 V, I_{OL} = 8 mA
Input Current					
High Level (Logic 1)	I_{IH}	–	20	μA	V_{CC} = 5.5 V, V_{IN} = 2.7 V
Low Level (Logic 0)	I_{IL}	–	−360	μA	V_{CC} = 5.5 V, V_{IN} = 0 V
Output Short Circuit Current					
Low Level (Logic 0)	I_{OS}	−15	−100	mA	V_{CC} = 5.5 V, V_{OUT} = 0 V
Power Dissipation	PD	–	490	mW	V_{CC} = 5.5 V

Maximum Ratings

Voltage on any pin with respect to ground ..... −0.5 to +7 V
Ambient Operating Temperature Range (TA) ..... −40 to +125 °C
Storage Temperature Range (Tstg) ..... −40 to +125 °C

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

The external leads can be bonded or soldered safely at temperatures up to 300 °C.

Timing Characteristics

Symbol	Description	Min	Typ	Max	Unit
Fmax	INCLK	7.0	10.0	–	MHz
tTSHICH	TSYNC High to INCLK High	95	122	150	ns
tICHLPL	INCLK High to LPCLK Low	–	60	100	ns
tICHC1H	INCLK High to CLK1 High	–	60	100	ns
tICHC3H	INCLK High to CLK3 High	–	60	100	ns
tICHICH	INCLK Period				
	(DS1)	146	162	178	ns
	(DS1C)	143	159	175	ns
tC1HC1H	CLK1 Period	–	648	–	ns
tC3HC3H	CLK3 Period	–	317	–	ns
tLPHLPH	LPCLK Period	–	31.25	–	μs

Timing Diagram

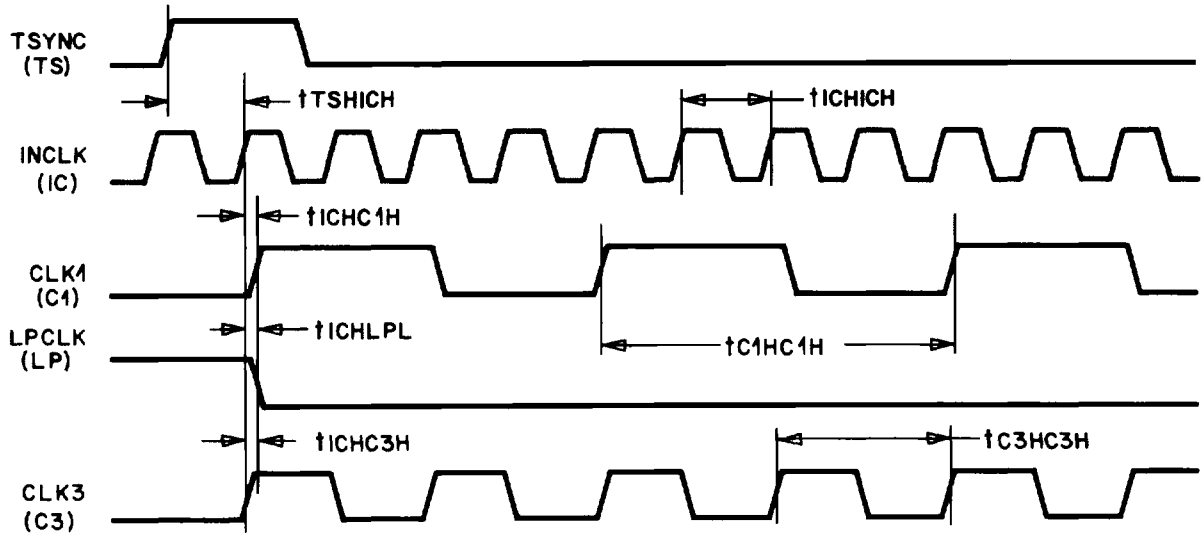
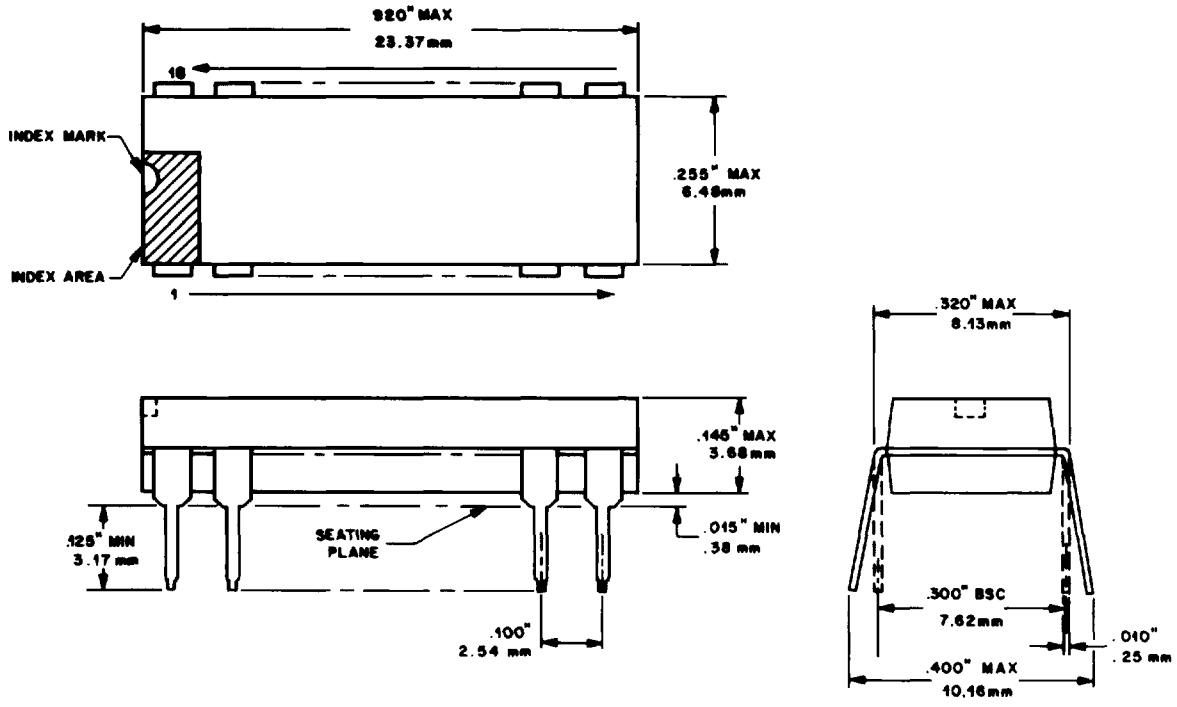
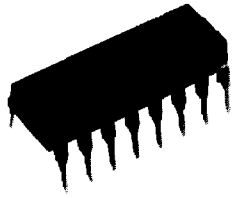


Figure 3. I/O Timing

Outline Diagram



NOTES : MEETS JEDEC STANDARDS.
INDEX MARK MAY BE SEMICIRCULAR NOTCH OR CIRCULAR DIMPLE LOCATED IN INDEX AREA.
INDEX MARK MAY BE CIRCULAR DIMPLE LOCATED IN INDEX AREA.



ORDERING INFORMATION

Device Code	Package	Temperature	COMCODE
41KW	16-pin plastic DIP	0 to +85 °C	103624490

Notes

Notes

Notes

For additional information contact your AT&T Account Manager, or call:

□ AT&T Technologies, 555 Union Boulevard, Dept. 50AL203140, Allentown, PA 18103
1-800-372-2447

In Europe, contact:

□ AT&T Microelectronics, Freischützstrasse 92, 8000 München 81, West Germany
Tel. 0 89/95 97 0 or **Telex 5 216 884**

Printed in United States of America **DS86-355DBIP**