August 1990
Edition 6.0

FUJITSU

DATA SHEET

MB40788
1 CHANNEL 10-BIT D/A CONVERTER

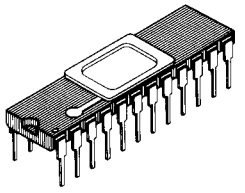
1 CHANNEL 10-BIT D/A CONVERTER (125MSPS)

The Fujitsu MB40788 is 10 bit Ultra-high speed low-power Digital to Analog Converter which is fabricated with Fujitsu Advanced Bipolar Technology.

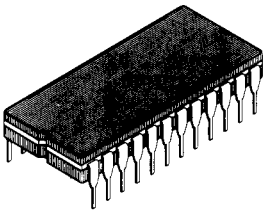
The device can convert 10-bit digital signal into analog signal at a rate of DC to 125 Mega-samples/sec. (MSPS).

Because of such high speed operation, the device is suitable for applications such as color television decoding system, video processing system with computer, and so on.

- Resolution : 10bits
- Linearity : ±0.2% max.
- Conversion Rate : 125MSPS min.
- Analog Output Voltage : 0V to –1V
- Digital Input Voltage : 10k ECL level
- Input Code : Binary or 2's complement
- Single Power Supply (–5.2V) : –5.2V
- Power Dissipation : 450mW typ.
- Standard 24-pin Cerdip Package : (Suffix: –Z)
  24-pin Ceramic Side Brazed Package : (Suffix: –C)

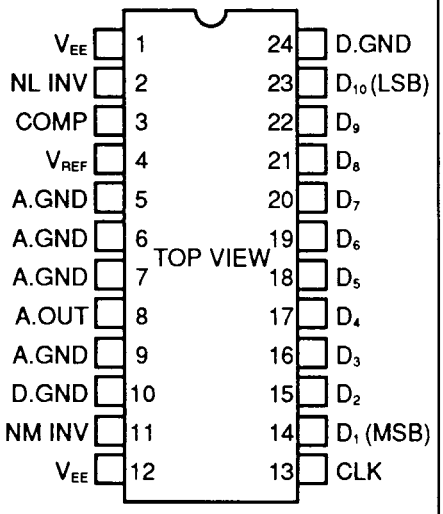


CERAMIC PACKAGE
DIP-24C-A10



CERAMIC PACKAGE
DIP-24C-C01

PIN ASSIGNMENT



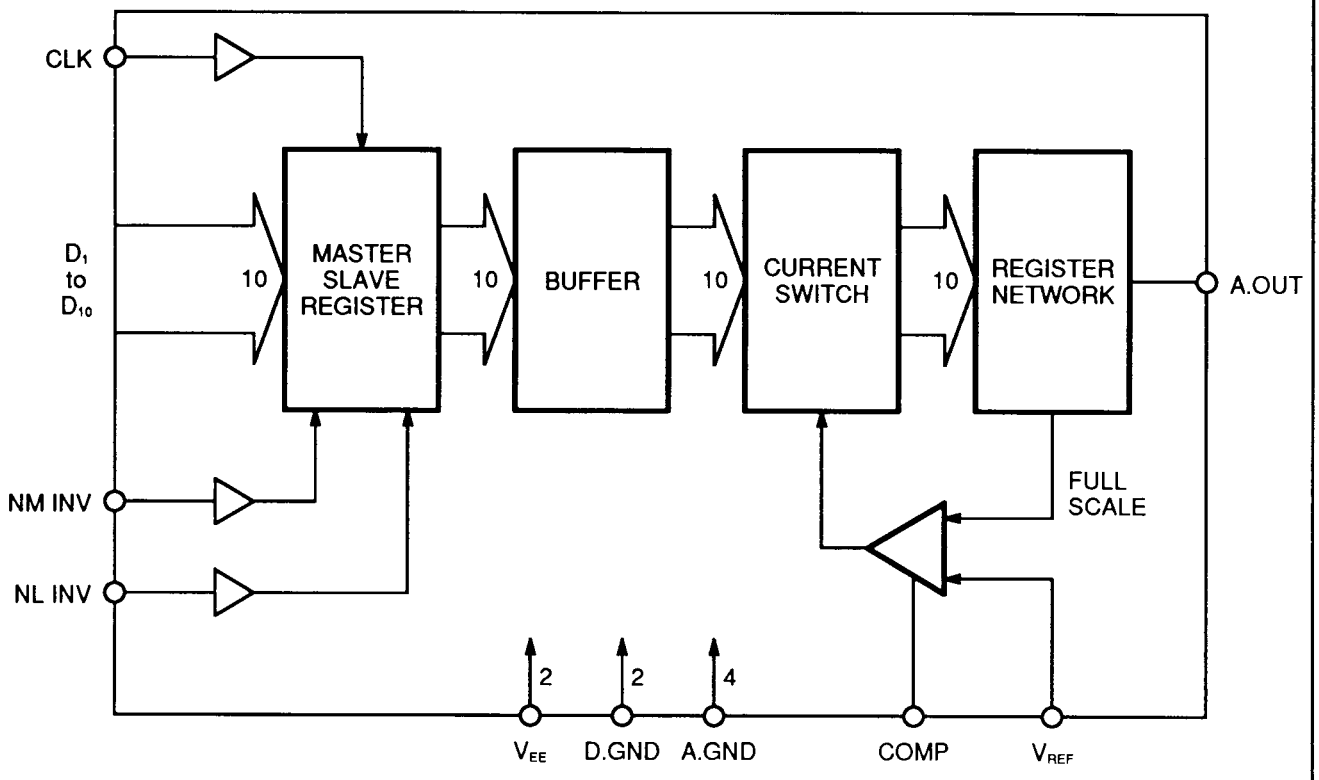
ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{EE}	–7.0 to +0.5	V
Digital Input Voltage	V_{IND}	V_{EE} to +0.5	V
Analog Reference Voltage	V_{REF}	V_{EE} to +0.5	V
Storage Temperature	T_{STG}	–55 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB40788 BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply Voltage	V_{EE}	–5.46	–5.20	–4.94	V
Analog Reference Voltage	V_{REF}	–1.2	–1.0	–0.8	V
Clock Pulse Width (High-level)	t_{W^+}	3.0			ns
Clock Pulse Width (Low-level)	t_{W^-}	3.5			ns
Data Setup Time	t_S	3.0			ns
Data Hold Time	t_H	2.4			ns
Operating Temperature	t_A	0		70	°C
Phase Compensation Capacitance*1	C_{COMP}	1			µF

*1: The capacitor should be connected between COMP and V_{EE}

ELECTRICAL CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted.) (V_{EE}=–5.2V, T_A=0V to +70V°C)

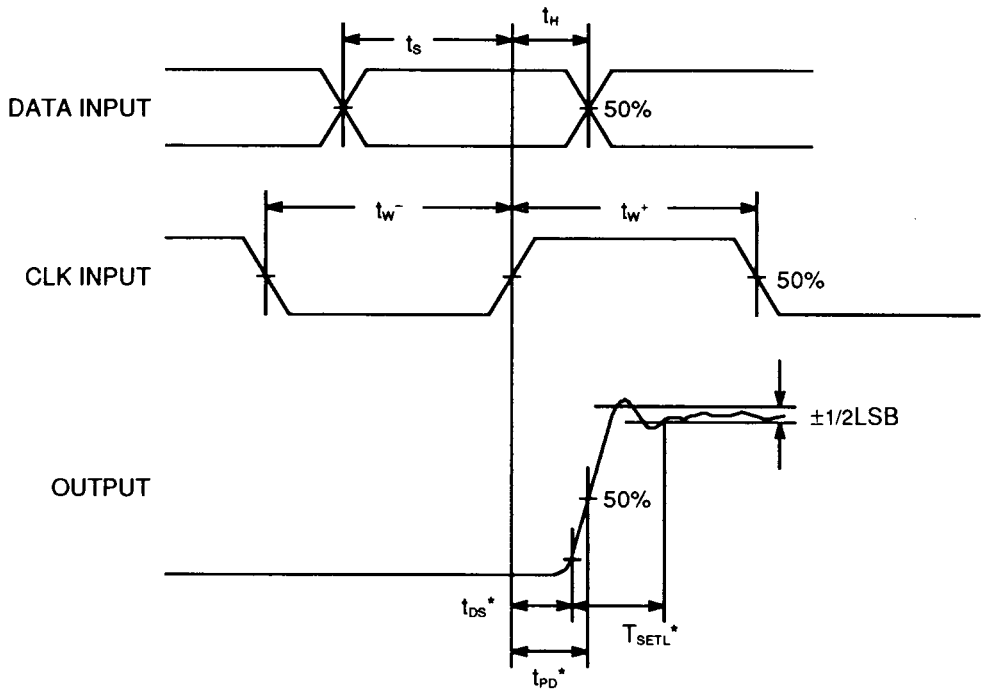
Parameter	Condition & Note	Symbol	Value			Unit
			Min.	Typ.	Max.	
Resolution					10	bits
Linearity Error	DC	L_E			±0.2	%
Full-scale Analog Output Voltage	V_{REF}=–1.00V Output is open.	V_{OFS}	–1.06	–1.00	–0.94	V
Zero-scale Analog Output Voltage	V_{REF}=–1.00V Output is open.	V_{OZS}	–15	0	15	mV
Reference Input Current	V_{REF}=–1.00V	I_{REF}			20	µA
Output Impedance	T_A=25°C	Z_{OUT}	70	80	90	Ω
High-level Digital Input Voltage	T_A=0°C T_A=+25°C T_A=+70°C	V_{IHD}	–1.145 –1.105 –1.045			V
Low-level Digital Input Voltage	T_A=0°C T_A=+25°C T_A=+70°C	V_{ILD}			–1.490 –1.475 –1.450	V
High-level Digital Input Current		I_{IHD}		150	500	µA
Low-level Digital Input Current		I_{ILD}	0.5	115		µA
Supply Current	V_{REF}=–1.00V	I_{EE}	–135	–84		mA

SWITCHING CHARACTERISTICS

(V_{EE}=–5.2V, T_A=0V to +70V°C)

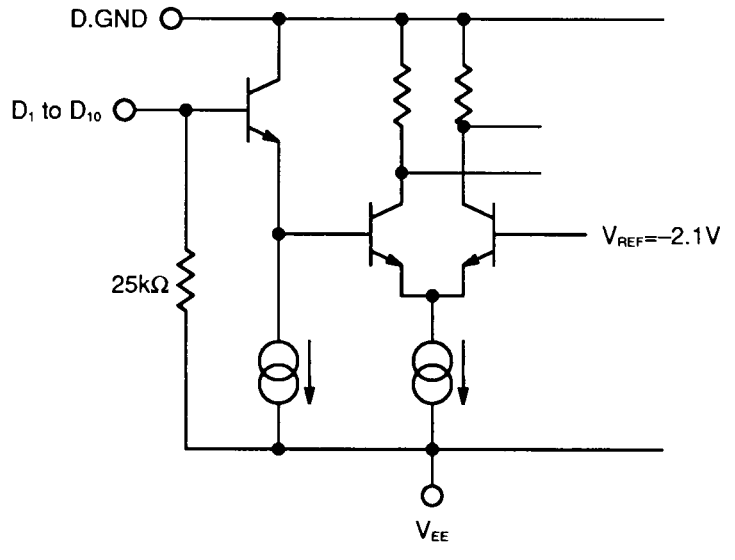
Parameter	Conditions	Symbol	Value			Unit
			Min.	Typ.	Max.	
Maximum Conversion Rate		FS	125			MSPS
Propagation Delay Time		t_{pd}	4.5	6.5	8.5	ns

Fig. 2 – TIMING CHART



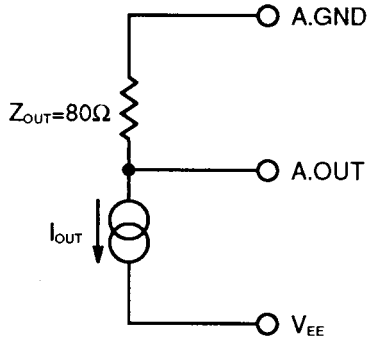
Note: *These values are not specified because they depend on application circuit.

Fig. 3 – EQUIVALENT DIGITAL INPUT CIRCUIT



V_{TH}=–1.30V

Fig. 4 – EQUIVALENT OUTPUT CIRCUIT



OUTPUT VOLTAGE

(Recommended Operating Conditions unless otherwise noted. V_{REF}=–1.024V) **(1LSB=1mV)**

Step		Binary		Offset 2's complement		Output Voltage (V)
	Logic	Positive	Negative	Positive	Negative	
	NMINV	1	0	0	1	
	MLINV	1	0	1	0	
0		0000000000	1111111111	1000000000	0111111111	–0.000
1		0000000001	1111111110	1000000001	0111111110	–0.001
⋮		⋮	⋮	⋮	⋮	⋮
511		0111111111	1000000000	1111111111	0000000000	–0.511
512		1000000000	0111111111	0000000000	1111111111	–0.512
513		1000000001	0111111110	0000000001	1111111110	–0.513
⋮		⋮	⋮	⋮	⋮	⋮
1022		1111111110	0000000001	0111111110	1000000001	–1.022
1023		1111111111	0000000000	0111111111	1000000000	–1.023

Fig. 5 – IDEAL OUTPUT OPERATION

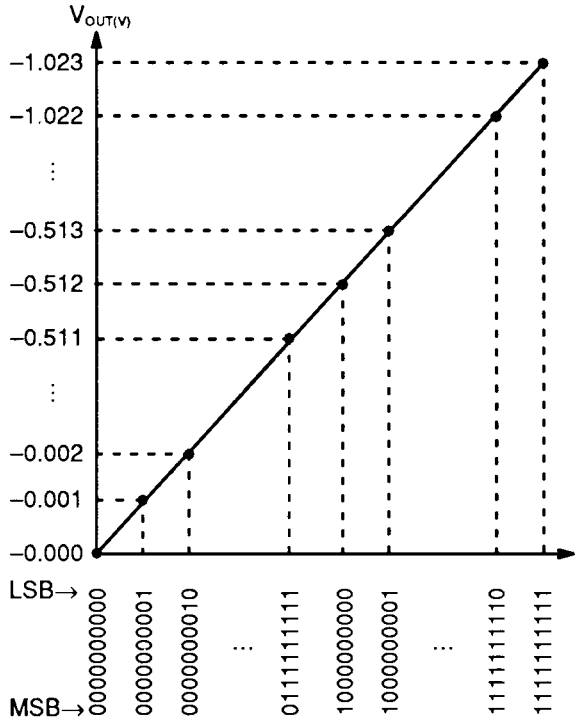
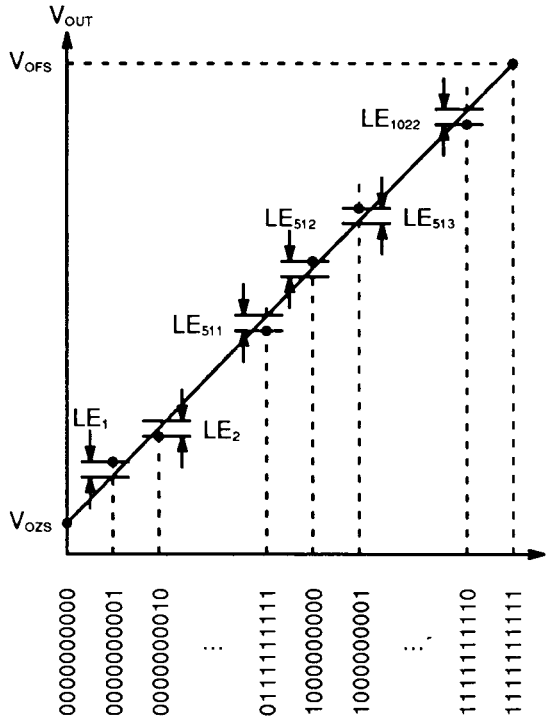


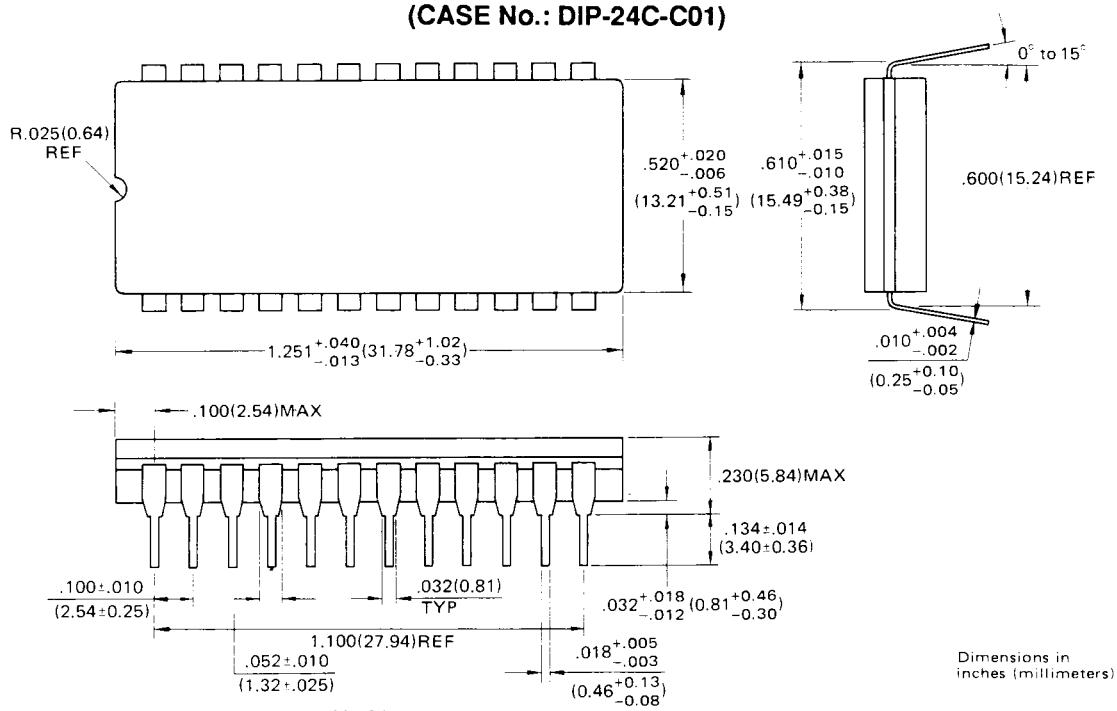
Fig. 6 – PRACTICAL OUTPUT OPERATION



$$\text{Linearity Error} = \frac{|LE_n|\,max}{|FS|}$$

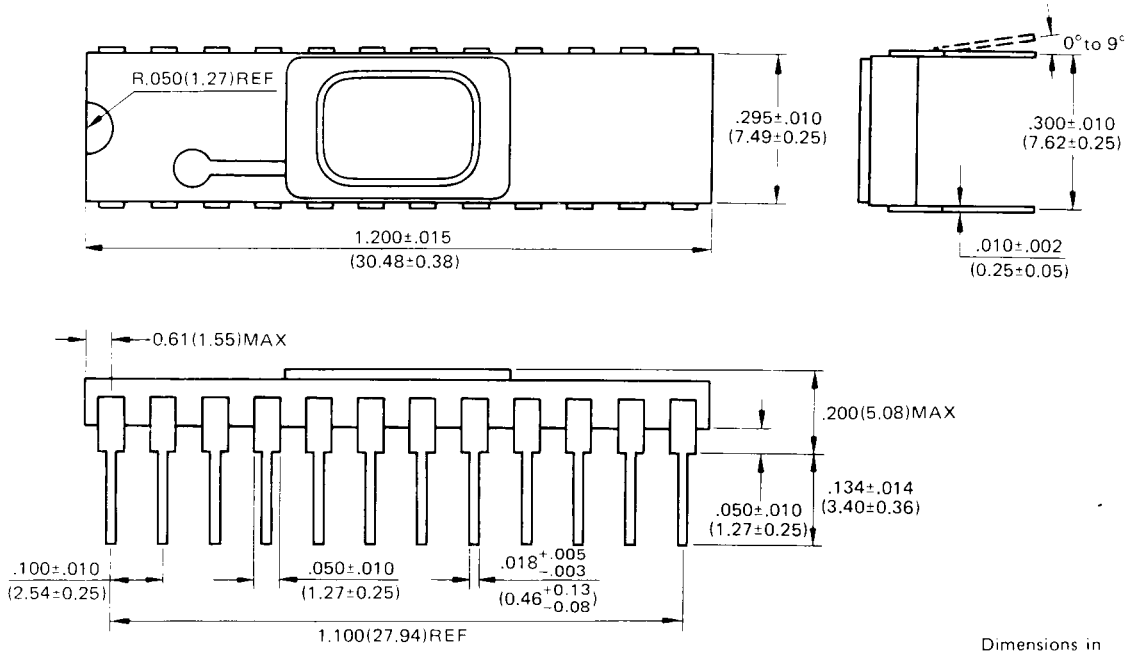
PACKAGE DIMENSIONS

24-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-24C-C01)



Dimensions in inches (millimeters)

24-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-24C-A10)



Dimensions in inches (milimeters)

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications. Complete Information sufficient for construction purposes is not necessarily given.

The information contained in this document has been carefully checked and is believed to be reliable. However, Fujitsu assumes no responsibility for inaccuracies.

The Information contained in this document does not convey any license under the copyrights, patent rights or trademarks claimed and owned by Fujitsu.

Fujitsu reserves the right to change products or specifications without notice.