Preliminary data

Bipolar IC
MOS Handling

Type	Ordering code	Package
SDA 4211	Q67000-A 8016	DIP 8

The SDA 4211 has been designed for application in television receivers operating according to the frequency synthesis tuning principle. It includes a preamplifier and an ECL divider stage with symmetrical ECL push-pull outputs. It can be operated with a divider ratio of 1:64 or 1:256.

The operating range of the IC extends to an input frequency of 1.3 GHz.

Features

- Pin programmable divider ratio of 1:64 or 1:256
- Symmetrical push-pull input
- Functional range up to 1.3 GHz
- Minimal current consumption of 23 mA

Circuit description

The preamplifier of the component has been designed with symmetrical push-pull inputs. During the asymmetrical drive of one of the inputs, the other input has to be disabled to ground by a capacitor (approx. 1.5 nF) of low series inductance.

The divider stage of the component is comprised of several status-controlled master-slave flipflops. Their divider ratio can be set with the switch-over input M as follows:

M to V_S = 1:64
M to ground = 1:256

The symmetrical push-pull outputs of the divider include an internal resistor of 500 Ω each. The DC voltage level at the outputs is connected to the supply voltage V_S (output "High" = V_S). The typical voltage swing is 1.0 V (peak-to-peak).

Maximum ratings

		min	max	
Supply voltage	V_S	−0.3	6	V
Input voltage (peak-to-peak) (pin 2, pin 3)	V_i		2.5	V
Output voltage (pin 6, pin 7)	V_q		V_S	V
Output current (pin 6, pin 7)	$-I_q$		10	mA
Input voltage (pin 5)	V_M	−0.3	V_S	V
Junction temperature	T_j		125	°C
Storage temperature range	T_{stg}	−40	125	°C
Thermal resistance (system-air)	R_{thSA}		115	K/W
Overload resistance[1] (ESD protection single discharge of 220 pF capacitor through a 1 kΩ resistor to each pin)	V_{MOS}	−600	1000	V

Operating range

Supply voltage	V_S	4.5	5.5	V
Input frequency	f_i	70	1300	MHz
Ambient temperature	T_A	0	70	°C

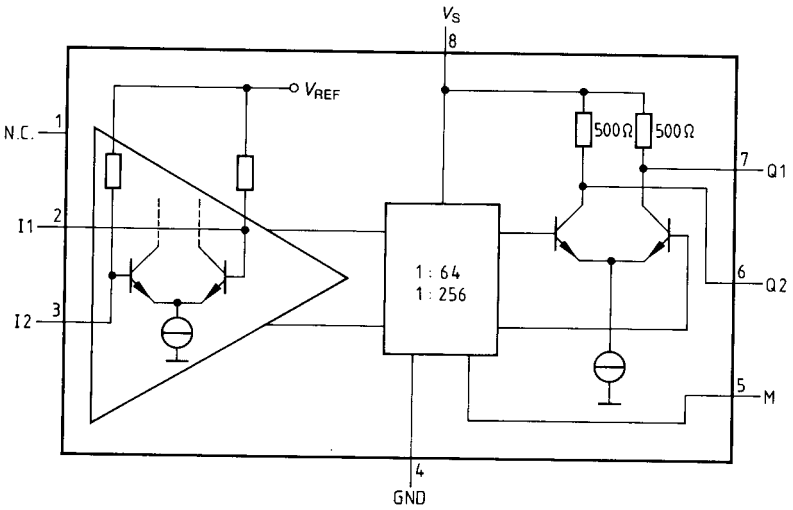
[1] not required pins float; pin 4 always to ground

Characteristics

$V_S = 5$ V; $T_A = 25$ °C

		Test conditions	Test circuit	min	typ	max	
Current consumption	I_S	inputs decoupled outputs enabled; M enabled			23.5	29.5	mA
Input level ("input sensitivity")	V_i	70 MHz	1	−26/11		3/315	dBm/mV
		80 MHz	1	−27/10		3/315	dBm/mV
		120 MHz	1	−30/7		3/315	dBm/mV
		250 MHz	1	−32/5.5		3/315	dBm/mV
		600 MHz	1	−27/10		3/315	dBm/mV
		1000 MHz	1	−27/10		3/315	dBm/mV
		1100 MHz	1	−27/10		3/315	dBm/mV
		1200 MHz	1	−21/20		3/315	dBm/mV
		1300 MHz	1	−15/40		3/315	dBm/mV
Output voltage swing (peak-to-peak)	V_q	$C_L \leq 15$pF; $f \leq 1000$MHz	1	0.8	1.0	1.2	V
Output voltage swing (peak-to-peak)	V_q	$R_L = 820\ \Omega$; $C_L = 56$pF $f \leq 1000$ MHz	2	0.25			V
DC voltage offset of outputs	ΔV_q		3			100	mV
M-input current "Low" (divider ratio 1:256)	I_M	M = ground	1		2	100	µA
M-input current "High" (divider ratio 1:64)	I_M	M = V_S	1		0	50	µA
M-input voltage "High"	V_{MH}		1	2.4			V
M-input voltage "Low"	V_{ML}		1			0.6	V
Amplitude of the 3rd harmonic at output (referenced to 1st harmonic)	a_3	$f = 700$-900 MHz; M = V_S	1.4		−13		dB
			2.4		−20		dB

Block diagram

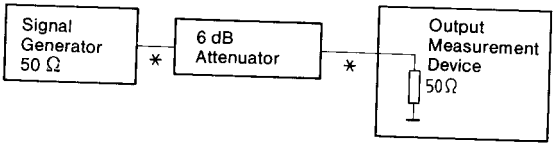


Pin description

Pin	Function
1	Not connected
2	Input I1
3	Input I2
4	Ground
5	Switch-over input M for divider ratio
6	Output Q2
7	Output Q1
8	Supply voltage V_S

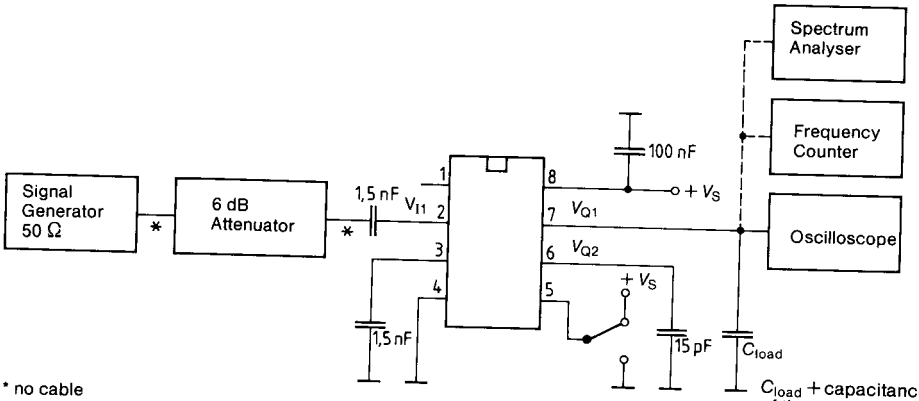
Measurement circuit 1

Calibration of signal generator



* no cable

Measurement of input sensitivity and output voltage swing

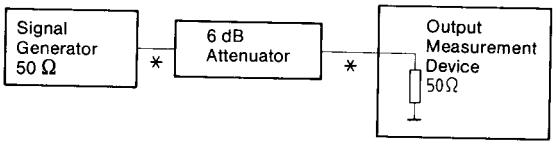


* no cable

C_{load} + capacitance of the measurement devices = 15 pF (For output voltage swing measurement)

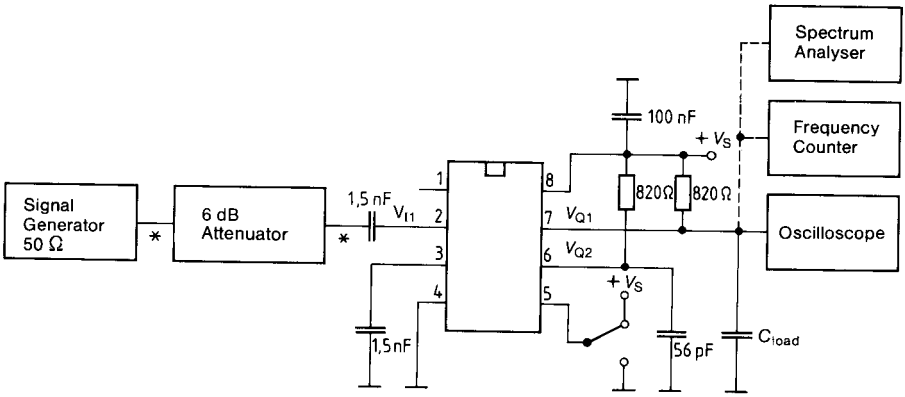
Measurement circuit 2

Calibration of signal generator



* no cable

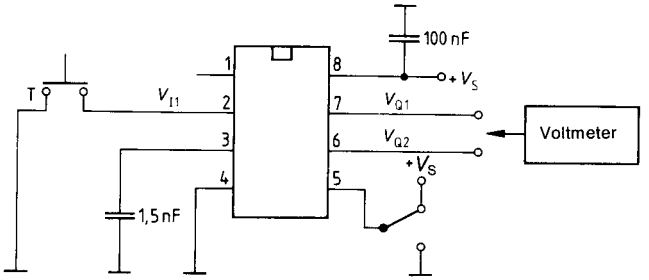
Measurement of input sensitivity and output voltage swing



* no cable

C_{load} + capacities of the measurement devices = 56 pF (for output voltage swing measurement)

Measurement circuit 3



Note: press key T until outputs turn over

Measurement circuit 4

PC board for measurement of 3rd harmonic