Rockwell

RC2122DPL, RC2123DPL, and RC2223DPL
Low Power, Modem Data Pump Device

INTRODUCTION

The Rockwell RC2122DPL, RC2123DPL, and RC2223DPL are low power, low speed, modem data pumps (MDPs) in a single VLSI package. They are identical except for unique features described for different models. The modems support data modes meeting requirements specified in ITU recommendations V.22, V.23, and V.21 (see Table 1).

Table 1. MDP Models and Modes

Model	Supported Modes		
	V.21	V.22	V.23
RC2122DPL	X	X	-
RC2123DPL	X	-	X
RC2223DPL	X	X	X

The modem operates over the public switched telephone network (PSTN) through the appropriate line termination.

The modem data pump includes two CMOS VLSI functions - a digital signal processor (DSP) and an integrated analog function (IA). The functions are integrated into a 68-pin plastic leaded chip carrier (PLCC) or a 100-pin plastic quad flat pack (PQFP).

The modem offers lower power consumption and a small footprint, low profile PQFP package meeting PCMCIA Type II envelope requirements for PCMCIA PC Cards and battery-powered portable applications, such as notebook and subnotebook computers.

This data sheet describes capabilities provided by these modems. Additional information such as RAM data scaling and host application flowcharts is provided in the RC9624DP, RC96V24DP, and RC14V24DP Modem Designer's Guide (Order No. 822).

FEATURES

- Single CMOS VLSI device
- Low power requirements
  - Single voltage: + 5 Vdc ± 5%
  - Operating: 190 mW (typical)
  - Sleep: 10 mW (typical)
- 2-wire, full-duplex (FDX) operation
- Data configurations (model dependent)
  - V.22, V.21, and/or V.23
- Voice pass-through mode
- Dual tone multifrequency (DTMF) detection
- Dynamic range: –9 dBm to –43 dBm
- Transmit level: -10 dBm ± 1 dB using internal hybrid circuit; attenuation selectable in 1 dB steps
- Serial data: synchronous and asynchronous
- Parallel data: synchronous (including HDLC) and asynchronous
- NRZI encoding/decoding
- Programmable features including dialer, ring detect, and tone detect bandpass filters
- Adjustable speaker output to monitor received signal
- Network diagnostics support
- TTL and CMOS compatible DTE/host interface
  - ITU V.24 (EIA/TIA-232-E) (data/control)
  - Microprocessor bus (data/configuration/control)
- Compromise equalization
- Local analog, local digital, and remote digital loopbacks
- Answer and originate handshake in data modes
- Leased line operation
- Flexible packaging options
  - One 68-pin PLCC package, or
  - One 100-pin PQFP

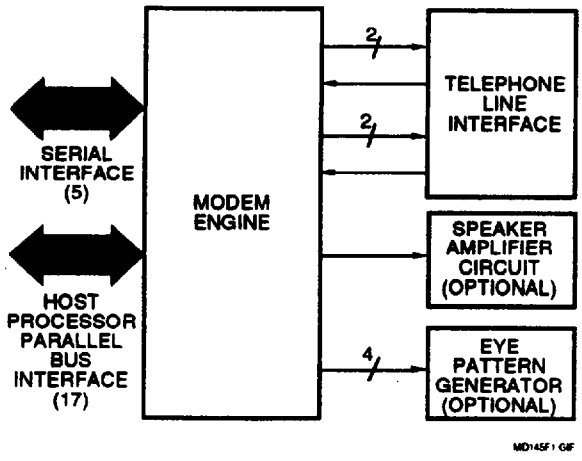


Figure 1. Modem General Interface

TECHNICAL DESCRIPTION

Configurations and Rates

The selectable modem configurations, along with the corresponding signaling (baud) rates and data rates, are listed inTable 2 (CONF bits).

Note: Bit names refer to control or status bits in DSP interface memory which are set or reset by the host processor (see Figure 4 and Table 12).

Data Encoding

The data encoding conforms to the requirements specified in ITU V.22, V.21 and V.23 depending on the model and the selected configuration.

Tone Generation

Answer Tone: A ITU (2100 ± 15 Hz) answer tone can be generated.

Guard Tone: A 1800 ± 20 Hz guard tone can be generated.

DTMF Tones: DTMF tones can be generated with a frequency accuracy of ± 1.5% (Table 3).

User Defined Tones: A user-defined single or dual tone can be generated from 200 Hz to 3000 Hz ± 5 Hz.

TONE DETECTION

Answer Tone and Call Progress Tones: Tones can be detected as follows:

Call progress frequency range: 340 ± 5 to 640 ± 5 Hz

Answer tone frequency ranges: 2100 ± 15 Hz

Detection range: –9 dBm to –43 dBm

Default detection threshold: –43 dBm

Response time: 75 ± 2 ms

The passband and tone detect thresholds can be changed in DSP RAM.

V.23 and V.21 Tones: Tones can be detected as follows:

V.23 forward channel mark: 1300 ± 10 Hz

V.23 backward channel mark: 390 ± 10 Hz

V.21 high band mark (1650 ± 10 Hz) or low band mark (980 ± 10 Hz)

Detection range: –9 dBm to –43 dBm

Default detection threshold: –43 dBm

Response time: 25 ± 2 ms

The passbands and tone detect thresholds can be changed in the DSP RAM.

DTMF DETECTION

The modem can detect a valid DTMF tone pair and load a corresponding hexadecimal code into the modem interface memory.

EQUALIZERS

Fixed compromise equalizers are provided in the transmitter and receiver to improve performance when operating over low quality lines. The equalizers are programmable in DSP RAM.

TRANSMIT LEVEL

The transmitter output level is –10 dBm ± 1 dB using the internal hybrid circuit (see Figure 5). The attenuation is selectable from 0 dB to 15 dB in 1 dB steps.

TRANSMIT TIMING (V.22)

Transmitter timing is selectable between internal (± 0.01%), external , or loopback. When external clock is selected, the external clock rate must equal the desired data rate ± 0.01% with a duty cycle of 50 ± 20%.

SCRAMBLER/DESCRAMBLER (V.22)

The modem incorporates a self-synchronizing scrambler/descrambler. The scrambler and descrambler can be enabled or disabled.

RECEIVE LEVEL

The receiver satisfies performance requirements for a received line signal from –9 dBm to –43 dBm. The default RLSD turn-on and RLSD turn-off thresholds are –43 dBm and –48 dBm, respectively. The RLSD threshold levels are programmable in DSP RAM.

RECEIVER TIMING (V.22)

The modem can track a frequency error up to ± 0.03% in the associated transmit timing source.

CARRIER RECOVERY (V.22)

The modem can track a frequency offset up to ± 7 Hz in the received carrier with less than a 0.2 dB degradation in bit error rate (BER).

Table 2. Configurations, Signaling Rates, and Data Rates

Configuration	Modulation[1]	Answer[2] Carrier Frequency (Hz) ± 0.01%	Originate[2] Carrier Frequency (Hz) ± 0.01%	Data Rate (bps) ± 0.01%	Baud (Symbols/ Sec.)	Bits Per Symbol	Constellation Points	Sample Rate (Samples/ Sec.)
V.22 1200	DPSK	2400	1200	1200[3]	600	2	4	7200
V.22 600	DPSK	2400	1200	600[3]	600	1	2	7200
V.21	FSK	1650 M 1850 S	980 M 1180 S	0–300[4]	300	1	–	
V.23 Forward Channel	FSK	1300 M 2100 S	1300 M 2100 S	1200	1200	1	1	7500
V.23 Backward Channel	FSK	390 M 450 S	390 M 450 S	75	75	1	1	9600[5]
Dial/Call Progress Mode					600			7200
Tone Generator Tone Detector Mode Transmit					600			7200

Notes:
1. Modulation legend: DPSK: Differential Phase Shift Keying
   FSK: Frequency Shift Keying
2. M indicates a mark condition; S indicates a space condition.
3. Synchronous accuracy = ± 0.01%; asynchronous accuracy = -2.5% to +1.0% (+2.3% if extended overspeed is selected).
4. Value is upper limit for serial (e.g., 0-300).
5. 9600 samples per second in V.23 FDX Tx75/Rx1200, or V.23 HDX Tx or Rx 1200;
   7200 samples per second in V.23 FDX Tx1200/Rx75, or V.23 HDX Tx or Rx 75.

Table 3. Dial Digits/Tone Pairs

Dial Digit	Tone 1(Hz)	Tone 2 (Hz)
1	697	1209
2	697	1336
3	697	1477
4	770	1209
5	770	1336
6	770	1477
7	852	1209
8	852	1336
9	852	1477
0	941	1336
*	941	1209
#	941	1477
A	697	1633
B	770	1633
C	852	1633
D	941	1633

RTS-CTS TURN-ON AND TURN-OFF SEQUENCES

RTS ON to CTS ON and RTS OFF to CTS OFF response times are listed in Table 4.

Table 4. RTS-CTS Response Times

Configuration	Turn On Time	Turn-Off Time
V.22 (CC bit = 0)	≤ 2 ms	≤ 2 ms
V.22 (CC bit = 1)	270 ms	≤ 2 ms
V.21	2-5 ms	10 ms
V.23	11 ms	≤ 2 ms

SERIAL OR PARALLEL INTERFACE

The TPDM bit selects serial or parallel interface.

Serial Interface. The five hardware lines (RXD, TXD, TDCLK, ~RDCLK, and XTCLK) are supported by four control and status bits in the interface memory (CTS, DSR, RTS, and RLSD).

Parallel Interface. An 8086-compatible parallel microprocessor bus is supported.

VOICE PASS-THROUGH MODE

Transmit Voice. Transmit voice samples are sent to the modem digital-to-analog converter (DAC) from the host through the transmit data buffer (TBUFFER).

Receive Voice. Received voice samples from the modem analog-to-digital converter (ADC) are read by the host from the receive data buffer (RBUFFER).

ASYNCHRONOUS CONVERSION

Asynchronous mode is selected by the ASYNC bit. The asynchronous character format is 1 start bit, 5 to 8 data bits (WDSZ bits), an optional parity bit (PARSL and PEN bits), and 1 or 2 stop bits (STB bit). Valid character size, including all bits, is 7, 8, 9, 10 or 11 bits per character.

Signaling Rate Range. Basic range (+1% to −2.5%) or Extended overspeed range (+2.3% to −2.5%) is selectable by the EXOS bit.

Break. Break is handled as described in V.22.

SLEEP MODE

Via host control, the modem enters sleep mode (SLEEP = 1) which significantly reduces modem power consumption. Return to normal modem operation is accomplished by either applying a reset pulse, or by performing a dummy interface memory write operation.

POWER AND ENVIRONMENTAL REQUIREMENTS

The power requirements are specified in Table 5. The environmental specifications are listed in Table 6.

HARDWARE INTERFACE SIGNALS

The modem functional hardware interface signals are shown in Figure 2. In this diagram, any point that is active low is represented by a small circle at the signal point.

Edge triggered inputs are denoted by a small triangle (e.g., TDCLK). Open-Collector (open-source or open-drain) outputs are denoted by a small half-circle (e.g., ~IRQ). Active low signals are overscored (e.g., ~POR).

A clock intended to activate logic on its rising edge (low-to-high transition) is called active low (e.g., ~RDCLK), while a clock intended to activate logic on its falling edge (high-to-low transition) is called active high (e.g., TDCLK). When a clock input is associated with a small circle, the input activates on a falling edge. If no circle is shown, the input activates on a rising edge.

The modem pin assignments are shown in Figure 3. The 68-pin PLCC pin assignments are listed in Table 5 and the 100-pin PQFP pin assignments listed in Table 6.

The hardware interface signal functions are summarized by major interface in Table 7.

Digital interface characteristics are defined in Table 8.

Analog interface characteristics are defined in Table 9.

Current and power requirements are listed in Table 10.

Absolute maximum ratings are specified in Table 11.

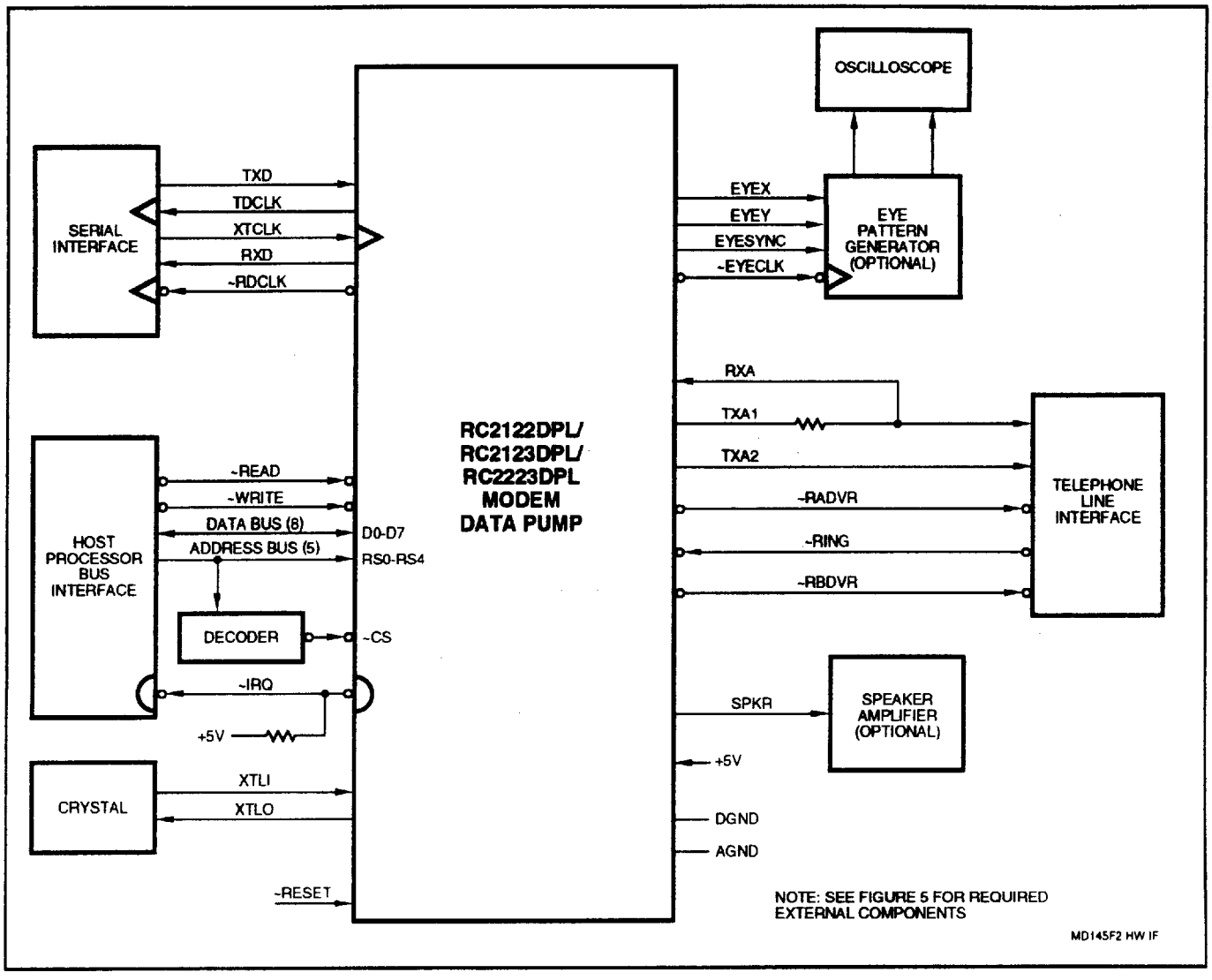
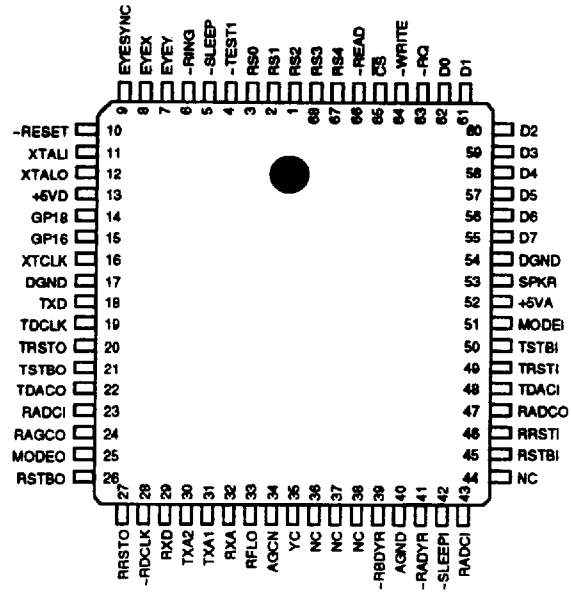
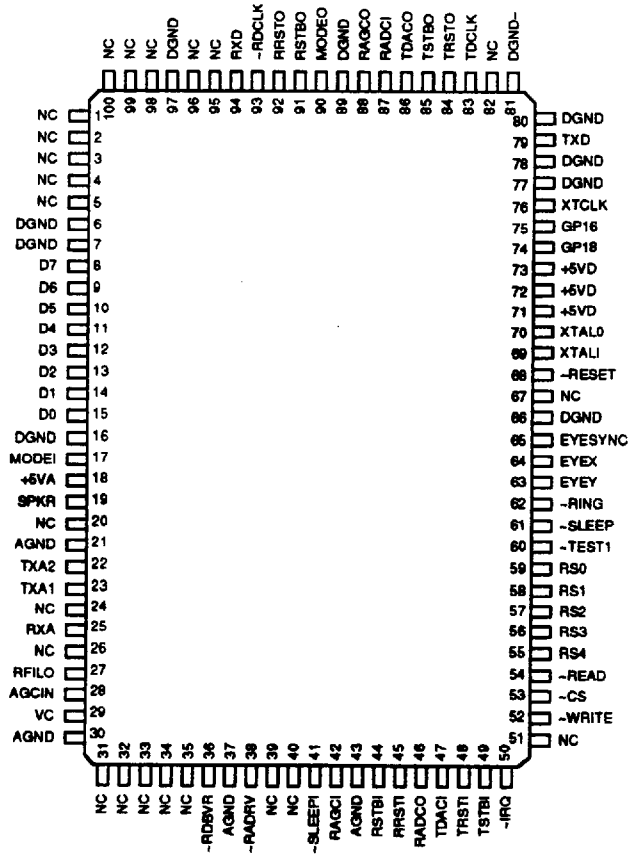


Figure 2. Modem Hardware Interface Signals



a. 68-Pin PLCC



b. 100-Pin PQFP

MD145F3 Pinouts

Figure 3. MDP Pin Signals

Table 5. MDP Pin Signals - 68-Pin PLCC

Pin Number	Signal Name	I/O Type	Pin Number	Signal Name	I/O Type
1	RS2	IA	35	VC	OA
2	RS1	IA	36	NC	NC
3	RS0	IA	37	NC	NC
4	~TEST1	NC	38	NC	NC
5	~SLEEP	OA	39	~RBDVR	OD
6	~RING	IA	40	AGND	GND
7	EYEY	OB	41	~RADVR	OD
8	EYEX	OB	42	~SLEEPI	IA
9	EYESYNC	OB	43	RAGCI	MI
10	~RESET	ID	44	NC	NC
11	XTLI	IE	45	RSTBI	MI
12	XTLO	OB	46	RRSTI	MI
13	+5VD	PWR	47	RADCO	MI
14	GP18	NC	48	TDACI	MI
15	GP16	NC	49	TRSTI	MI
16	XTCLK	IA	50	TSTBI	MI
17	DGND	GND	51	MODEI	MI
18	TXD	IA	52	+5VA	PWR
19	TDCLK	OA	53	SPKR	O(DF)
20	TRSTO	MI	54	DGND	GND
21	TSTBO	MI	55	D7	IA/OB
22	TDACO	MI	56	D6	IA/OB
23	RADCI	MI	57	D5	IA/OB
24	RAGCO	MI	58	D4	IA/OB
25	MODEO	MI	59	D3	IA/OB
26	RSTBO	MI	60	D2	IA/OB
27	RRSTO	MI	61	D1	IA/OB
28	~RDCLK	OA	62	D0	IA/OB
29	RXD	OA	63	~IRQ	OC
30	TXA2	O(DD)	64	~WRITE	IA
31	TXA1	O(DD)	65	~CS	IA
32	RXA	I(DA)	66	~READ	IA
33	RFILO	MI	67	RS4	IA
34	AGCIN	MI	68	RS3	IA

Notes:
1. MI = Modem Interconnection.
2. NC = No connection (may have internal connection; leave pin disconnected (open)).
3. Digital and analog I/O types are described in Table 8 and Table 9, respectively.

Table 6. MDP Pin Signals - 100-Pin PQFP

Pin Number	Signal Name	I/O Type	Pin Number	Signal Name	I/O Type
1	NC	NC	51	NC	NC
2	NC	NC	52	~WRITE	IA
3	NC	NC	53	~CS	IA
4	NC	NC	54	~READ	IA
5	NC	NC	55	RS4	IA
6	DGND	GND	56	RS3	IA
7	DGND	GND	57	RS2	IA
8	D7	IA/OB	58	RS1	IA
9	D6	IA/OB	59	RS0	IA
10	D5	IA/OB	60	~TEST1	NC
11	D4	IA/OB	61	~SLEEP	OA
12	D3	IA/OB	62	~RING	IA
13	D2	IA/OB	63	EYEY	OB
14	D1	IA/OB	64	EYEX	OB
15	D0	IA/OB	65	EYESYNC	OB
16	DGND	GND	66	DGND	GND
17	MODEI	MI	67	NC	NC
18	+5VA	PWR	68	~RESET	ID
19	SPKR	O(DF)	69	XTLI	IE
20	NC	NC	70	XTLO	OB
21	AGND	GND	71	+5VD	PWR
22	TXA2	O(DD)	72	+5VD	PWR
23	TXA1	O(DD)	73	+5VD	PWR
24	NC	NC	74	GP18	NC
25	RXA	I(DA)	75	GP16	NC
26	NC	NC	76	XTCLK	IA
27	RFILO	MI	77	DGND	GND
28	AGCIN	MI	78	DGND	GND
29	VC	OA	79	TXD	IA
30	AGND	GND	80	DGND	GND
31	NC	NC	81	DGND	GND
32	NC	NC	82	NC	NC
33	NC	NC	83	TDCLK	OA
34	NC	NC	84	TRSTO	MI
35	NC	NC	85	TSTBO	MI
36	~RBDVR	OD	86	TDACO	MI
37	AGND	GND	87	RADCI	MI
38	~RADVR	OD	88	RAGCO	MI
39	NC	NC	89	DGND	GND
40	NC	NC	90	MODEO	MI
41	~SLEEPI	IA	91	RSTBO	MI
42	RAGCI	MI	92	RRSTO	MI
43	AGND	GND	93	~RDCLK	OA
44	RSTBI	MI	94	RXD	OA
45	RRSTI	MI	95	NC	NC
46	RADCO	MI	96	NC	NC
47	TDACI	MI	97	DGND	GND
48	TRSTI	MI	98	NC	NC
49	TSTBI	MI	99	NC	NC
50	~IRQ	OC	100	NC	NC

Notes:

1. MI = Modem Interconnection.
2. NC = No connection [may have internal connection; leave pin disconnected (open)].
3. Digital and analog I/O types are described in Table 8 and Table 9, respectively.

Table 7. Hardware Interface Signal Definitions

Label	I/O Type	Signal/Definition
		OVERHEAD SIGNALS
XTLI, XTLO	IE, OB,	**Crystal/Clock In and Crystal Out.** The DSP must be connected to an external crystal circuit consisting of a 24.00014 MHz, two capacitors, and a resistor. Alternatively, XTLI, may be driven with a buffered clock (e.g., square wave generator) or a sine wave oscillator.
~RESET	ID	**Reset.** The active low ~RESET input resets the internal modem logic. Upon transition of ~RESET from low-to-high, the DSP interface memory bits are set to the default values.
+ 5VD	PWR	**+ 5V Digital Supply.** +5V ±5% is required.
+ 5VA	PWR	**+ 5V Analog Supply.** +5V ±5% is required.
DGND	GND	**Digital Ground.**
AGND	GND	**Analog Ground.**
		SERIAL INTERFACE
Five TTL-level hardware interface circuits implement a ITU V.24-compatible serial data interface with control signals provided through the DSP interface memory.		
~RDCLK	OA	**Receive Data Clock.** In synchronous mode, the modem outputs a Receive Data Clock (~RDCLK) in the form of 50 ±1% duty cycle square wave. The low-to-high transitions of this output coincide with the center of received data bits.
TDCLK	OA	**Transmit Data Clock.** In synchronous mode, the modem outputs a Transmit Data Clock (TDCLK). The TDCLK clock frequency is data rate ±0.01% with a duty cycle of 50 ± 1%.
XTCLK	IA	**External Transmit Clock.** In synchronous mode, an external transmit data clock input (XTCLK) can be supplied.
RXD	OA	**Received Data.** The modem presents received serial data on the Received Data (RXD) output and to the interface memory Receive Data Register (RBUFFER) in both serial and parallel modes.
TXD	IA	**Transmitted Data.** The modem obtains serial data to be transmitted on the TXD input in serial mode, or from the interface memory Transmit Data Register (TBUFFER) in parallel mode. (See TPDM bit.)
		PARALLEL MICROPROCESSOR INTERFACE
Address, data, control and interrupt hardware interface signals implement an 8086-compatible parallel microprocessor interface to a host processor. This parallel interface allows the host to change modem configuration, read or write channel and diagnostic data, and supervise modem operation by writing control bits and reading status bits.		
D0–D7	IA/OA	**Data Lines.** Eight bidirectional data lines (D0–D7) provide parallel transfer of data between the host and the modem.
~CS	IA	**Chip Select.** The active low Chip Select (~CS) input enables parallel data transfer over the microprocessor bus.
RS0–RS4	IA	**Register Select Lines.** The five active high Register Select inputs (RS0–RS4) address interface memory registers in the modem when ~CS is low. These lines are typically connected to address lines A0–A4 to address one of 32 8-bit internal interface memory registers (00–1F). The selected register can be read from, or written into, via the 8-bit parallel data bus (D0–D7).
~READ, WRITE	IA, IA	**Read Enable and Write Enable.** Reading or writing is controlled by the host pulsing either ~READ or ~WRITE input low, respectively, during the microprocessor bus access cycle. During a write cycle, data from the data bus is copied into the addressed DSP interface memory register, with high and low bus levels representing one and zero bit states, respectively.
~IRQ	OA	**Interrupt Request.** The ~IRQ output structure is an open-drain field-effect-transistor (FET). The ~IRQ output can be enabled in the interface memory to allow immediate indication of change of conditions in the modem. The use of ~IRQ is optional depending upon modem application.

Table 7. Hardware Interface Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
		HYBRID CIRCUIT
TXA1, TXA2	O(DF)	**Transmit Analog 1 and 2.** The TXA1 and TXA2 outputs are differential outputs 180 degrees out of phase with each other.
RXA	I(DA)	**Receive Analog.** RXA is a single-ended receive data input from the telephone line interface or an optional external hybrid circuit.
VC	OA	**Centerpoint Voltage.** VC is a +2.5 VDC centerpoint voltage which serves as the internal "analog ground" reference point.
		TELEPHONE LINE INTERFACE
~RADVR	OD	**Relay A Driver.** ~RADVR is an open drain output which can directly drive a relay with greater than 360 Ω coil resistance and having a "must operate" voltage of no greater than 4.0 VDC. The ~RADVR output is controlled by the state of the RA bit, except in pulse dial mode. When RA is a 1, the ~RADVR output is active which applies current to the relay coil. In a typical application, ~RADVR is connected to the normally open Off-Hook relay. In this case, ~RADVR active closes the Off-Hook relay to connect the modem to the telephone line.
~RBDVR	OD	**Relay B Driver.** ~RBDVR is an open drain output which can directly drive a relay with greater than 360 Ω coil resistance and having a "must operate" voltage of no greater than 4.0 VDC. ~RBDVR output is controlled by the state of the RB bit. When RB is a 1, the ~RBDVR output is active which applies current to the relay coil. In a typical application, ~RBDVR is connected to the normally closed Talk/Data relay. In this case, ~RBDVR active opens the relay to disconnect the handset from the telephone line.
~RING	IA	**Ring Frequency.** A low-going edge on the ~RING input initiates a ring frequency measurement. A valid ring detection is indicated by the RI bit.
		SPEAKER INTERFACE
SPKR	O(DF)	**Speaker Analog Output.** The SPKR output reflects the received analog input signal. The SPKR on/off and three levels of attenuation are controlled by interface memory bits. When the speaker is turned off, the SPKR output is clamped to the voltage at the VC pin. The SPKR output can drive an impedance as low as 300 ohms. In a typical application, the SPKR output is an input to an external LM386 audio power amplifier.
		SLEEP MODE SIGNALS
~SLEEP, ~SLEEPI	OA IA	**Sleep Mode Output and Sleep Mode Input.** ~SLEEP output high indicates the DSP is operating in its normal mode. ~SLEEP low indicates that the DSP is in the sleep mode. This signal must be connected to the ~SLEEPI input to power down the IA in the sleep mode. ~SLEEP can also be used to control power to other devices (e.g., as a speaker enable).
		DIAGNOSTIC SIGNALS Four signals provide the timing and data necessary to create an oscilloscope quadrature eye pattern. The eye pattern is simply a display of the received baseband constellation. By observing this constellation, common line disturbances can usually be identified.
EYEX, EYEY	OB	**Eye Pattern Data X and Eye Pattern Data Y.** The EYEX and EYEY outputs provide two serial bit streams containing data for display on the oscilloscope horizontal (X) axis and vertical (Y) axis, respectively. This serial digital data can be converted to analog form using two shift registers and two digital-to-analog converters (DACs).
~EYECLK (RRSTO	OA	**Eye Pattern Clock.** ~EYECLK is a clock for use by the serial-to-parallel converters. The ~EYECLK output is a 7200/9600 Hz clock.
EYESYNC	OA	**Eye Pattern Sync.** EYESYNC is a strobe for word synchronization. The falling edge of EYESYNC may be used to transfer the 8 bit word from the shift register to a holding register. Digital-to-analog conversion can then be performed for driving the X and Y inputs of an oscilloscope

Table 7. MDP Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
		MODEM INTERCONNECT
RFILO	MI	**Receive Filter Output.** RFILO is the output of the internal receive analog filter which must be connected to AGCIN through a 0.0022 µF, 20%, DC decoupling capacitor.
AGCIN	MI	**Receive AGC Gain Amplifier Input.** See RFILO.
MODEO (DSP), MODEI (IA)	MI	**Mode Control.** Serial IA mode control bits. Direct modem interconnect line.
TDACO (DSP), TDACI (IA)	MI	**Transmitter DAC Signal.** Transmitter serial digital DAC signal. Direct modem interconnect line.
TSTBO (DSP), TSTBI (IA)	MI	**Transmitter Strobe.** Transmitter 576 kHz digital timing reference. Direct modem interconnect line.
TRSTO (DSP), TRSTI (IA)	MI	**Transmitter Reset.** Transmitter 7200/9600 Hz digital timing reference. Direct modem interconnect line.
RADCI (DSP), RADCO (IA)	MI	**Receiver ADC Signal.** Receiver serial digital ADC signal. Direct modem interconnect line.
RAGCO (DSP), RAGCI (IA)	MI	**Receiver AGC Signal.** Receiver serial digital AGC signal. Direct modem interconnect line.
RSTBO (DSP), RSTBI (IA)	MI	**Receiver Strobe.** Receiver 576 kHz digital timing reference. Direct modem interconnect line.
RRSTO (DSP), RRSTI (IA)	MI	**Receiver Reset.** Receiver 7200/9600 Hz digital timing reference. Direct modem interconnect line.
RRSTO (DSP), RRSTI (IA)	MI	**Receiver Reset.** Receiver 7200/9600 Hz digital timing reference. Direct modem interconnect line.

Table 8. Digital Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input High Voltage	V_{IH}				VDC	
Type IA		2.0	–	V_{CC}		
Type ID		0.8 V_{CC}	–	V_{CC}		
Type IE		–	4.0	V_{CC}		Note 2.
Input Low Voltage	V_{IL}				VDC	Note 2.
Type IA and ID		0.3		0.8		
Type IE		–	1.0	–		Note 2.
Input Leakage Current	I_{IN}				µADC	
Type IA (Non-multiplexed)		–	–	±2.5		V_{IN} = 0 to V_{CC}
Type IE		–	–	±2.5		V_{IN} = 0 to +5V, V_{CC} = 5.25V
Input Low Current Type IB	I_{IL}	–	–	-400	µA	V_{CC} = 0 to +5.25V
Output High Voltage	V_{OH}		–	–	VDC	
Types OA and OB		3.5	–	–		I_{LOAD} = – 100 µA
Type OD			–	V_{CC}		I_{LOAD} = 0 mA
Output Low Voltage	V_{OL}				VDC	
Types OA and OC		–	–	0.4		I_{LOAD} = 1.6 mA
Type OB		–	–	0.4		I_{LOAD} = 0.8 mA
Type OD		–	–	0.75		I_{LOAD} = 15 mA
Output High Current Type OD	I_{OH}	–	–	-1	mA	
Output Low Current Type OD	I_{OL}	–	–	-100	µA	
Output Leakage Current Types OA and OB	I_{LO}	–	–	±10	µADC	V_{IN} = 0.4 to V_{CC} -1
Capacitive Load Types IA and IB	C_L	–	5	–	pF	
Capacitive Load	C_D				pF	
Types OA and OB		–	100	–		
Type OD		–	50	–		
Circuit Type						
Type IA						TTL
Type D						POR
Types OA and OB						TTL with 3-state
Type OC						Open drain
Type OD						Clock
Three-State (Off) Current	I_{TSI}			±10	µADC	
Type OA				±10	µADC	V_{IN} = 0.8 to 4.5V @ 500 kHz
Types OB and OC				±10	µADC	V_{IN} = 0.8 to V_{CC}-1

Notes:

1. Test Conditions: V_{CC} = 5V ± 5%, TA = 0°C to 70°C, unless otherwise noted.
2. Type IE inputs are centered at approximately 2.5V and swing 1.5 V_{PEAK} in each direction.

Table 9. Analog Electrical Characteristics

Signal Name	Type	Characteristic	Value
RXA	I (DA)	Input Impedance Voltage Range	> 50K Ω +2.5 ± 1.6 V
TXA1, TXA2	O (DD)	Minimum Load Maximum Capacitive Load Output Impedance Output Voltage DC Offset Voltage	300 Ω 0.01 µF 10 Ω +2.5 ± 1.6 V < 200 mV
SPKR	O (DF)	Minimum Load Maximum Capacitive Load Output Impedance Output Voltage DC Offset Voltage	300 Ω 0.01 µF 10 Ω +2.5 ± 1.6 V < 20 mV

Table 10. Current and Power Requirements

Mode	Current (ID)		Power (PD)	
	Typical @ 25° (mA)	Maximum @ 0°C (mA)	Typical @ 25°C (mW)	Maximum @ 0°C (mW)
Normal mode	38	48	190	240
Sleep mode	2	2.5	10.0	12.5

Notes:
1. Maximum power @ -40°C specified only for extended temperature range parts.
2. Test conditions: VCC = 5.0 VDC for typical values; VCC = 5.25 VDC for maximum values.
3. Input Ripple ≤ 0.1 $V_{PEAK-PEAK}$.

Table 11. Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
Supply Voltage	V_{DD}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-0.5 to (+5VD +0.5)	V
Operating Temperature Range	T_A		°C
Commercial		-0 to +70	
Extended		-40 to +85	
Storage Temperature Range	T_{STG}	-55 to +125	°C
Analog Inputs	V_{IN}	-0.3 to (+5VA + 0.3)	V
Voltage Applied to Outputs in High Impedance (Off) State	V_{HZ}	-0.5 to (+5VD + 0.5)	V
DC Input Clamp Current	I_{IK}	± 20	mA
DC Output Clamp Current	I_{OK}	± 20	mA
Static Discharge Voltage (25°C)	V_{ESD}	± 2500	V
Latch-up Current (25°C)	I_{TRIG}	± 200	mA

SOFTWARE INTERFACE

INTERFACE MEMORY

The DSP communicates with the host by means of a dual-port, interface memory. The interface memory in the DSP contains thirty-two 8-bit registers, labeled register 00 through 1F. Each register can be read from, or written into, by both the host and the DSP. The host communicates with the DSP interface memory via the microprocessor bus.

The host can control modem operation by writing control bits to DSP interface memory and writing parameter values to DSP RAM through the interface memory. The host can monitor modem operation by reading status bits from DSP interface memory and reading parameter values from DSP RAM through interface memory.

INTERFACE MEMORY MAP

The memory maps of DSP interface memory identifying the contents of the 32 addressable registers are shown in Figure 4. These 8-bit registers may be read or written during any host read or write cycle. In order to operate on a single bit or group of bits in a register, the host must read a register then mask out unwanted data. When writing a single bit or group of bits in a register, the host must perform a read-modify-write operation. That is, the host must read the entire register, set or reset the necessary bits without altering the other register bits, then write the unaffected and modified bits back into the interface memory register.

INTERFACE MEMORY BIT FUNCTIONS

Table 12 summarizes the functions of the individual bits in the interface memory. Bits in the interface memory are referred to using the format Z:Q. The register number is denoted by Z (00 through 1F) and the bit number is located by Q (0 through 7, where 0 = LSB).

Register	Bit 7	6	5	4	3	2	1	0
1F	NSIA	NCIA	—	NSIE	NEWS	NCIE	—	NEWC
1E	TDBIA	RDBIA	TDBIE	—	TDBE	RDBIE	—	RDBF
1D	XACC	—	—	—	IOX	XCRD	XWT	XCR
1C	X RAM Address (XADD)							
1B	YACC	—	—	—	—	YCRD	YWT	YCR
1A	Y RAM Address (YADD)							
19	X RAM Data MSB (XDAM)							
18	X RAM Data LSB (XDAL)							
17	Y RAM Data MSB (YDAM)							
16	Y RAM Data LSB (YDAL)							
15	—	—	—	—	—	—	—	—
14	—	—	—	—	—	—	—	—
13	TLVL				VOL		TXCLK	
12	Configuration (CONF)							
11	—	—	—	—	—	—	—	TXP
10	Transmit Data Buffer (TBUFFER)							
0F	RLSD	FED	CTS	DSR	RI	TM	SYNCD	FLAGS
0E	—	BRKD	PE	FE	OE	SPEED		
0D	—	—	—	SCR1	U1DET	SADET	—	—
0C	EDET	—	—	—	DTDIG			
0B	TONEA	TONEB	TONEC	ATV25	ATBELL	—	DTDET	BEL103
0A	—	—	—	—	—	—	—	CRCS
09	NV25	CC	DTMF	ORG	LL	DATA	—	SLEEP
08	—	TPDM	—	DDIS	TRFZ	—	—	RTS
07	RDLE	RDL	L2ACT	—	L3ACT	RB	RA	ABORT
06	BRKS	EXOS	PARSL		PEN	STB	WDSZ	
05	—	DTMFE	FRZSL	TXSQ	TONDT/ CEQE	RCEQ	TXVOC	RXVOC
04	EQRES	SWRES	—	—	EQFZ	IFIX	AGCFZ	CRFZ
03	NRZIE	HDLC	SPLIT	—	—	SDIS	GTE	—
02	—	—	—	—	—	—	—	—
01	—	—	—	—	—	—	—	RXP
00	Receive Data Buffer (RBUFFER)							

Notes:
1. — in the "Bit" columns indicates reserved for modem use only.

Figure 4. Modem Interface Memory Map

Table 12. Interface Memory Bit Definitions

Mnemonic	Location	Default	Name/Description
ABORT	07:0	0	**SDLC/HDLC Abort.** When control bit ABORT is a 1, the transmitter sends continuous marks in SDLC/HDLC mode. When ABORT is a 0, normal SDLC/HDLC transmission is enabled. This bit is valid only in SDLC/HDLC mode.
AGCFZ	04:1	0	**AGC Freeze.** Inhibits updating of the receiver AGC.
ASYNC	08:7	0	**Asynchronous/Synchronous.** When control bit ASYNC is a 1, asynchronous data mode is selected. When ASYNC changes from a 0 to a 1, the receiver's synchronous to asynchronous converter and the transmitter's asynchronous to synchronous converter are configured according to the EXOS, PARSL, PEN, STB and WDSZ bits at that time. ASYNC may be used to switch between synchronous and asynchronous modes at any time in idle or data mode. When ASYNC is a 0, synchronous data mode is selected. The HDLC bit further selects one of two synchronous modes.
ATBELL	0B:3	0	**Bell Answer Tone Detected.** Status bit ATBELL is a 1 when the 2225 Hz answer tone is being detected. ATBELL is a 0 when the 2225 Hz answer tone is not being detected. ATBELL is active only in the originate Dial/Call Progress and originate handshake modes (ORG = 1).
ATV25	0B:4	0	**V25 Answer Tone Detected.** Status bit ATV25 is a 1 when the 2100 Hz answer tone is being detected. ATV25 is a 0 when the 2100 Hz answer tone is not being detected. ATV25 is only active in the Dial/Call Progress and originate handshake modes (ORG = 1).
BEL103	0B:0	0	**Bell 103 Mark Frequency Detected.** Status bit BEL103 is a 1 when the Bell 103 mark frequency (1270 Hz) is being detected. BEL103 is a 0 when the Bell 103 mark frequency is not being detected. BEL103 is active only in answer handshake mode (ORG = 0). **Note**: In order to activate the BEL103 bit after making the transition from Tone mode to Answer handshake mode, the following steps must be taken: a) set ORG, b) set NEWC, c) wait for NEWC to reset, then reset ORG, and d) set NEWC and wait for it to reset.
BRKD	0E:6	0	**Break Detected.** Status bit BRKD is a 1 when continuous space is being received. BRKD is a 0 when continuous space is not being received. (Asynchronous mode only, ASYNC = 1.)
BRKS	06:7	0	**Break Sequence.** **For DPSK Modulation:** When the control bit BRKS is a 1 in parallel asynchronous mode, the modem will send continuous space. When BRKS is a 0, the modem will transmit parallel data from the TBUFFER. (BRKS is valid only when TPDM = 1 and Asynchronous mode is selected, i.e., ASYNC = 1.) **For FSK Modulation:** To send continuous SPACE in parallel asynchronous mode (ASYNC = 1, TPDM = 1), the host must a) read the SPACE frequency Delphi value at TXDPHI2 (XCR = 0, X RAM Address 6Dh) and the MARK frequency Delphi value at TXDPHI1 (XCR = 0, X RAM Address 6Ch) and store the MARK frequency Delphi value in host memory, and b) write the SPACE frequency Delphi value into location TXDPHI1 (XCR = 0, X RAM Address 6Ch). The host should not write any data into TBUFFER. To transmit parallel data from the TBUFFER in parallel asynchronous mode, the host must write the MARK frequency Delphi value from host memory into location TXDPHI1 (XCR = 0, X RAM Address 6Ch). To calculate mark and space frequency values, see the Designer's Guide, Section 4, Parameters 11 and 12.
CC	09:6	0	**Controlled Carrier.** When control bit CC is a 1, the modem operates in controlled carrier (i.e., the carrier is controlled by the RTS bit); when 0, the modem operates in constant carrier (i.e., the carrier stays on when the RTS bit is a 0). Controlled carrier allows the modem transmitter to be controlled by the RTS bit (see Table 4). In PSK modes, when the RTS bit is set to a 1, the transmitter immediately sends scrambled ones for 270 ms and then turns on the CTS bit.
CEQE	05:3	1	**Transmitter Compromise Equalizer Enable.** When control bit CEQE is a 1, the transmitter's passband digital compromise equalizer is inserted into the transmit path. When CEQE is a 0, the equalizer is not inserted into the transmit path.

Table 12. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
CONF	12:0-7	-	**Configuration.** The CONF control bits select the modem operating mode from one of the following configuration codes: Mode / Transmit Data Rate (bps) / Receive Data Rate (bps) / CONF (Hex) / Notes V.22 / 1200 / 1200 / 52 / See Table 1 V.22 / 600 / 600 / 51 / See Table 1 V.21 / 300 / 300 / A0 / See Table 1 V.23 (HDX-Tx1200/Rx1200) / 1200 / 1200 / 42 V.23 (HDX-Tx75/Rx75) / 75 / 75 / 40 V.23 (FDX-Tx75/Rx1200) / 75 / 1200 / 46 V.23 (FDX-Tx1200/Rx75) / 1200 / 75 / 47 Tone / / / 80 Dial/Call Progress Monitor / / / 81 **Notes:** 1. The host must write the desired CONF value upon startup to select the desired mode of operation (see Table 1 for available options). 2. The host must set NEWC to a 1 with the DATA bit = 1 and CONF set to the proper mode code to initiate the mode change from Idle Mode. CONF should be changed only when in the Idle Mode.
CRCS	0A:0	0	**CRC Sending.** Status bit CRCS is a 1 when the transmitter is sending the 2-byte CRC in SDLC/HDLC mode. CRCS is a 0 when the CRC is not being sent.
CRFZ	04:0	0	**Carrier Recovery Freeze.** When control bit CRFZ is a 1, updating of the receiver's carrier recovery phase lock loop (PLL) is inhibited. When reset to a 0, normal updating is enabled.
CTS	0F:5	0	**Clear to Send.** Status bit CTS is set to a 1 when the training sequence has been completed and any data present at TXD (serial data mode) or in TBUFFER (parallel data mode) will be transmitted (see TPDM). CTS response times from an RTS ON or OFF transition after the modem has completed a handshake are shown in Table 4. CTS is 0 when data is not being transmitted.
DATA	09:2	0	**Data Mode.** When the DATA control bit is set to 1, the modem enters data mode in either leased line mode (LL = 1) or handshake mode (LL = 0). This bit should be set to a 1 by the host at a suitable time after completion of dialing or answering. When DATA = 0, the modem is forced to idle mode and no data is transmitted. The modem is prevented from entering/proceeding with the handshake sequence & will ignore the RTS bit.
DDIS	08:4	0	**Descrambler Disable.** When control bit DDIS is a 1, the receiver's descrambler circuit is disabled; when a 0, the descrambler circuit is enabled.
DSR	0F:4	0	**Data Set Ready.** Status bit DSR is set to a 1 at the start of a training sequence.
DTDET	0B:1	0	**DTMF Digit Detected.** Status bit DTDET is set to 1 when a DTMF tone pair is detected and the corresponding hex code has been loaded into DTDIG bits. Status bit DTDET is reset to 0 when a DTMF tone pair is not detected. NEWS is set when DTDET is set. (Tone Mode.)
DTDIG	0C:0-3	0	**Detected DTMF Digit.** When the modem is configured for Tone Mode (CONF = 80h) and DTDET is set, DTDIG contains the hexadecimal code corresponding to the detected digit. The codes are: DTMF Digit / DTDIG Code (Hex) / DTMF Digit / DTDIG Code (Hex) 1 / 0 / 3 / 8 4 / 1 / 6 / 9 7 / 2 / 9 / A * / 3 / # / B 2 / 4 / A / C 5 / 5 / B / D 8 / 6 / C / E 0 / 7 / D / F

Table 12. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
DTMF	09:5	0	**DTMF Dial Select.** When the modem is configured for dialing mode (CONF = 81h), the modem will dial using DTMF tones or pulses. When control bit DTMF is 1, the modem will dial using DTMF tones. When DTMF is 0, the modem will dial using pulses. The DTMF bit can be changed during the dialing process to allow either tone or pulse dialing of consecutive digits. When in dialing mode, the data placed in the Transmitter Data Buffer (TBUFFER) is treated as the digit to be dialed (see TDBE). The number to be dialed must be represented by two hexadecimal digits. The TBUFFER codes are: DTMF Digit / TBUFFER Code (Hex) / DTMF Digit / TBUFFER Code (Hex) 0 00 8 08 1 01 9 09 2 02 * 0A 3 03 A 0B 4 04 B 0C 5 05 C 0D 6 06 # 0E 7 07 D 0F See Note 2 10 See Note 3 11 **NOTES:** 1. Dialing timing is host programmable in DSP RAM (see Section 4). 2. Data modem calling tone (1300 Hz) is generated. 3. Fax modem calling tone (1100 Hz) is generated. 4. If DTMF duration (TONTME) is set to zero, the DTMF tones will be on indefinitely, and this can be used for PTT approval testing.
DTMFE	05:6	1	**DTMF Detector Enable.** When control bit DTMFE is set, the DTMF detector is enabled in Tone mode. When DTMFE is reset, the DTMF detector is disabled.
EDET	0C:7	0	**DTMF Early Detection.** Status bit EDET is set by the modem when the received signal may be a DTMF tone. EDET is set approximately 20 ms after the DTMF signal energy is detected. This bit is reset by the modem if the received signal fails to satisfy any DTMF criteria. (Tone Mode 80h and DTMFE = 1 only.)
EQFZ	04:3	0	**Equalizer Freeze.** When control bit EQFZ is a 1, updating of the receiver's adaptive equalizer taps is inhibited. When a 0, updating is enabled.
EQRES	04:7	0	**Equalizer Reset.** When control bit EQRES is a 1, the receiver adaptive equalizer taps are reset to zero. When a 0, the equalizer taps are updated normally.
EXOS	06:6	0	**Extended Overspeed.** When control bit EXOS is a 1, extended overspeed mode is selected in the transmitter asynchronous-to-synchronous converter and in the receiver synchronous-to-asynchronous converter. When a 0, normal overspeed mode is selected. (See SPLIT.)
FE	0E:4	0	**Framing Error.** Status bit FE is set to a 1 when more than 1 in 8 (or 1 in 4 for extended overspeed) characters are received without a Stop bit in asynchronous mode or an ABORT sequence is detected in SDLC/HDLC synchronous mode. When reset to a 0, no framing error is detected.
FED	0F:6	0	**Fast Energy Detector.** Status bit FED is a 1 when energy above the Turn-On Threshold is being detected. FED is a 0 when energy above the Turn-On Threshold is not being detected. Note that FED may not turn on for very low-level single frequency tones.
FLAGS	0F:0	0	**Flag Sequence.** Status bit FLAGS is a 1 when the transmitter is sending the Flag sequence in parallel synchronous HDLC mode or a constant mark in parallel asynchronous mode. FLAGS is a 0 when the transmitter is sending data.
FRZSL	05:5	0	**Freeze Slew Rate.** When control bit FRZSL is set, the modem will not change the slew rate. When FRZSL is reset, the AGC slew rate is controlled by the modem.

Table 12. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
GTE	03:1	0	**Guard Tone Enable**. When control bit GTE is a 1, sending of the guard tone is enabled (ITU configurations only). The guard tone will be transmitted only by the answering modem. When GTE is a 0, sending of the guard tone is disabled. Set GTE after DSR is set.
HDLC	03:6	0	**HDLC Enable**. When control bit HDLC is a 1, HDLC (High Level Data Link Control) protocol support in parallel synchronous data mode is enabled (the resultant mode is referred to as parallel synchronous HDLC data mode). When HDLC is a 0, HDLC protocol support in parallel synchronous data mode is disabled (the resultant mode is referred to as parallel synchronous normal data mode or parallel synchronous data mode).
IFIX	04:2	1	**Eye Fix**. When control bit IFIX is a 1, the serial diagnostic data output on the EYEX and EYEY pins reflects the Rotated Equalizer Output. When IFIX is a 0, the data on EYEX and EYEY is selected by the addresses in X RAM Address and Y RAM Address registers, respectively.
IOX	1D:3	0	**I/O Register Select**. When control bit IOX is a 1, the X RAM Address is an internal I/O register address. When IOX is a 0, the X RAM Address is an internal RAM address.
L2ACT	07:5	0	**Loop 2 (Local Digital Loopback) Activate**. When control bit L2ACT is a 1, the receiver's digital output is internally connected to the transmitter's digital input (locally activated digital loopback) in accordance with ITU Recommendation V.54. (Data modem modes only.)
L3ACT	07:3	0	**Loop 3 (Local Analog Loopback) Activate**. When control bit L3ACT is a 1, the transmitter's analog output is internally coupled to the receiver's analog input (local analog loopback) in accordance with ITU Recommendation V.54. (Data modem modes only.) The modem may only be placed into loop 3 mode when in idle mode (DATA bit is a 0). After setting the L3ACT bit to a 1, the NEWC bit must also be set then set the DATA bit to a 1, followed by NEWC set to a 1 again. The loopback is then completed when the modem sets DSR, CTS, and RLSD bits to a 1. To terminate the loopback, reset the DATA bit and the L3ACT bit to a 0 and then set NEWC to a 1.
LL	09:3	0	**Leased Line**. in a data modem mode, control bit LL enables entry into leased line training (LL = 1) or non-leased line modes (LL = 0) from the Idle Mode. When LL = 0, mode selection from Idle Mode is determined by the CONF, L3ACT, and ORG bits. (See Designer's Guide, Section 5)
NCIA	1F:6	0	**NEWC Interrupt Active**. When the new configuration interrupt is enabled (NCIE is a 1) and a new configuration is implemented (NEWC is a 0), the modem asserts ~IRQ and sets status bit NCIA to a 1 to indicate that NEWC being a 0 caused ~IRQ to be asserted. The NCIA bit is cleared and ~IRQ due to NEWC is negated when the host resets NCIE to a 0. (See NEWC and NCIE.)
NCIE	1F:2	0	**NEWC Interrupt Enable**. When control bit NCIE is a 1 (interrupt enabled), the modem will assert ~IRQ and set NCIA to a 1 when the NEWC bit is a 0. When NCIE is a 0 (interrupt disabled), NEWC has no effect on ~IRQ or NCIA. (See NEWC and NCIA.)

Table 12. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
NEWC	1F:0	0	**New Configuration.** When control bit NEWC is set to a 1 by the host, the modem will implement the new configuration. The DSP resets the NEWC bit to a 0 to acknowledge the configuration change. A configuration change can also cause ~IRQ to be asserted. (See NCIE and NCIA.) **Note:** Control bit NEWC must be set to a 1 by the host after the host changes the contents of any of the following control bits. Bits that control basic mode entry from Idle Mode: CONF Configuration DATA Data L3ACT Loop 3 Activate LL Leased Line Mode ORG Originate Mode Bits that control basic Data Mode selection: ASYNC Asynchronous Mode Bits that control parallel synchronous mode operation: HDLC HDLC Mode Bits that control parallel and serial asynchronous mode operation: PARSL Parity Select PEN Parity Enable STB Stop Bit Number WDSZ Word Size Bits that control general operation (mode independent): GTE Guard Tone Enable RA Relay A Activate RB Relay B Activate TLVL Transmit Level SLEEP Sleep Enable VOL Volume Control
NEWS	1F:3	0	**New Status.** Status bit NEWS is set to a 1 by the modem when one or more status bits located in registers 0A, 0B, 0E, or 0F have changed state, or a DSP RAM read or write has been completed. NEWS can be reset to a 0 only by the host writing a 0 to this bit position. When set to a 1, this bit can cause ~IRQ to be asserted. (See NSIE and NSIA.)
NRZIE	03:7	0	**Non-Return to Zero Inverted Enable.** When NRZIE is set, NRZI coding is applied to data before scrambling, and NRZI decoding is performed on data after descrambling. (HDLC mode only.)
NSIA	1F:7	0	**NEWS Interrupt Active.** When the new status interrupt is enabled (NSIE is a 1) and a change of status occurs (NEWS is a 1), the modem asserts ~IRQ and sets status bit NSIA to a 1 indicate that NEWS being a 1 caused ~IRQ to be asserted. The NSIA bit is cleared and ~IRQ due to NEWS is negated when the host resets NEWS to a 0. (See NEWS and NSIE.)
NSIE	1F:4	0	**NEWS Interrupt Enable.** When control bit NSIE is a 1 (interrupt enabled), the modem will assert ~IRQ and set NSIA to a 1 when NEWS is a 1. When NSIE is a 0 (interrupt disabled), NEWS has no effect on ~IRQ or NSIA. (See NEWS and NSIA.)
NV25	09:7	0	**No V.25 Answer Sequence** If the modem is in a ITU answer mode (i.e., not Tone or Call Progress), the modem will not transmit (NV25 = 1) or will transmit (NV25 = 0) the 2100 Hz ITU answer tone when a handshake sequence is initiated
OE	0E:3	0	**Overrun Error.** Status bit OE is set to a 1 when the Receiver Data Buffer (RBUFFER) was loaded from the RXA input before the host read the old data from RBUFFER. OE is set to a 0 when RBUFFER was read before new receive data was loaded into RBUFFER. This is valid for both ASYNC mode and SDLC/HDLC mode.
ORG	09:4	0	**Originate.** When control bit ORG is a 1, the modem is set for originate mode; when a 0, the modem is set for answer mode. **Note:** The NEWC bit must be set after the ORG bit is changed.

Table 12. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
PARSL	06:4-50	0	**Parity Select**. Control bits PARSL select the method by which parity is generated and checked in the parallel asynchronous data mode (ASYNC = 1). The options are: 5 4 **Parity Selected** 0 0 Stuff Parity ("9th Data Bit") (see TXP, RXP) 0 1 Space Parity 1 0 Even Parity 1 1 Odd Parity
PE	0E:5	0	**Parity Error**. Status bit PE is set to a 1 when a character with bad parity is received in the asynchronous mode, or a frame with bad CRC is detected in the SDLC/HDLC synchronous mode. PE is set to a 0 when a character with good parity is received or a frame with good CRC is detected.
PEN	06:3	0	**Parity Enable**. When set to a 1, control bit PEN enables parity generation and checking in the parallel data asynchronous mode. When reset to a 0, parity generation and checking is disabled.
RA	07:1	0	**Relay A Activate**. When control bit RA is set to a 1, the ~RADVR output is activated to close the normally open relay (off-hook); when RA is reset to 0, the ~RADVR is turned off to allow the normally open relay to open (on-hook). **Note:** The host has exclusive control of the ~RADVR output through the RA bit except in pulse dial mode.
RB	07:2	0	**Relay B Activate**. When control bit RB is set to a 1, the ~RBDVR output is activated to open the normally closed relay (data); when RB is reset to 0, ~RBDVR is turned off to allow the normally closed relay to close (talk). **Note:** The host has exclusive control of the ~RBDVR output through the RB bit.
RBUFFER	00:0-7, 01:0	0	**Receive Data Buffer**. The host obtains parallel data (or voice sample data) from the modem receiver by reading a data byte from the RBUFFER when RDBF = 1.
RCEQ	05:2	0	**Receiver Compromise Equalizer Enable**. When control bit RCEQ is a 1, the receiver's passband digital compromise equalizer is inserted into the receive path. When RCEQ is a 0, the equalizer is not inserted into the receive path.
RDBF	1E:0	-	**Receiver Data Buffer Full**. When set to a 1, status bit RDBF signifies that the modem wrote valid received data into register 00 (RBUFFER). This condition can also cause ~IRQ to be asserted. The host reading or writing register 00 resets the RDBF bit to 0. (See RDBIE and RDBIA.)
RDBIA	1E:6	0	**Receiver Data Buffer Interrupt Active**. When the receiver data buffer full interrupt is enabled (RDBIE is a 1) and register 00 is written to by the DSP (RDBF is a 1), the modem asserts ~IRQ and sets RDBIA to a 1 to indicate that RDBF being a 1 caused ~IRQ to be asserted. The RDBF bit is cleared and ~IRQ due to RDBF is negated when the host reads or writes register 00. (See RDBF and RDBIE.)
RDBIE	1E:2	0	**Receiver Data Buffer Interrupt Enable**. When control bit RDBIE is a 1 (interrupt enabled), the modem will assert ~IRQ and set the RDBIA bit to a 1 when RDBF is a 1. When RDBIE is a 0 (interrupt disabled), RDBF has no effect on ~IRQ or RDBIA. (See RDBF and RDBIA.)
RDL	07:6	0	**Remote Digital Loopback Request**. When control bit RDL is a 1 (i.e., modem is RDL requester), the modem initiates a request for the remote modem to go into digital loopback, RXD is clamped to mark, and the RLSD bit is reset to a 0 until the loop is established. When the host resets the RDL bit, the modem sends the RDL terminating sequence. If a remote digital loopback request is not acknowledged, the host must reset the RDL bit.
RDLE	07:7	0	**Remote Digital Loopback Response Enable**. When set to a 1, control bit RDLE enables the modem to respond to the remote modem's digital loopback request, thus going into loopback. When this occurs, the modem resets the CTS and RLSD bits to a 0. The TM bit is set to a 1 to inform the host of the test status. RXD is not clamped thus allowing monitoring of the loopback data. While the modem is in digital loopback, the RDL bit is set to a 1. The host may reset the RDL bit causing the modem to exit digital loopback and return to data mode.

Table 12. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
RI	0F:3	0	**Ring Indicator**. Status bit RI is a 1 when a valid ringing signal is being detected. RI is a 0 when a valid ringing signal is not being detected. Ringing is detected if pulses are present on the ~RING input in the 15 - 68 Hz frequency range (default frequency range). The RI bit follows the ringing signal with a 1 during the ON time and a 0 during the OFF time. The minimum and maximum valid ring frequencies are host programmable in DSP RAM.
RLSD	0F:7	0	**Received Line Signal Detector**. Status bit RLSD is a 1 when the carrier is being detected and receive data is valid. RLSD is a 0 when the carrier is not being detected; in this case, RXD output is clamped to mark. **Note:** RXD is also clamped to mark during retrain while the RLSD bit remains on.
RTS	08:0	0	**Request to Send**. Control bit RTS is set to a 1 to request the transmitter to send data.
RXP	01:0	0	**Received Parity Bit**. This status bit is only valid when parity is enabled (PEN = 1), and word size is set for 8 bits per character (WDSZ = 11). In this case, the parity bit received (or ninth data bit) will be available at this location. The host must read this bit before reading the received data buffer (RBUFFER).
RXVOC	05:0	1	**Receiver Voice**. Enables reception of voice samples.
SADET	0D:2	0	**Scrambled Alternating Ones Sequence Detected**. Status bit SADET is a 1 when the Scrambled Alternating Ones sequence is being detected. SADET is a 0 when the Scrambled Alternating Ones sequence is not being detected. **Note:** SADET is used to indicate the response of the remote modem to a remote digital loopback request.
SCR1	0D:4	0	**Scrambled Ones Sequence Detected**. Status bit SCR1 is a 1 when Scrambled Ones is being detected during handshake. SCR1 is a 0 when Scrambled Ones is not being detected.
SDIS	03:2	0	**Scrambler Disable**. When control bit SDIS is a 1, the transmitter scrambler is disabled; when SDIS is a 0, the scrambler is enabled.
SLEEP	09:0	0	**Sleep Enable**. When set to a 1, control bit SLEEP enables the DSP sleep mode. When reset to a 0, the DSP operates in its normal mode.
SPEED	0E:0-2	3	**Speed Indication**. The SPEED status bits indicate the data rate at handshake completion: 2 1 0 — Data Rate* (bps) — Notes 0 0 0 — 75* — V.23 mode 0 0 0 — 300 — Other than V.23 mode 0 0 1 — 600 0 1 0 — 1200 * In V.23, the SPEED bits reflect the received rate only, i.e., not the transmit rate.
SPLIT	03:5	0	**TX Basic Overspeed/RX Extended Overspeed Split**. When control bit SPLIT is a 1 and EXOS is a 1, the transmitter will transmit at the basic overspeed rate while the receiver receives at the extended overspeed rate. This bit applies only in the parallel asynchronous mode (TPDM = 1 and ASYNC = 1).
STB	06:2	0	**No. of Stop Bits**. When control bit STB is a 0, one stop bit is selected in asynchronous mode; when a 1, two stop bits are selected.
SWRES	04:6	0	**Software Reset**. When control bit SWRES is set to a 1, the modem data pump reinitializes to the same state that occurs as a result of a power-on reset (see 5.1).
SYNCD	0F:1	0	**Sync Pattern Detected**. In HDLC mode (i.e., HDLC = 1), status bit SYNCD is a 1 when HDLC flags (7E pattern) are being detected. This bit is valid only in HDLC mode.
TBUFFER	10:0-7, 11:0	0	**Transmit Data Buffer**. The host conveys output data [i.e., dial digits when dial configuration is selected (CONF = 81), or transmit data when transmitter parallel data mode is selected (TPDM = 1) by writing a data byte to the TBUFFER when the TDBE bit is a 1. Bit 0 of the data is transmitted first.
TDBE	1E:3	1	**Transmitter Data Buffer Empty**. When set to a 1, status bit TDBE signifies that the modem has read transmit data from register 10 (TBUFFER) and the host can write new data into register 10. This condition can also cause ~IRQ to be asserted. The host reading or writing register 10 resets the TDBE bit to 0. (See TDBIE and TDBIA.)

Table 12. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
TDBIA	1E:7	0	**Transmitter Data Buffer Interrupt Active.** When the transmitter data buffer empty interrupt is enabled (TDBIE is a 1) and register 10 is empty (TDBE is a 1), the modem asserts ~IRQ and sets status bit TDBIA to a 1 to indicate that TDBE being a 1 caused ~IRQ to be asserted. The TDBIA bit is cleared and ~IRQ due to TDBE is negated when the host writes register 10 or resets TDBIE to a 0 (See TDBIE and TDBE.)
TDBIE	1E:5	0	**Transmitter Data Buffer Interrupt Enable.** When control bit TDBIE is a 1 (interrupt enabled), the modem will assert ~IRQ and set the TDBIA bit to a 1 when TDBE is a 1. When TDBIE is a 0 (interrupt disabled), TDBE has no effect on ~IRQ or TDBIA. (See TDBE and TDBIA.)
TLVL	13:4-7	6	**Transmit Level Attenuation Select.** The TLVL control code selects the transmitter analog output level attenuation at the TXA1/TXA2 pins as follows: **7 6 5 4 — Transmit Level Attenuation (dB ± 0.5 dB)** 0 0 0 0 — 0 dB 0 0 0 1 — 1 dB 0 0 1 0 — 2 dB 0 0 1 1 — 3 dB 0 1 0 0 — 4 dB 0 1 0 1 — 5 dB 0 1 1 0 — 6 dB 0 1 1 1 — 7 dB 1 0 0 0 — 8 dB 1 0 0 1 — 9 dB 1 0 1 0 — 10 dB 1 0 1 1 — 11 dB 1 1 0 0 — 12 dB 1 1 0 1 — 13 dB 1 1 1 0 — 14 dB 1 1 1 1 — 15 dB The host can fine tune the transmit level to a value lying within a 1 dB step by changing a value in DSP RAM (TSCALE).
TM	0F:2	0	**Test Mode.** Status bit TM is set when the modem responds to a remote modem's digital loopback request (RDLE = 1). Otherwise, TM = 0.
TONDT	05:3	1	**Tone Detector Select.** Selects number of tone detect filters as follows: **TONDT — Selection** 1 — All 3 tone detectors 0 — Tone A detector only
TONEA	0B:7	0	**Tone Filter A Energy Detected.** Status bit TONEA is a 1 when: 1. Energy above the threshold is being detected by the Call Progress Monitor filter in the Dial Configuration (CONF = 81h), 2. A 1300 Hz FSK tone energy is being detected by the Tone A bandpass filter in Tone mode (CONF = 80h)
TONEB	0B:6	0	**Tone Filter B Energy Detected.** Status bit TONEB is a 1 when 390 Hz FSK tone energy above the threshold is being detected by the Tone B bandpass filter in Tone mode (CONF = 80). TONEB is a 0 when energy is not being detected. The biquad filter coefficients are host programmable in DSP RAM; see Tone Detect Threshold (THDB) in Section 4.
TONEC	0B:5	0	**Tone Filter C Energy Detected.** Status bit TONEC is a 1 when either 1650 Hz (ORG = 1) or 980 Hz (ORG = 0) FSK tone energy above the threshold is being detected by the Tone C bandpass filter in Tone mode (CONF = 80). TONEC is a 0 when energy is not being detected. The biquad filter coefficients are host programmable in DSP RAM; see Tone Detect Threshold (THDC) in Section 4.

Table 12. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
TPDM	08:6	0	**Transmitter Parallel Data Mode.** When control bit TPDM is a 1, the transmitter accepts parallel data from the host microprocessor interface via the TBUFFER register for transmission rather than serial data from the TXD input pin. When TPDM is a 0, serial data from the TXD input pin is accepted for transmission rather than parallel data from TBUFFER.
TRFZ	08:3	0	**Timing Recovery Freeze.** When control bit TRFZ is a 1, updating of the receiver's timing recovery algorithm is inhibited. When TRFZ is a 0, normal updating occurs.
TXCLK	13:0-1	0	**Transmit Clock Select.** The TXCLK control bits designate the transmitter data clock origin: 1 0 — Transmit Clock 0 0 — Internal (TDCLK and ~RDCLK outputs are independently generated internally) 0 1 — Disable (TDCLK and ~RDCLK outputs are disabled) 1 0 — Slave (TDCLK output is phase locked to the ~RDCLK output 1 1 — External (TDCLK output follows XTCLK input) The suggested use of the Transmit Clock Select bits is: 1. Select mode 01 for asynchronous modes. 2. Select mode 01 for parallel data mode. 3. Select modes 00, 10, or 11 for serial synchronous mode only. When the external clock is chosen, the host supplied clock must be connected to the XTCLK input pin. The external clock will then be reflected at the TDCLK output pin.
TXP	11:0	0	**Transmit Parity Bit (or 9th Data Bit).** Control bit TXP contains the stuffed parity bit (or ninth data bit) for transmission when parity is enabled (PEN = 1), stuff parity is selected (PARSL = 00), and word size is set for 8 bits per character (WDSZ = 11). The host must load the stuffed parity bit (or 9th data bit) into TXP before loading the other 8 bits of data in TBUFFER.
TXSQ	05:4	0	**Transmitter Squelch.** When control bit TXSQ is set to a 1, no energy is transmitted. When TXSQ is a 0, normal transmission is enabled.
TXVOC	05:1	0	**Transmit Voice.** Control bit TXVOC, when set to a 1, enables the transmitting of voice samples in Tone mode (CONF = 80h). When enabled, transmit voice samples are sent to the modem digital-to-analog converter (DAC) from the host through the transmit data buffer (TBUFFER).
U1DET	0D:3	0	**Unscrambled Ones Sequence Detected.** Status bit U1DET is set to a 1 when Unscrambled Ones sequence has been detected. U1DET is reset to a 0 at the end of the Unscrambled Ones sequence. (V.22)
VOL	13:2-3	0	**Volume Control.** The encoded VOL control bits select speaker off or one of three volume attenuation levels. Changing the VOL bits in half-duplex receive modes (V.23 half duplex with DATA = 1) will not affect the speaker volume. 3 2 — Description 0 0 — Speaker off 0 1 — Speaker volume attenuation = 0 dB 1 0 — Speaker volume attenuation = 6 dB 1 1 — Speaker volume attenuation = 12 dB
WDSZ	06:0-1	0	**Data Word Size.** The WDSZ control field sets the number of data bits per character in asynchronous mode as follows: 1 0 — Data Bits/Character 0 0 — 5 0 1 — 6 1 0 — 7 1 1 — 8 The total number of bits per character depends on WDSZ, PEN, and STB bits.

Table 12. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
XACC	1D:7	0	**X RAM Access Enable.** When control bit XACC is a 1, the DSP accesses the X RAM addressed by XADD and XCR. XWT determines if a read or write is performed. The DSP resets XACC to a 0 and sets NEWS to a 1 upon RAM access completion.
XADD	1C:0-7	0	**X RAM Address.** XADD contains the X RAM address used to access the DSP's X Data RAM (XCR = 0) or X Coefficient RAM (XCR = 1) via the X RAM Data LSB and MSB registers (addresses 18 and 19, respectively). (See Table 3-2.)
XCR	1D:0	0	**X Coefficient RAM Select.** When control bit XCR is a 1, XADD applies to the X Coefficient RAM. When XCR is a 0, XADD applies to the X Data RAM. This bit must be set according to the desired RAM address (Table 3-2).
XCRD	1D:2	0	**X RAM Continuous Read.** When control bit XCRD is set to 1, the XACC and XWT bits are ignored & an X RAM read is performed every sample from the location addressed by XADD. When XCRD is set to 0, a single read or write is enabled as controlled by XACC and XWT.
XDAL	18:0-7	0	**X RAM Data LSB.** XDAL is the least significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in the DSP.
XDAM	19:0-7	0	**X RAM Data MSB.** XDAM is the most significant byte of the 16-bit X RAM data word used in reading or writing X RAM locations in the DSP.
XWT	1D:1	0	**X RAM Write.** When XWT is a 1 and XACC is set to a 1, the DSP copies data from the X RAM Data registers (18 and 19) into the X RAM location addressed by XADD and XCR. When control bit XWT is a 0 and XACC is set to a 1, DSP reads X RAM at the location addressed by XADD and XCR and stores the data into the X RAM Data registers (18 and 19).
YACC	1B:7	0	**Y RAM Access Enable.** When control bit YACC is a 1, the DSP accesses the Y RAM addressed by YADD and YCR. YWT determines if a read or write is performed. The DSP resets YACC to a 0 and sets NEWS to a 1 upon RAM access completion.
YADD	1A:0-7	0	**Y RAM Address.** YADD contains the Y RAM address used to access the DSP's Y Data RAM (YCR = 0) or Y Coefficient RAM (YCR = 1) via the Y RAM Data LSB and MSB registers (addresses 16 and 17, respectively). (See Table 3-2.)
YCR	1B:0	0	**Y Coefficient RAM Select.** When control bit YCR is a 1, YADD applies to the DSP's Y Coefficient RAM. When YCR is a 0, YADD applies to the Y Data RAM. This bit must be set according to the desired RAM address (Table 3-2).
YCRD	1B:2	0	**Y RAM Continuous Read.** When control bit YCRD is set to 1, the YACC and YWT bits are ignored & a Y RAM read is performed every sample from the location addressed by YADD. When YCRD is set to 0, a single read or write is enabled as controlled by YACC and YWT.
YDAL	16:0-7	0	**Y RAM Data LSB.** YDAL is the least significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM locations in the DSP.
YDAM	17:0-7	0	**Y RAM Data MSB.** YDAM is the most significant byte of the 16-bit Y RAM data word used in reading or writing Y RAM locations in the DSP.
YWT	1B:1	0	**Y RAM Write.** When YWT is a 1 and YACC is set to a 1, the DSP copies data from the Y RAM Data registers (16 and 17) into the Y RAM location addressed by YADD and YCR. When control bit YWT is a 0 and YACC is set to a 1, the DSP reads Y RAM at the location addressed by YADD and YCR and stores the data into the Y RAM Data registers (16 and 17).

DSP RAM ACCESS

The DSP contains four sections of 16-bit wide random access memory (RAM). Because the DSP is optimized for performing complex arithmetic, the RAM is organized into real (X RAM) and imaginary (Y RAM) sections, as well as data and coefficient sections. The host processor can access (read or write) the X RAM only, the Y RAM only, or both the X RAM and the Y RAM simultaneously in either the data or coefficient section.

INTERFACE MEMORY ACCESS TO DSP RAM

The DSP interface memory acts as an intermediary during host to DSP RAM or DSP RAM to host data exchanges. The addresses stored in modem interface memory RAM Address registers (i. e., XADD and YADD) by the host, in conjunction with the data or coefficient RAM bits (i. e., XCR and YCR) determine the DSP RAM addresses for data access.

HOST PROGRAMMABLE DATA

The parameters available in DSP RAM are listed in along with the X RAM or Y RAM address and corresponding XCR or YCR bit value. The scaling for the host programmable data is described in the RC9624DP, RC96V24DP, and RC14V24DP Modem Designer's Guide (Order No. 822).

MODEM INTERFACE CIRCUIT

The recommended modem interface circuit for the modem packaged in a 68-pin PLCC is shown in Figure 5.

Table 13. DSP RAM Parameters

No.	XCR/YCR*	X RAM Addr	Y RAM Addr	Parameter
1	1	0-1E		Adaptive Equalizer Coefficients, Real
	1	0	–	First Coefficient, Real (1) (Data/ Fax)
	1	10	–	Last Coefficient, Real (17) (Data)
	1	1E	–	Last Coefficient, Real (31) (Fax)
2	1		0-1E	Adaptive Equalizer Coefficients, Imag.
	1	–	0	First Coefficient, Imag. (1) (Data/ Fax)
	1	–	10	Last Coefficient, Imag. (17) (Data)
	1	–	1E	Last Coefficient, Imag. (31) (Fax)
3	0	49	–	Rotated Error, Real (RERRX)
4	0	–	49	Rotated Error, Imaginary (RERRY)
5	0	3F	–	Max AGC Gain Word (MAXG)
6	0	71	–	Pulse Dial Interdigit Time (INTERP)
7	0	7C	–	Tone Dial Interdigit Time (INTERT)
8	0	72	–	Pulse Dial Relay Make Time (PONTME)
9	0	7D	–	Pulse Dial Relay Break Time (POFTME)
10	0	7E	–	DTMF Duration (TONTME)
11	0	6C	–	Tone 1 Angle Increment Per Sample (TXDPHI1)
12	0	6D	–	Tone 2 Angle Increment Per Sample (TXDPHI2)
13	0	6E	–	Tone 1 Amplitude (TXAMP1)
14	0	6F	–	Tone 2 Amplitude (TXAMP2)
15	0	73	–	Max Samples Per Ring Frequency Period (RDMAXP)
16	0	74	–	Min Samples Per Ring Frequency Period (RDMINP)
17	0	5E	–	Real Part of Error (ERRX)
18	0	–	5E	Imaginary Part of Error (ERRY)
19	0	–	3D	Rotation Angle for Carrier Recovery (THETA)
20	0	59	–	Rotated Equalizer Output, Real (WREQX)
21	0	–	59	Rotated Equalizer Output, Imaginary (WREQY)
22	0	3C	–	Lower Part of Phase Error (LPER)
23	0	–	3C	Upper Part of Phase Error (UPER)
24	1	3F	–	Upper Part of AGC Gain Word (UGAIN)
25	1	3E	–	Lower Part of AGC Gain Word (LGAIN)
26	1	2E	–	Average Power (AVGPWR)
27	1	2D	–	Phase Error (PHERR)
28	1	2F	–	Tone Power (TONEA) [TPWRA]
29	1	30	–	Tone Power (ATBELL, BEL103, or TONEB) [TPWRB]

Table 13. DSP RAM Parameters

No.	XCR/YCR*	X RAM Addr	Y RAM Addr	Parameter
30	1	31	–	Tone Power (TONEC, ATV25) [TPWRC]
31	1	36	–	Tone Detect Threshold for TONEA (THDA)
32	1	37	–	Tone Detect Threshold for ATBELL, BEL103, or TONEB (THDB)
33	1	38	–	Tone Detect Threshold for TONEC or ATV25 (THDC)
34	1	–	6C	Biquad 1 Coefficient a0 (CBQ10)
	1	–	6D	Biquad 1 Coefficient a1 (CBQ11)
	1	–	6E	Biquad 1 Coefficient a2 (CBQ12)
	1	–	6F	Biquad 1 Coefficient b1 (CBQ13)
	1	–	70	Biquad 1 Coefficient b2 (CBQ14)
	1	–	71–75	Biquad 2 Coefficients a0 – b2
	1	–	76–7A	Biquad 3 Coefficients a0 – b2
	1	–	7B–7F	Biquad 4 Coefficients a0 – b2
	1	–	62–66	Biquad 5 Coefficients a0 – b2
	1	–	67–6B	Biquad 6 Coefficients a0 – b2
35	0	32	–	Turn-on Threshold (EONTHD)
36	1	35	–	Turn-off Threshold (FEOFTAD)
37	1	–	21	RLSD Turn-off Time (FRZLEN)
38	0	70	–	Transmit Level Output Attenuation (TSCALE)
39	1	52	–	Eye Quality Monitor (EQM) [EQMOUT]
56	0	–	4D	DAC Output Word (WDAC)
57	1	39	–	AGC Slewrate

* XCR if an XRAM address is listed; YCR if a YRAM address is listed.

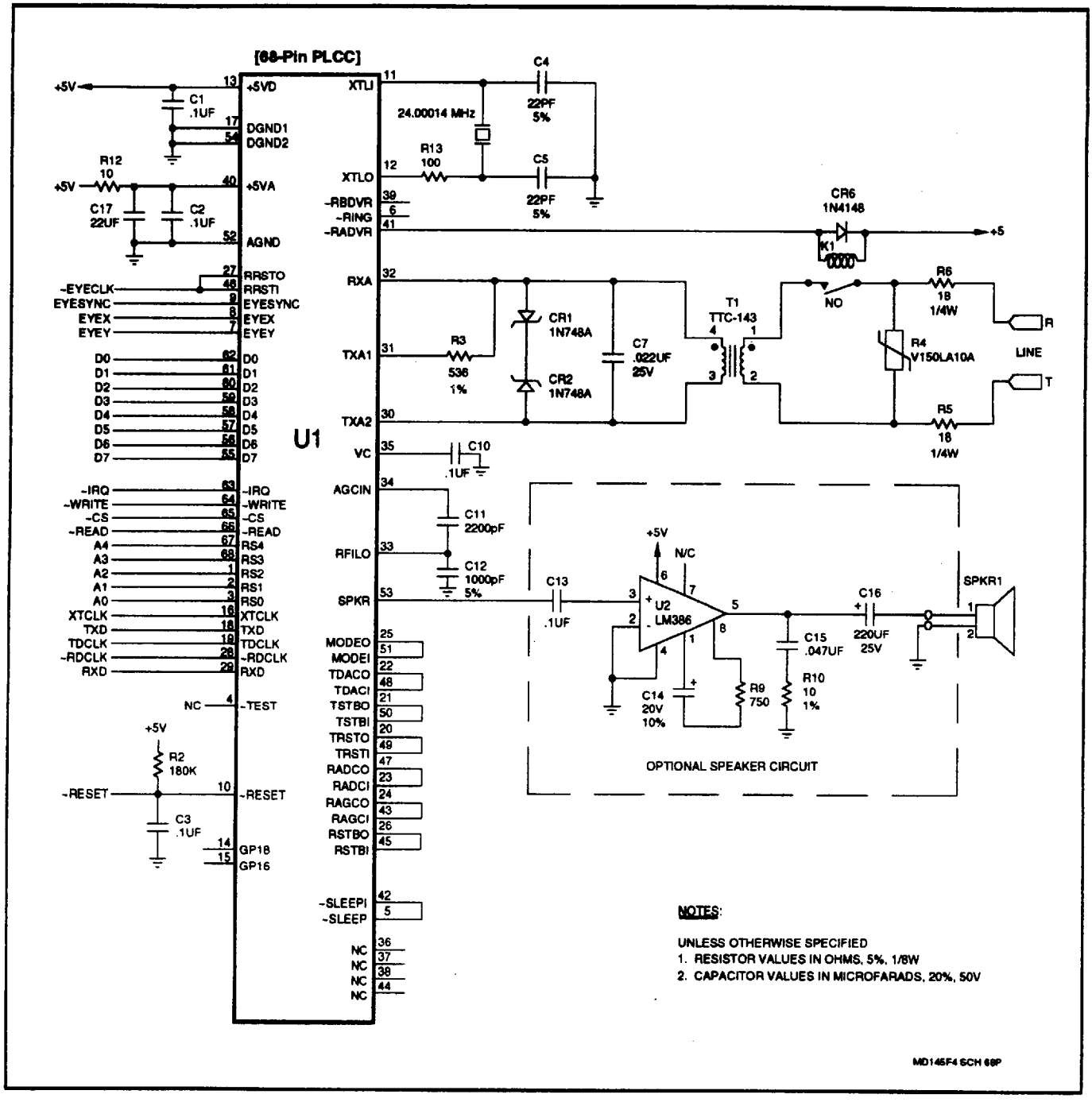
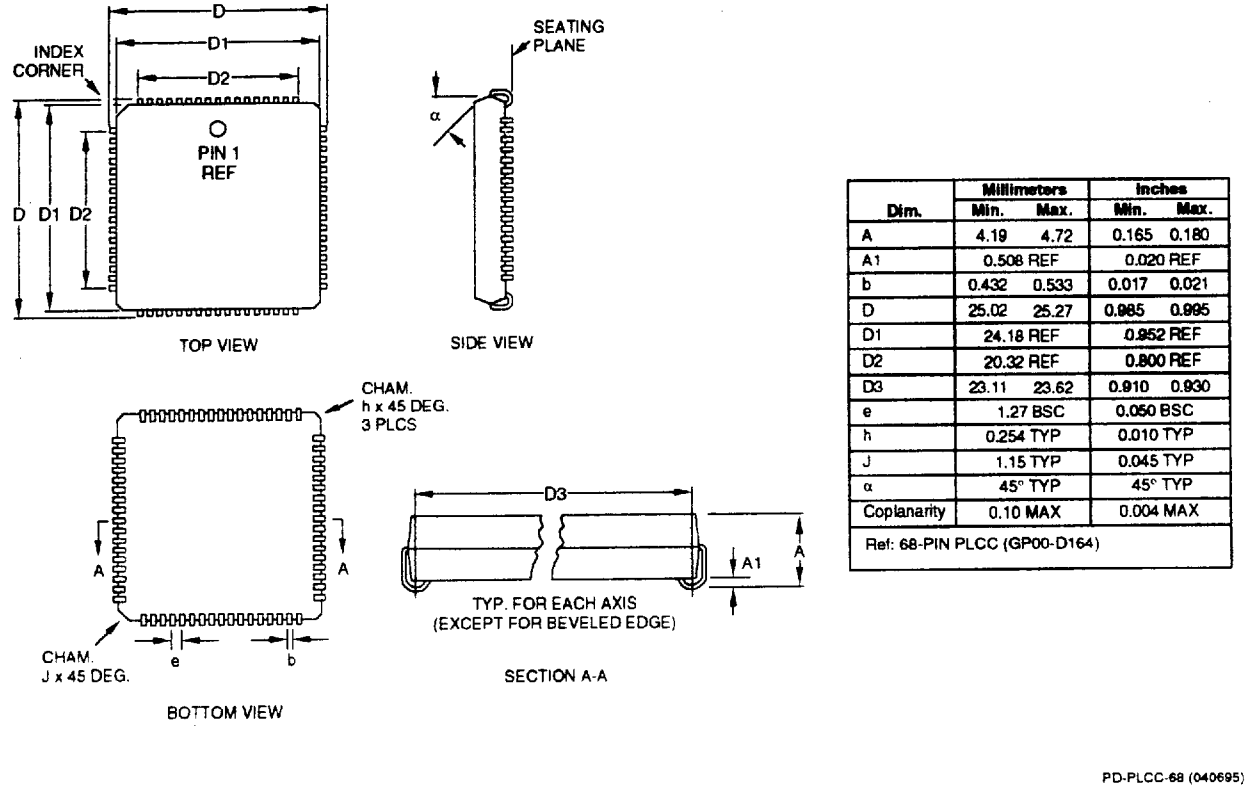


Figure 5. Interconnect Diagram - 68-Pin PLCC

PACKAGE DIMENSIONS

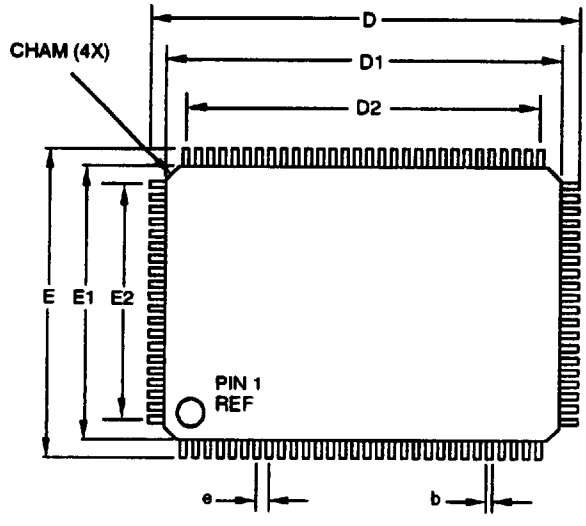
Package dimensions for the 68-pin PLCC are shown in Figure 6.

Package dimensions for the 100-pin PQFP are shown in Figure 7.

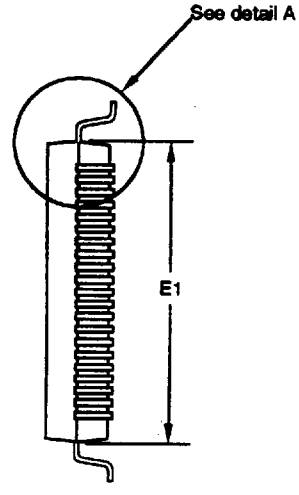


Dim.	Millimeters Min.	Millimeters Max.	Inches Min.	Inches Max.
A	4.19	4.72	0.165	0.180
A1	0.508 REF		0.020 REF	
b	0.432	0.533	0.017	0.021
D	25.02	25.27	0.985	0.995
D1	24.18 REF		0.952 REF	
D2	20.32 REF		0.800 REF	
D3	23.11	23.62	0.910	0.930
e	1.27 BSC		0.050 BSC	
h	0.254 TYP		0.010 TYP	
J	1.15 TYP		0.045 TYP	
α	45° TYP		45° TYP	
Coplanarity	0.10 MAX		0.004 MAX	
Ref: 68-PIN PLCC (GP00-D164)				

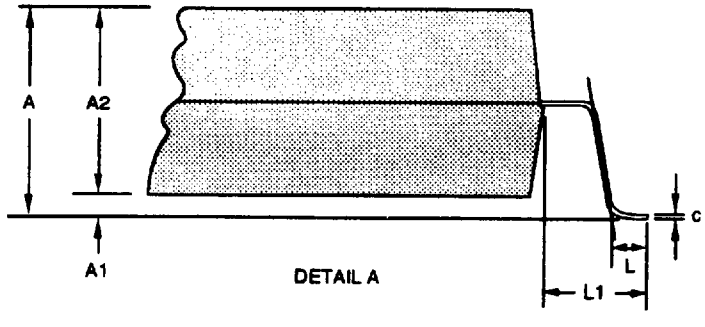
Figure 6. Package Dimensions - 68-Pin PLCC



TOP VIEW



SIDE VIEW



Dim.	Millimeters Min.	Millimeters Max.	Inches* Min.	Inches* Max.
A		2.4 MAX		0.0945 MAX
A1	0.05	0.35	0.0020	0.0138
A2		2.0 REF		0.0787 REF
D	22.95	23.45	0.9035	0.9232
D1		20.0 REF		0.7874 REF
D2		18.85 REF		0.7421 REF
E	16.95	17.45	0.6673	0.6870
E1		14.0 REF		0.5512 REF
E2		12.35 REF		0.4862 REF
L	0.73	1.03	0.0287	0.0406
L1		1.6 REF		0.0630 REF
e		0.65 BSC		0.0256 BSC
b	0.25	0.45	0.0098	0.0177
c	0.13	0.19	0.0051	0.0075
Coplanarity		0.10 MAX		0.004 MAX
Ref: 100-PIN PQFP (GP00-D234)				

* Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may include round-off errors.

PD-PQFP-100 (040695)

Figure 7. Package Dimensions - 100-Pin PQFP