

MITSUBISHI LSIs

M5M411665AJ, TP2-5, -6, -7, -5S, -6S, -7S

HYPER PAGE MODE 1048576-BIT(65536-WORD BY 16-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 65536-word by 16-bit dynamic RAMs, fabricated with a high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of quadruple-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

Self or extended refresh current is small enough for battery back-up application.

This device has $2\overline{W}$ and $1\overline{CAS}$ terminals with a refresh cycle of 256 cycles every 4ms.

FEATURES

Type name	$\overline{RAS}$ access time (max ns)	$\overline{CAS}$ access time (max ns)	Address access time (max ns)	$\overline{OE}$ access time (max ns)	Cycle time (min ns)	Power dissipation (typ mW)
M5M411665AXX-5, -5S	50	13	25	13	90	625
M5M411665AXX-6, -6S	60	15	30	15	110	550
M5M411665AXX-7, -7S	70	20	35	20	130	475

XX=TP2, J

- TP2: 44 pin TSOP(II)/400mil, J: 40 pin SOJ/400mil
- Single 5V $\pm 10\%$ supply
- Low stand-by power dissipation
 - CMOS Input level 5.5 mW(Max)
 - CMOS Input level 550 μ W(Max)*
- Operating power dissipation
 - M5M411665AXX- 5, 5S 688 mW(Max)
 - M5M411665AXX- 6, 6S 605 mW(Max)
 - M5M411665AXX- 7, 7S 523 mW(Max)
- Self refresh capability *
 - Self refresh current 150 μ A(max)
- Extended refresh capability
 - Extended refresh current 150 μ A(max)
- Hyper-page mode (256-column random access), Read-modify-write, $\overline{RAS}$ -only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities.
- Early-write mode, $\overline{OE}$ and $\overline{W}$ to control output buffer impedance
- 256 refresh cycles every 4ms ($A_0 \sim A_7$)
- 256 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles every 32ms ($A_0 \sim A_7$)* for extended refresh
- Byte control for Read / Write operation($2\overline{W}, 1\overline{CAS}$ type)
 - * :Applicable to self refresh version(M5M411665AXX-5S, -6S, -7S :option) only

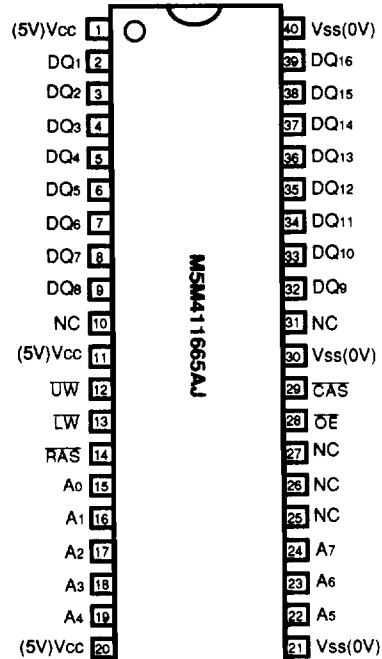
APPLICATION

Microcomputer memory, Refresh memory for CRT, Frame Buffer memory for CRT.

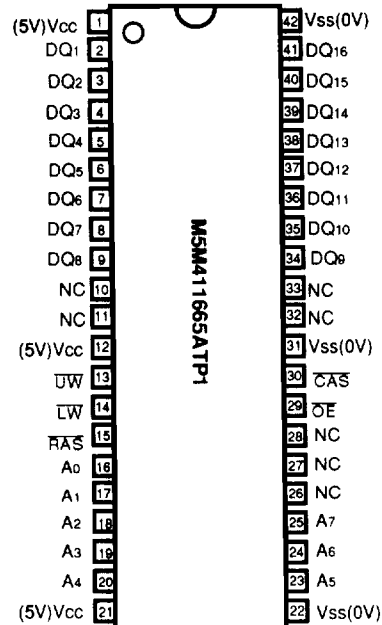
PIN DESCRIPTION

Pin Name	Function
$A_0 \sim A_7$	Address Inputs
$DQ_1 \sim DQ_{16}$	Data Inputs / Outputs
$\overline{RAS}$	Row Address Strobe Input
$\overline{CAS}$	Column Address Strobe Input
$\overline{LW}$	Lower Byte Control Write Control Input
$\overline{UW}$	Upper Byte Control Write Control Input
$\overline{OE}$	Output Enable Input
Vcc	Power Supply (+5V)
Vss	Ground (0V)

PIN CONFIGURATION (TOP VIEW)



Outline 40P0K(400mil 40 pin SOJ)

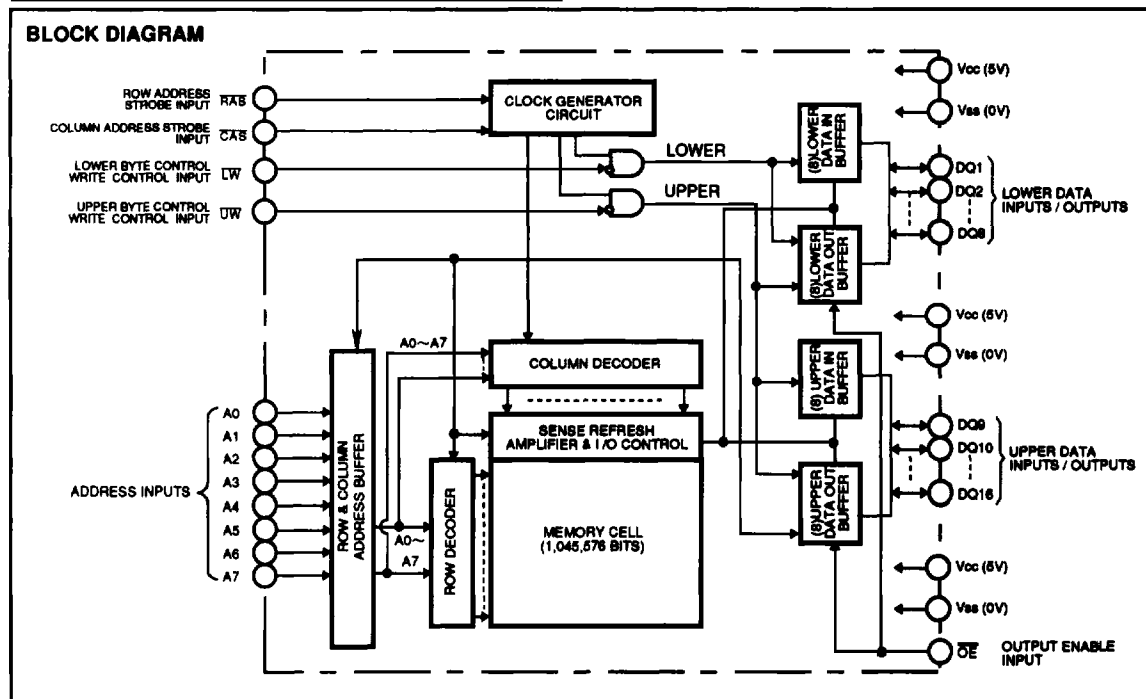
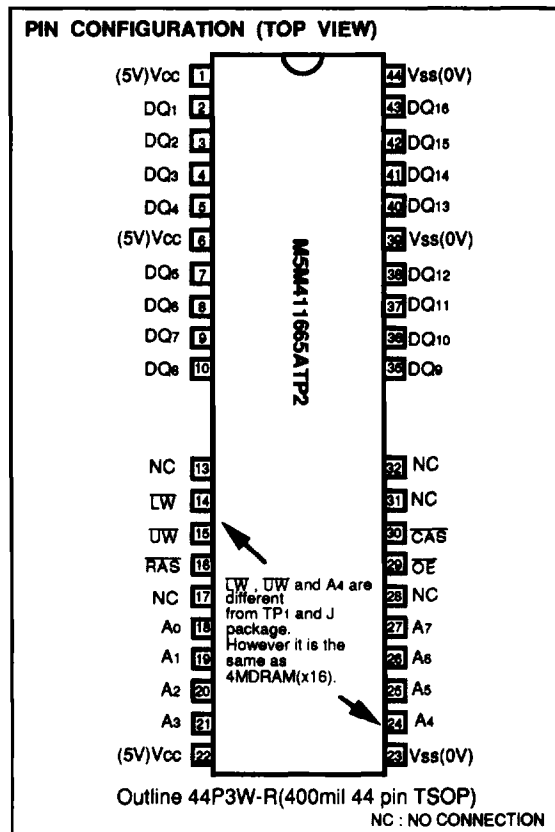


Outline 42P3U-E(300mil 42 pin TSOP)

NC: NO CONNECTION

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FUNCTION

In addition to normal read,write, and read-modify-write operations the M5M411665 ATP2, AJ provides a number of other functions,e.g., Hyper Page Mode, RAS-only refresh,and delayed-write.

The input conditions for each are shown in Table 1.

Table 1. Input conditions for each mode

Operation	Inputs							input / output				Refresh	Remark
	RAS	LW	UW	CAS	OE	Row address	Column address	Lower		Upper			
								D	Q	D	Q		
Read	ACT	NAC	NAC	ACT	ACT	APD	APD	OPN	VLD	OPN	VLD	YES	Hyper page mode identical
Early write	ACT	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	VLD	OPN	YES	
Upper early	ACT	NAC	ACT	ACT	DNC	APD	APD	DNC	OPN	VLD	OPN	YES	
Lower early	ACT	ACT	NAC	ACT	DNC	APD	APD	VLD	OPN	DNC	OPN	YES	
Delayed write	ACT	ACT	ACT	ACT	ACT	APD	APD	VLD	OPN	VLD	OPN	YES	
Upper delayed	ACT	NAC	ACT	ACT	ACT	APD	APD	DNC	OPN	VLD	OPN	YES	
Lower delayed	ACT	ACT	NAC	ACT	ACT	APD	APD	VLD	OPN	DNC	OPN	YES	
Read-modify-W	ACT	ACT	ACT	ACT	ACT	APD	APD	VLD	OPN	VLD	OPN	YES	
Upper RMW	ACT	NAC	ACT	ACT	ACT	APD	APD	DNC	OPN	VLD	OPN	YES	
Lower RMW	ACT	ACT	NAC	ACT	ACT	APD	APD	VLD	OPN	DNC	OPN	YES	
RAS only-R	ACT	DNC	DNC	NAC	DNC	APD	DNC	DNC	OPN	DNC	OPN	YES	
Hidden refresh	ACT	NAC	NAC	ACT	ACT	DNC	DNC	OPN	VLD	OPN	VLD	YES	
CBRefresh (Extended)	ACT	DNC	DNC	ACT	DNC	DNC	DNC	DNC	OPN	DNC	OPN	YES	
Self Refresh*	ACT	DNC	DNC	ACT	DNC	DNC	DNC	DNC	OPN	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	DNC	OPN	NO	

Note :ACT ; active DNC ; don't care VLD ; valid IVD ; invalid APD ; applied OPN ; open NAC ; nonactive

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ABSOLUTE MAXIMUN RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage	With respect to V _{SS}	-1~7	V
V _I	Input voltage		-1~7	V
V _O	Output voltage		-1~7	V
I _O	Output current		50	mA
P _d	Power dissipation	T _a =25°C	1000	mW
T _{opr}	Operating temperature		0~70	°C
T _{stg}	Storage temperature		-65~150	°C

RECOMMENDED OPERATING CONDITIONS (T_a=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Norm	Max	
V _{CC}	Supply voltage	4.5	5.0	5.5	V
V _{SS}	Supply voltage	0	0	0	V
V _{IH}	High-level input voltage, all inputs	2.4		6.0	V
V _{IL}	Low-level input voltage, all inputs	-0.5**		0.8	V

Note 1: All voltage values are with respect to V_{SS}

** : V_{IL}(min) is -2.0V when pulse width is less than 25ns.(pulse width is with respect to V_{SS}.)

ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{CC}= 5V±10%, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V _{OH}	High-level output voltage		I _{OH} = -2mA	2.4		V _{CC}	V
V _{OL}	Low-level output voltage		I _{OL} = 2mA	0		0.4	V
I _{OZ}	Off-state output voltage		Q floating, 0V ≤ V _{OUT} ≤ 5.5V	-10		10	μA
I _I	Input current		0V ≤ V _{IH} ≤ 6.0V, Other inputs pins = 0V	-10		10	μA
I _{CC1} (AV)	Average supply current from V _{CC} operating (Note 3,4,5)	M5M411665A-5,-5S	RAS, CAS cycling trc = twc = min. output open			125	mA
		M5M411665A-6,-6S				110	
		M5M411665A-7,-7S				95	
I _{CC2}	Supply current from V _{CC} , stand-by (Note 6)		RAS = CAS = V _{IH} , output open			2	mA
			RAS = CAS ≥ V _{CC} -0.5V output open			1.0	
						0.1*	
I _{CC3} (AV)	Average supply current from V _{CC} , RAS only refresh mode (Note 3,5)	M5M411665A-5,-5S	RAS cycling, CAS = V _{IH} trc = min. output open			125	mA
		M5M411665A-6,-6S				110	
		M5M411665A-7,-7S				95	
I _{CC4} (AV)	Average supply current from V _{CC} Hyper Page Mode (Note 3,4,5)	M5M411665A-5,-5S	RAS = V _{IL} , CAS cycling trc = min. output open			125	mA
		M5M411665A-6,-6S				110	
		M5M411665A-7,-7S				95	
I _{CC6} (AV)	Average supply current from V _{CC} CAS before RAS refresh mode (Note 3,5)	M5M411665A-5,-5S	CAS before RAS refresh cycling trc = min. output open			115	mA
		M5M411665A-6,-6S				100	
		M5M411665A-7,-7S				85	
I _{CC8} (AV) *	Average supply current from V _{CC} Extended-Refresh mode (Note 6)		RAS cycling CAS ≤ 0.2V or CAS before RAS refresh cycling RAS ≤ 0.2V or ≥ V _{CC} -0.2V CAS ≤ 0.2V or ≥ V _{CC} -0.2V W ≤ 0.2V or ≥ V _{CC} -0.2V OE ≤ 0.2V or ≥ V _{CC} -0.2V A ₀ ~A ₇ ≤ 0.2V or ≥ V _{CC} -0.2V DQ = open trc = 125 μs, tRAS=tRAS min ~1 μs			150	μA
I _{CC9} (AV) *	Average supply current from V _{CC} Self-Refresh mode (Note 6)		RAS = CAS ≤ 0.2V output open			150	μA

Note 2: Current flowing into an IC is positive, out is negative.

3: I_{CC1} (AV), I_{CC3} (AV), I_{CC4} (AV), and I_{CC6} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

Address transient between RAS and CAS happens once or less. Address transient during CAS cycle happens once or less.

4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.

5: Column Address can be changed once or less while RAS=V_{IL} and CAS=V_{IH}.



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CAPACITANCE (Ta=0~70°C, Vcc= 5V±10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C _{I(A)}	Input capacitance, address inputs	V _I =V _{ss} f=1MHz V _I =25mVrms			5	pF
C _{I(CLK)}	Input capacitance, clock inputs				7	pF
C _{I/O}	Input/Output capacitance, data ports				7	pF

SWITCHING CHARACTERISTICS (Ta=0~70°C, Vcc= 5V±10%, Vss=0V, unless otherwise noted) (Note 6,14,15)

Symbol	Parameter	Limits						Unit
		M5M411665A-5, -5S		M5M411665A-6, -6S		M5M411665A-7, -7S		
		Min	Max	Min	Max	Min	Max	
tCAC	Access time from $\overline{\text{CAS}}$ low (Note 7,8)		13		15		20	ns
tRAC	Access time from $\overline{\text{RAS}}$ low (Note 7,9)		50		60		70	ns
tAA	Column address access time (Note 7,10)		25		30		35	ns
tCPA	Access time from $\overline{\text{CAS}}$ precharge (Note 7,11)		28		33		38	ns
tOEA	Access time from $\overline{\text{OE}}$ low (Note 7)		13		15		20	ns
tOHC	Output hold time from $\overline{\text{CAS}}$ (Note 13)	5		5		5		ns
tOHR	Output hold time from $\overline{\text{RAS}}$ (Note 13)	5		5		5		ns
tCLZ	Output low impedance time from $\overline{\text{CAS}}$ low (Note 7)	5		5		5		ns
tOEZ	Output disable time after $\overline{\text{OE}}$ high (Note 12)		13		15		20	ns
tWEZ	Output disable time after $\overline{\text{WE}}$ high (Note 12)		13		15		20	ns
tOFF	Output disable time after $\overline{\text{CAS}}$ high (Note 12,13)		13		15		20	ns
tREZ	Output disable time after $\overline{\text{RAS}}$ high (Note 12,13)		13		15		20	ns

Note 6: An initial pause of 500 μ s is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{\text{RAS}}$ clock such as $\overline{\text{RAS}}$ -Only refresh).

Note the $\overline{\text{RAS}}$ may be cycled during the initial pause. And any 8 $\overline{\text{RAS}}$ or $\overline{\text{RAS}}/\overline{\text{CAS}}$ cycles are required after prolonged periods (greater than 4 ms) of $\overline{\text{RAS}}$ inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to 1TTL loads and 50pF.

The reference levels for measuring of output signals are 2.0V(V_{OH}) and 0.8V(V_{OL}).

8: Assumes that t_{RCD} ≥ t_{RCD(max)} and t_{ASC} ≥ t_{ASC(max)} and t_{CP} ≥ t_{CP(max)}.

9: Assumes that t_{RCD} ≤ t_{RCD(max)} and t_{RAD} ≤ t_{RAD(max)}. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table,

t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

10: Assumes that t_{RAD} ≥ t_{RAD(max)} and t_{ASC} ≤ t_{ASC(max)}.

11: Assumes that t_{CP} ≤ t_{CP(max)} and t_{ASC} ≥ t_{ASC(max)}.

12: t_{OEZ}(max), t_{WEZ}(max), t_{OFF}(max) and t_{REZ}(max) defines the time at which the output achieves the high impedance state (I_{OUT} ≤ |±10 μ A|) and is not reference to V_{OH}(min) or V_{OL}(max).

13: Output is disabled after both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ go to high.

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TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Hyper-Page Mode Cycles)

(Ta=0 ~70°C, Vcc = 5V ±10%, Vss=0V, unless otherwise noted) (Note 14,15)

Symbol	Parameter	Limits						Unit
		M5M411665A-5,-5S		M5M411665A-6,-6S		M5M411665A-7,-7S		
		Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time		4		4		4	ms
tREF	Refresh cycle time*		32		32		32	ms
tRP	RAS high pulse width	30		40		50		ns
tRCD	Delay time, RAS low to CAS low (Note 16)	18	32	20	38	20	42	ns
tCRP	Delay time, CAS high to RAS low	5		5		5		ns
tRPC	Delay time, RAS high to CAS low	0		0		0		ns
tCPN	CAS high pulse width	8		10		13		ns
tRAD	Column address delay time from RAS low (Note 17)	13	25	15	30	15	35	ns
tASR	Row address setup time before RAS low	0		0		0		ns
tASC	Column address setup time before CAS low (Note 18)	0	10	0	13	0	13	ns
tRAH	Row address hold time after RAS low	8		10		10		ns
tCAH	Column address hold time after CAS low	8		10		10		ns
tDZC	Delay time, data to CAS low (Note 19)	0		0		0		ns
tDZO	Delay time, data to OE low (Note 19)	0		0		0		ns
tRDD	Delay time, RAS high to data (Note 20)	13		15		20		ns
tCDD	Delay time, CAS high to data (Note 20)	13		15		20		ns
tODD	Delay time, OE high to data (Note 20)	13		15		20		ns
tT	Transition time (Note 21)	1	50	1	50	1	50	ns

Note 14 : The timing requirements are assumed tT = 2ns.

15 : VIH(min) and VIL(max) are reference levels for measuring timing of input signals.

16 : tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA.

17 : tRAD(max) is specified as a reference point only. If tRAD ≥ tRAD(max) and tASC ≤ tASC(max), access time is controlled exclusively by tAA.

18 : tASC(max) is specified as a reference point only. If tRCD ≥ tRCD(max) and tASC ≥ tASC(max), access time is controlled exclusively by tCAC.

19 : Either tDZC or tDZO must be satisfied.

20 : Either tRDD or tCDD or tODD must be satisfied.

21 : tT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		M5M411665A-5,-5S		M5M411665A-6,-6S		M5M411665A-7,-7S		
		Min	Max	Min	Max	Min	Max	
tRC	Read cycle time	90		110		130		ns
tRAS	RAS low pulse width	50	10000	60	10000	70	10000	ns
tCAS	CAS low pulse width	8	10000	10	10000	13	10000	ns
tCSH	CAS hold time after RAS low	40		48		55		ns
tRSH	RAS hold time after CAS low	13		15		20		ns
tRCS	Read Setup time before CAS low	0		0		0		ns
tRCH	Read hold time after CAS high (Note 22)	0		0		0		ns
tRRH	Read hold time after RAS high (Note 22)	0		0		0		ns
tRAL	Column address to RAS hold time	25		30		35		ns
tCAL	Column address to CAS hold time	13		18		23		ns
tORH	RAS hold time after OE low	13		15		20		ns
tOCH	CAS hold time after OE low	13		15		20		ns

Note 22: Either tRCH or tRRH must be satisfied for a read cycle.

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Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits						Unit
		M5M411665A-5,-5S		M5M411665A-6,-6S		M5M411665A-7,-7S		
		Min	Max	Min	Max	Min	Max	
tWC	Write cycle time	90		110		130		ns
tRAS	RAS low pulse width	50	10000	60	10000	70	10000	ns
tCAS	CAS low pulse width	8	10000	10	10000	13	10000	ns
tCSH	CAS hold time after RAS low	40		48		55		ns
tRSH	RAS hold time after CAS low	13		15		20		ns
twCS	Write setup time before CAS low (Note 24)	0		0		0		ns
twCH	Write hold time after CAS low	8		10		13		ns
tcWL	CAS hold time after W low	8		10		13		ns
trWL	RAS hold time after W low	8		10		13		ns
tWP	Write pulse width	8		10		13		ns
tDS	Data setup time before CAS low or W low	0		0		0		ns
tDH	Data hold time after CAS low or W low	8		10		13		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M411665A-5,-5S		M5M411665A-6,-6S		M5M411665A-7,-7S		
		Min	Max	Min	Max	Min	Max	
trWC	Read write / read modify write cycle time (Note 23)	109		133		161		ns
tRAS	RAS low pulse width	75	10000	89	10000	107	10000	ns
tCAS	CAS low pulse width	38	10000	44	10000	57	10000	ns
tCSH	CAS hold time after RAS low	70		82		99		ns
tRSH	RAS hold time after CAS low	38		44		57		ns
trCS	Read setup time before CAS low	0		0		0		ns
tcWD	Delay time, CAS low to W low (Note 24)	28		32		42		ns
trWD	Delay time, RAS low to W low (Note 24)	65		77		92		ns
tAWD	Delay time, address to W low (Note 24)	40		47		57		ns
toEH	OE hold time after W low	13		15		20		ns

Note 23 : trWC is specified as trWC(min)=trAC(max)+tODD(min)+trWL(min)+trP(min)+5tT.

24 : twCS, tcWD, trWD and tAWD and, tcPWD are specified as reference points only. If twCS ≥ twCS(min) the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If tcWD ≥ tcWD(min), trWD ≥ trWD(min), tAWD ≥ tAWD(min) and tcPWD ≥ tcPWD(min) (for Hyper Page Mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until CAS or OE goes back to VIH) is indeterminate.

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Hyper Page Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle,
Read Write Mix Cycle, Hi-Z control by $\overline{OE}$ or $\overline{W}$) (Note 25)

Symbol	Parameter	Limits						Unit
		M5M411665A-5,-5S		M5M411665A-6,-6S		M5M411665A-7,-7S		
		Min	Max	Min	Max	Min	Max	
tHPC	Hyper Page Mode read / write cycle time (Note26)	20		25		30		ns
tHPRWC	Hyper Page Mode read write / read modify write cycle time	57		66		79		ns
tDOH	Output hold time from $\overline{CAS}$ low	5		5		5		ns
tRAS	RAS low pulse width for read write cycle (Note27)	65	100000	77	100000	92	100000	ns
tCP	$\overline{CAS}$ high pulse width (Note28)	8	13	10	16	13	16	ns
tCPRH	RAS hold time after $\overline{CAS}$ precharge	28		33		38		ns
tCPWD	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note24)	43		50		60		ns
tCHOL	Hold time to maintain the data Hi-Z until $\overline{CAS}$ access	7		7		7		ns
tOEPE	$\overline{OE}$ Pulse Width (Hi-Z control)	7		7		7		ns
tWPE	$\overline{W}$ Pulse Width (Hi-Z control)	7		7		7		ns
tHCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low after read	28		32		42		ns
tHAWD	Delay time, Address to $\overline{W}$ low after read	40		47		57		ns
tHPWD	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low after read	43		50		60		ns
tHCOD	Delay time, $\overline{CAS}$ low to $\overline{OE}$ high after read	13		15		20		ns
tHAOD	Delay time, Address to $\overline{OE}$ high after read	25		30		35		ns
tHPOD	Delay time, $\overline{CAS}$ precharge to $\overline{OE}$ high after read	28		33		38		ns

Note 25: All previously specified timing requirements and switching characteristics are applicable to their respective Hyper Page Mode cycle.

26: tHPC(min) is specified in the case of read-only and early write-only in Hyper Page Mode.

27: tRAS(min) is specified as two cycles of $\overline{CAS}$ input are performed.

28: tCP(max) is specified as a reference point only.

$\overline{CAS}$ before RAS Refresh Cycle (Note 29)

Symbol	Parameter	Limits						Unit
		M5M411665A-5,-5S		M5M411665A-6,-6S		M5M411665A-7,-7S		
		Min	Max	Min	Max	Min	Max	
tCSR	CAS setup time before RAS low	5		5		5		ns
tCHR	CAS hold time after RAS low	10		10		15		ns

Note 29: Eight or more $\overline{CAS}$ before RAS cycles instead of eight RAS cycles are necessary for proper operation of $\overline{CAS}$ before RAS refresh mode.

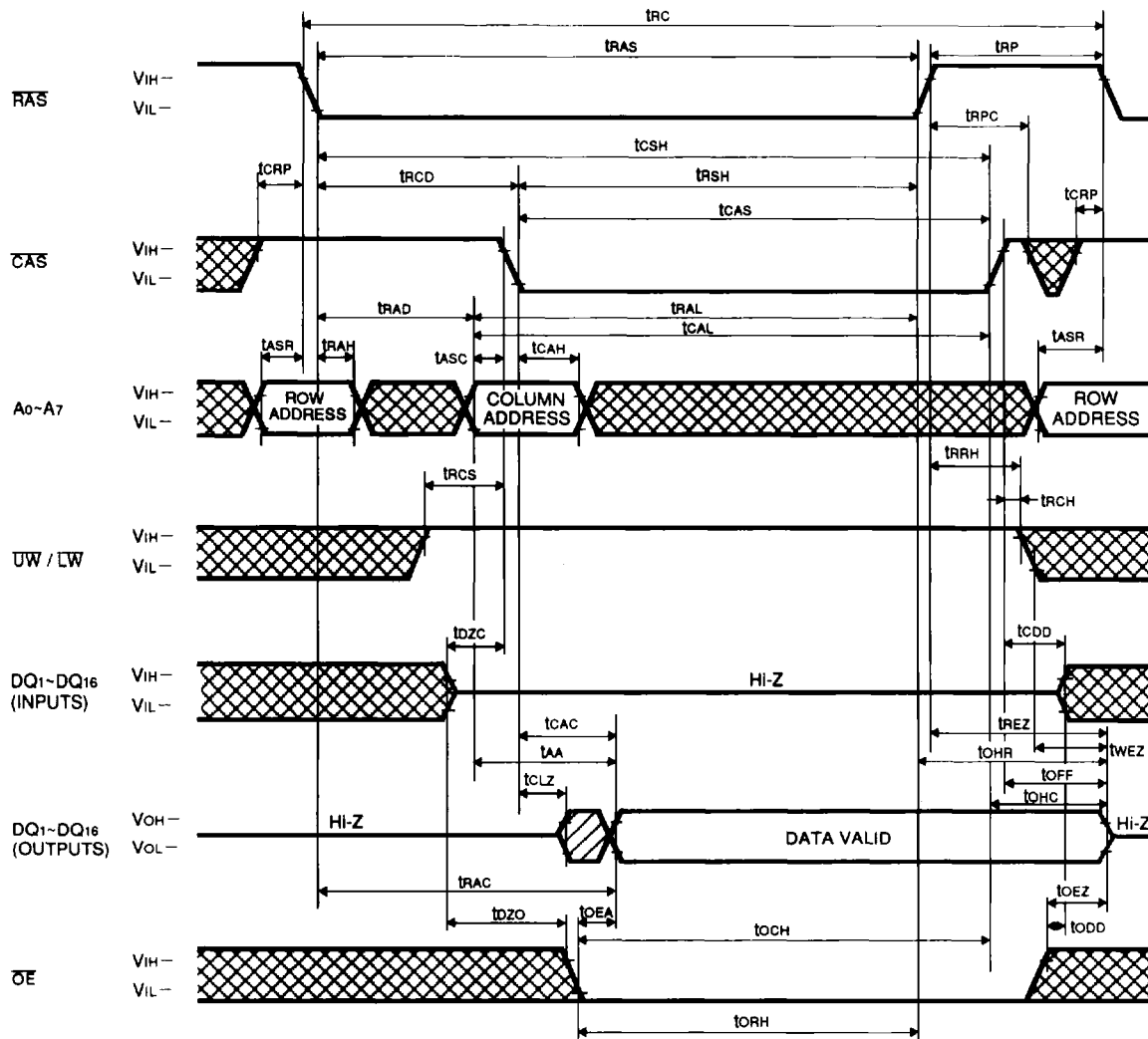
Self Refresh Cycle* (Note 32)

Symbol	Parameter	Limits						Unit
		M5M411665A-5,-5S		M5M411665A-6,-6S		M5M411665A-7,-7S		
		Min	Max	Min	Max	Min	Max	
tRASS	CBR self refresh RAS low pulse width	100		100		100		μs
tRPS	CBR self refresh RAS high precharge time	90		110		130		ns
tCHS	CBR self refresh CAS hold time	- 50		- 50		- 50		ns

M5M411665AJ, TP2-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 1048576-BIT(65536-WORD BY 16-BIT) DYNAMIC RAM

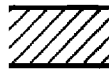
Timing Diagrams (Note 30) Read Cycle



Note 30



Indicates the don't care input.
 $V_{IH}(\min) \leq V_{IN} \leq V_{IH}(\max)$ or $V_{IL}(\min) \leq V_{IN} \leq V_{IL}(\max)$

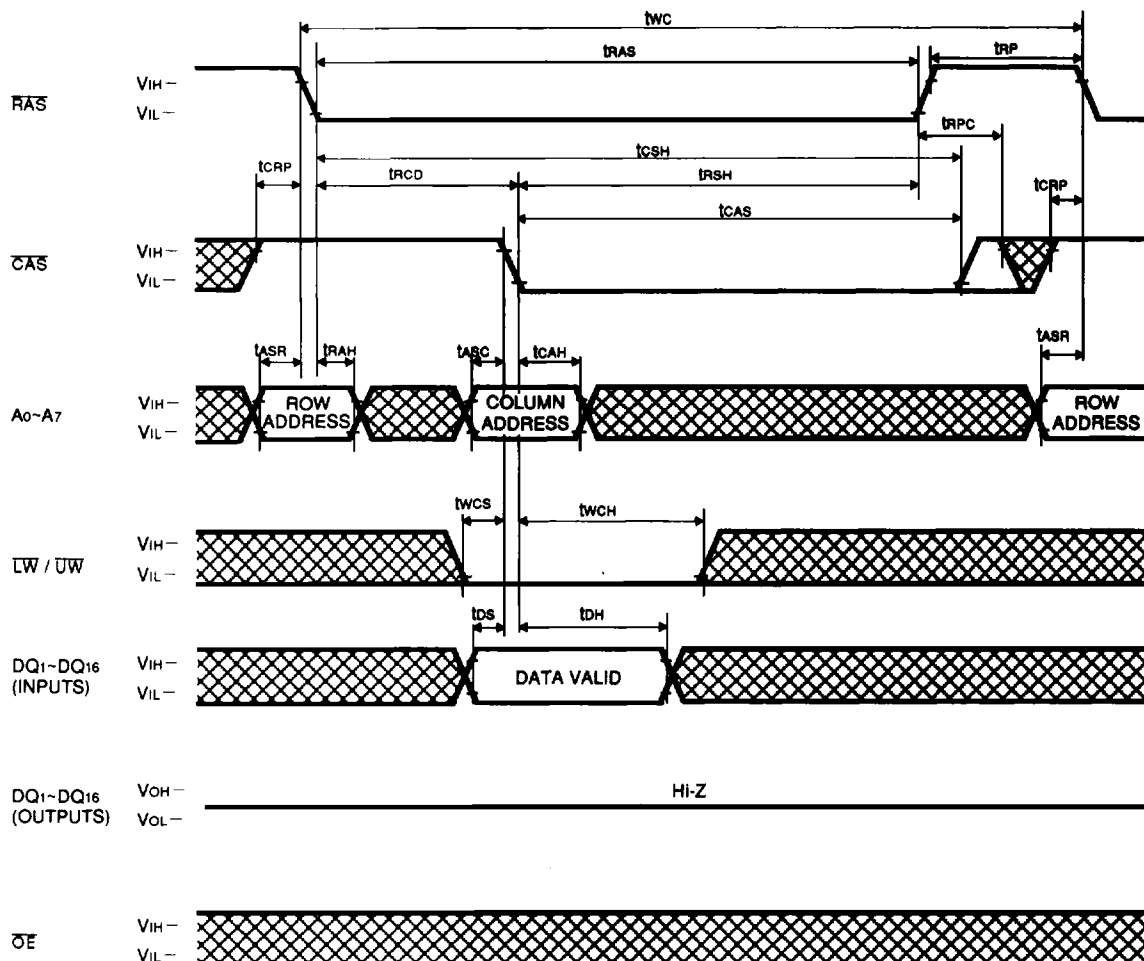


Indicates the invalid output.

M5M411665AJ,TP2-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 1048576-BIT(65536-WORD BY 16-BIT) DYNAMIC RAM

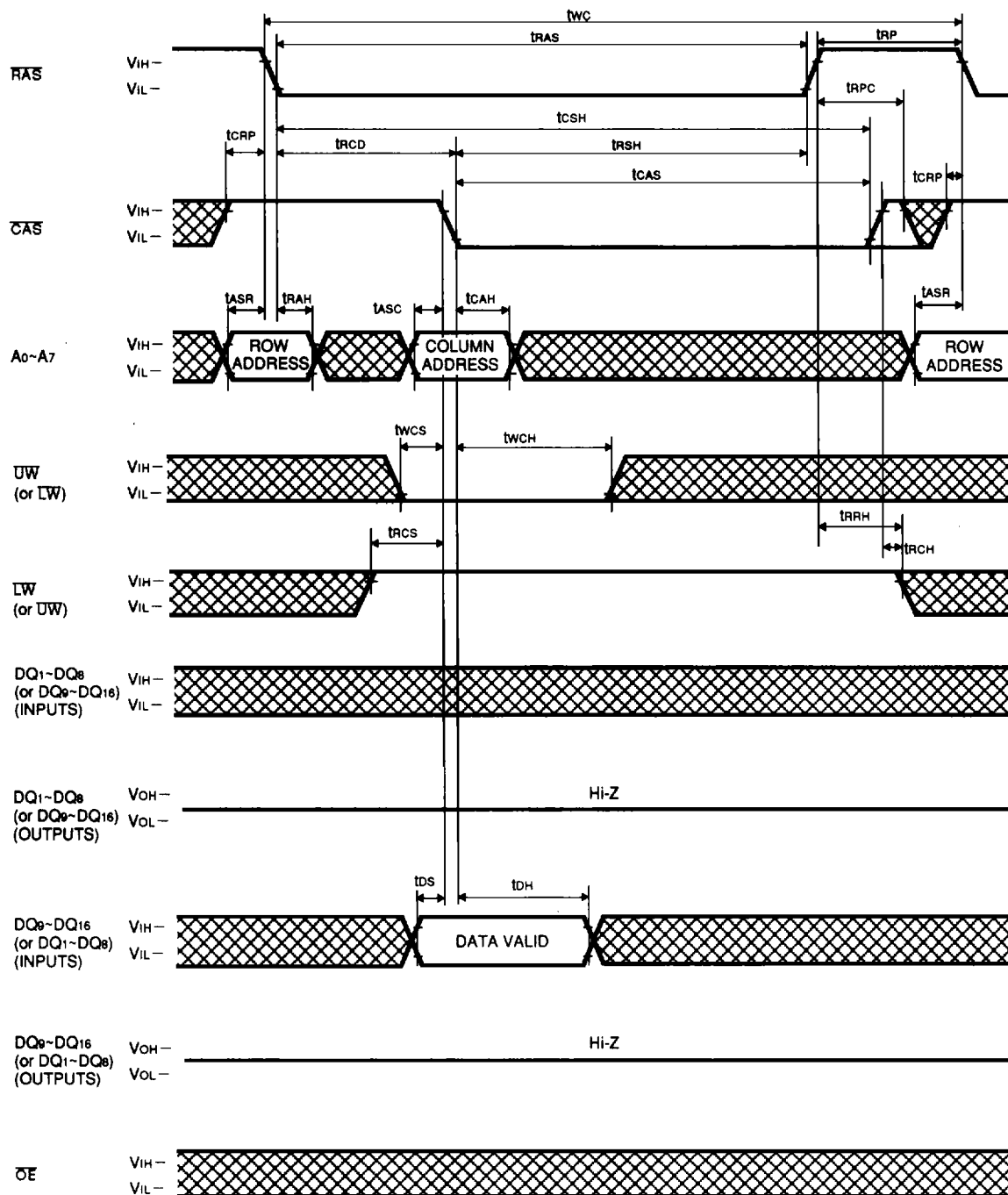
Early Write Cycle



M5M411665AJ,TP2-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 1048576-BIT(65536-WORD BY 16-BIT) DYNAMIC RAM

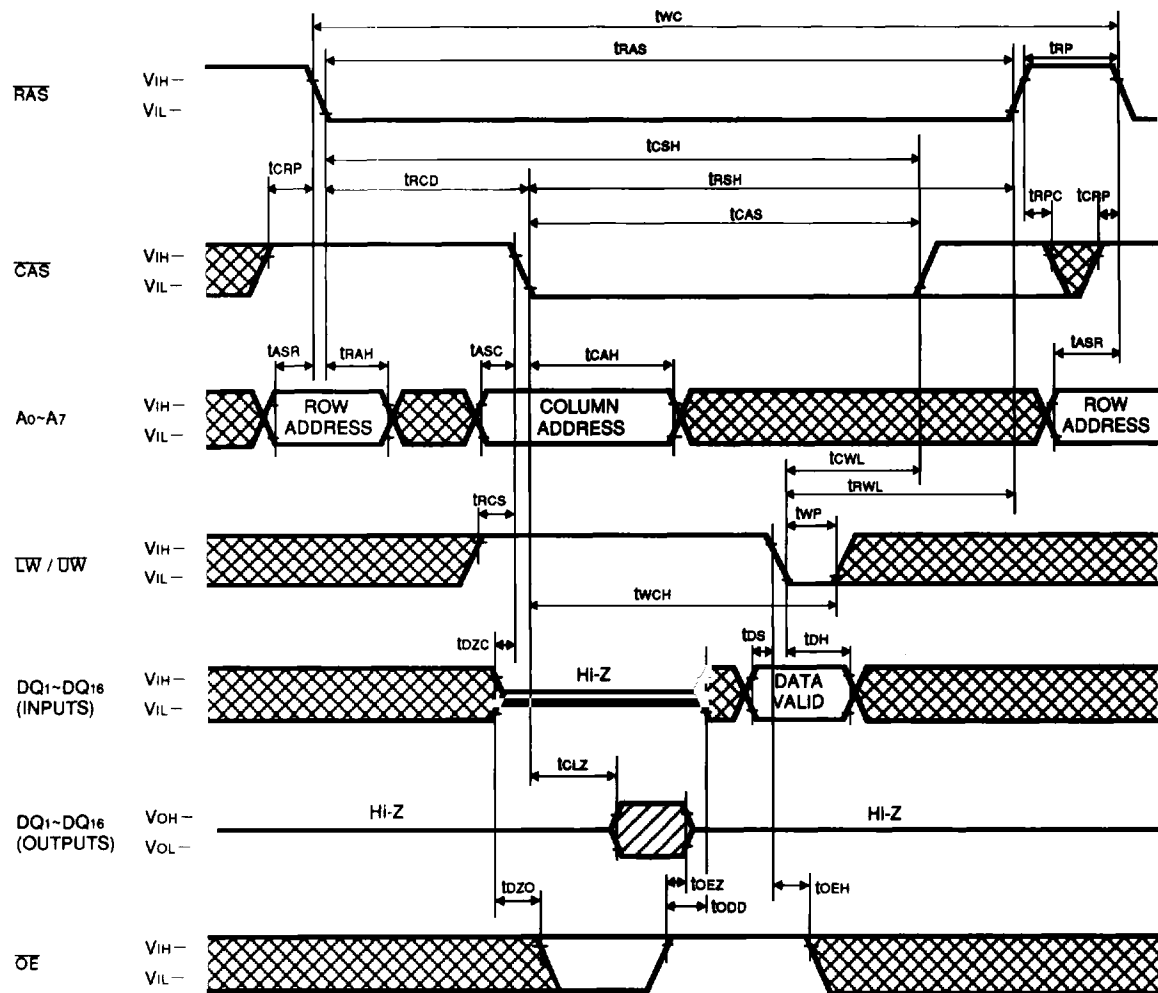
Byte Early Write Cycle



M5M411665AJ, TP2-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 1048576-BIT(65536-WORD BY 16-BIT) DYNAMIC RAM

Delayed Write Cycle

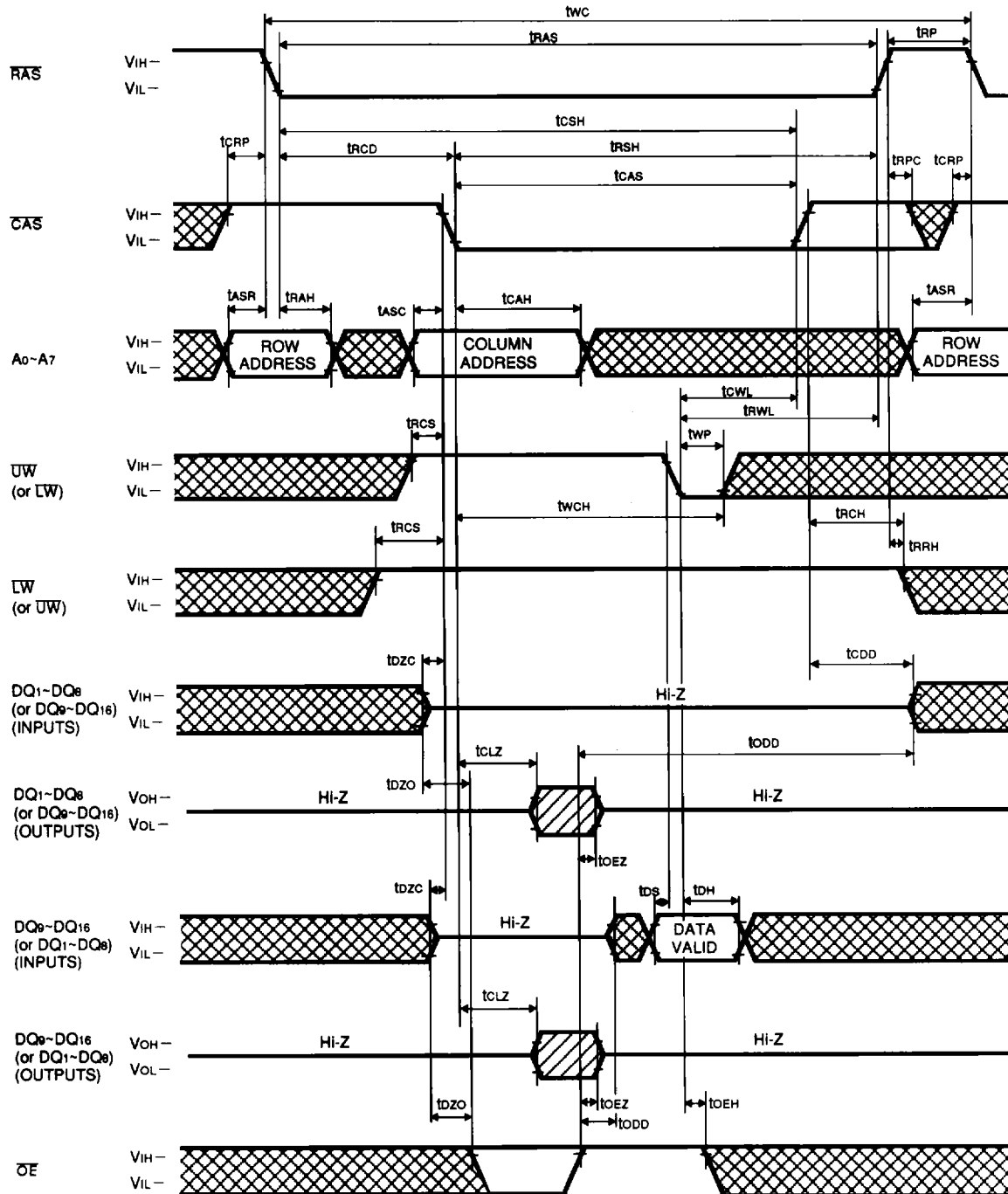


MITSUBISHI LSIs

M5M411665AJ, TP2-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 1048576-BIT(65536-WORD BY 16-BIT) DYNAMIC RAM

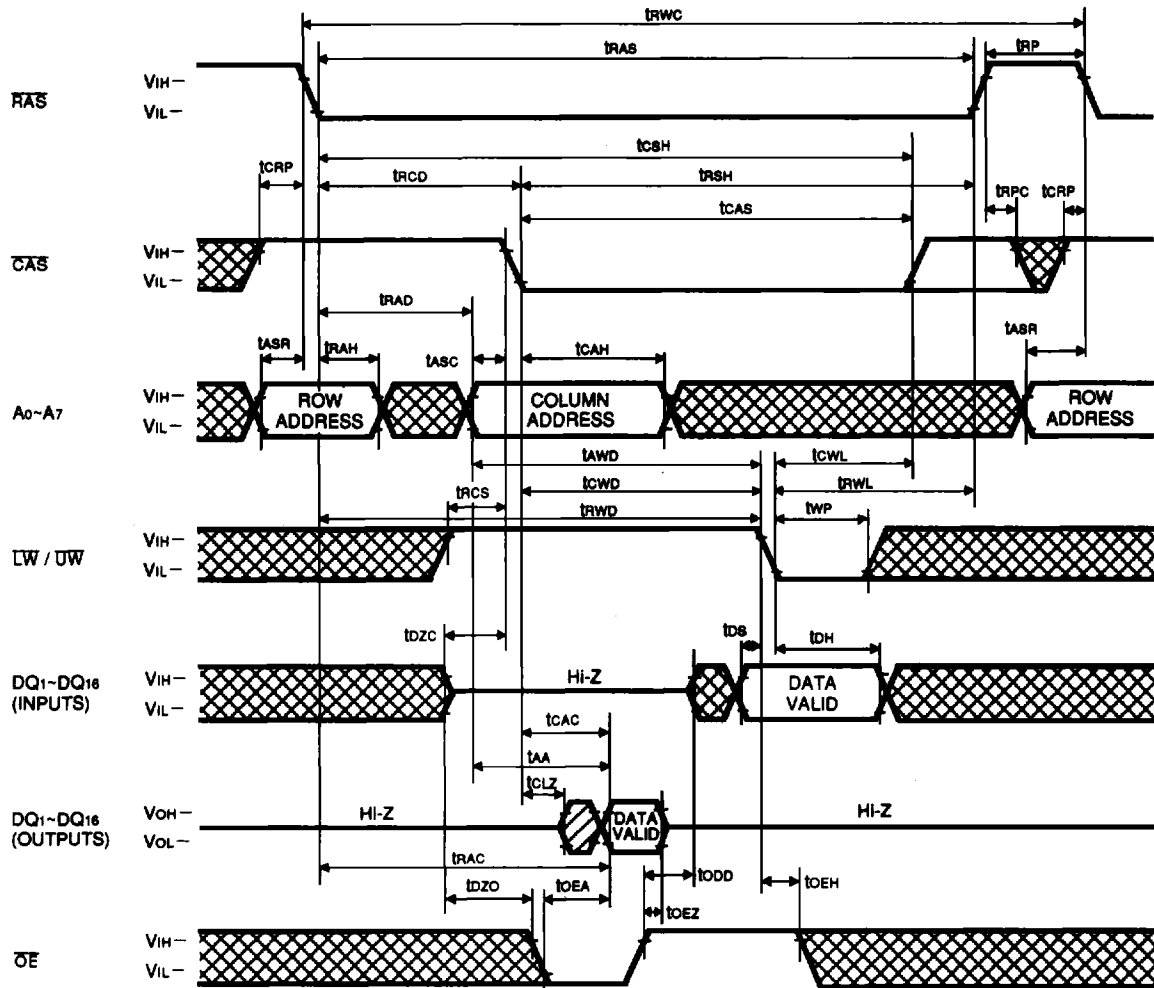
Byte Delayed Write Cycle



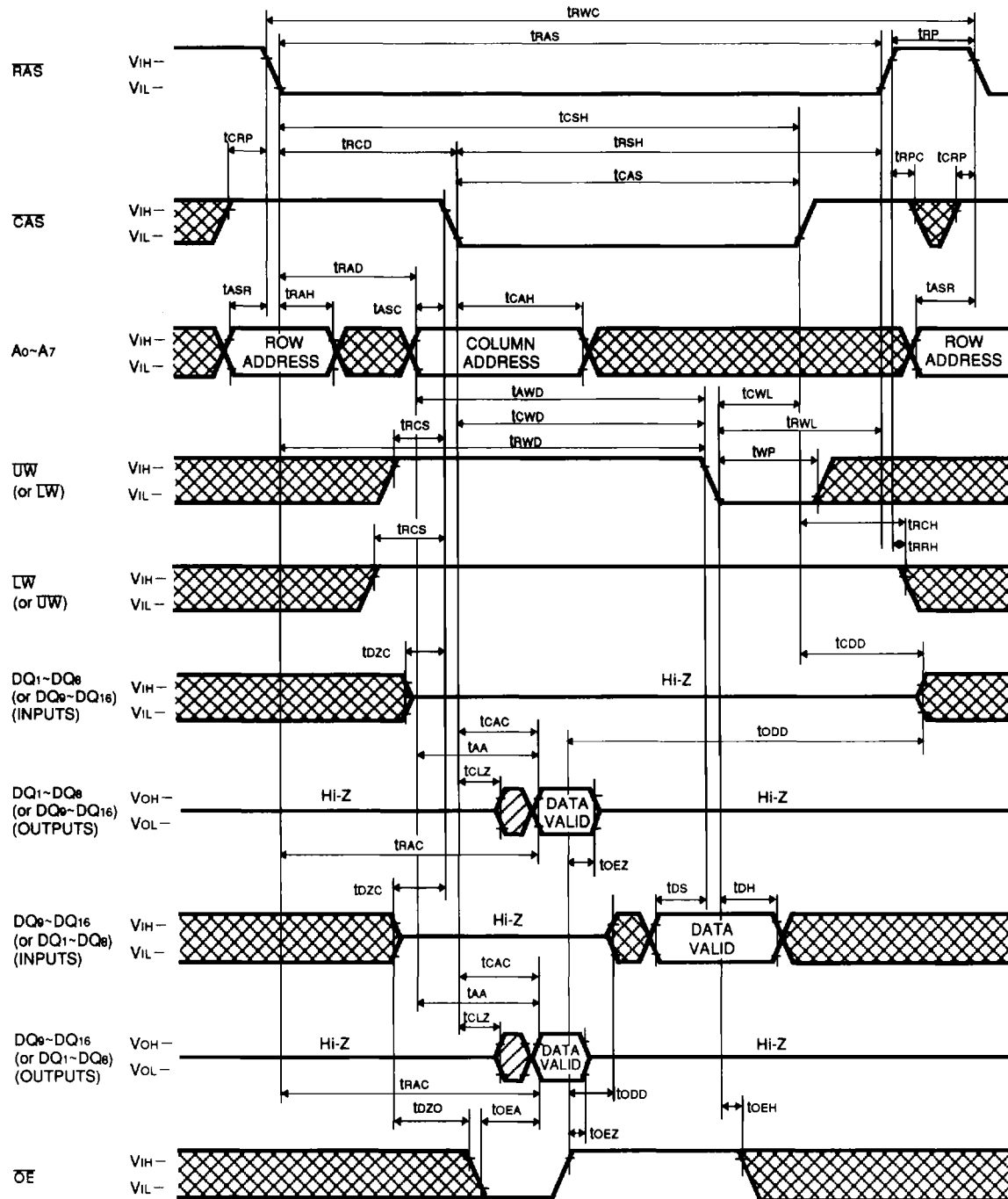
M5M411665AJ,TP2-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 1048576-BIT(65536-WORD BY 16-BIT) DYNAMIC RAM

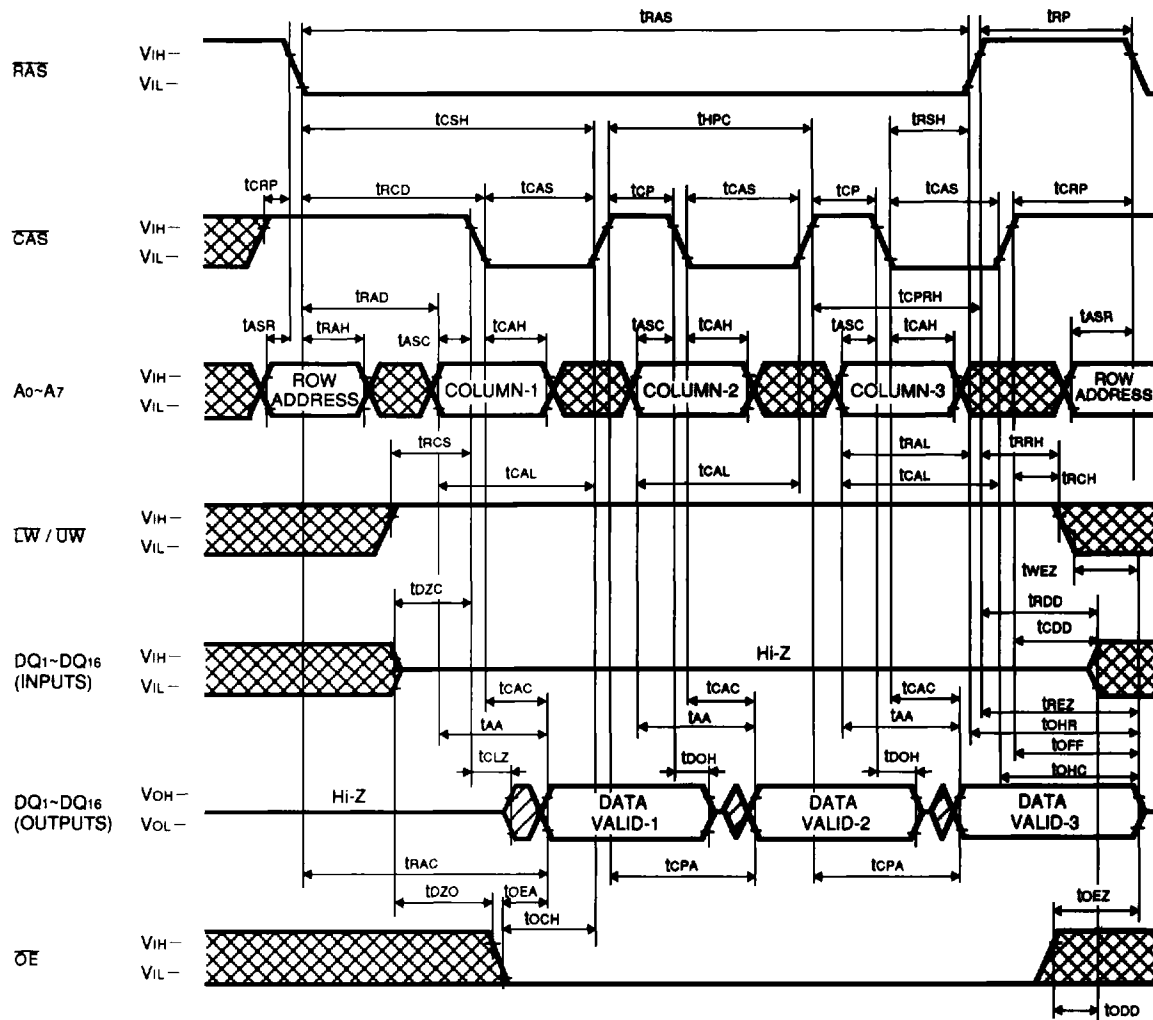
Read-Write, Read-Modify-Write Cycle



Byte Read-Write, Read-Modify-Write Cycle



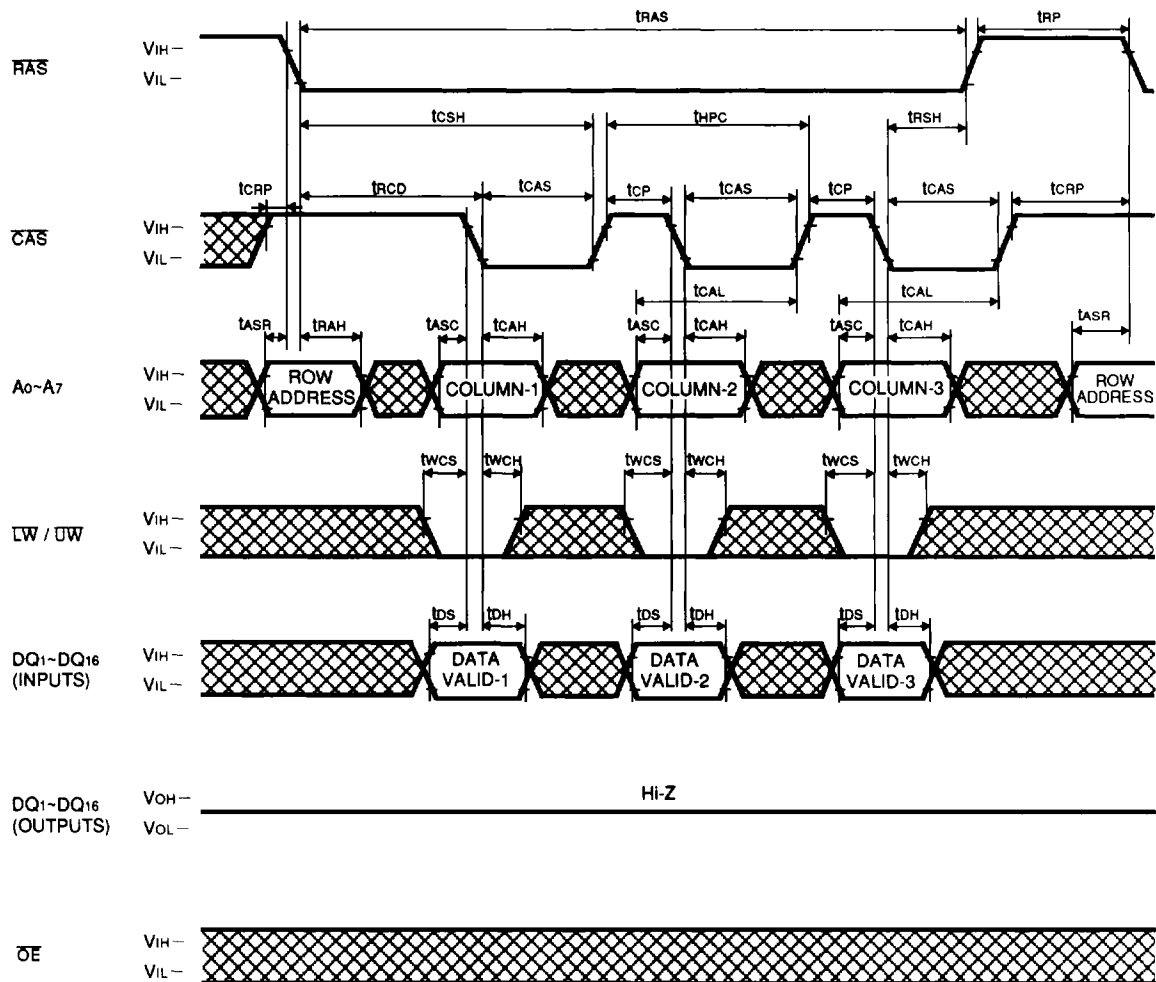
Hyper Page Mode Read Cycle



M5M411665AJ,TP2-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 1048576-BIT(65536-WORD BY 16-BIT) DYNAMIC RAM

Hyper Page Mode Early Write Cycle

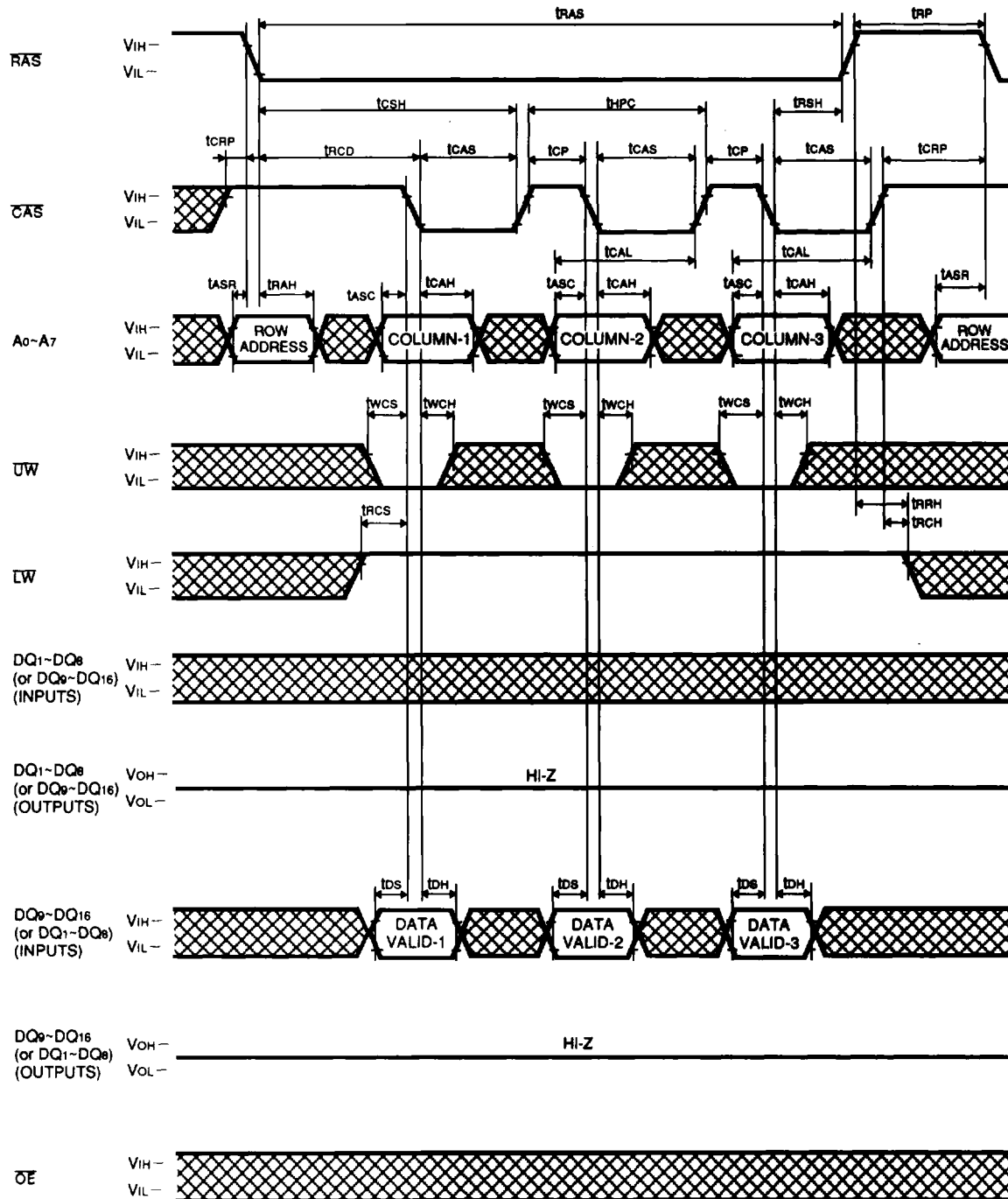


MITSUBISHI LSIs

M5M411665AJ, TP2-5, -6, -7, -5S, -6S, -7S

HYPER PAGE MODE 1048576-BIT(65536-WORD BY 16-BIT) DYNAMIC RAM

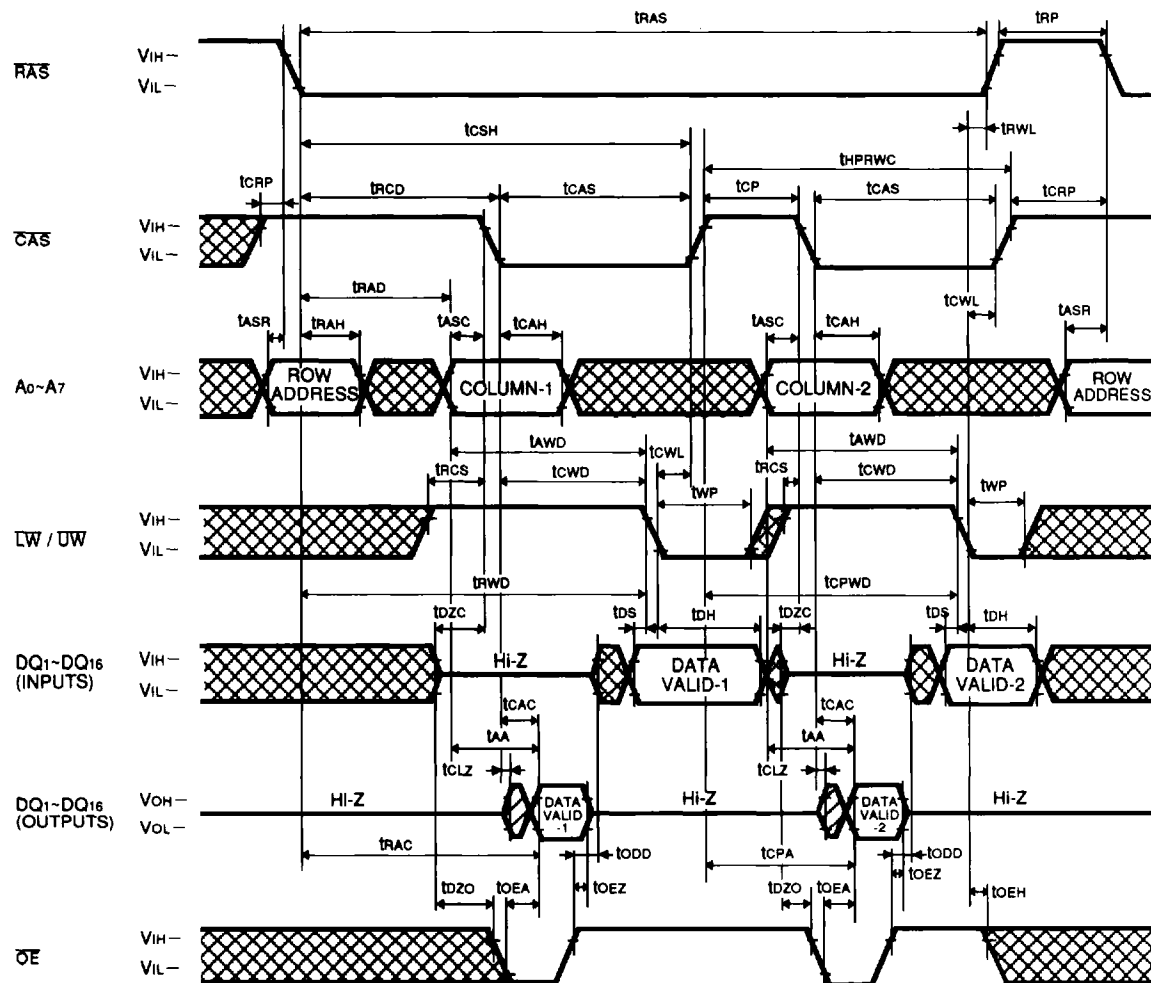
Hyper Page Mode Byte Early Write Cycle



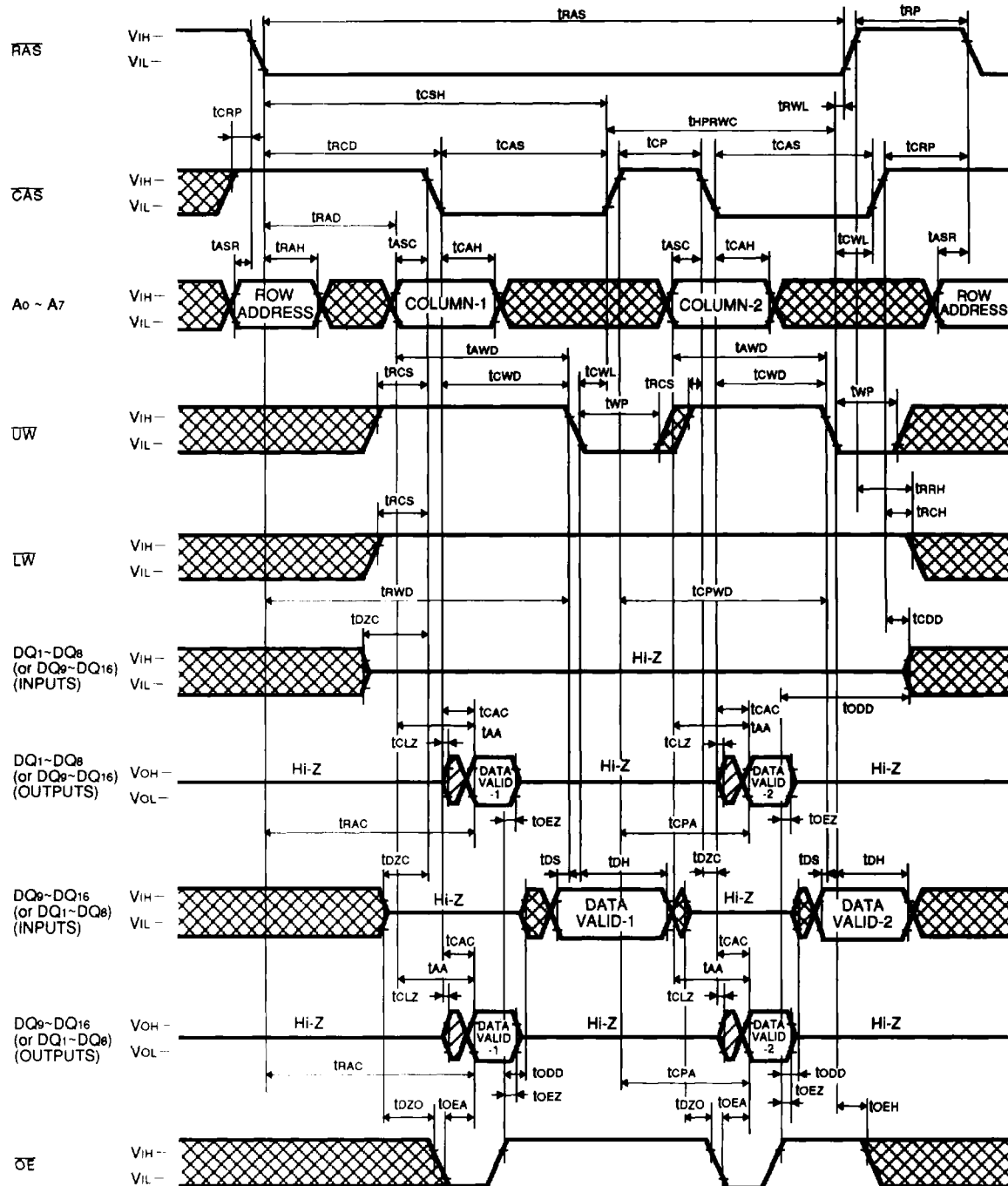
M5M411665AJ,TP2-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 1048576-BIT(65536-WORD BY 16-BIT) DYNAMIC RAM

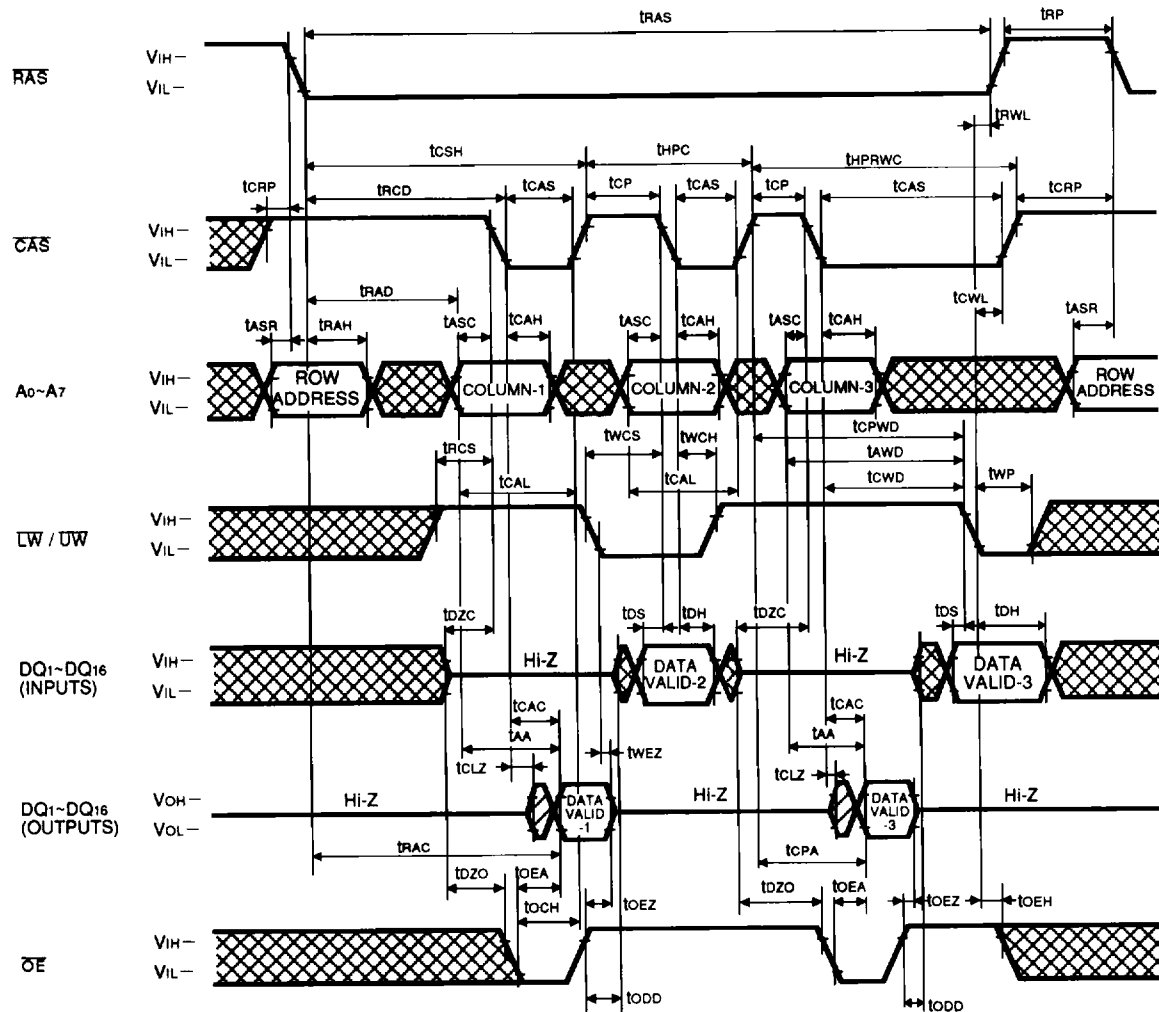
Hyper Page Mode Read-Write, Read-Modify-Write Cycle



Hyper Page Mode Byte Read-Write, Read-Modify-Write Cycle



Hyper Page Mode Mix Cycle (1)

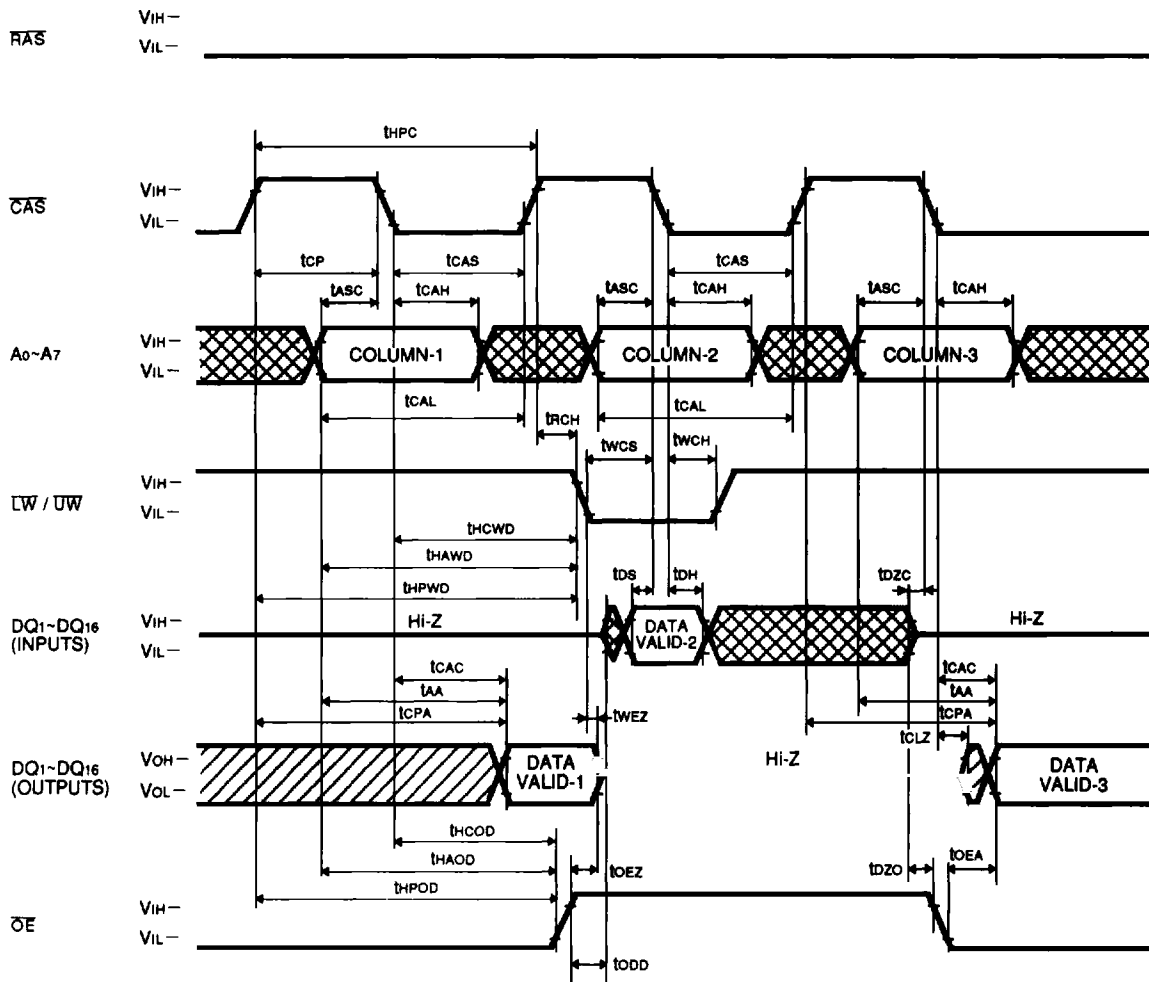


MITSUBISHI LSIs

M5M411665AJ, TP2-5, -6, -7, -5S, -6S, -7S

HYPER PAGE MODE 1048576-BIT (65536-WORD BY 16-BIT) DYNAMIC RAM

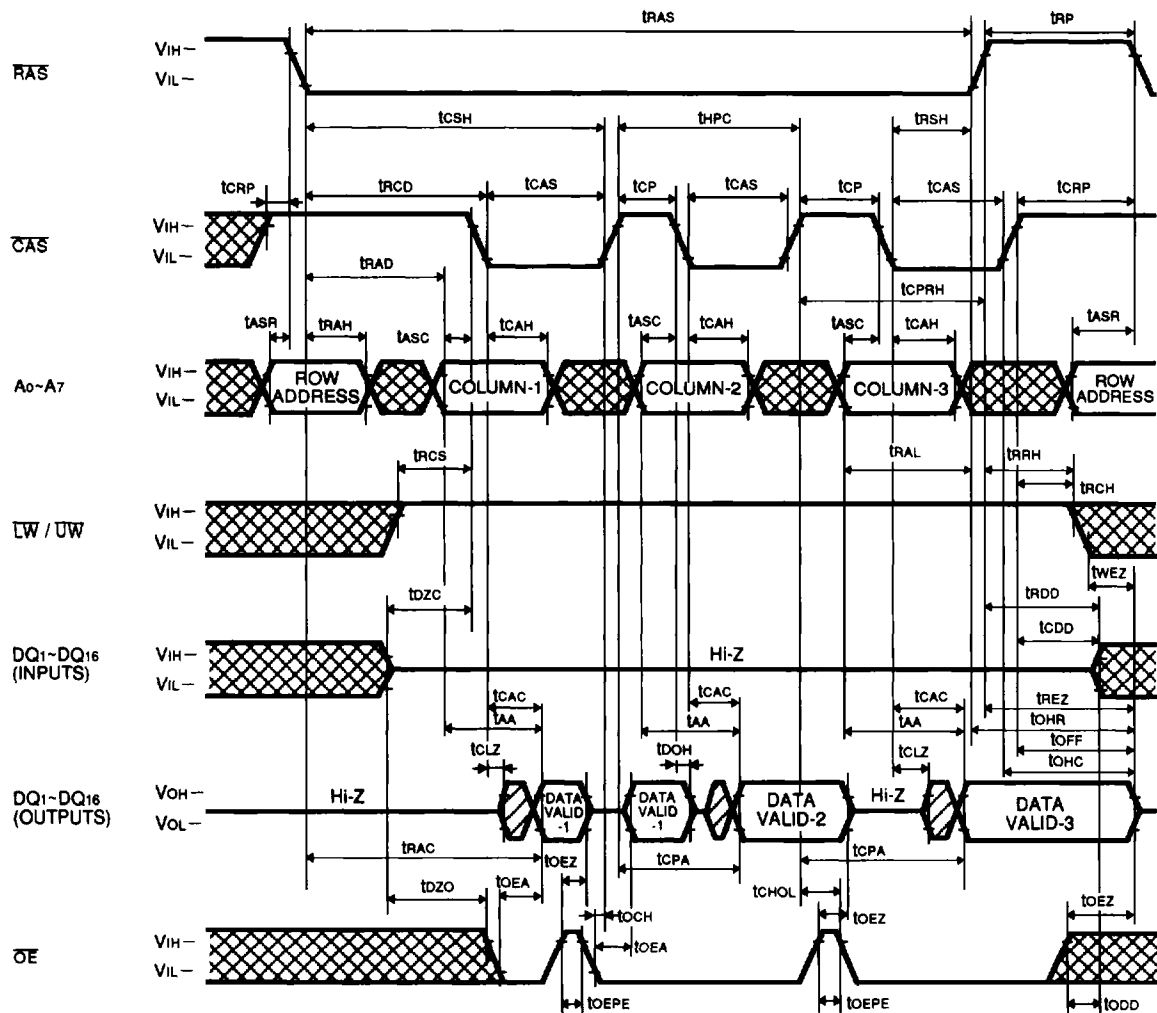
Hyper Page Mode Mix Cycle (2)



M5M411665AJ,TP2-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 1048576-BIT(65536-WORD BY 16-BIT) DYNAMIC RAM

Hyper Page Mode Read Cycle (Hi-Z control by $\overline{OE}$)

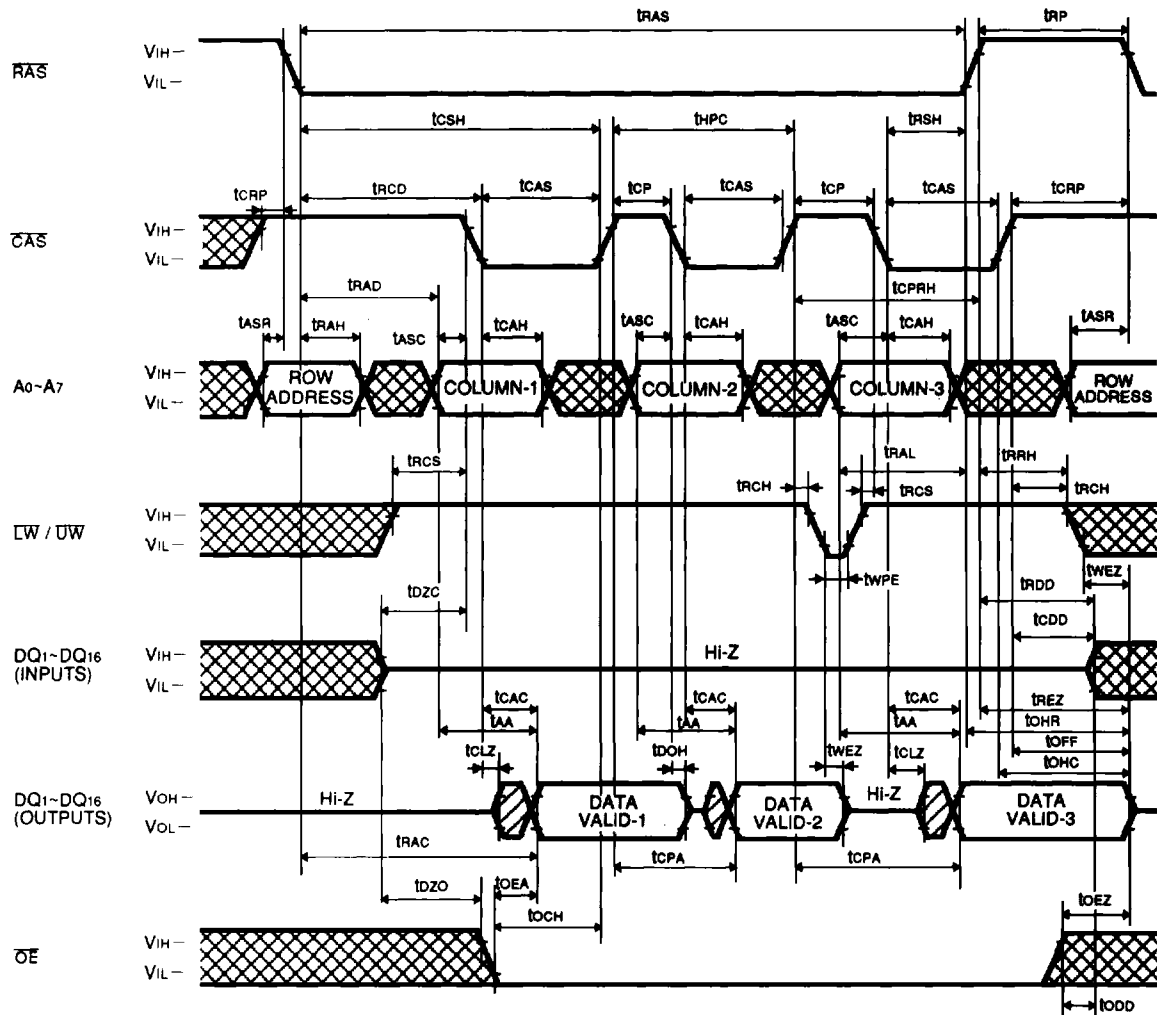


MITSUBISHI LSIs

M5M411665AJ, TP2-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 1048576-BIT(65536-WORD BY 16-BIT) DYNAMIC RAM

Hyper Page Mode Read Cycle (Hi-Z control by $\overline{W}$)

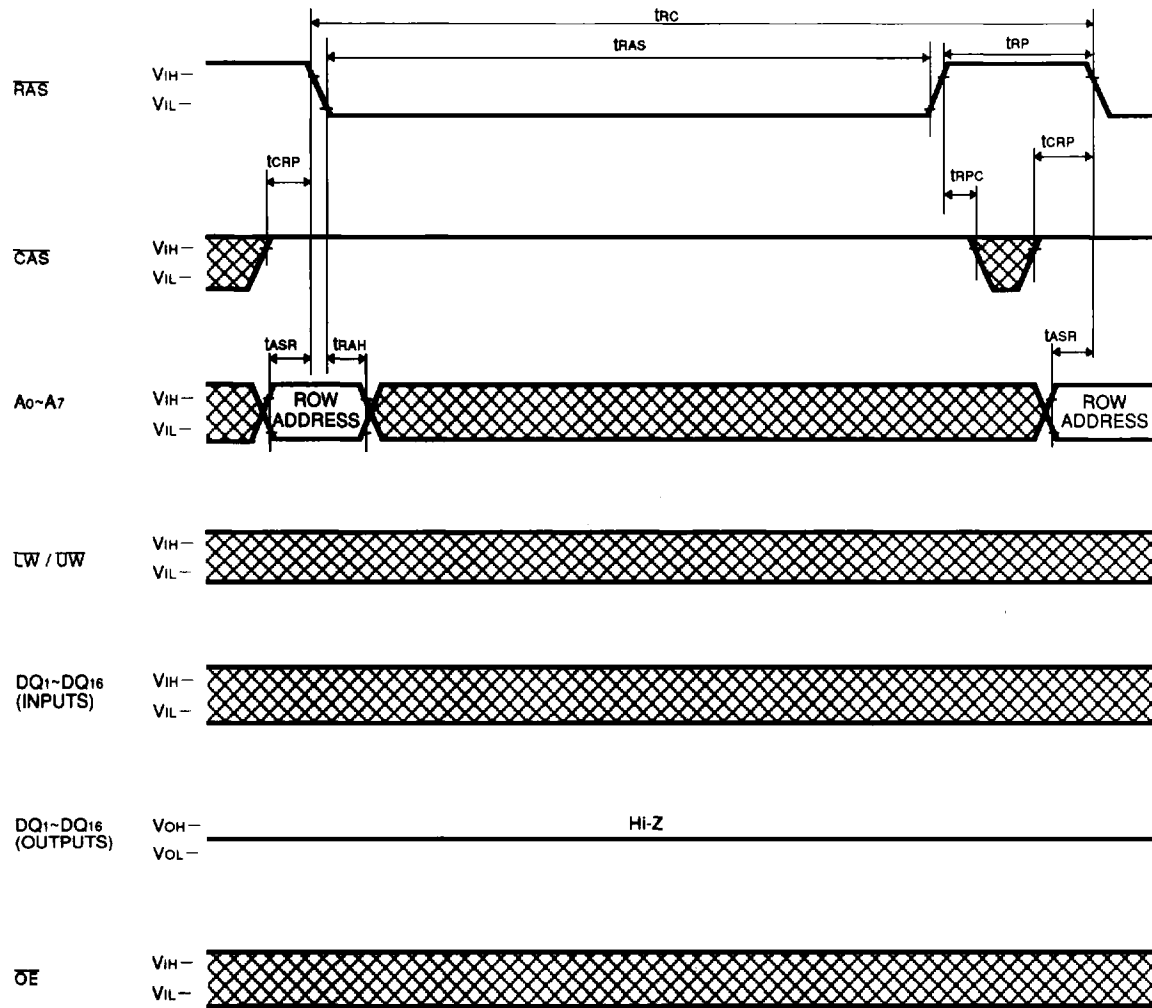


MITSUBISHI LSIs

M5M411665AJ,TP2-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 1048576-BIT(65536-WORD BY 16-BIT) DYNAMIC RAM

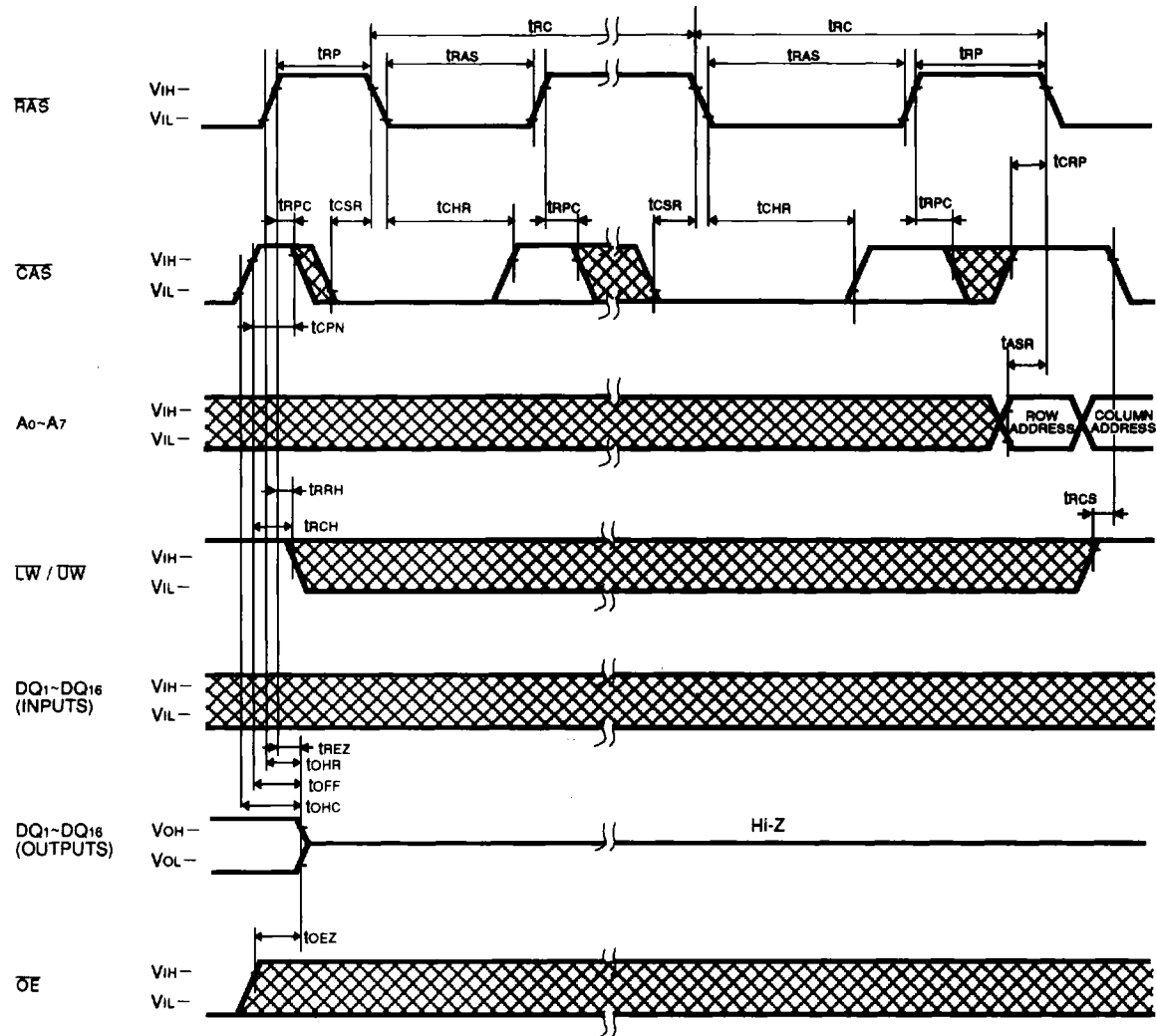
RAS-only Refresh Cycle



M5M411665AJ, TP2-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 1048576-BIT(65536-WORD BY 16-BIT) DYNAMIC RAM

CAS before RAS Refresh Cycle, Extended Refresh Cycle *

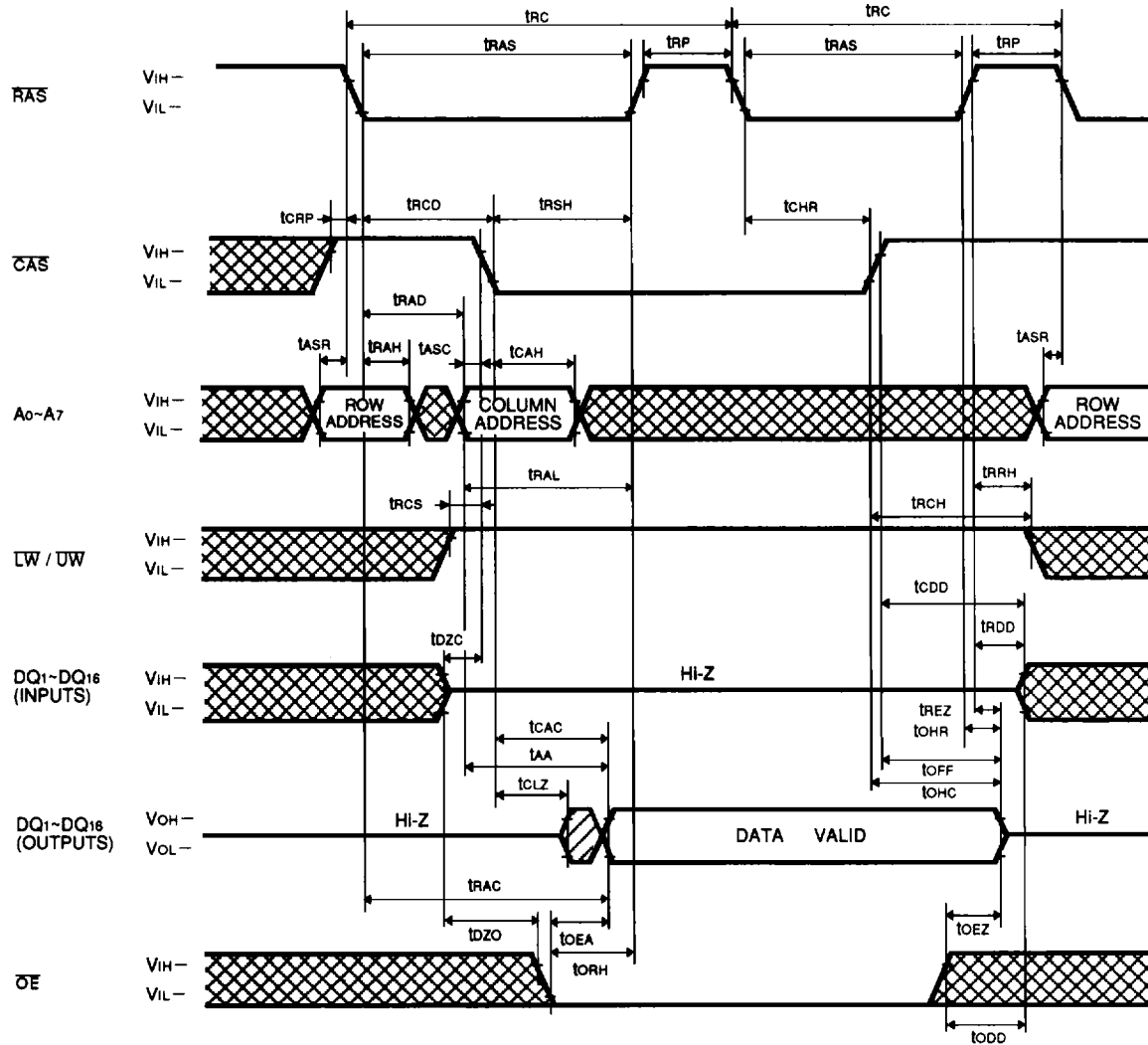


MITSUBISHI LSIs

M5M411665AJ, TP2-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 1048576-BIT(65536-WORD BY 16-BIT) DYNAMIC RAM

Hidden Refresh Cycle (Read) (Note 31)



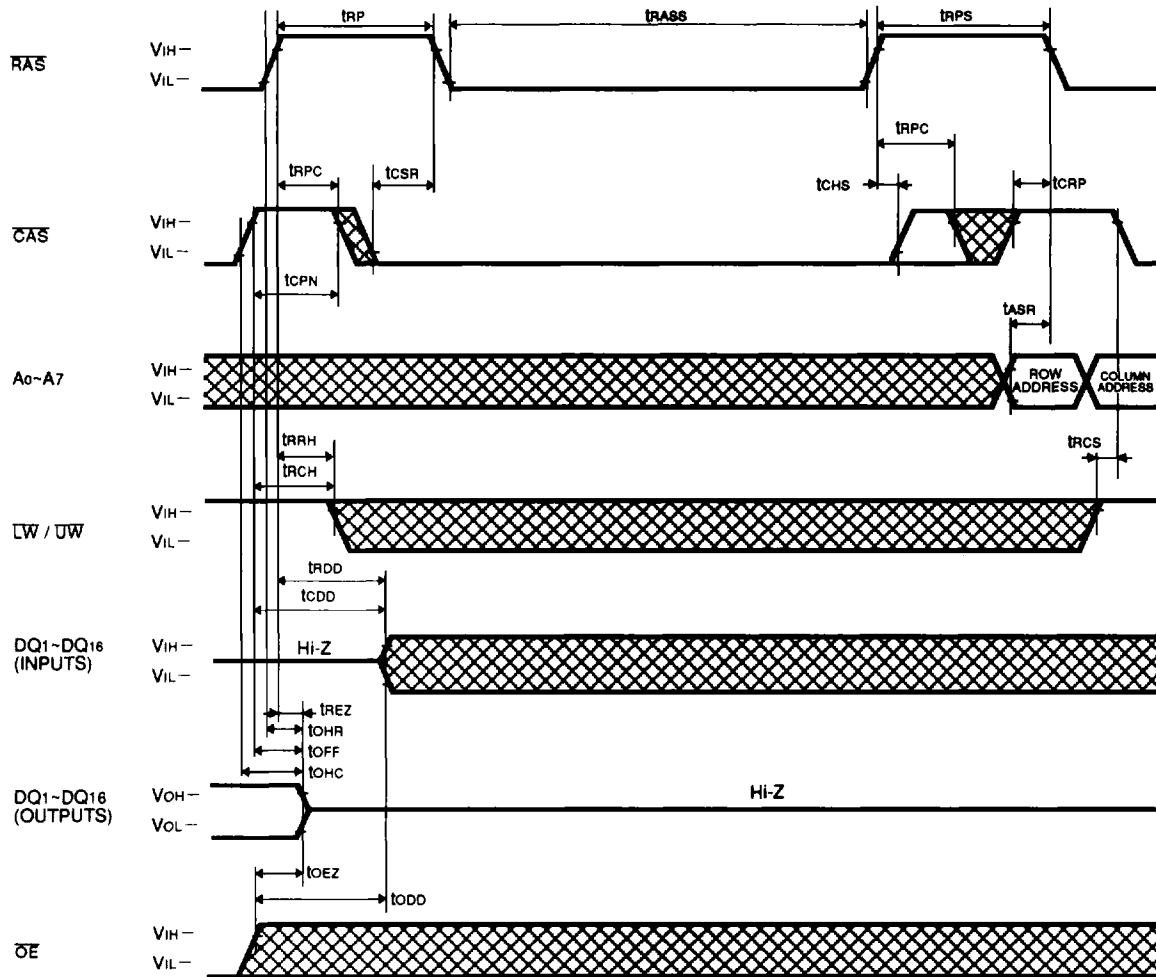
Note 31: Early write, delayed write, read write or read-modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

MITSUBISHI LSIs

M5M411665AJ, TP2-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 1048576-BIT(65536-WORD BY 16-BIT) DYNAMIC RAM

Self Refresh Cycle (Note 32)



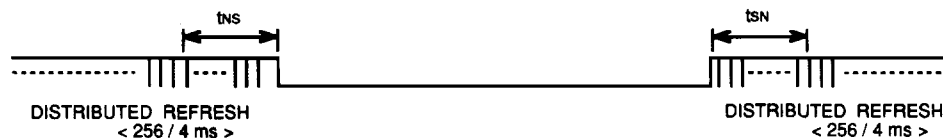
M5M411665AJ,TP2-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 1048576-BIT(65536-WORD BY 16-BIT) DYNAMIC RAM

Note32 : SELF REFRESH ENTRY & EXIT CONDITIONS

(1) In case of distributed refresh

The last and first full refresh cycles (256) must be done within t_{NS} and t_{SN} before and after self refresh ,
on the condition of $t_{NS} \leq 4 \text{ ms}$ and $t_{SN} \leq 4 \text{ ms}$.



(2) In case of burst refresh

The last and first full refresh cycles (256) must be done within t_{NS} and t_{SN} before and after self refresh ,
on the condition of $t_{NS} \leq 4 \text{ ms}$ and $t_{SN} \leq 4 \text{ ms}$.

