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LR4906 Analog-Digital Interface for MODEM

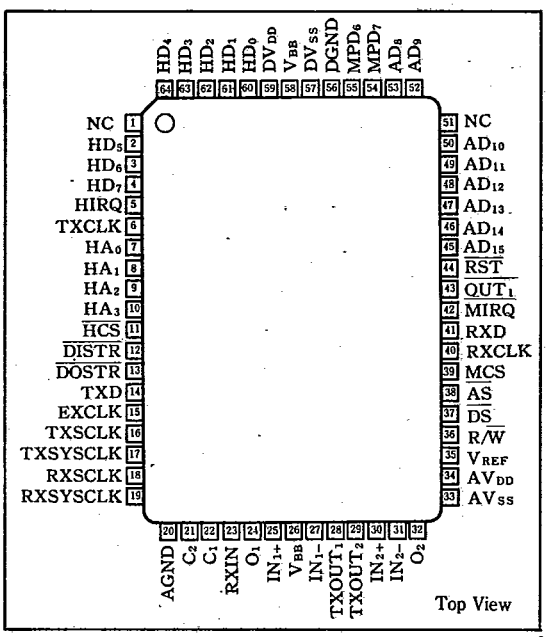
■ Description

The LR4906 is an analog/digital interface LSI providing an analog iterface with the telephone line and a digital interface with the host CPU. When used together with digital signal processor LR490302, it is possible to compose a half duplex system which meets the communication standards for V29, V27 ter, V21-2, and G Ⅱ/G Ⅲ, etc.

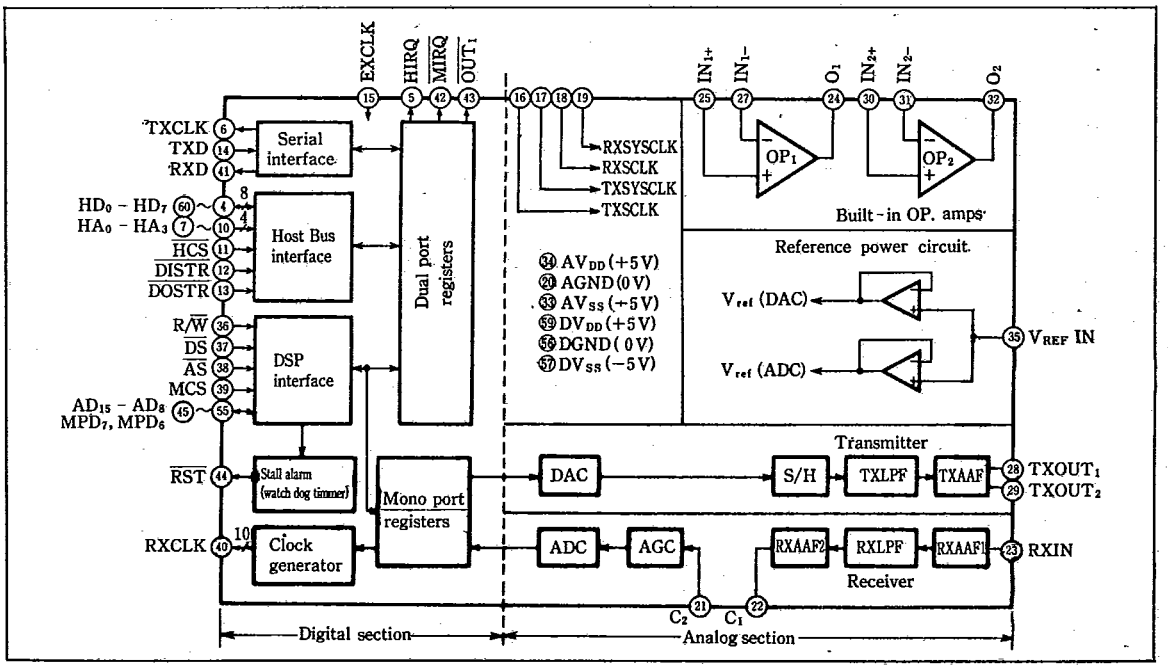
■ Features

1. Suited for 2-core half duplex communication (300 to 9600bps)
2. Compatible with CCITT V27ter, V29, and V21-2 modems.
3. Receiving BPF and transmission LPF based on SCF (Switched Capacitor Filter) are incorporated
4. Built-in 10-bit A/D and D/A converter. Max conversion speed : 9600bps
5. Transmission and receiving amplifiers are incorporated for line transformer driving
6. Built-in interface drive circuit
7. Built-in 6-bit AGC circuit
8. Low power consumption 250mW (TYP.)
9. +5V power supply
10. 64-pin quad flat package

■ Pin Connections



■ Block Diagram



Pin Functions

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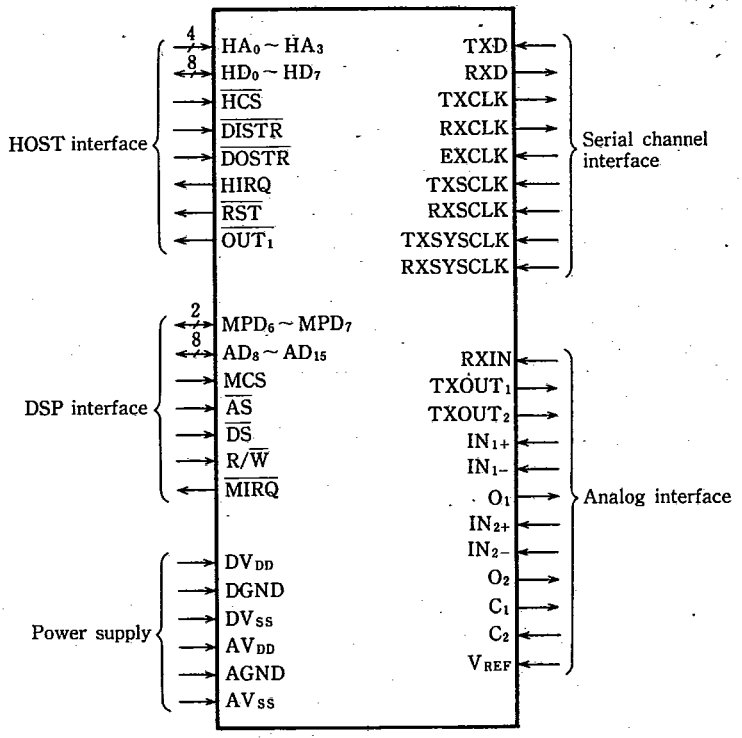

No.	Symbol	I/O	Pin name	No.	Symbol	I/O	Pin name
1	NC	—	Non-connection	31	IN_{2-}	AI2	OP2 input (−)
2-4	HD_5-HD_7	DIO	Host data bus 5 to 7	32	O_2	AO2	OP2 output
5	HIRQ	DO	Host interrupt request	33	AV_{SS}	—	Analog V_{SS} (−5V)
6	TXCLK	DO	Not used. NC when mounting.	34	AV_{DD}	—	Analog V_{DD} (+5V)
7-10	HA_0-HA_3	DI	Host address bus 0 to 3	35	V_{REF}	AI2	Reference input (+2.6V)
11	HCS	DI	Host chip select	36	R/W	DI	DSP read/write strobe
12	DISTR	DI	Host read strobe	37	DS	DI	DSP data strobe
13	DOSTR	DI	Host write strobe	38	AS	DI	DSP address strobe
14	TXD	DI	Not used. Pulled up when mounting.	39	MSC	DI	DSP chip select
15	EXCLK	DI	Not used. Pulled up when mounting.	40	RXCLK	DO	Clock output
16	TXSCLK	DI	Transmisssion sample clock	41	RXD	DO	Not used. NC when mounting.
17	TXSYSCLK	DI	Transmission system clock (230.4k)	42	MIRQ	DO	Bit output
18	RXSCLK	DI	Reception sample clock	43	OUT1	DO	Bit output
19	RXSYSCLK	DI	Reception system clock (230.4k)	44	RST	DOD	Reset output
20	AGND	—	Analog GND	45-50	AD_{15}-AD_{10}	DIO	DSP address data bus 15 to 10
21	C_2	AI1	AGC input	51	NC	—	Non-connection
22	C_1	AO2	Filter output	52	AD_9	DIO	DSP address data bus 9
23	RXIN	AI1	Analog input	53	AD_8	DIO	DSP address data bus 8
24	O_1	AO2	OP1 output	54	MPD_7	DIO	DSP data bus 7
25	IN_{1+}	AI2	OP1 input (+)	55	MPD_6	DIO	DSP data bus 6
26	V_{BB}	—	Printed circuit board (−5V)	56	DGND	—	Digital GND
27	IN_1 (−)	AI2	OP1 input (−)	57	DV_{SS}	—	Digital V_{SS} (−5V)
28	$TXOUT_1$	AO1	Analog transmission output 1	58	V_{BB}	—	Printed circuit board (−5V)
29	$TXOUT_2$	AO2	Analog transmission output 2	59	DV_{DD}	—	Digital V_{DD} (+5V)
30	IN_2 (+)	AI2	OP2 input (+)	60-64	HD_0-HD_4	DIO	Host data bus 0 to 4

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■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Supply voltage	V_{DD}	−0.3 to +6.0	V	1
	V_{SS}	−6.0 to +0.3	V	1
Analog input voltage	AV_{IN}	AV_{SS}−0.3 to AV_{DD}+0.3	V	
Digital input voltage	DV_{IN}	DGND−0.3 to DV_{DD}+0.3	V	
Operating temperature	T_{opr}	0 to +65	℃	
Storage temperature	T_{stg}	−65 to +150	℃	

Note 1 : Referenced to GND.

■ Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Analog supply voltage	AV_{DD}	4.75	5.0	5.25	V
	AV_{SS}	−5.25	−5.0	−4.75	V
Digital supply voltage	DV_{DD}	4.75	5.0	5.25	V
	DV_{SS}	−5.25	−5.0	−4.75	V

■ DC Characteristics

($DV_{DD}=AV_{DD}=5V\pm5\%$, $DV_{SS}=AV_{DD}=-5V\pm5\%$, Ta=0 to +70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input "Low" voltage	V_{IL}				0.8	V
Input "High" voltage	V_{IH}		2.2			V
Input leakage current	I_L	0V<V_{IN}<+5.25V	−10		+10	μA
Output "Low" voltage	V_{OL}	I_{OL}=+1.6mA			0.5	V
Output "High" voltage	V_{OH}	I_{OH}=−250μA	2.4			V
Current consumption	$I_{DD(D)}$	$DV_{DD}=AV_{DD}=5.25V$ $DV_{SS}=AV_{DD}=-5.25V$		10	15	mA
	$I_{DD(A)}$			30	45	
	I_{SS}			35	50	
D/A converter unit (Note 1)						
Conversion speed	f_{CRD}			9600		Hz
Resolution			10			bit
Linearity	L_{inD}		8			bit
Full-scale output	V_{OFS}			V_{REF}		
Transmitter filter unit (TXLPF)						
Load resistance	R_L			10		kΩ
Tx gain	A_{TX}		−0.3		0.3	dB
Tx offset	V_{OS}			200		mV
Programmable gain amplifier unit (AGC)						
Gain (lower limit)	A_L			0		dB
Gain (upper limit)	A_H			47.25		dB
Gain step	ΔA			0.75		dB
Gain set deviation	D_{ev}		−0.5	0	+0.5	dB
A/D converter unit (Note 2)						
Conversion speed	f_{CRA}			9600		Hz
Resolution			10			bit
Linearity	L_{inA}		8.5			bit
Full-scale input	V_{IFS}			V_{REF}		

Note 1 : Input data format of D/A converter is 2's complement of 10 bits.
Note 2 : Output data format of A/D converter is 2's complement of 10 bits.

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■ AC Characteristics

(1) Read cycle (Host interface)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Address setup time	t_{AR}	30			ns
$\overline{HCS}$ setup time	t_{CSR}	30			ns
$\overline{DISTR}$ pulse width	t_{DIW}	310			ns
Read cycle delay time	t_{RC}	20			ns
Read cycle time	RC	405			ns
$\overline{DISTR}$ output floating retention time	t_{DDD}		130	220	ns
$\overline{DISTR}$ output floating time	t_{HZ}	0			ns

(2) Write cycle (Host interface)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Address setup time	t_{AW}	30			ns
$\overline{HCS}$ setup time	t_{CSW}	30			ns
$\overline{DISTR}$ pulse width	t_{DOW}	310			ns
Write cycle delay time	t_{WC}	20			ns
Write cycle time	WC	405			ns
Data setup time	t_{DS}	90			ns
Data hold time	t_{DH}	15			ns

(3) Read cycle (DSP interface)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Address setup time	t_{AS}	35			ns
Address hold time	t_{AH}	40			ns
$\overline{AS}$·$\overline{DS}$ delay time	t_{ADR}	55			ns
$\overline{DS}$ pulse width	t_{DSRW}	185			ns
$\overline{DS}$ access time	t_{DSRD}			95	ns
Read cycle delay time	t_{RWC}	75			ns
Data hold time	t_{DSRH}	0			ns

(4) Write cycle (DSP interface)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Address setup time	t_{AS}	35			ns
Address hold time	t_{AH}	40			ns
Data setup time	t_{ADW}	35			ns
$\overline{DS}$ pulse width	t_{DSWW}	110			ns
Data hold time	t_{DSWH}	45			ns
Write cycle delay time	t_{RWC}	75			ns

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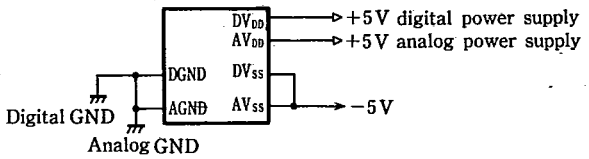
■ Electrical Characteristics (Op. Amp.)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Op. Amp. 1 (R_L=10kΩ, C_L=47pF)						
Output voltage amplitude	V_{O1}			±2.5		V
Open loop voltage gain	A_{VO1}			2000		
Gain band product	GB_1			1.4		MHz
Phase margin				40		degrees
Settling time	t_{s1}	0.1%		2	2.5	μs
Op. Amp. 2 (R_L=600, C_L=47pF)						
Output voltage amplitude	V_{O2}			±2.5		V
Open loop voltage gain	A_{VO2}			2000		
Gain band product	GB_2			2		MHz
Phase margin				60		degrees
Settling time	t_{s2}	0.1%		2	3.5	μs

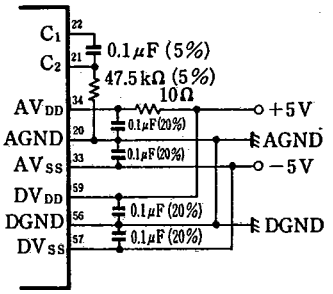
(1) Connection of power supply



* DV_{SS} pin and AV_{SS} pin should be in identical potential to be mutually connected.
* In the case digital GND and analog GND are separated, connect them close to the devise.
* DV_{DD} pin and AV_{DD} pin may not be in indentical potential. Good result will be obtained as long as they are not connected.

(2) External circuits

At least four pieces of decoupling capacitors should be provided in the power line, and a capacitor and a resistor should be provided across C_1 and C_2 pins to cut the DC offset to be input to the AGC circuit as shown below for normal operation of this IC.



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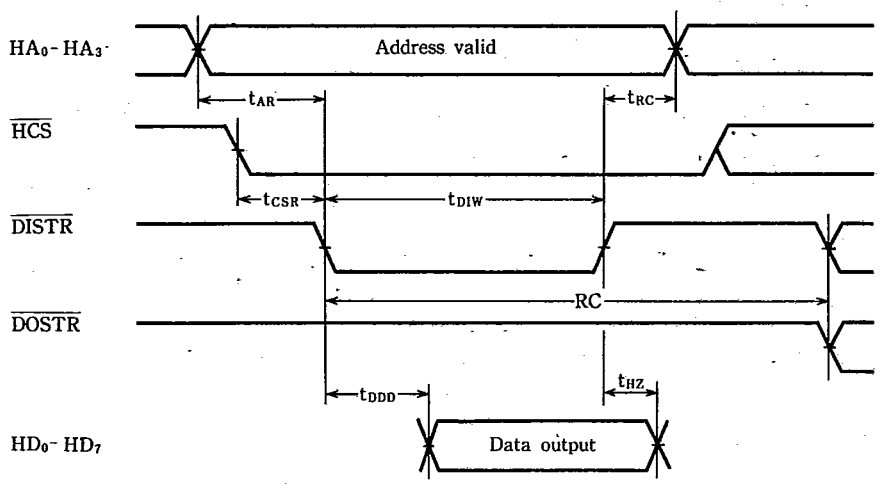
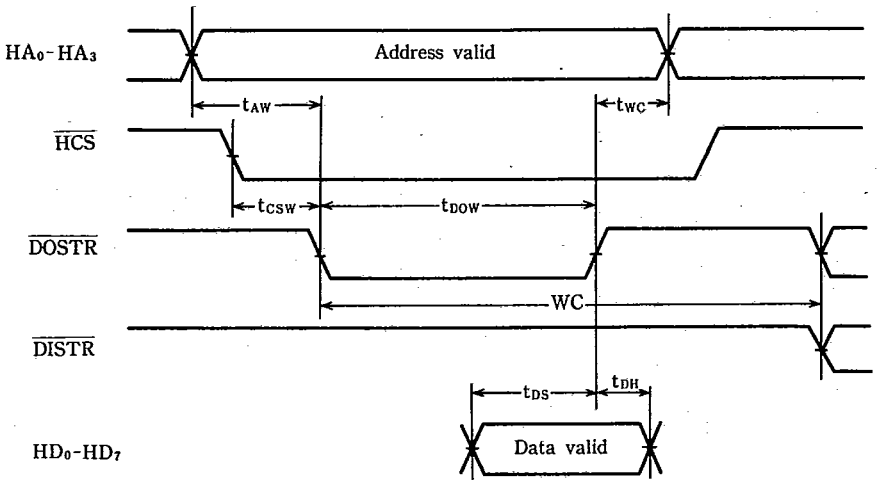
■ Timing Diagram

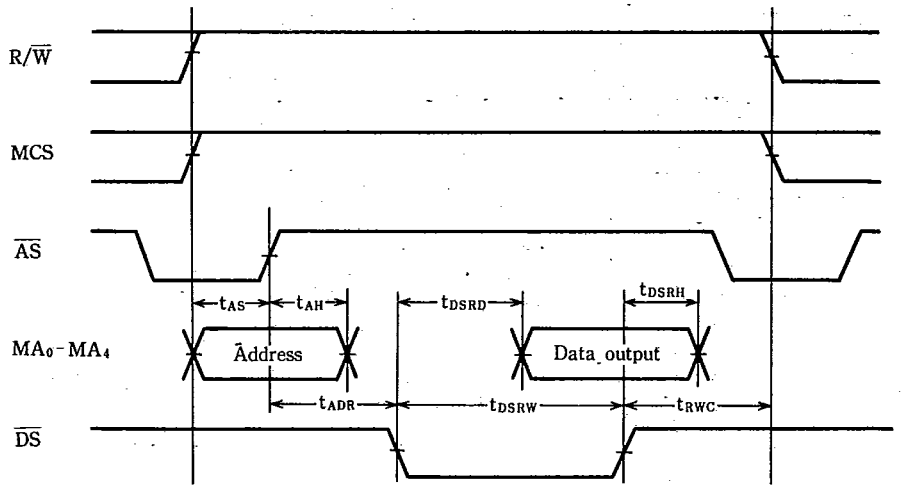
(1) Read cycle (Host interface)



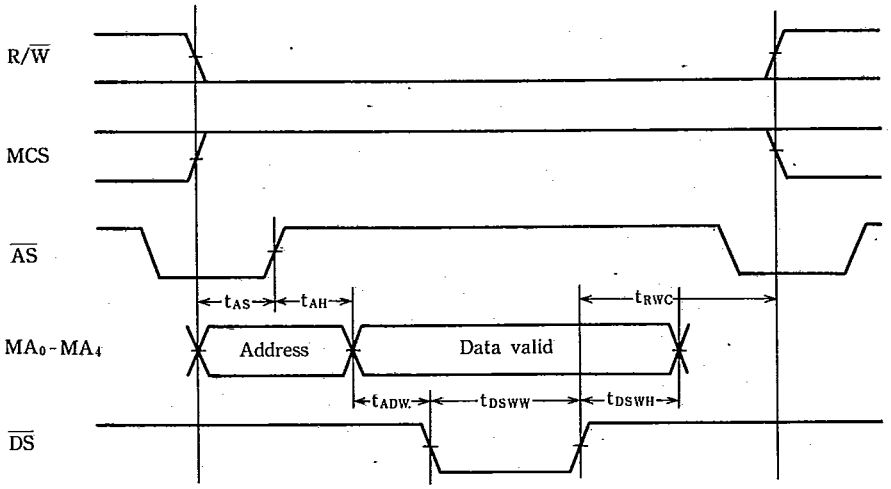
(2) Write cycle (Host interface)



(3) Read cycle (DSP interface)



(4) Write cycle (DSP interface)



■ Functional Operation

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(1) Analog Interface

The analog interface consists of two blocks of transmitter and receiver. The transmitter integrates 10-bit D/A converter, sample hold circuit (S/H), TXLPF and antiareas filter (AAF). The receiver integrates AAF ,RXLPF, programmable gain amplifier (AGC) and 10-bit A/D converter.

(a) Transmitter The transmitter (TX) executes interface from DSP to network hybrid. The transmission data obtained through D/A register of the monoport register is transferred to 10-bit D/A converter. After sampling, its output is passed through the low pass filter.

① D/A converter The D/A converter is composed of 10-bit electric charge redistribution type circuit, and its accuracy is determined by the ratio of capacitors. Therefore, high accuracy D/A conversion is made possible.

② S/H circuit The D/A converter output is sampled and held by 7.2kHz or 9.6kHz clock and is transferred to LPF.

③ TXLPF The TXLPF is composed of 5th elliptic function type switched capacitor filter. Its sampling frequency is 230.4kHz, and cut-off frequency of TXLPF is 3.3kHz. Fig. 1 shows frequency characteristics of TXLPF.

④ TXAAF The TVAAF is secondary active filter to cut off reflected noises around 230.4kHz caused by TXLPF. Its cut-off frequency is 15.6kHz.

(b) Receiver The receiver (RX) executes interface from network hybrid to DSP. An analog channel signal is limited around 3.4kHz band by receiving filter unit (AAF1, RXLPF, AAF2) due to it executes sampling at 7.2kHz or 9.6kHz. After that, DC cut signal by the external RC circuit is properly amplified by AGC (programmable gain controller) and is stored in the A/D register of monoport register as 10-bit digital value.

① AAF1 and AAF2 The AAF1 and AAF2 are secondary active filters with 15.6kHz cut-off frequency.

② RXLPF The RXLPF is composed of 5th elliptic function type switched capacitor filter. Its sampling frequency is 230.4kHz, and cut-off frequency of RXLPF is 3.3kHz. Switching between 0dB and 10dB of the gain is possible by AGC register of the monoport register.

③ Programmable gain amplifier (AGC) With AGC, 64 kinds of programs are available with 0.75dB interval. Gain programming is controlled by setting the corresponding bit of AGC register of monoport register.

(2) Digital Interface

(a) Dual-port register The data such as communication speed, etc. are set from the host to the register. Another data including communication error and error status, etc. are set from DSP to notify them to the host side. Asynchronous reading and writing are possible from both host side and DSP.

(b) Monoport register The monoport registers include five registers which can be accessed from DSP. They execute AGC control, mode set and transmission of A/D and D/A conversion data.

(3) Built-in general purpose operational amplifier

Built-in a couple of operational amplifier give high flexibility to the user from hybrid circuit design and are useful for reducing the number of parts in a system.

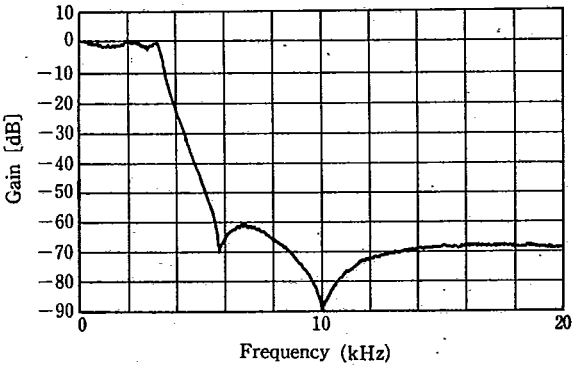

Fig. 1 TXLPF, RXLPF frequency characteristics

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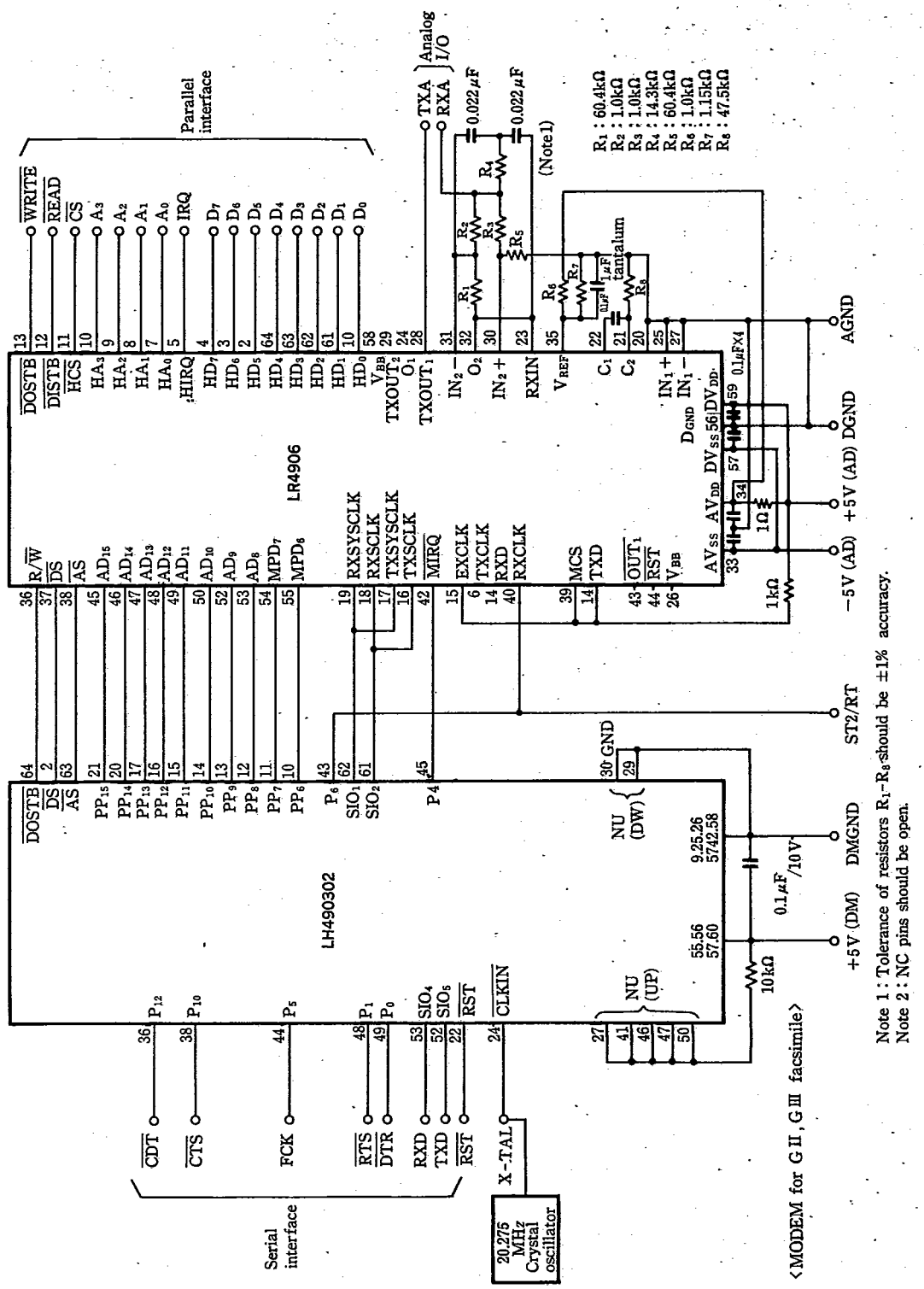
System Configuration Example



Note 1 : Tolerance of resistors R_1–R_8 should be ±1% accuracy.
Note 2 : NC pins should be open.