1 Short Description

The CME8000 is a BiCMOS integrated straight through receiver with build in very high sensitivity and a pre-decoding of the time signal transmitted from WWVB, DCF77, JJY, MSF and HBG. The receiver is prepared for multi-mode reception by using an integrated logic. Integrated functions as stand by mode, integrated antenna switching, integrated crystal switching and a hold mode function offer features for universal applications.
The power down mode increases the battery lifetime significantly and makes the device ideal for all kinds of radio controlled time pieces.

2 Features

- o Low power consumption (<100µA)
- o Very high sensitivity (0.4µV)
- o Build in pulse decoding for different protocols
- o Switchable for 3 different frequencies
- o High selectivity by using crystal filter
- o Power down mode
- o Only a few external components necessary
- o AGC hold mode
- o Wide frequency range (40 ... 120 kHz)
- o Low power applications (1.2 .. 5.0 V)
- o Automatic protocol recognition
- o Pre-decoded protocol information
- o Fast data transfer to CPU (100ms)
- o Use of the CPU clock (32768Hz)
- o Improved noise resistance
- o Integrated AGC adaptation
  Two built-in low impedance antenna switches (40 Ohm/3V)
- o True Bit strength indication

Benefits

- o Extended Battery operating time
- o Decoding of the signal extremely simplified
- o Simplified micro controller software
- o Simplified multi frequency handling
- o Easy world time piece design
- o Automatic country recognition
- o True signal quality information

Block Diagram

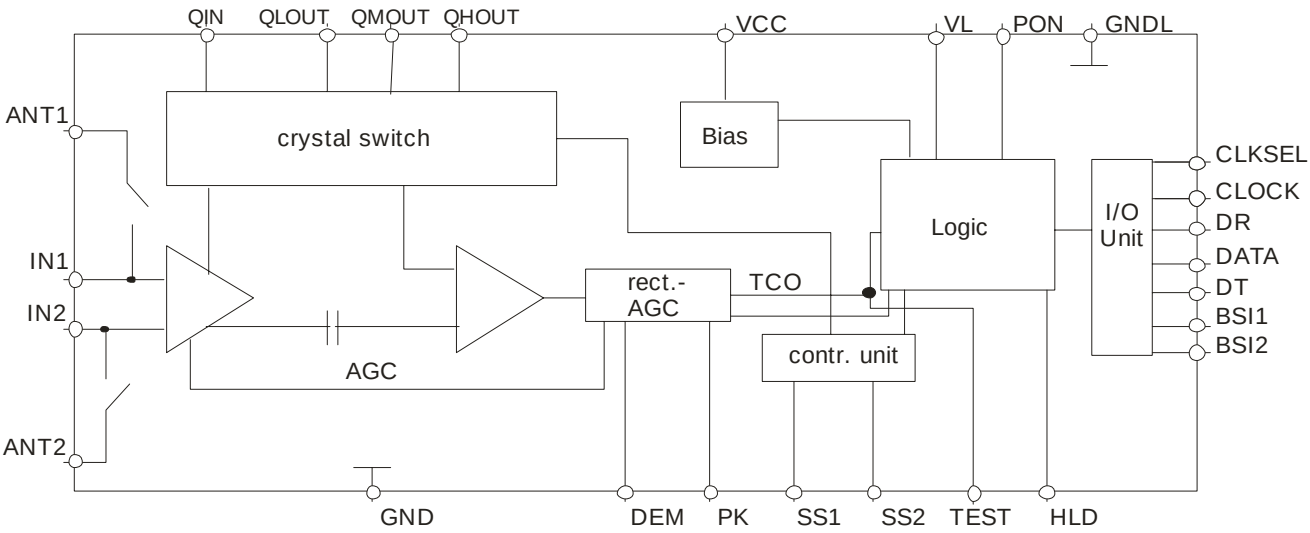


Figure 1.

3 Ordering Information

Extended Type Number	Package	Remarks
CME8000-DDT	no	die in trays
CME8000-TLSH	yes	SSO28
CME8000-TLPH	Yes	SSO28 Taped and reeled

*The packaged version of CME8000 is prepared for lead-free soldering.

4 Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Supply voltage	VCC	5.5	V
Ambient temperature range 1.2 – 2.49V	T_{amb}	-20 to +75	°C
Ambient temperature range 2.5 – 5.5V	T_{amb}	-40 to +85	°C
Storage temperature range	R_{stg}	-55 to +150	°C
Junction temperature	T_j	125	°C
Electrostatic handling (MIL Standard 883 D HMB)	+/- V_{ESD}	4	kV
Electrostatic handling (MIL MM)	+/- V_{ESD}	400	V

5 PAD Coordinates

The CME8000 is available as die for "chip-on-board" mounting and in SSO28 package.
DIE size: 2,73mm x 2,5mm
PAD size: contact window 84µm / 84µm
Thickness: 300µm±10µm

Symbol	Function	x-axis (µm)	y-axis (µm)	Pad # (dice)	Pin # (SSO28*)
ANT2	Antenna switch 2	924.0	2243.6	1	1
IN2	Input antenna	582.4	2243.6	2	2
IN1	Input antenna	395.3	2243.6	3	3
ANT1	Antenna switch 1	156.5	2101.4	4	4
VCC	Supply voltage analog part	156.5	1908.1	5	5
QHOUT	Crystal 3 output	156.5	1715.3	6	6
QMOUT	Crystal 2 output	156.5	1519.2	7	7
QLOUT	Crystal 1 output	156.5	1322.0	8	8
GND	Ground analog part	153.8	1161.6	9	9
QIN	Crystal input	156.5	881.3	10	10
DEM	Capacity for peak-detector	505.2	172.4	11	12
PK	Capacity for AGC	767.0	172.4	12	13
TEST	Test I/O	1547.2	181.6	13	14
PON	Power on	1711.3	181.6	14	16
HLD	AGC hold	1959.5	181.6	15	17
GNDL	Ground logic part	2319.8	174.5	16	18
BSI 2	Bit strength indicator 2	2518.1	355.0	17	19
BSI 1	Bit strength indicator 1	2518.1	805.6	18	20
DT	Data send clock	2517.8	1070.3	19	21
Data	Data output	2517.8	1468.7	20	22
DR	Data ready in register	2518.1	1919.2	21	23
Clock	Input 1024 / 4096Hz	2517.5	2185.9	22	24
SS2	Transmitter select 2	2332.0	2243.7	23	25
SS1	Transmitter select 1	1950.1	2243.7	24	26
VL	Supply voltage logic part	1574.9	2241.9	25	27
CLKSEL	Clock select	1287.4	2243.7	26	28

6. Pad Layout

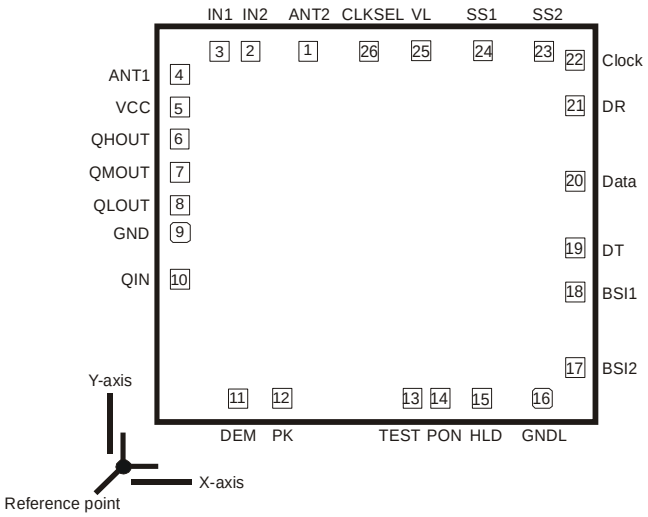
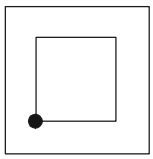


Figure 2. Pad layout



The PAD coordinates are referred to the left bottom point of the contact window

Pin Layout SSO28

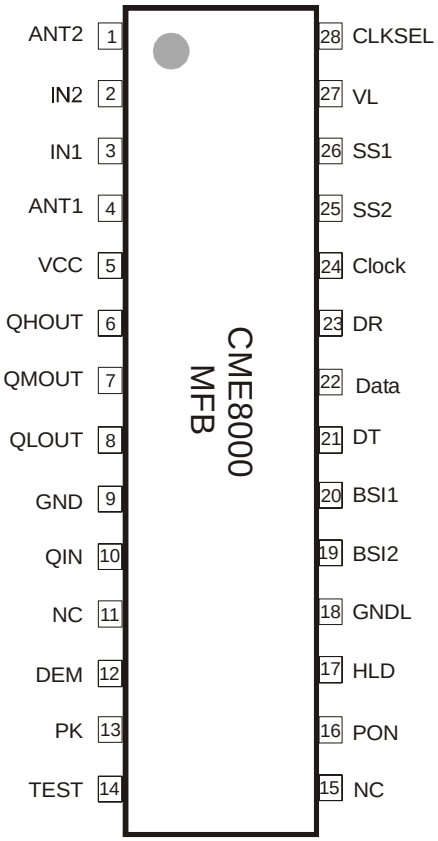


Figure 3. Pin layout SSO28

IN1, IN2

A ferrite antenna is connected between IN1 and IN2. For high sensitivity, the Q factor of the antenna circuit should be as high as possible. Please note that a high Q factor requires temperature compensation of the resonant frequency in most cases. We recommend a Q factor between 40 and 150, depending on the application. An optimal signal-to-noise ratio will be achieved by a resonator resistance of 40 kOhm to 100 kOhm.

ANT1, ANT2

To realize a reception at different frequencies with one antenna, it is possible to connect additional capacitors between the inputs. An internal MOS-switch is closed when a 60kHz protocol is activated. A second internal switch is closed choosing the JJY40 protocol (see table page 9).
The capacitors have to be connected between ANT2 and IN1 for adjusting the 60kHz frequency, and between ANT1 and IN2 to adjust the frequency to 40kHz. Note in this case both switches are closed.
In applications with supply voltages below 2.5V the impedance of the switches is probably too high for a good Q-factor.
In applications with less than 3 frequencies leave the unused pins open

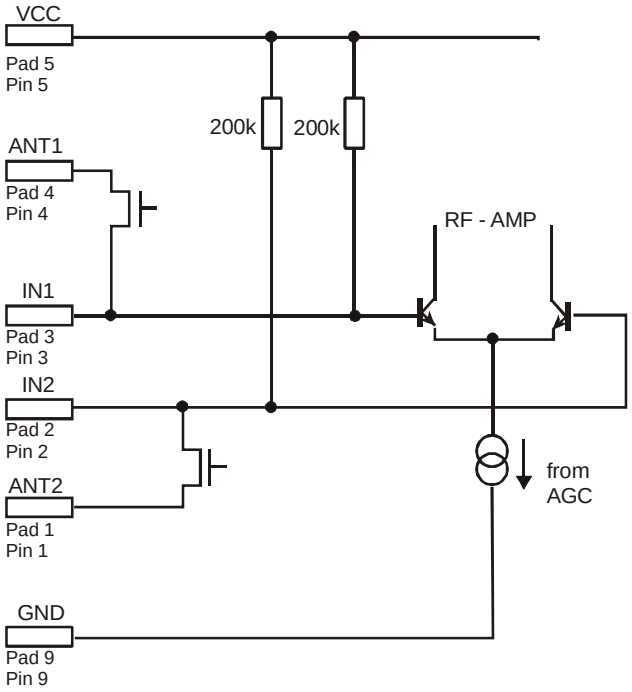


Figure 4.

QHOUT, QMOUT, QLOUT

In order to achieve a high selectivity, a crystal is connected between the Pins QOUT and QIN. It is used with the serial resonant frequency according to the time-code transmitter and acts as a serial resonator. Up to 3 crystals could be connected from QLOUT, QMOUT and QHOUT to the common input QIN. The outputs will be automatically selected by the pin SS1 and SS2 (see table). Only one of the outputs is active. Note that the output QLOUT is active if JJY40 is selected. QMOUT is active if a 60kHz protocol is selected, and QHOUT is only active for DCF or HBG.
In applications with less than 3 different frequencies, leave the unused output pins open.
The given parallel capacitor of the filter crystal (about 1.4 pF) is internally compensated so that the bandwidth of the filter is about 10 Hz. The impedance of QIN is high. Parasitic loads have to be avoided.

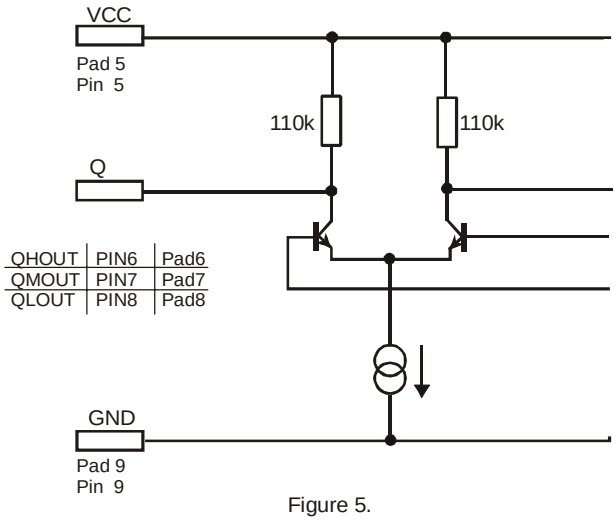


Figure 5.

QIN

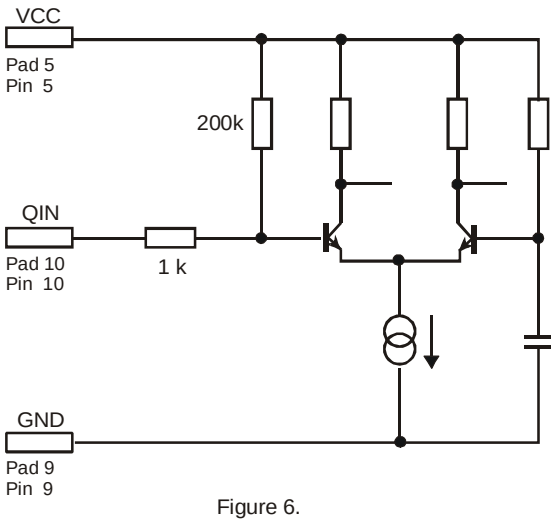


Figure 6.

DEM

Demodulator output. To ensure the function, an external capacitor has to be connected at this output.

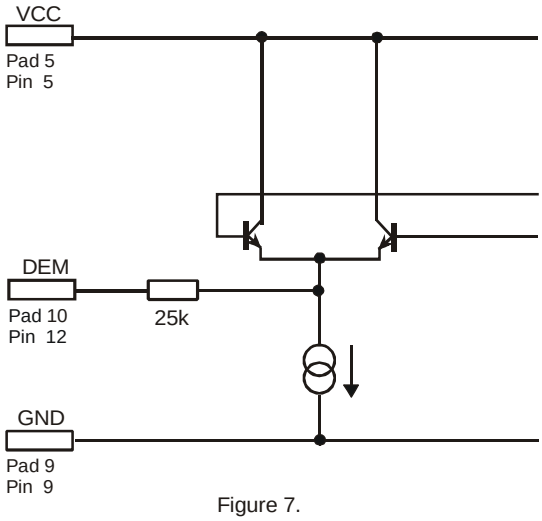


Figure 7.

NOTE: Automatic adjustment of PK and DEM timing

To realize a good regulation timings of the demodulator and the peak detector the charge and discharge currents for the capacitors at DEM and PK have different values for the different protocols. This is automatically switched internally by choosing the protocol with SS1 and SS2.

VCC, GND, VL, GNDL

V_{CC} and GND are the supply voltage inputs for the analog part. V_L and GNDL are the supply voltage inputs for the digital part. The positive supplies have to be connected externally, and also the ground pins.

To power down the circuitry it is recommended to use the PON input and not to switch the power supply. Switching the power supply results in a long power up waiting time.

PK

Peak detector output. An external capacitor has to be connected to ensure the function of the peak detector. The value of the capacitance influences the AGC regulation time.

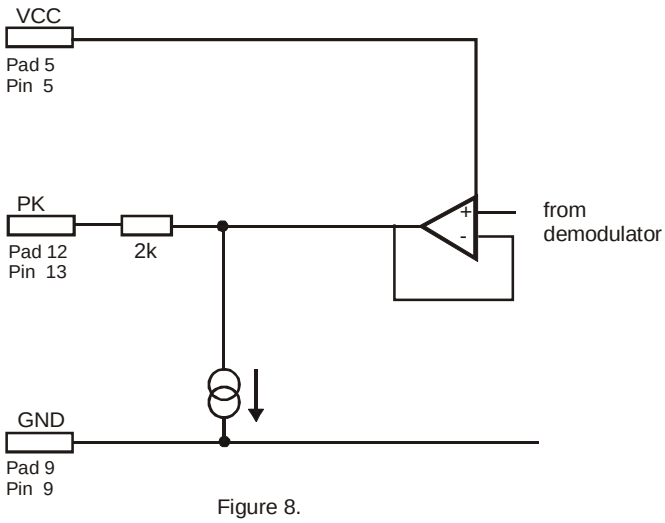


Figure 8.

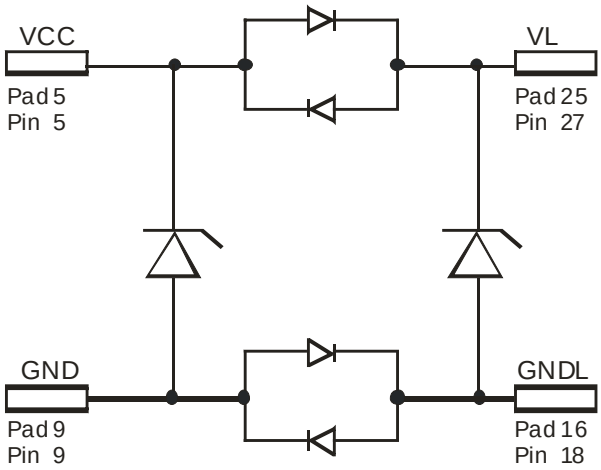


Figure 9.

CLOCK, DT, PON, HLD
These pins are high impedant MOS-inputs and require MOS-levels for operating

CLOCK
To run the IC it is necessary to apply the clock chosen by CLKSEL.
All the timings given referred to this clock cycles.
In power down mode a clocking is not necessary.

HLD
AGC hold mode: HLD high ($V_{HLD} = V_{CC}$) sets AGC HLD off, HLD low ($V_{HLD} = 0$) sets AGC HLD on, that is it holds for a short time the AGC voltage. This can be used to prevent the AGC from peak voltages, created by e.g. a stepper motor. Additional, there will be internal hold function generated, especially during read-out of data.

PON
PON must be either connected to V_{CC} or GND. If PON is connected to GND, the receiver will be activated. The set-up time is typically 0.5 s after applying GND at this pin. If PON is connected to V_{CC}, the receiver will switch to power-down mode. A power down period of min. 2msec is necessary after switching on the power supply and before switching to another protocol.

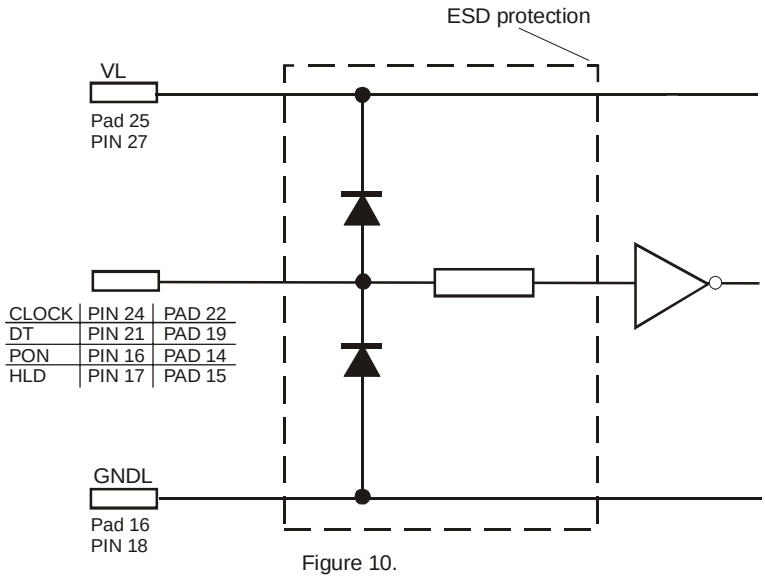


Figure 10.

BSI1, BSI2, DATA, DR
These 4 pin are MOS-outputs, which deliver MOS-level.

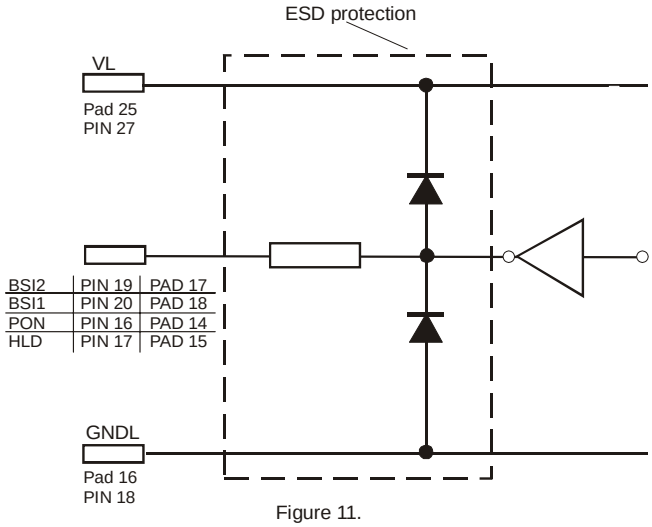


Figure 11.

SS1, SS2, CLKSEL

SS1, SS2

5 different protocols and 2 test modes are selected by this 2 tri-state input pins (see table). The selection is done in the first 20msec after the power down period. Then the selected protocol is internally stored and active until the next power down.

CLKSEL

The IC can be clocked by 2 different frequencies. A clock 4096Hz (32768Hz / 8) is expected if CLKSEL is connected to VCC. CLKSEL connected to GND implies that CME8000 CLOCK pin requires a 1024Hz (32768Hz / 32) clock frequency. The selection is done in the first 20msec after the power down period. Then the selected frequency is fix until the next power down.

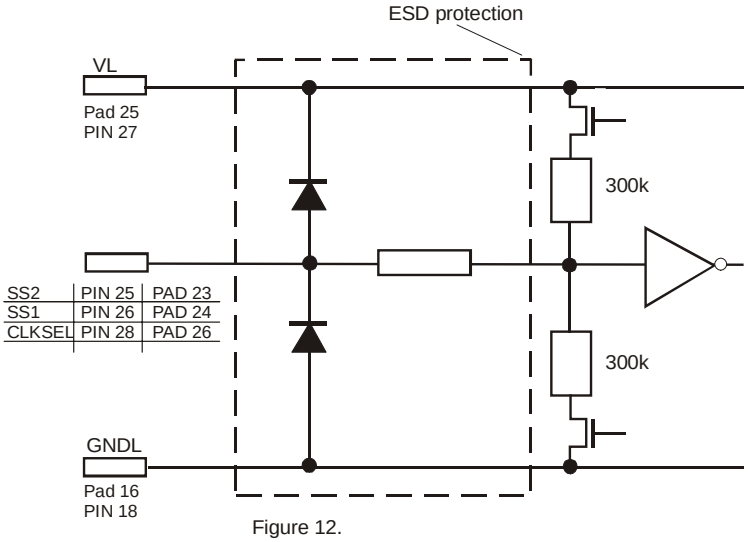


Figure 12.

7 Electrical Characteristics

V_{CC} = 3V, input signal frequency 77.5 kHz +/- 5 Hz; carrier voltage 100% reduction to 25% for t_{MOD} = 200ms; t_{amb} = 25°C, max./min. limits are at +25...C ambient temperature, unless otherwise specified.

Parameter	Test condition / Pin	Symbol	Min.	Typ.	Max.	Unit	**
Supply voltage range (V_L, V_{CC} No different supply voltages allowed!)		V_{CC}	1.2		5.0	V	
Supply current		I_{CC}		90	<120	µA	
Set-up time after V_{CC} ON*	V_{CC} = 3V	t		1.5		s	
Reception frequency range		F_{in}	40		120	kHz	
Minimum input voltage	IN1, IN2	V_{in}		0.5	0.8	µV	
Maximum input voltage	IN1, IN2	V_{in}	30	50		mV	
Setup time after PON for receiver part*		t		1.5		s	
Power-ON control; PON Pad/Pin PON							
Quiescent current receiver OFF	V_{PON}=V_{CC}, Pad/Pin V_{CC}	I_{CC0}		0.03	0.05	µA	
Set-up time after PON*		t		0.5	2	s	
Logical Part (digital inputs: PON, HLD, DT, Clock)							
Pins PON, HLD, DT, Clock	Low level High level		 0.85 V_L		0.15 V_L	V V	
Input leakage current	0<V_i < V_L		-1		1	µA	
Logical Part (digital outputs: DR, Data, BSI1, BSI2)							
Pins DR, Data, BSI1, BSI2							
Output low	Iol = 10µA				0.1 x V_L	V	
Output High	Ioh = -10µA		0.9 x V_L			V	

* During analog test mode at pin TEST
**) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Parameter	Test condition / Pin	Symbol	Min.	Typ.	Max.	Unit	**
Logical Part (tristate inputs: SS1, SS2, clksel) **Active only during the first 16 clock cycles (1024Hz) after Power-on-Reset**							
Pins SS1, SS2, clksel	Low level (R to GND) High level (R to V_L) Open (leakage current) Input leakage current after detection				20 20 100 +1	kOhm kOhm nA µA	A A A A
	$0 < V_i < V_L$		-1				
Antenna switch (Pins ANT1, ANT2) V_{CC} **= 3V**							
Resistance to IN	Switch open (SS1 = open)		1M			Ohm	A
Resistance to IN	Switch closed (SS1 = SS2 = not open)			30	50	Ohm	A

**) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

8 Logical function of SS1 and SS2

SS1	SS2	Mode	Protocol	Crystal	ANT2	ANT1	Checked protocols	Data out*
L	L	**normal**	**JJY40**	**QL**	**On**	**On**	**JJY**	**100**
L	H	**Normal**	**WWVB**	**QM**	**On**	**Off**	**WWVB** **JJY** **MSF**	**110** **100** **111**
H	L	**normal**	**JJY60**	**QM**	**On**	**Off**	**JJY**	**001**
H	H	**normal**	**MSF**	**QM**	**On**	**Off**	**MSF**	**111**
O	L	**normal**	**DCF77**	**QH**	**Off**	**Off**	**DCF77**	**101**
O	H	**normal**	**DCF77**	**QH**	**Off**	**Off**	**DCF77**	**101**
O	O	Not allowed						
O	= open							

***Protocol identifier bits 1-3 (refer to "data out timing table") Bit 1 is the first bit of output from CME8000**
After connecting power supply or/and after choosing a different country, PON (Reset mode) has to be performed.

9 Protocol recognition

To get a fast information of the received protocol, after every power on the received signal will be compared with the chosen protocol. The bit stream is checked for pulses with characteristically pulse duration.
To start a new protocol recognition it is necessary to reset via PON.

Three bits are output on Data_Out pin when the protocol is detected. Output on Data_Out pin is specified in the table “Logical function of SS1, SS2” (page 9).

WWVB is designed such that when S1, S2 selected WWVB, CME8000 scans automatically in parallel the 3 possibilities in JJY, WWVB and MSF. Once protocol identified is not WWVB, user should switch to its correct protocol setting and confirm once again on the correct setting in 60kHz.

10 Bit Strength Indicator

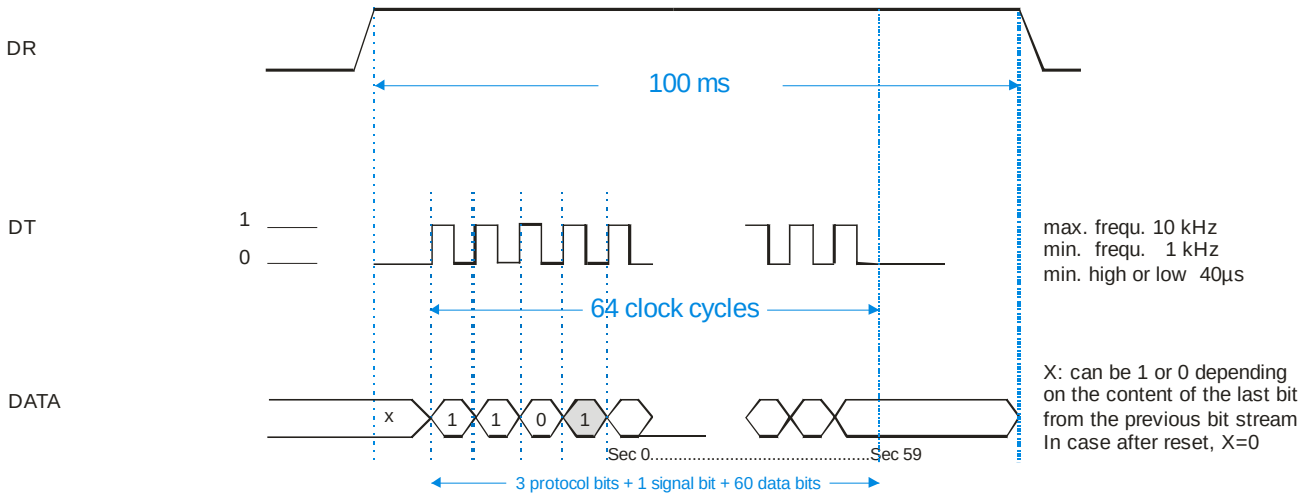
Refresh rate: Information will be refreshed every second
Output as binary digital output on BSI1 and BSI2

BSI1	BSI2	Level	
1	1	3	Near 100% correct bits
0	1	2	Some bit error, but still decodable
1	0	1	More bit errors, can try to decode, incorrect information possible
0	0	0	Decoding impossible

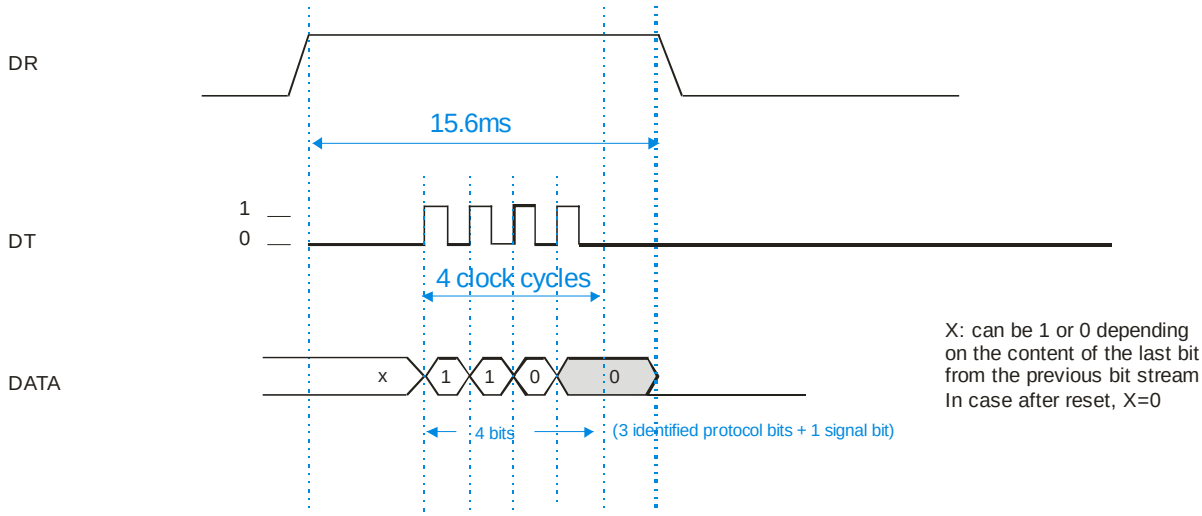
Bit strength indication

The pins BSI2 and BSI1 are the output pins for the bit strength indication with 4 levels. The bit strength indication is only influenced by the quality of the received bit and not of the field strength.
The bit strength indication starts after every power on at 0. So the outputs will be updated every second.

11 Time Diagram for normal read out (only at end-of-minute)



Time diagram for protocol-identified read out (any time other than end-of minute)

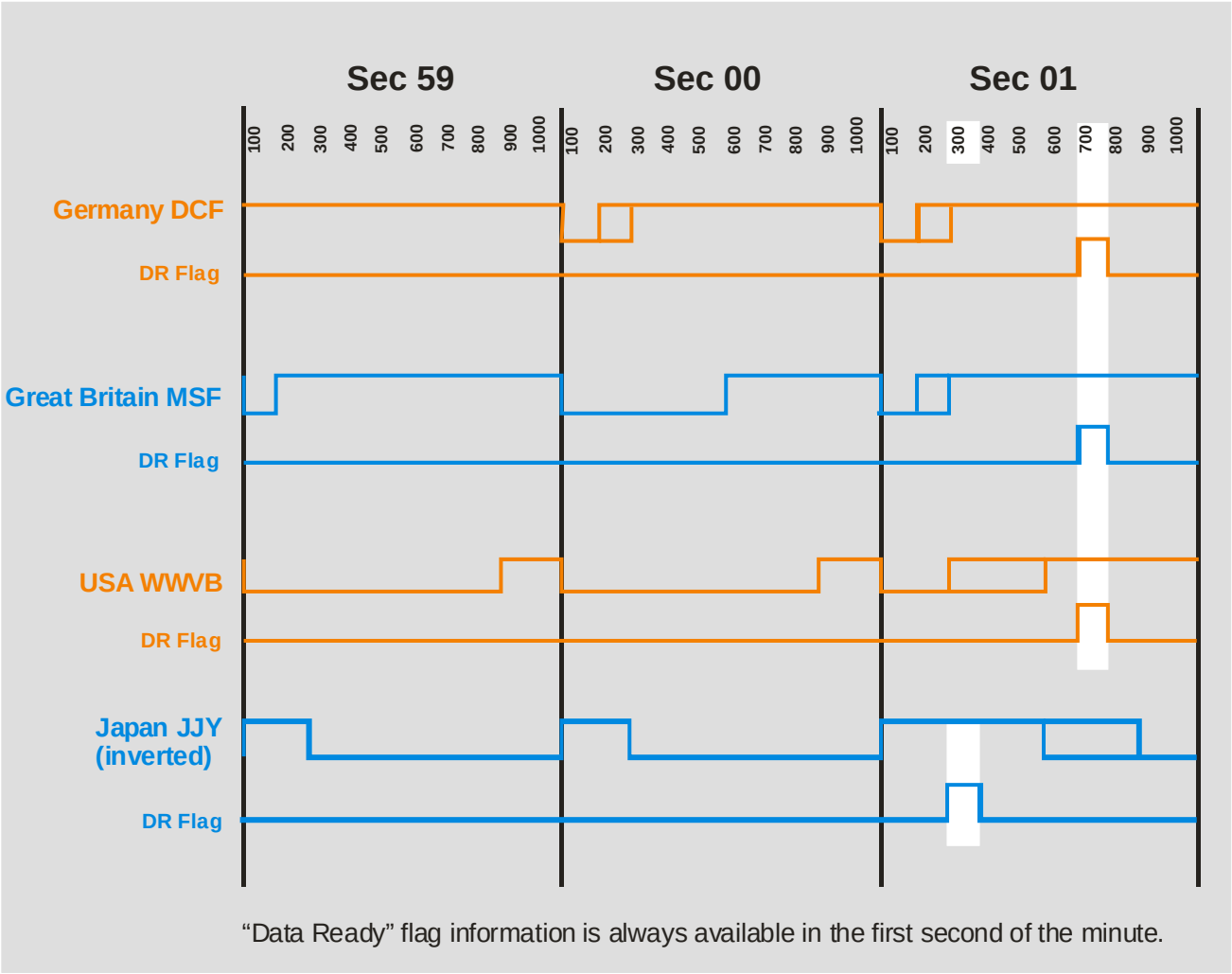


Note: CONTROL BIT = 1 stands for data bits to be followed behind, continue clocking data_out for 60 more data bits
= 0 stands for no data bits to be followed, no need to contin ue clocking data_out

Timing test condition: clock frequency = 1024Hz
max. input CLOCK frequency: 1025Hz
min. input CLOCK frequency: 1023Hz

Wake up time before DT: 1ms

12 "Data Ready" Flag and Framestart is active based on the following criteria for the different protocols :



"Data Ready" flag information is always available in the first second of the minute.

Behaviour of the Hardware Logic

DCF77 Signal: at minimum 1µV input voltage all 60 bit of the signal are decoded without failure and the frame marker (no modulation at bit 60) is recognized also. A pulse of ~200ms is recognized as binary 1 and a pulse of ~100ms is recognized as a binary 0. After the reception of a complete string, including the frame marker, all bit are stored in the equivalent place in the shift register (bit 1 in cell1, bit 60 in cell 60)

WWVB Signal: at minimum 1µV input voltage all 60 bit of the signal are decoded without failure and the frame marker and the position markers (800ms) are recognized also. A pulse of ~500ms is recognized as a binary 1 and a pulse of ~200ms is recognized as a binary 0. After reception of a complete string, including the frame marker, all bit are stored in the equivalent place in the shift register (bit 1 in cell1, bit 60 in cell 60).

MSF Signal: at minimum 1µV input voltage all 60 bit of the signal are decoded without failure and the frame marker (500ms) is recognized also. A pulse of ~200ms is recognized as a binary 1 and a pulse of ~100ms is recognized as a binary 0. After reception of a complete string, including the frame marker, all bit are stored in the equivalent place in the shift register (bit 1 in cell 1, bit 60 in cell 60)
The bits 53 - 58 (parity checks bits) have a special treatment, a pulse of ~300msec is recognized as a binary 1 and a pulse of ~200msec as a binary 0.

JJY Signal: At minimum 1µV input voltage all 60 bit of the signal are decoded without failure and the frame marker and the position markers (200ms) are recognized also. A pulse of ~500ms is recognized as binary 1 and a pulse of ~800ms is recognized as a binary 0. After reception of a complete string, including the frame marker, all bit are stored in the equivalent place in the shift register (bit 1 in cell 1, bit 60 in cell 60).

Every unused bit will be stored with the same condition as the normal bits of this protocol (e.g. for MSF ~100msec is stored as a binary 0, and a ~200msec pulse as binary 1)

Unused bits are listed as follows:
MSF: 1- 16, 52;
WWVB: 4, 10 ,11, 14, 20 ,21, 24, 34-38, 40-44,54
JJY: 4, 10, 11, 14, 20, 21, 24, 34, 35, 53-58
DCF: no special treatment for unused bits

Storage of Position Markers and Frame start Bits

These bits will be stored as a 1, if the pulse is about the expected length (WWVB 800msec), otherwise a binary 0 is stored.

List of position markers, and frame start bits:
WWVB, JJY: 0, 9, 19, 29, 39, 49, 59
MSF: 0
DCF: 59

Test modes

In the analog test mode, which could be selected by SS1 and SS2 (see table “Logical function of SS1, SS2”), Pin TEST is connected internally to the output of the analog part. The signal TCO is now available for testing, and is internally still connected to the logic part.

In the digital Test mode the pin TEST is an input for the logic part. With a digital pattern the logic part can be tested. The internal connection TCO is open in the digital test mode.

13 Application Circuitry for 1 antenna solution (77.5 kHz)

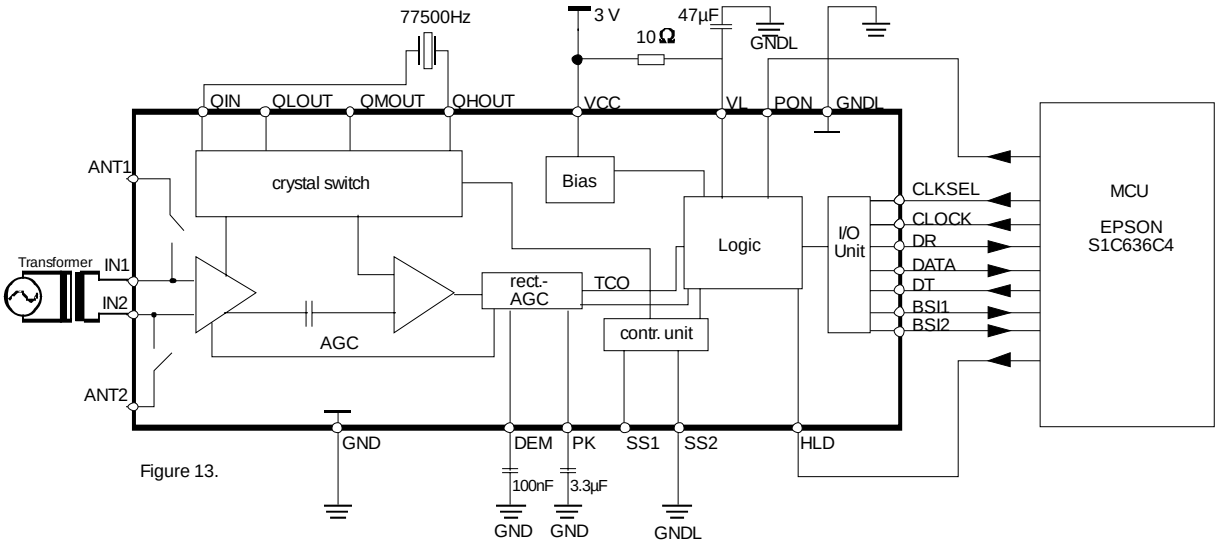


Figure 13.

14 Application Circuitry for multi frequency antenna use (3 frequencies: 40kHz, 60kHz, 77.5kHz)

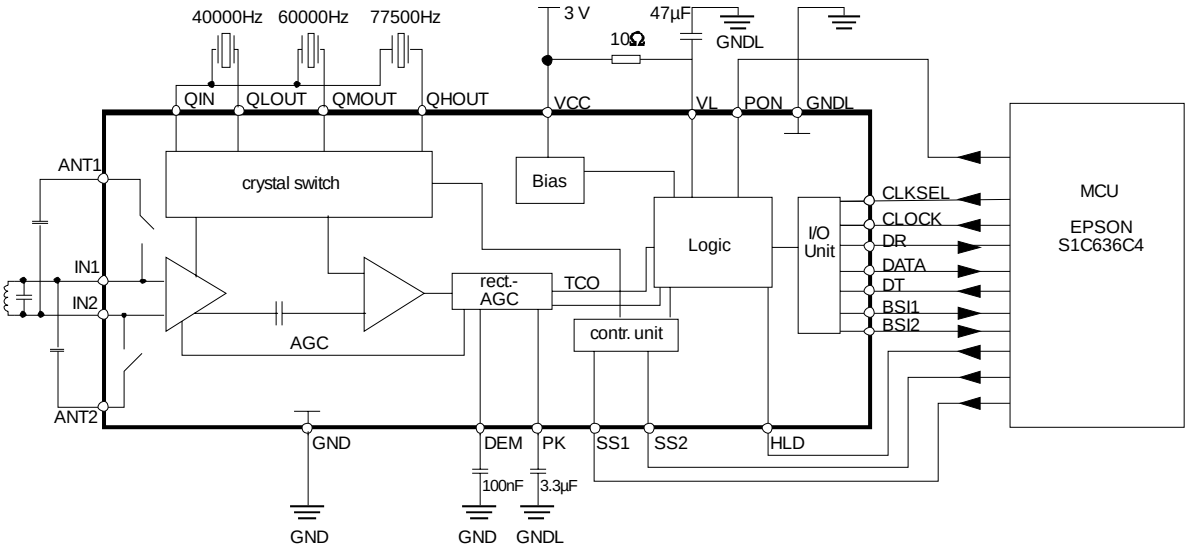
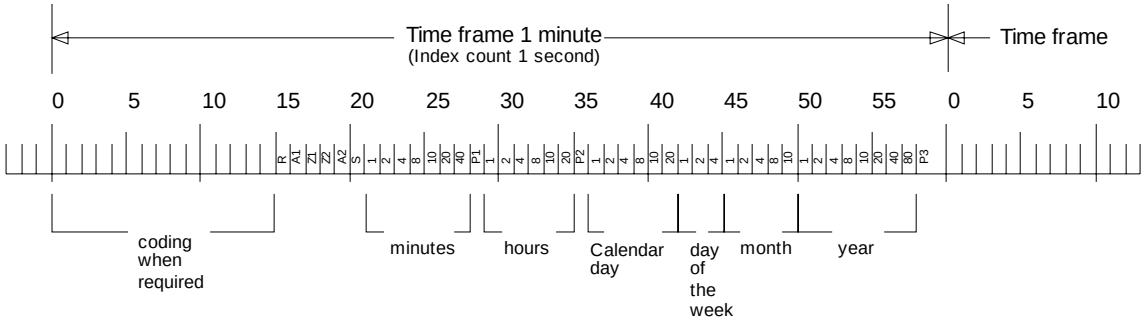


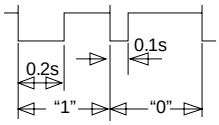
Figure 14.

15 Information on the German Transmitter

(Customer is responsible to verify this information)

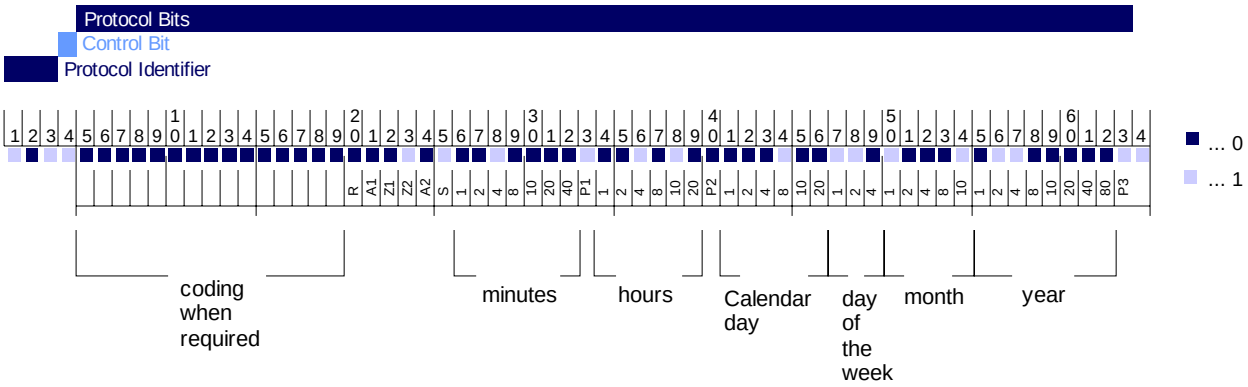
Station:	DCF 77	Location:	Mainflingen/Germany
Frequency:	77.5 kHz	Geographical coordinates:	50° 01'N, 09° 00'E
Transmitting power:	50 kW	Time of transmission:	permanent





M = Minute marker (100ms)
R = Second marker (200ms = transmission by reserve antenna)
A1 = Announcement of change-over to summer-time or vice versa
Z1 = DST (summertime = 200ms, otherwise 100ms)
Z2 = DST (summertime = 100ms, otherwise 100ms)
A2 = Announcement of leap second
S = Startbit of time code information
P1-P3 = Parity check bits

Example of DCF77 data out:
2006 / 11 months / 8 days / 14 hours / 04 minutes



Modulation

The carrier amplitude is reduced to 25% at the beginning of each second for a period of 100 ms (binary zero) or 200 ms (binary one), except the 59th second.

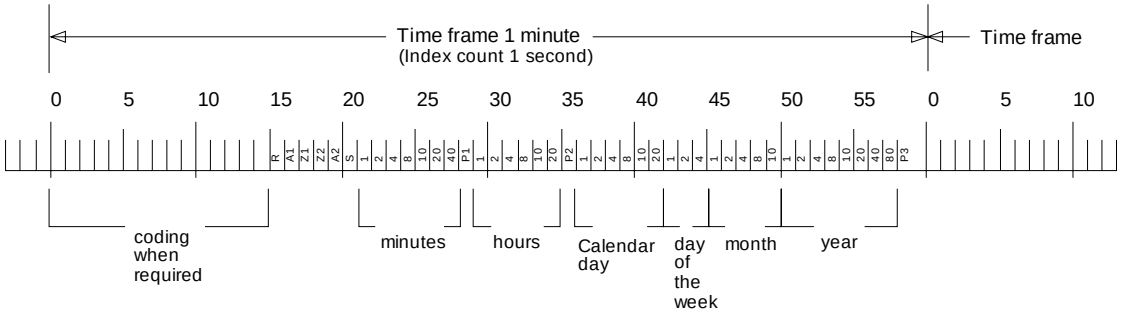
Time-Code Format (based on Information of Deutsche Bundespost)

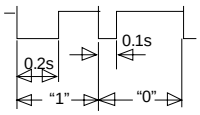
The time-code format consists of 1-minute time frames. There is no modulation at the beginning of the 59th second to indicate the switch over to the next 1-minute time frame. A time frame contains BCD-coded information of minutes, hours, calendar day, day of the week, month and year between the 20th second and 58th second of the time frame, including the start bit S (200 ms) and parity bits P1, P2 and P3. Furthermore, there are 5 additional bits R (transmission by reserve antenna), A1 (announcement of change-over to summer time), Z1 (during summer time 200 ms, otherwise 100 ms), Z2 (during winter time 200 ms, otherwise 100 ms) and A2 (announcement of leap second) transmitted between the 15th second and 19th second of the time frame.

16 Information on the Swiss Transmitter

(Customer is responsible to verify this information)

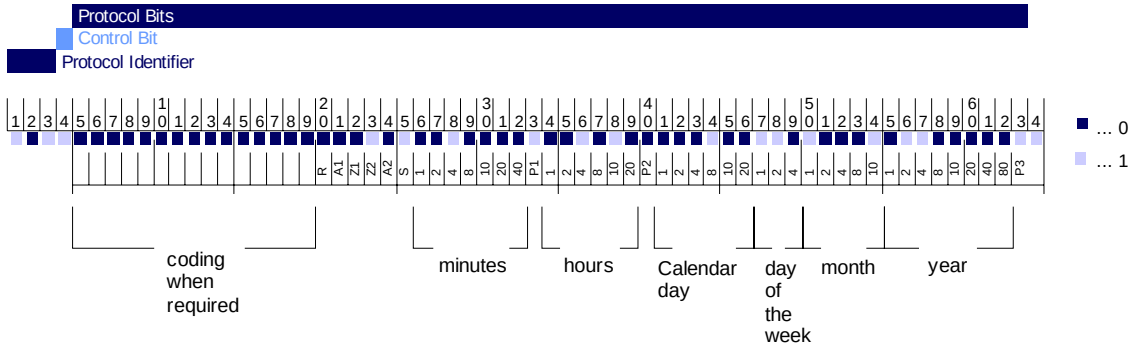
Station:	HBG	Location:	Prangins/Switzerland
Frequency:	75 kHz	Geographical coordinates:	46° 24'N, 06° 15'E
Transmitting power:	20 kW	Time of transmission:	permanent





M = Minute marker (100ms)
R = Second marker (200ms = transmission by reserve antenna)
A1 = Announcement of change-over to summer-time or vice versa
Z1 = DST (summertime = 200ms, otherwise 100ms)
Z2 = DST (summertime = 100ms, otherwise 100ms)
A2 = Announcement of leap second
S = Startbit of time code information
P1-P3 = Parity check bits

Example of HBG data out:
2006 / 11 months / 8 days / 14 hours / 04 minutes



Modulation

The carrier amplitude is reduced to 25% at the beginning of each second for a period of 100 ms (binary zero) or 200 ms (binary one), except the 59th second.

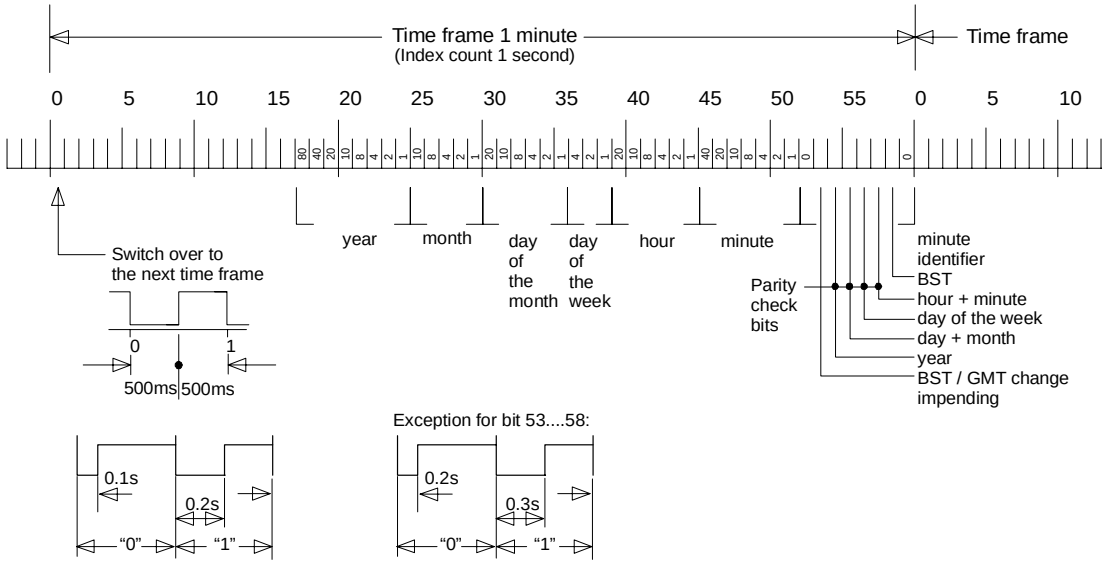
Time-Code Format (based on Information of Bundesamt für Metrologie und Akkreditierung (METAS))

The time-code format consists of 1-minute time frames. There is no modulation at the beginning of the 59th second to indicate the switch over to the next 1-minute time frame. A time frame contains BCD-coded information of minutes, hours, calendar day, day of the week, month and year between the 20th second and 58th second of the time frame, including the start bit S (200 ms) and parity bits P1, P2 and P3. Furthermore, there are 5 additional bits R (transmission by reserve antenna), A (announcement of change-over to summer time), E (during summer time 200 ms, otherwise 100 ms), H (during winter time 200 ms, otherwise 100 ms) and L (announcement of leap second) transmitted between the 15th second and 19th second of the time frame.

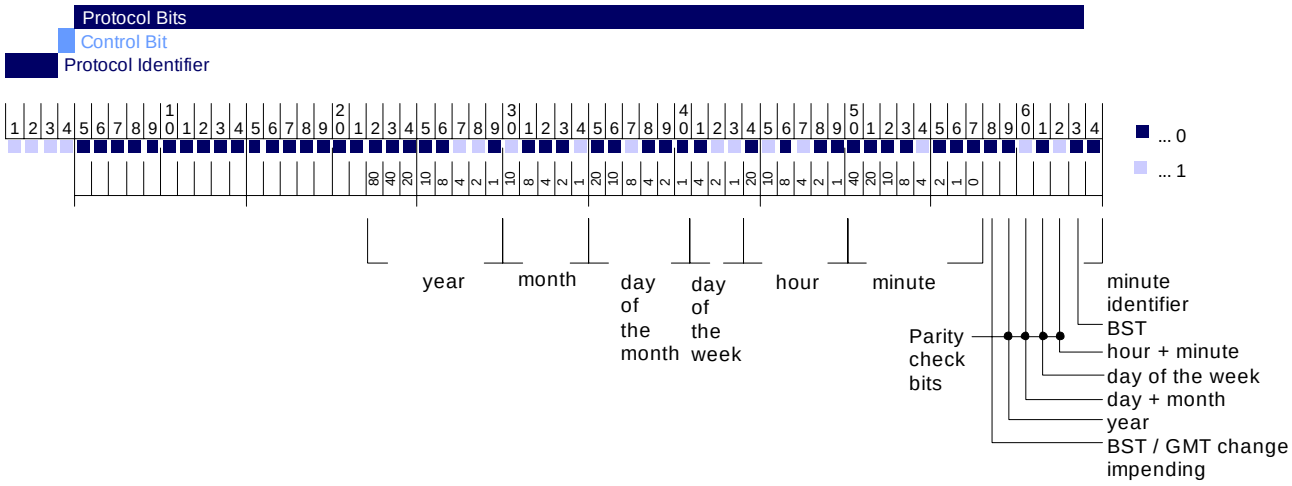
17 Information on the British Transmitter

(Customer is responsible to verify this information)

Station:	MSF	Location:	Rugby
Frequency:	60 kHz	Geographical coordinates:	52° 22'N, 01° 11'W
Transmitting power:	50 kW	Time of transmission:	permanent, except for quarterly and annual outages



Example of MSF data out:
2006 / 11 months / 8 days / 14 hours / 04 minutes



Modulation

The carrier amplitude is switched off at the beginning of each second for a period of 100 ms (binary zero) or 200 ms (binary one).

Exception:
Bit 53, 54, 55, 56, 57, 58. For these bits, a binary zero is defined with 200 ms, a binary one with 300ms.

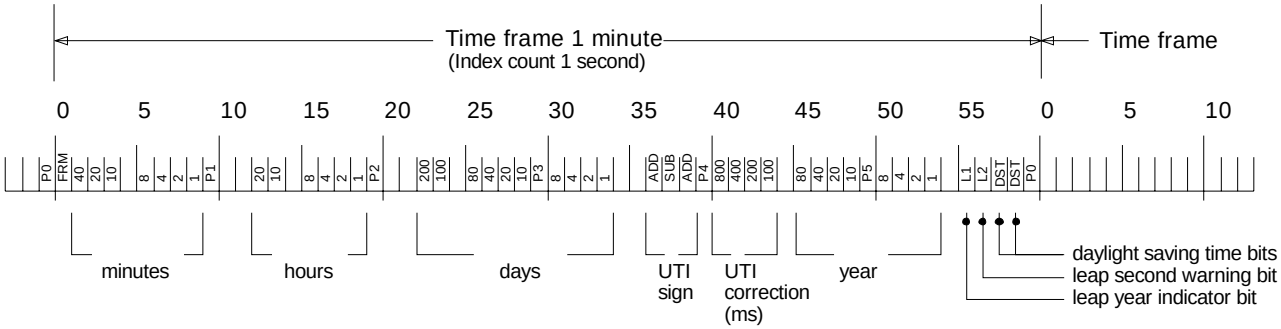
Time-Code Format

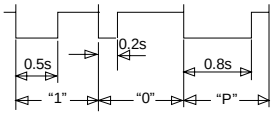
The time-code format consists of 1-minute time frames. A time frame contains BCD coded information of year, month, calendar day, day of the week, hours and minutes. At the switch-over to the next time frame, the carrier amplitude is reduced for a period of 500 ms.
The presence of the fast code during the first 500 ms at the beginning of the minute is not guaranteed. The transmission rate is 100 bit/s and the code contains information of hour, minute, day and month.

18 Information on the US Transmitter

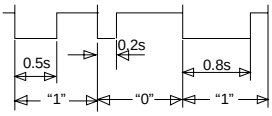
(Customer is responsible to verify this information)

Station:	WWVB	Location:	Fort Collins/Colorado
Frequency:	60 kHz	Geographical coordinates:	40° 40'N, 105° 03' W
Transmitting power:	50 kW	Time of transmission:	permanent





CME8000 digital out:



FRM = Frame Marker

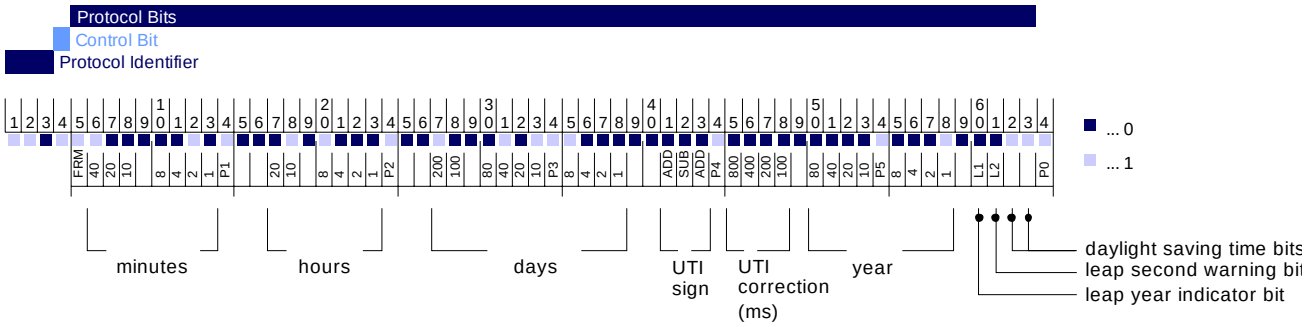
L1 = Leap year indicator
"1" = non leap year
"0" = leap year
The bit is set to 1 during each leap year after January 1 but before February 29. It is set back to 0 on January 1 of the year following the leap year.

L2 = Leap second warning bit
The bit is set to 1 near the start of the month in which a leap second is added. It is set to 0 immediately after the leap second insertion.

DST = Daylight savings time bit

P0 - P5 = Position marker

Example of WWVB data out:
2001 / 258 days / 18 hours / 42 minutes



Modulation

The carrier amplitude is reduced by 10 dB at the beginning of each second and is restored within 500 ms (binary one) or within 200 ms (binary zero) or within 800 ms (position-identifier marker or frame reference marker).

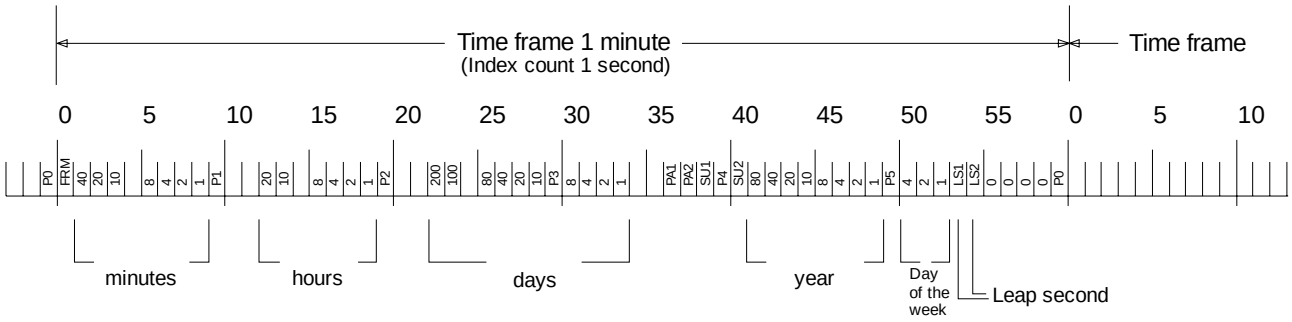
Time-Code Format

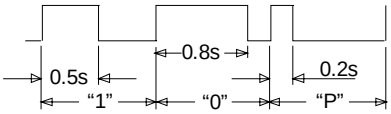
The time-code format consists of 1-minute time frames. A time frame contains BCD-coded information of minutes, hours, days and year. In addition, there are 6 position-identifier markers (P0 thru P5) and 1 frame-reference marker with reduced carrier amplitude of 800 ms duration

19 Information on the Japanese Transmitter

(Customer is responsible to verify this information)

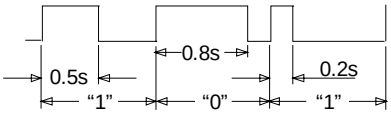
Station:	Ohtakadoya-yama	Location:	Miyakoji Vil.,Fukushima Pref.
Frequency:	40 kHz	Geographical coordinates:	37° 22'N, 140° 51'E
Transmitting power:	50 kW	Time of transmission:	permanent
Station:	Hagane-yama	Location:	Fuji Vil., Saga Pref.
Frequency:	60 kHz	Geographical coordinates:	33° 28'N, 130° 11'E
Transmitting power:	50 kW	Time of transmission:	permanent





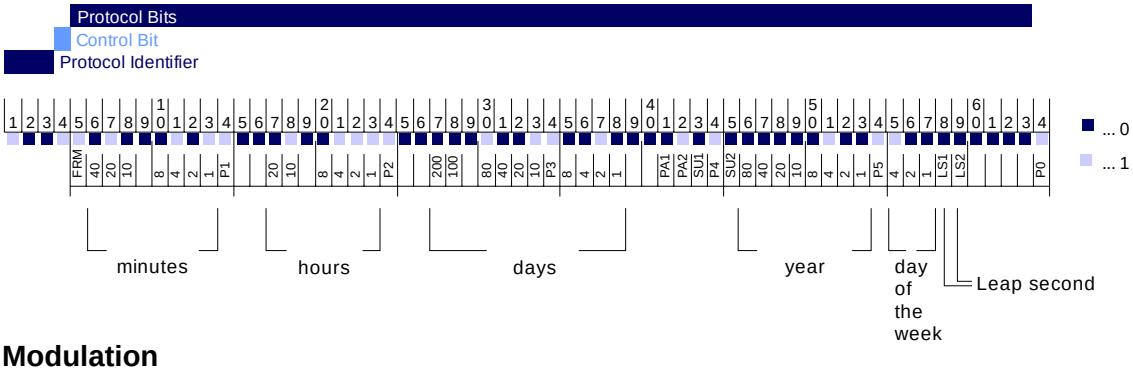
0.5 second: Binary one
0.8 second: Binary zero
0.2 second: Position identifier markers P0...P5

CME8000 digital out:



FRM	=	Frame marker
LS1	=	Leap second
LS2	=	Leap second
P0-P5	=	Position identifier markers
Pa1+Pa2	=	Parity bits

Example of JJY data out:
2004 / 92 days (1st April) / 17 hours / 25 minutes



Modulation

The carrier amplitude is 100% at the beginning of each second and is switched to 10% after 500 ms (binary one) or after 800 ms (binary zero) or after 200 ms for Position-identifier marker (P0...P5) and frame reference marker.

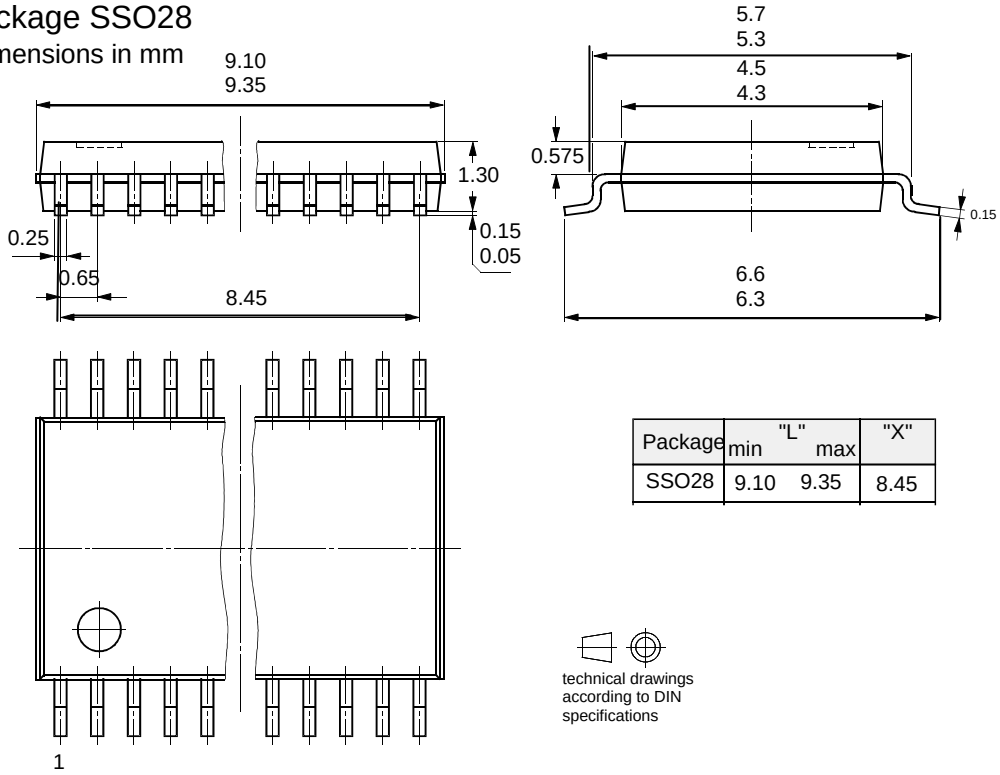
Time-Code Format

The time-code format consists of 1-minute time frames. A time frame contains BCD-coded information of minutes, hours, days, weeks and year. In addition, there are 6 position-identifier markers (P0 through P5) with reduced carrier amplitude of 800 ms duration.

20 Package information

Package SSO28

Dimensions in mm



Package	"L" min	"L" max	"X"
SSO28	9.10	9.35	8.45

technical drawings according to DIN specifications

Recommended Infrared/Convection Solder Reflow Profile (SMD packages) according JEDEC J-STD-020B you will find on our webpage http://www.c-maxgroup.com In the download area. Please look for “soldering condition”.

21 Ozone Depleting Substances Policy Statement

It is the policy of **C-MAX** to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere, which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

C-MAX has been able to use the policy of continuous improvements to eliminate the use of ODSs listed in following documents.

1. Annex A,B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA.
3. Council Decision 88/540/EEC and 91/690/EEC Annex A,B and C (transitional substances) respectively.

C-MAX can certify that our semiconductor CME8000 is not manufactured with ozone depleting substances and do not contain such substances.

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