**MOSEL VITELIC**

# *V53C511740500*
# *4M X 4 EDO PAGE MODE*
# *CMOS DYNAMIC RAM*

| V53C511740500 | 50 | 60 | 70 |
|---|---|---|---|
| Max. $\overline{RAS}$ Access Time, ($t_{RAC}$) | 50 ns | 60 ns | 70 ns |
| Max. Column Address Access Time, ($t_{CAA}$) | 25 ns | 30 ns | 35 ns |
| Min. Extended Data Out Page Mode Cycle Time, ($t_{PC}$) | 20 ns | 25 ns | 30 ns |
| Min. Read/Write Cycle Time, ($t_{RC}$) | 84 ns | 104 ns | 124 ns |

## *Features*

- 4M x 4-bit organization
- EDO Page Mode for a sustained data rate of 50 MHz
- $\overline{RAS}$ access time: 50, 60, 70 ns
- Low power dissipation
- Output unlatched at cycle end allows two-dimensional chip selection.
- Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh, Hidden Refresh, and Self Refresh.
- Refresh Interval – 2048 cycles/32 ms
- Available in 24/26-pin 300 mil SOJ, and 24/26-pin 300 mil TSOP-II
- Single +5 V ±10% Power Supply
- TTL Interface

## *Description*

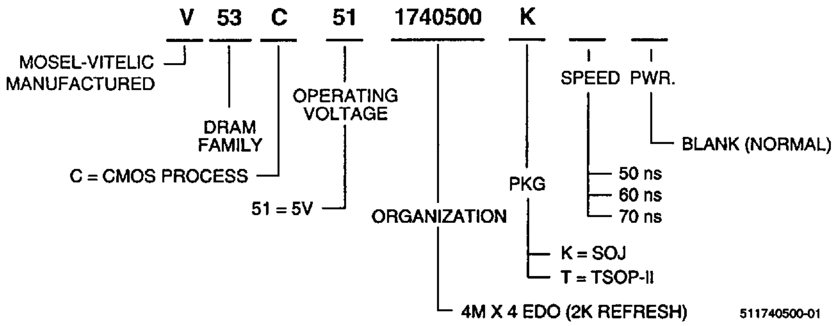
The V53C511740500 is a 4,194,304 x 4 bit high-performance CMOS dynamic random access memory. The V53C511740500 offers Page mode operation with Extended Data Output. The V53C511740500 has a symmetric address, 11-bit row and 11-bit column.

All inputs are TTL compatible. EDO Page Mode operation allows random access up to 2048 x 4 bits, within a page, with cycle times as short as 20ns.

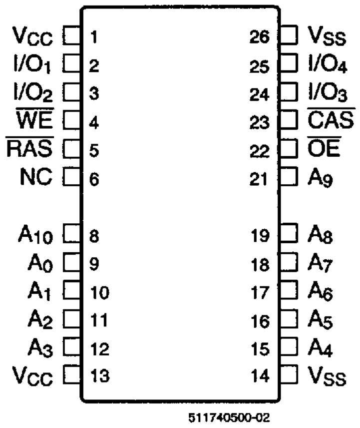
These features make the V53C511740500 ideally suited for a wide variety of high performance computer systems and peripheral applications.

## *Device Usage Chart*

| Operating Temperature Range | Package Outline | | Access Time (ns) | | | Power | | Temperature Mark |
|---|---|---|---|---|---|---|---|---|
| | K | T | 50 | 60 | 70 | Std. | L | |
| 0°C to 70 °C | • | • | • | • | • | • | • | Blank |



### *24/26 Pin Plastic SOJ /TSOP-II PIN CONFIGURATION Top View*



| Description | Pkg. | Pin Count |
|---|---|---|
| SOJ | K | 24/26 |
| TSOP-II | T | 24/26 |

### *Pin Names*

| | |
|---|---|
| $A_0$–$A_{10}$ | Row, Column Address Inputs |
| $\overline{RAS}$ | Row Address Strobe |
| $\overline{CAS}$ | Column Address Strobe |
| $\overline{WE}$ | Write Enable |
| $\overline{OE}$ | Output Enable |
| $I/O_1$–$I/O_4$ | Data Input, Output |
| $V_{CC}$ | +5V Supply |
| $V_{SS}$ | 0V Supply |
| NC | No Connect |

## *Absolute Maximum Ratings**

| | |
|---|---|
| Operating temperature range | 0 to 70 °C |
| Storage temperature range | -55 to 150 °C |
| Soldering temperature | 260 °C |
| Soldering time | 10 s |
| Input/output voltage | -0.5 to min ($V_{CC}$+0.5, 7) V |
| Power supply voltage | -1.0V to 7V |
| Power dissipation | 1.0 W |
| Data out current (short circuit) | 50 mA |

***Note:** Operation above Absolute Maximum Ratings can adversely affect device reliability.

## *Capacitance**

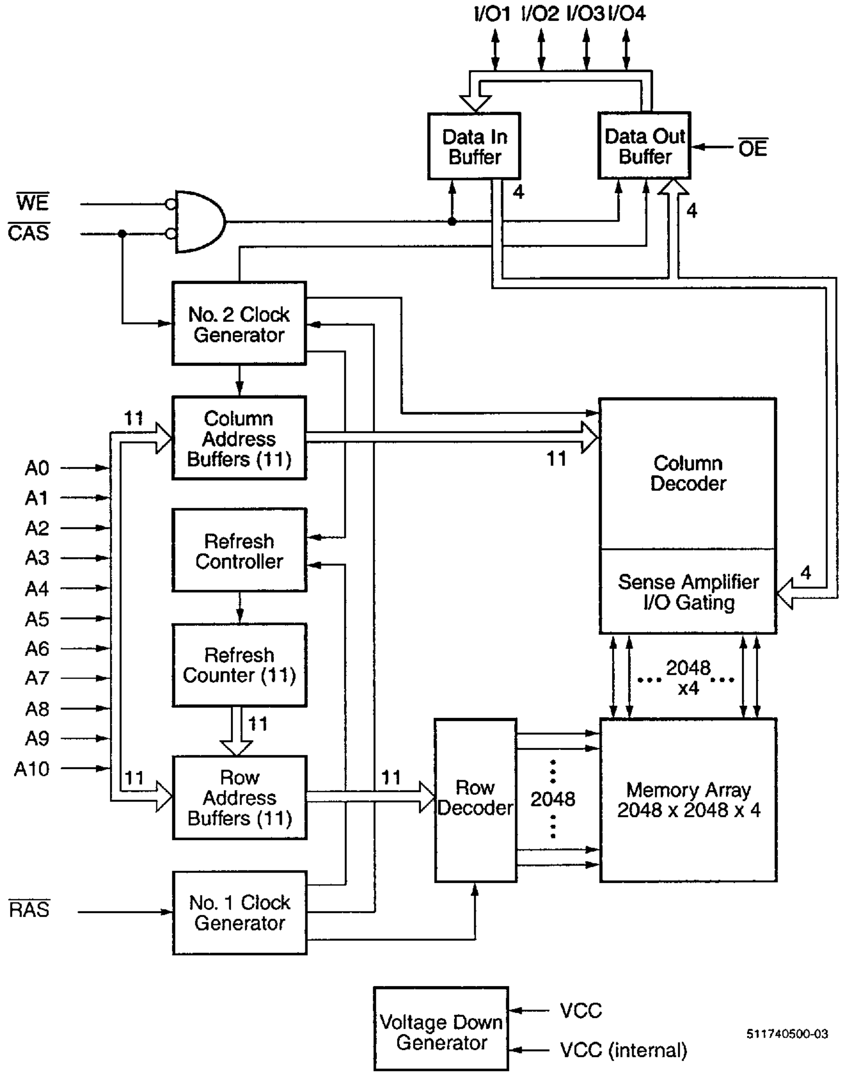
$T_A = 25°C, V_{CC} = 5\ V \pm 10\%, V_{SS} = 0\ V, f = 1\ MHz$

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $C_{IN1}$ | Address Input | — | 5 | pF |
| $C_{IN2}$ | $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ | — | 7 | pF |
| $C_{OUT}$ | Data Input/Output | — | 7 | pF |

***Note:** Capacitance is sampled and not 100% tested.

## *Block Diagram*

**4096 x 4**



511740500-03

## *DC and Operating Characteristics* (1-2)

$T_A$ = 0°C to 70°C, $V_{CC}$ = 5 V ± 10%, $V_{SS}$ = 0 V, unless otherwise specified.

| Symbol | Parameter | Access Time | V53C511740500 | | | Unit | Test Conditions | Notes |
|---|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | | |
| $I_{LI}$ | Input Leakage Current (any input pin) | | –10 | | 10 | µA | $V_{SS} \le V_{IN} \le V_{CC} + 0.3V$ | 1 |
| $I_{LO}$ | Output Leakage Current (for High-Z State) | | –10 | | 10 | µA | $V_{SS} \le V_{OUT} \le V_{CC} + 0.3V$<br>$\overline{RAS}$, $\overline{CAS}$ at $V_{IH}$ | 1 |
| $I_{CC1}$ | $V_{CC}$ Supply Current, Operating | 50 | | | 120 | mA | $t_{RC} = t_{RC}$ (min.) | 2, 3, 4 |
| | | 60 | | | 110 | | | |
| | | 70 | | | 100 | | | |
| $I_{CC2}$ | $V_{CC}$ Supply Current, TTL Standby | | | | 2 | mA | $\overline{RAS}$, $\overline{CAS}$ at $V_{IH}$<br>other inputs $\ge V_{SS}$ | |
| $I_{CC3}$ | $V_{CC}$ Supply Current, $\overline{RAS}$-Only Refresh | 50 | | | 120 | mA | $t_{RC} = t_{RC}$ (min.) | 2, 4 |
| | | 60 | | | 110 | | | |
| | | 70 | | | 100 | | | |
| $I_{CC4}$ | $V_{CC}$ Supply Current, EDO Page Mode Operation | 50 | | | 70 | mA | Minimum Cycle | 2, 3, 4 |
| | | 60 | | | 55 | | | |
| | | 70 | | | 45 | | | |
| $I_{CC5}$ | $V_{CC}$ Supply Current, CMOS Standby | | | | 1.0 | mA | $\overline{RAS} \ge V_{CC} - 0.2$ V,<br>$\overline{CAS} \ge V_{CC} - 0.2$ V | 1 |
| $I_{CC6}$ | Average Self Refresh Current CBR cycle with $t_{RAS} > t_{RASS}$ min., $\overline{CAS}$ held low, $\overline{WE} = V_{CC} - 0.2V$, Address and $D_{IN} = V_{CC} - 0.2V$ or 0.2V | | | | 1.0 | mA | | |
| $I_{CC7}$ | $V_{CC}$ Supply Current, during $\overline{CAS}$-before-$\overline{RAS}$ Refresh | 50 | | | 120 | mA | | 2, 4 |
| | | 60 | | | 110 | | | |
| | | 70 | | | 100 | | | |
| $V_{IL}$ | Input Low Voltage | | –0.5 | | 0.8 | V | | 1 |
| $V_{IH}$ | Input High Voltage | | 2.4 | | $V_{CC}$+0.5 | V | | 1 |
| $V_{OL}$ | Output Low Voltage | | | | 0.4 | V | $I_{OL}$ = 4.2 mA | 1 |
| $V_{OH}$ | Output High Voltage | | 2.4 | | | V | $I_{OH}$ = –5 mA | 1 |

## *AC Characteristics*$^{5)6)}$

$T_A$ = 0 to 70 °C, $V_{CC}$ = 5 V ± 10 %, $t_T$ = 2 ns

| Symbol | Parameter | -50 |  | -60 |  | -70 |  | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
|  |  | min. | max. | min. | max. | min. | max. |  |  |
| **Common Parameters** |  |  |  |  |  |  |  |  |  |
| $t_{RC}$ | Random read or write cycle time | 84 | – | 104 | – | 124 | – | ns |  |
| $t_{RP}$ | $\overline{\text{RAS}}$ precharge time | 30 | – | 40 | – | 50 | – | ns |  |
| $t_{RAS}$ | $\overline{\text{RAS}}$ pulse width | 50 | 10k | 60 | 10k | 70 | 10k | ns |  |
| $t_{CAS}$ | $\overline{\text{CAS}}$ pulse width | 8 | 10k | 10 | 10k | 12 | 10k | ns |  |
| $t_{ASR}$ | Row address setup time | 0 | – | 0 | – | 0 | – | ns |  |
| $t_{RAH}$ | Row address hold time | 8 | – | 10 | – | 10 | – | ns |  |
| $t_{ASC}$ | Column address setup time | 0 | – | 0 | – | 0 | – | ns |  |
| $t_{CAH}$ | Column address hold time | 8 | – | 10 | – | 12 | – | ns |  |
| $t_{RCD}$ | $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time | 12 | 37 | 14 | 45 | 14 | 53 | ns |  |
| $t_{RAD}$ | $\overline{\text{RAS}}$ to column address delay | 10 | 25 | 12 | 30 | 12 | 35 | ns |  |
| $t_{RSH}$ | $\overline{\text{RAS}}$ hold time | 13 |  | 15 | – | 17 | – | ns |  |
| $t_{CSH}$ | $\overline{\text{CAS}}$ hold time | 40 |  | 50 | – | 60 | – | ns |  |
| $t_{CRP}$ | $\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time | 5 | – | 5 | – | 5 | – | ns |  |
| $t_T$ | Transition time (rise and fall) | 1 | 50 | 1 | 50 | 1 | 50 | ns | 7 |
| $t_{REF}$ | Refresh period for V53C511740500 | – | 32 | – | 32 | – | 32 | ms |  |
| **Read Cycle** |  |  |  |  |  |  |  |  |  |
| $t_{RAC}$ | Access time from $\overline{\text{RAS}}$ | – | 50 | – | 60 | – | 70 | ns | 8, 9 |
| $t_{CAC}$ | Access time from $\overline{\text{CAS}}$ | – | 13 | – | 15 | – | 17 | ns | 8, 9 |
| $t_{CAA}$ | Access time from column address | – | 25 | – | 30 | – | 35 | ns | 8,10 |
| $t_{OEA}$ | $\overline{\text{OE}}$ access time | – | 13 | – | 15 | – | 17 | ns |  |
| $t_{RAL}$ | Column address to $\overline{\text{RAS}}$ lead time | 25 | – | 30 | – | 35 | – | ns |  |
| $t_{RCS}$ | Read command setup time | 0 | – | 0 | – | 0 | – | ns |  |
| $t_{RCH}$ | Read command hold time | 0 | – | 0 | – | 0 | – | ns | 11 |
| $t_{RRH}$ | Read command hold time referenced to $\overline{\text{RAS}}$ | 0 | – | 0 | – | 0 | – | ns | 11 |
| $t_{CLZ}$ | $\overline{\text{CAS}}$ to output in low-Z | 0 | – | 0 | – | 0 | – | ns | 8 |
| $t_{OFF}$ | Output buffer turn-off delay | 0 | 13 | 0 | 15 | 0 | 17 | ns | 12 |
| $t_{OEZ}$ | Output turn-off delay from $\overline{\text{OE}}$ | 0 | 13 | 0 | 15 | 0 | 17 | ns | 12 |
| $t_{DZC}$ | Data to $\overline{\text{CAS}}$ low delay | 0 | – | 0 | – | 0 | – | ns | 13 |
| $t_{DZO}$ | Data to $\overline{\text{OE}}$ low delay | 0 | – | 0 | – | 0 | – | ns | 13 |
| $t_{CDD}$ | $\overline{\text{CAS}}$ high to data delay | 10 | – | 13 | – | 15 | – | ns | 14 |
| $t_{ODD}$ | $\overline{\text{OE}}$ high to data delay | 10 | – | 13 | – | 15 | – | ns | 14 |

## *AC Characteristics*[5][6]

$T_A$ = 0 to 70 °C,$V_{CC}$ = 5 V ± 10 %, $t_T$ = 2 ns

| Symbol | Parameter | -50 | | -60 | | -70 | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | min. | max. | min. | max. | min. | max. | | |
| **Write Cycle** | | | | | | | | | |
| $t_{WCH}$ | Write command hold time | 8 | – | 10 | – | 10 | – | ns | |
| $t_{WP}$ | Write command pulse width | 8 | – | 10 | – | 10 | – | ns | |
| $t_{WCS}$ | Write command setup time | 0 | – | 0 | – | 0 | – | ns | 15 |
| $t_{RWL}$ | Write command to $\overline{\text{RAS}}$ lead time | 13 | – | 15 | – | 17 | – | ns | |
| $t_{CWL}$ | Write command to $\overline{\text{CAS}}$ lead time | 13 | – | 15 | – | 17 | – | ns | |
| $t_{DS}$ | Data setup time | 0 | – | 0 | – | 0 | – | ns | 16 |
| $t_{DH}$ | Data hold time | 8 | – | 10 | – | 12 | – | ns | 16 |
| **Read-modify-Write Cycle** | | | | | | | | | |
| $t_{RWC}$ | Read-write cycle time | 113 | – | 138 | – | 162 | – | ns | |
| $t_{RWD}$ | $\overline{\text{RAS}}$ to WE delay time | 64 | – | 77 | – | 89 | – | ns | 15 |
| $t_{CWD}$ | $\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time | 27 | – | 32 | – | 36 | – | ns | 15 |
| $t_{AWD}$ | Column address to $\overline{\text{WE}}$ delay time | 39 | – | 47 | – | 54 | – | ns | 15 |
| $t_{OEH}$ | $\overline{\text{OE}}$ command hold time | 10 | – | 13 | – | 15 | – | ns | |
| **EDO Page Mode Cycle** | | | | | | | | | |
| $t_{PC}$ | EDO page mode cycle time | 20 | – | 25 | – | 30 | – | ns | |
| $t_{CP}$ | $\overline{\text{CAS}}$ precharge time | 8 | – | 10 | – | 10 | – | ns | |
| $t_{CPA}$ | Access time from $\overline{\text{CAS}}$ precharge | – | 27 | – | 32 | – | 37 | ns | 7 |
| $t_{COH}$ | Output data hold time | 5 | – | 5 | – | 5 | – | ns | |
| $t_{RAS}$ | $\overline{\text{RAS}}$ pulse width in EDO mode | 50 | 200k | 60 | 200k | 70 | 200k | ns | |
| $t_{RHPC}$ | $\overline{\text{CAS}}$ precharge to $\overline{\text{RAS}}$ Delay | 27 | – | 32 | – | 37 | – | ns | |
| **EDO Page Mode Read-modify-Write Cycle** | | | | | | | | | |
| $t_{PRWC}$ | EDO page mode read-write cycle time | 58 | – | 68 | – | 77 | – | ns | |
| $t_{CPWD}$ | $\overline{\text{CAS}}$ precharge to $\overline{\text{WE}}$ | 41 | – | 49 | – | 56 | – | ns | |
| **$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh Cycle** | | | | | | | | | |
| $t_{CSR}$ | $\overline{\text{CAS}}$ setup time | 10 | – | 10 | – | 10 | – | ns | |
| $t_{CHR}$ | $\overline{\text{CAS}}$ hold time | 10 | – | 10 | – | 10 | – | ns | |
| $t_{RPC}$ | $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time | 5 | – | 5 | – | 5 | – | ns | |
| $t_{WRP}$ | Write to $\overline{\text{RAS}}$ precharge time | 10 | – | 10 | – | 10 | – | ns | |
| $t_{WRH}$ | Write hold time referenced to $\overline{\text{RAS}}$ | 10 | – | 10 | – | 10 | – | ns | |

## *AC Characteristics*[5)6)]

$T_A$ = 0 to 70 °C, $V_{CC}$ = 5 V ± 10 %, $t_T$ = 2 ns

| Symbol | Parameter | -50 | | -60 | | -70 | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | min. | max. | min. | max. | min. | max. | | |
| **$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Counter Test Cycle** | | | | | | | | | |
| $t_{CPT}$ | $\overline{\text{CAS}}$ precharge time | 35 | – | 40 | – | 40 | – | ns | |
| **Self Refresh Cycle** | | | | | | | | | |
| $t_{RASS}$ | $\overline{\text{RAS}}$ pulse width | 100k | – | 100k | – | 100k | – | ns | 17 |
| $t_{RPS}$ | $\overline{\text{RAS}}$ precharge | 95 | – | 110 | – | 130 | – | ns | 17 |
| $t_{CHS}$ | $\overline{\text{CAS}}$ hold time | -50 | – | -50 | – | -50 | – | ns | 17 |
| **Test Mode** | | | | | | | | | |
| $t_{WTS}$ | Write command setup time | 10 | – | 10 | – | 10 | – | ns | |
| $t_{WTH}$ | Write command hold time | 10 | – | 10 | – | 10 | – | ns | |
| $t_{CHRT}$ | $\overline{\text{CAS}}$ hold time | 30 | – | 30 | – | 30 | – | ns | |

### *Notes:*

1) All voltages are referenced to $V_{SS}$.
2) $I_{CC1}$, $I_{CC3}$, $I_{CC4}$ and $I_{CC6}$ depend on cycle rate.
3) $I_{CC1}$ and $I_{CC4}$ depend on output loading. Specified values are obtained with the output open.
4) Address can be changed once or less while RAS = Vil. In case of ICC4 it can be changed once or less during a EDO page mode cycle
5) An initial pause of 200 ms is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using the internal refresh counter, a minimum of 8 $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ initialization cycles instead of 8 $\overline{\text{RAS}}$ cycles are required.
6) AC measurements assume $t_T$ = 2 ns.
7) $V_{IH\,(min.)}$ and $V_{IL\,(max.)}$ are reference levels for measuring timing of input signals. Transition times are also measured between $V_{IH}$ and $V_{IL}$.
8) Measured with the specified current load and 100 pF at Vol = 0.8 V and Voh = 2.0 V. Access time is determined by the latter of $t_{RAC}$, $t_{CAC}$, $t_{CAA}$, $t_{CPA}$, $t_{OEA}$ . $t_{CAC}$ is measured from tristate.
9) Operation within the $t_{RCD\,(max.)}$ limit ensures that $t_{RAC\,(max.)}$ can be met. $t_{RCD\,(max.)}$ is specified as a reference point only. If $t_{RCD}$ is greater than the specified $t_{RCD\,(max.)}$ limit, then access time is controlled by $t_{CAC}$.
10) Operation within the $t_{RAD\,(max.)}$ limit ensures that $t_{RAC\,(max.)}$ can be met. $t_{RAD\,(max.)}$ is specified as a reference point only. If $t_{RAD}$ is greater than the specified $t_{RAD\,(max.)}$ limit, then access time is controlled by $t_{CAA}$.
11) Either $t_{RCH}$ or $t_{RRH}$ must be satisfied for a read cycle.
12) $t_{OFF\,(max.)}$, $t_{OEZ\,(max.)}$ define the time at which the output achieves the open-circuit conditions and are not referenced to output voltage levels. $t_{OFF}$ is referenced from the rising edge of $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$, whichever occurs last.

13) Either $t_{DZC}$ or $t_{DZO}$ must be satisfied.

14) Either $t_{CDD}$ or $t_{ODD}$ must be satisfied.

15) $t_{WCS}$, $t_{RWD}$, $t_{CWD}$ and $t_{AWD}$ are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS\ (min.)}$, the cycle is an early write cycle and data out pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} > t_{RWD\ (min.)}$, $t_{CWD} > t_{CWD\ (min.)}$ and $t_{AWD} > t_{AWD\ (min.)}$, the cycle is a read-write cycle and I/O will contain data read from the selected cells. If neither of the above sets of condition is satisfied, the condition of I/O (at access time) is indeterminate.

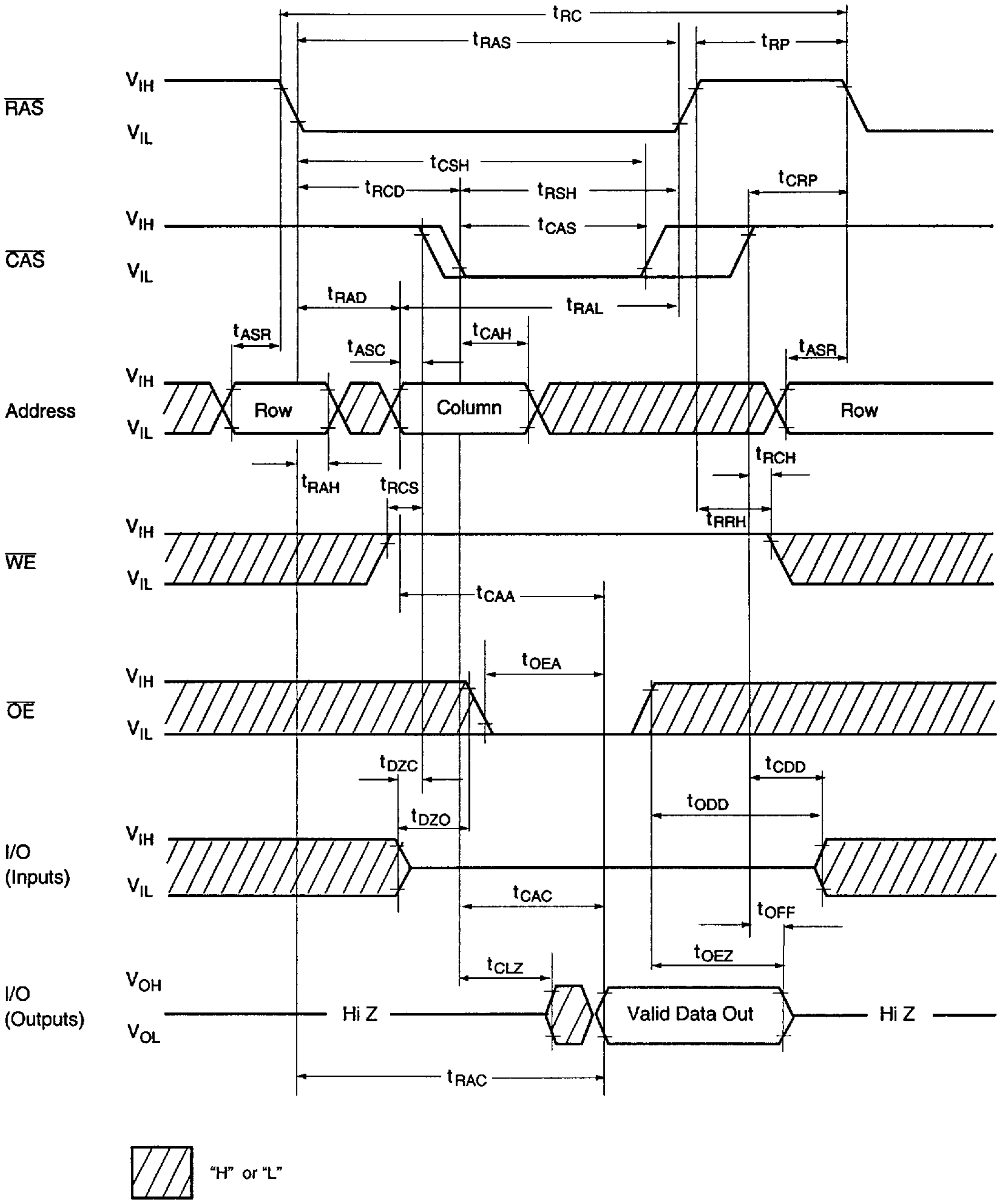
16) These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.

17) When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:

    If row addresses are being refreshed on an evenly distributed manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh.

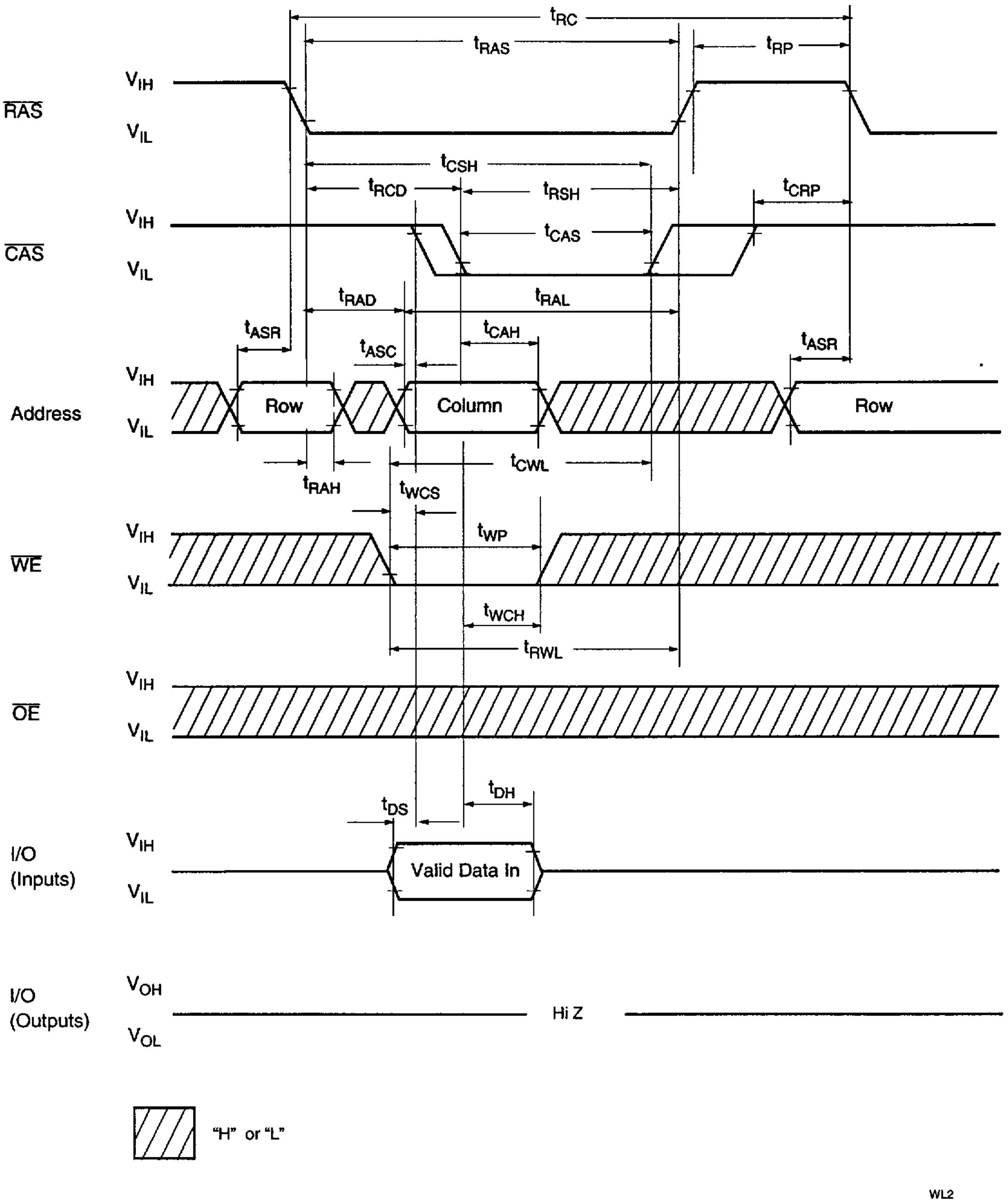
    If row addresses are being refreshed in any other manner (ROR - Distributed/Burst; or CBR-Burst) over the refresh interval, then a full set of row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh

## *Waveforms of Read Cycle*

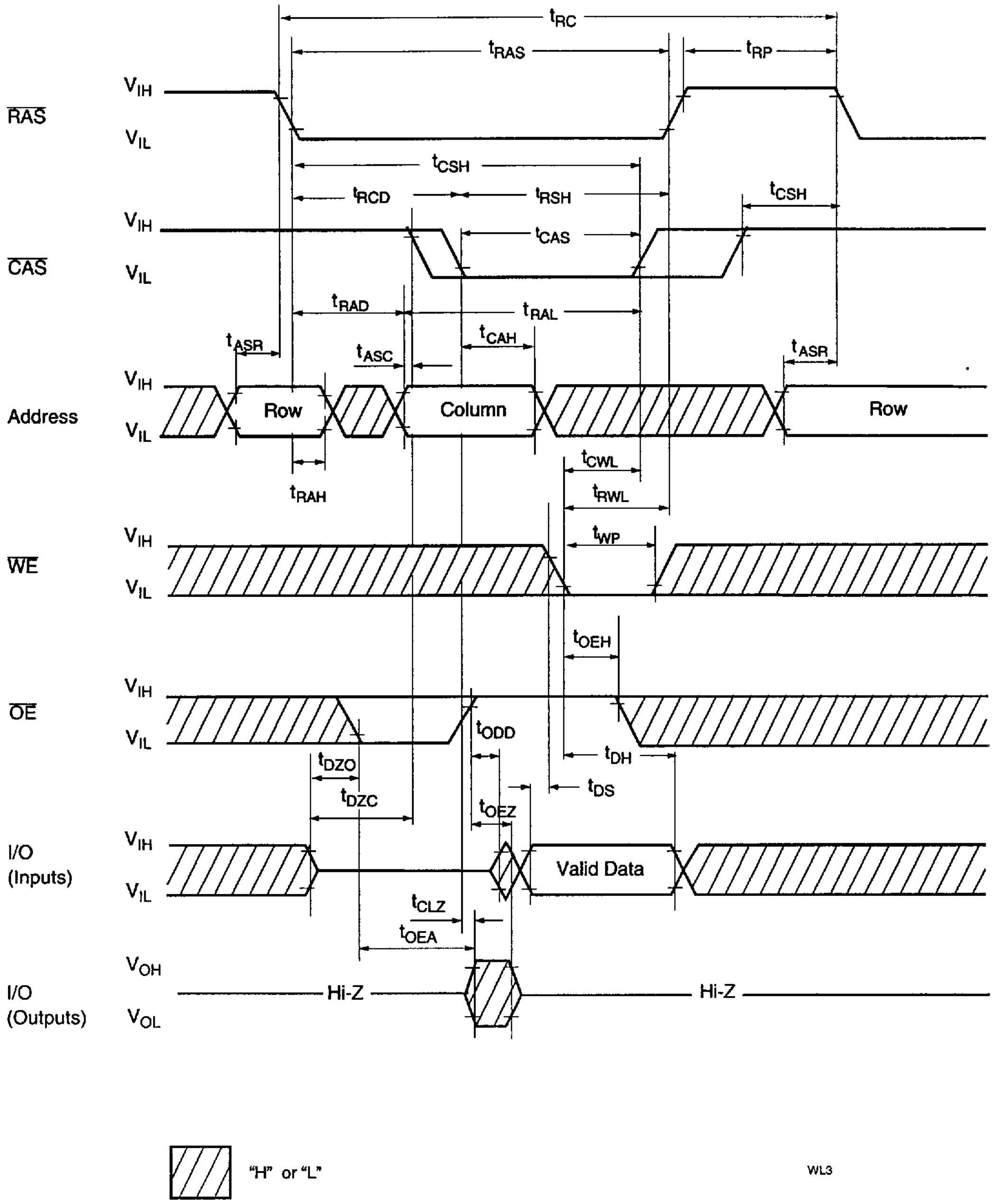


WL1

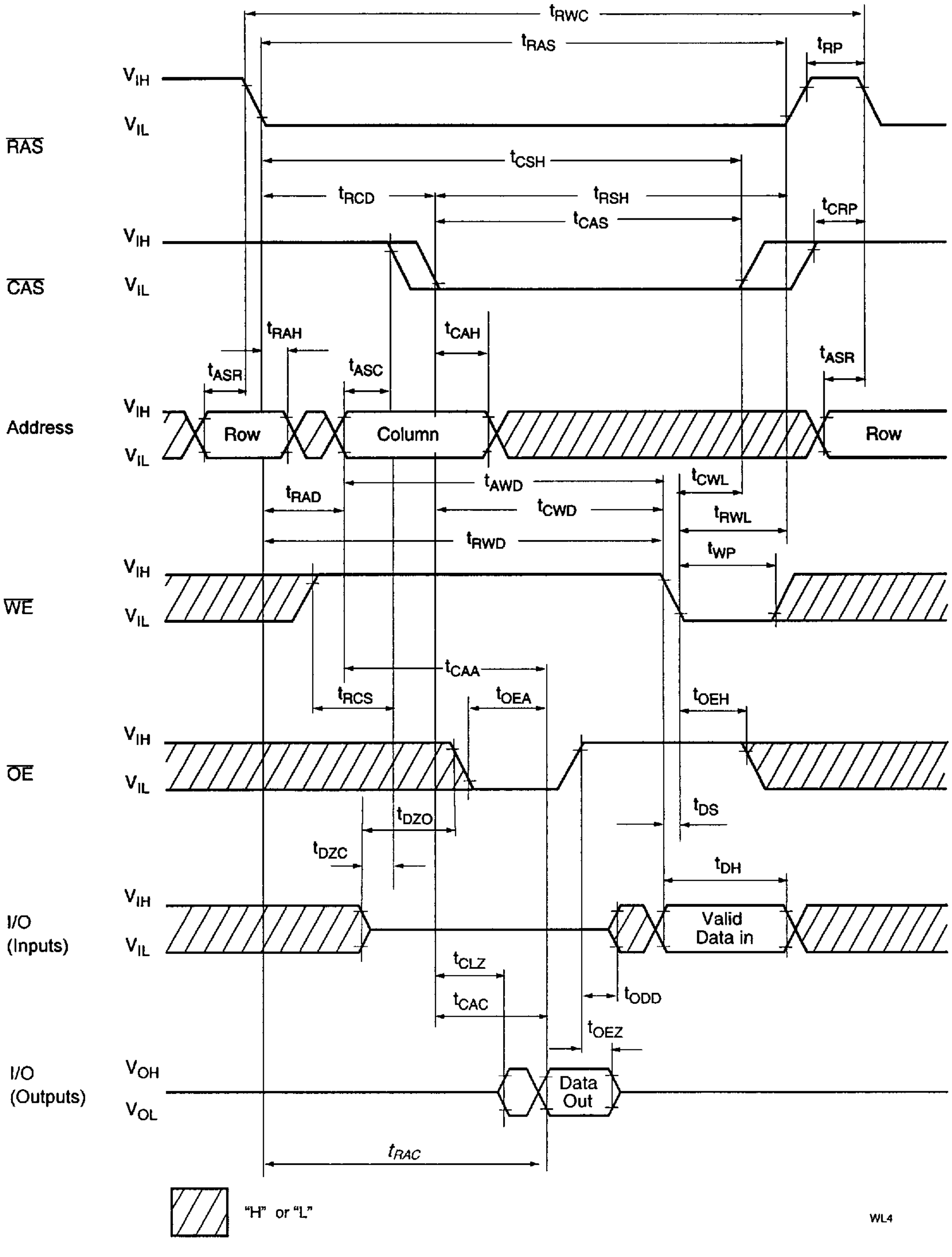
## *Waveforms of Write Cycle (Early Write)*



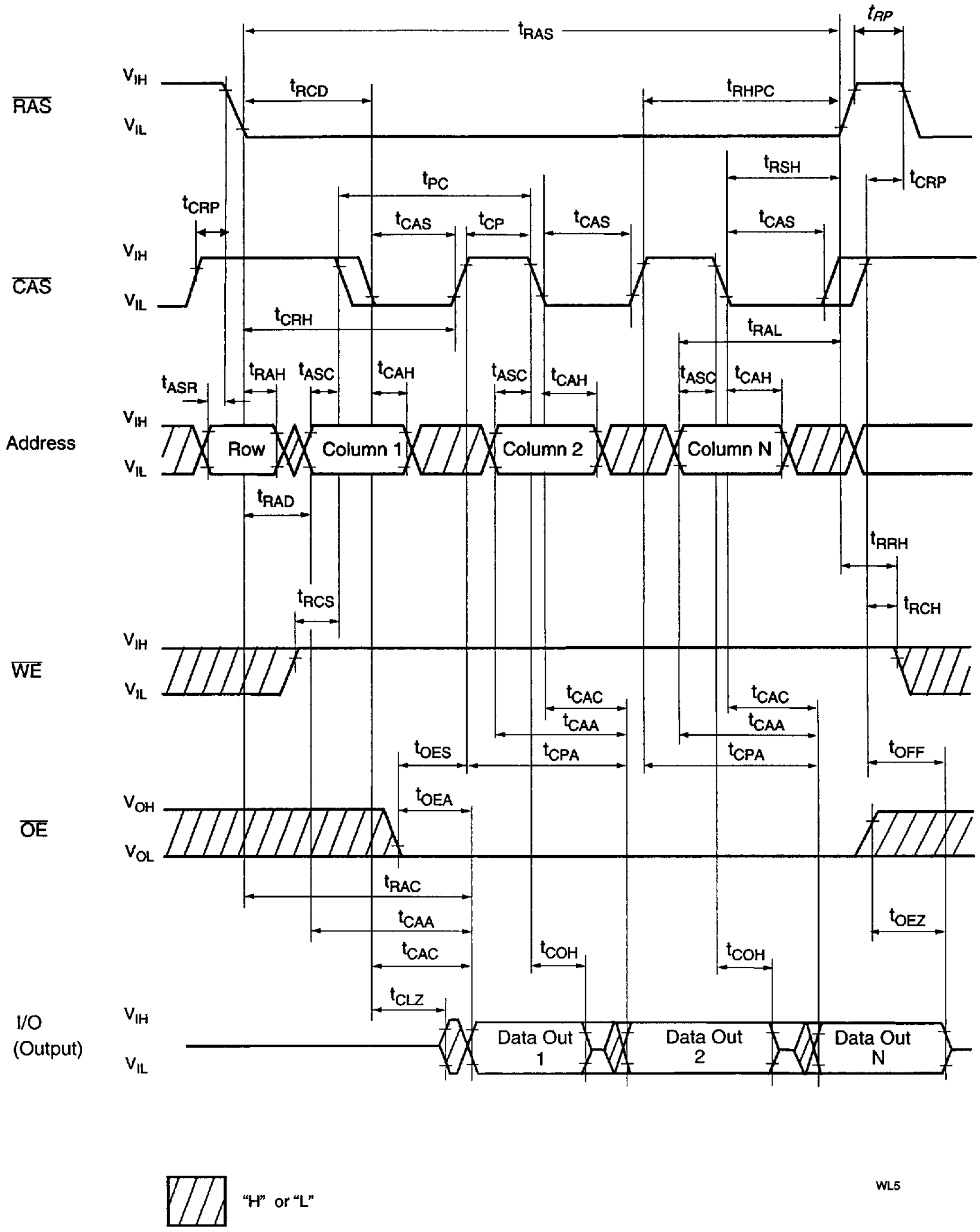
## *Waveforms of Write Cycle ($\overline{\text{OE}}$ Controlled Write)*



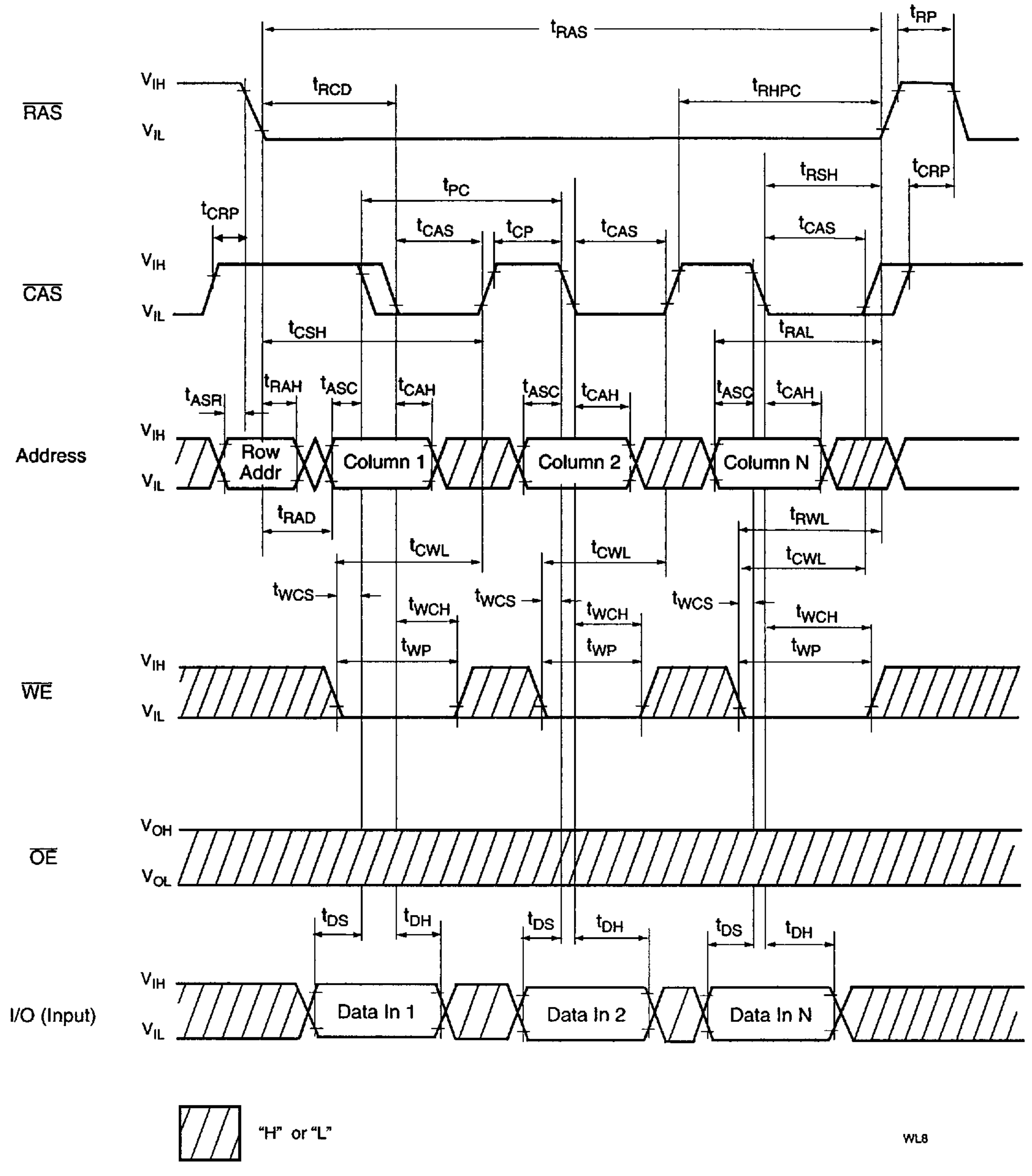
## *Waveforms of Read-Write (Read-Modify-Write) Cycle*



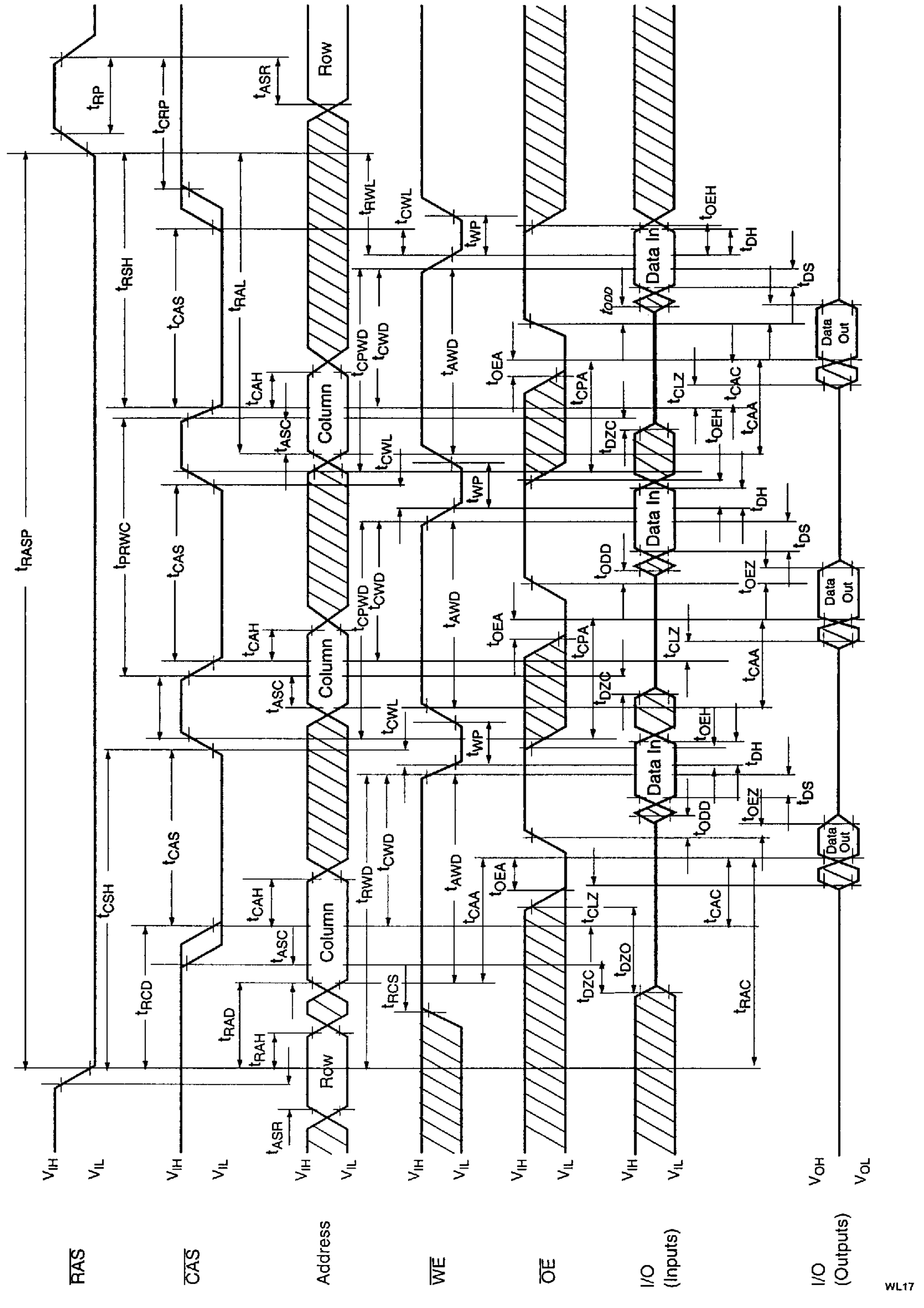
## *Waveforms of EDO Page Mode Read Cycle*



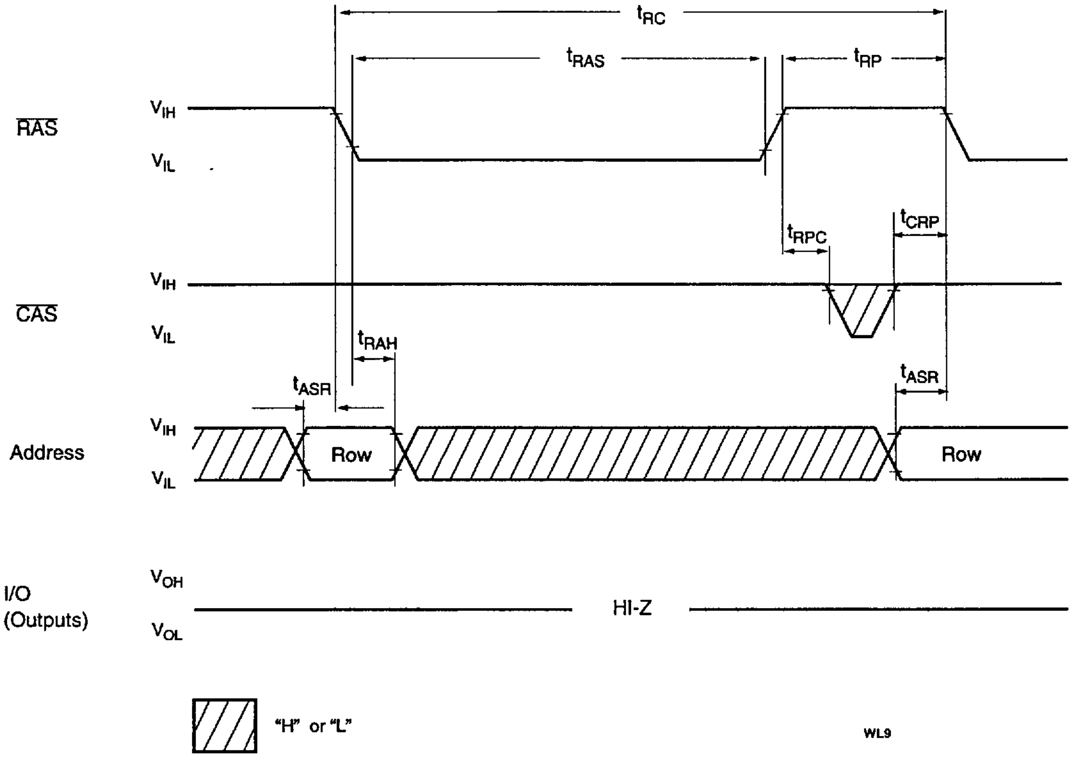
## *Waveforms of EDO Page Mode Early Write Cycle*



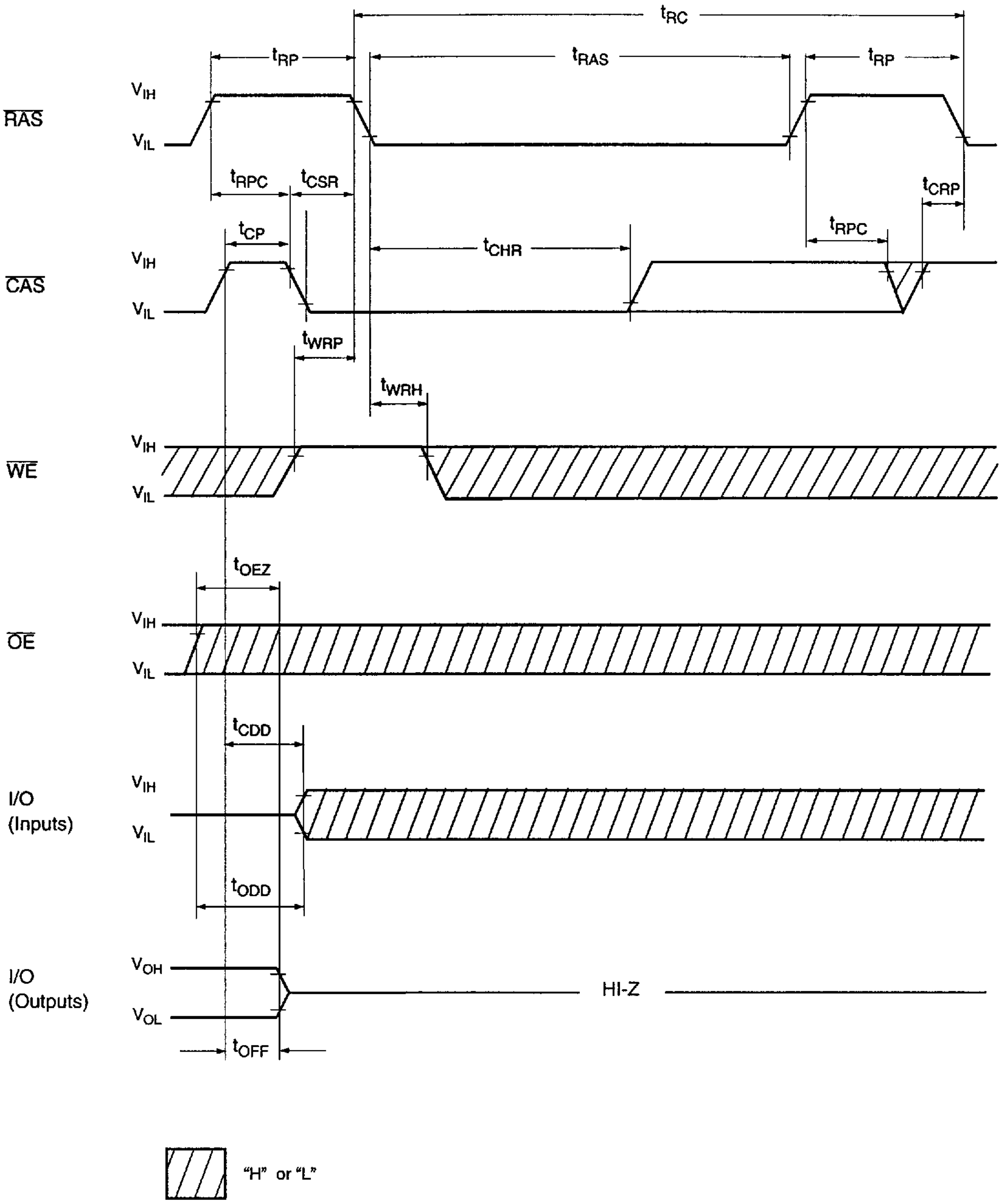
### *Waveforms of EDO Page Mode Late Write and Read-Modify-Write Cycle*



## *Waveforms of $\overline{RAS}$ Only Refresh Cycle*

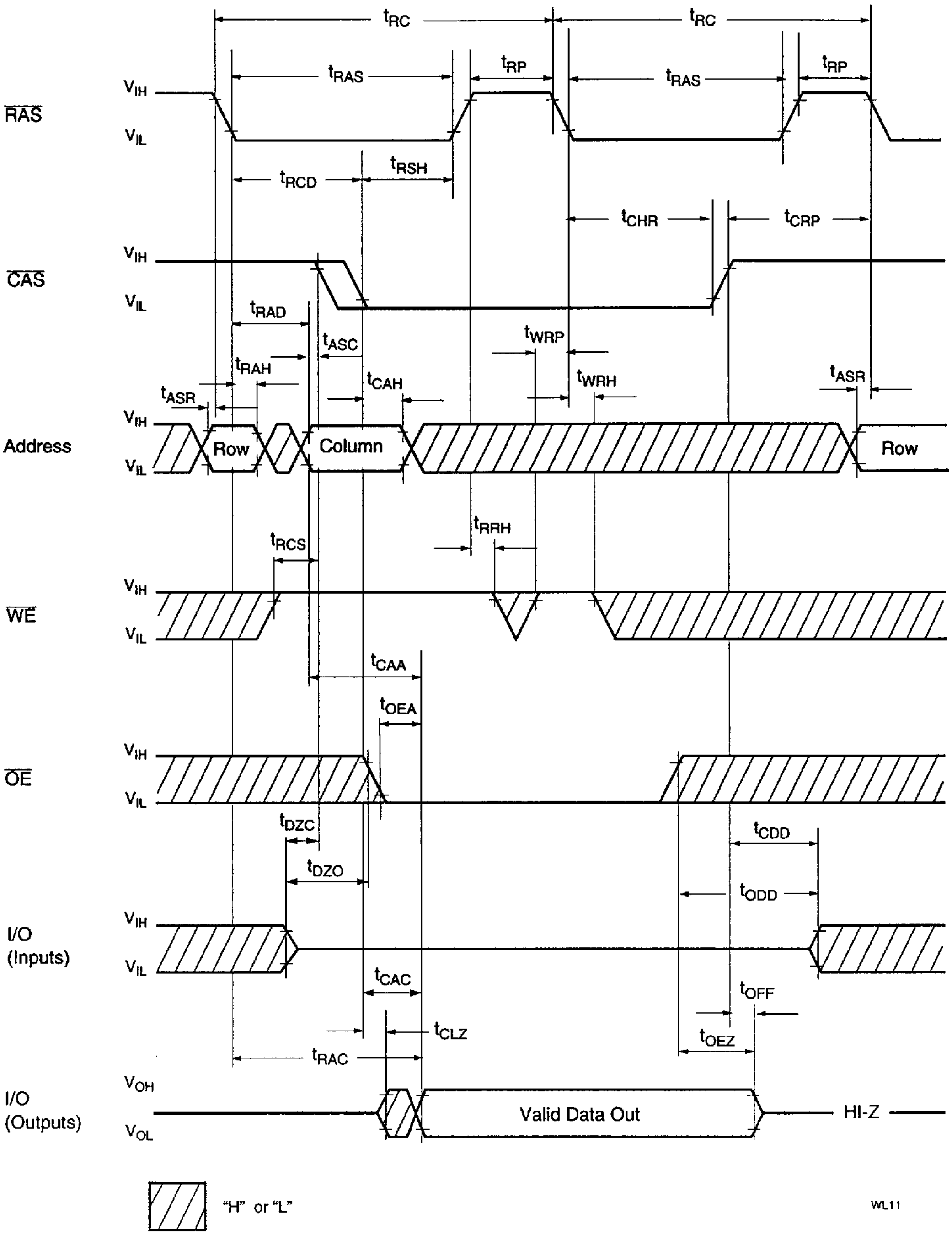


## *Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle*

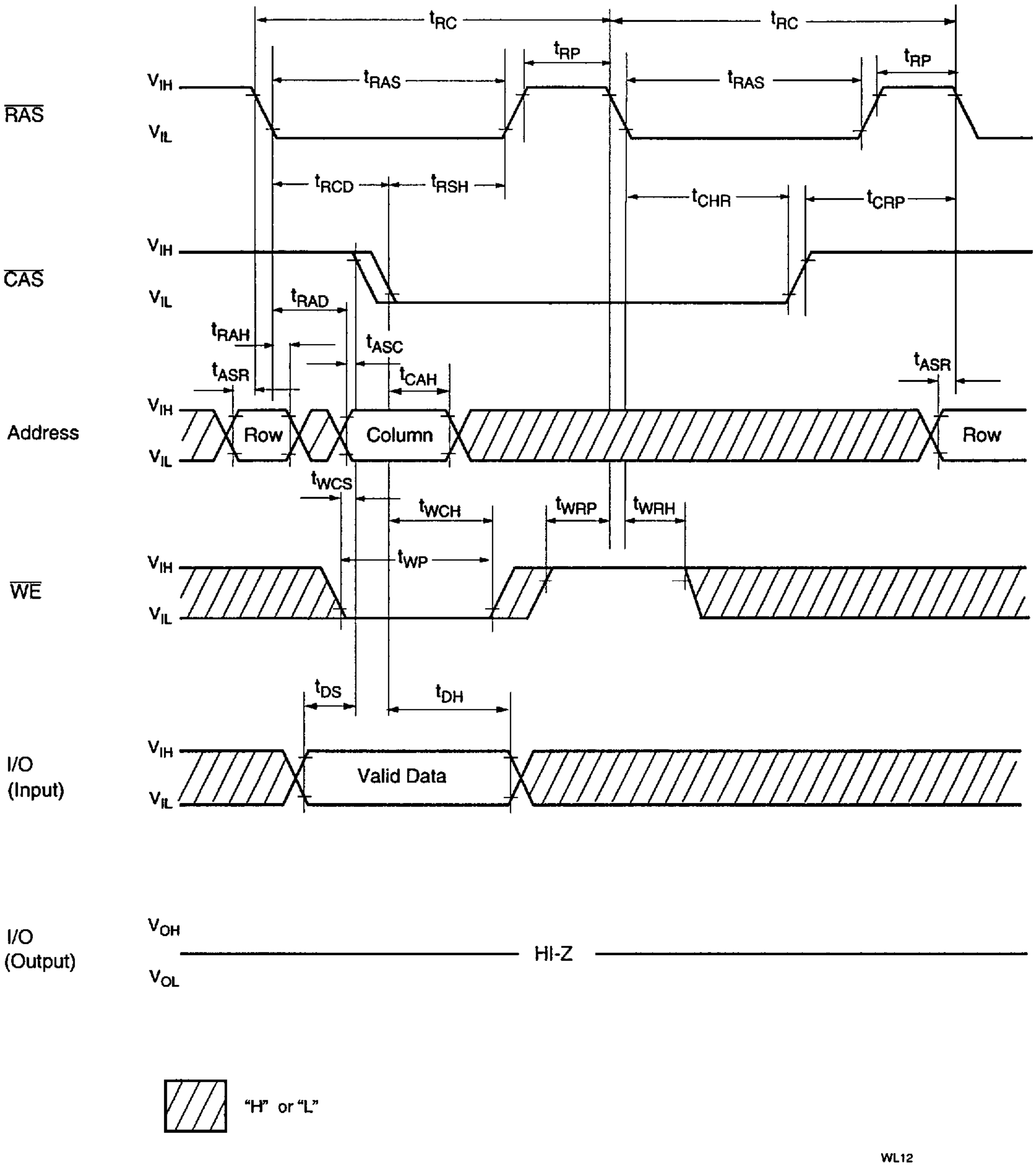


WL10

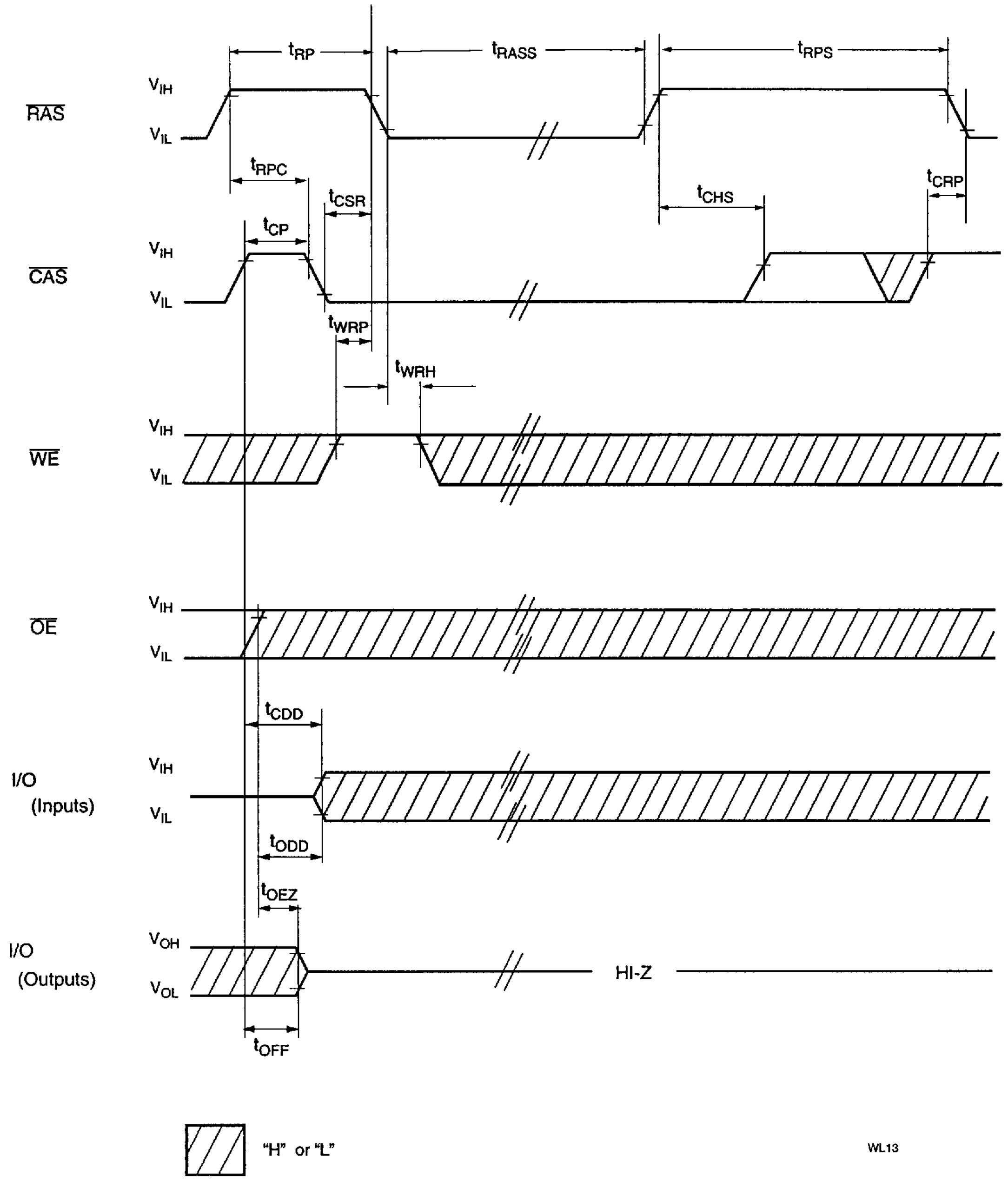
## *Waveforms of Hidden Refresh Read Cycle*



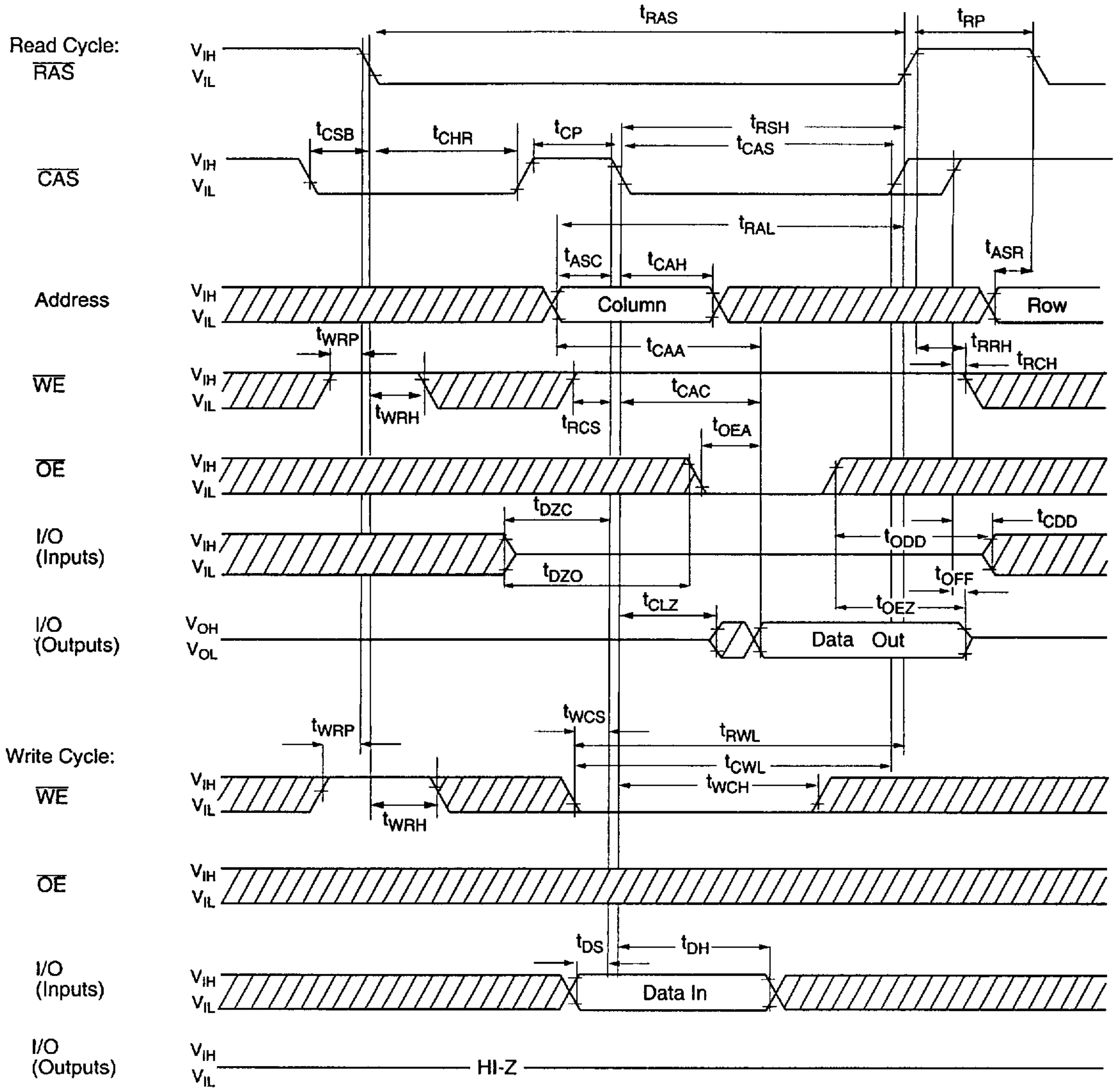
## *Waveforms of Hidden Refresh Early Write Cycle*



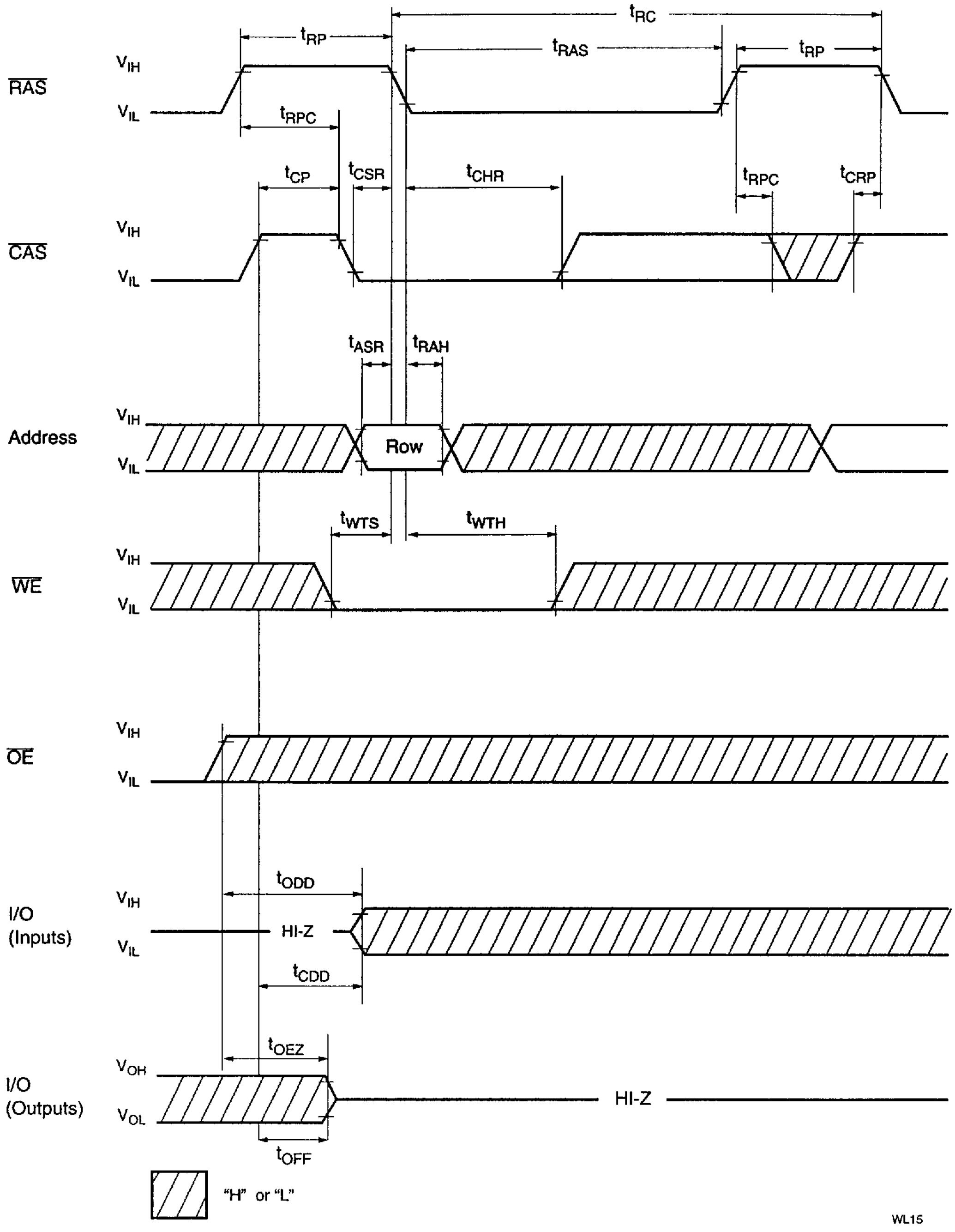
## *Waveforms of $\overline{CAS}$ before $\overline{RAS}$ Self Refresh Cycle*



## *Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle*



## *Waveforms of Test Mode Entry*



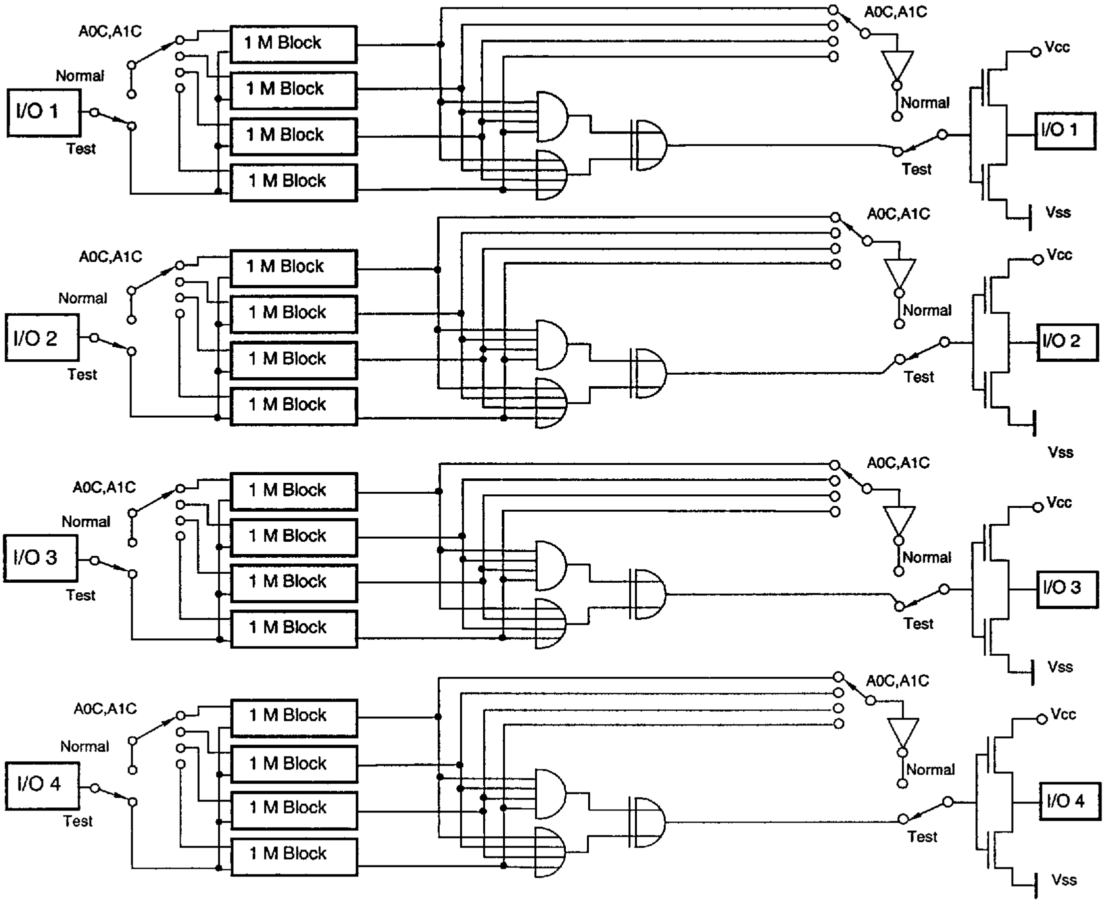
### *Test Mode*

As the V53C511740500 is organized internally as 1M x 16-bits, a test mode cycle using 4:1 compression can be used to improve test time. Note that in the 4M x 4 version the test time is reduced by 1/4 for a N test pattern.

In a test mode "write" the data from each I/O pin is written into four 1M blocks simultaneously (all "1" s or all "0" s). In test mode "read" each I/O output is used for indicating the test mode result. If the internal four bits are equal, the I/O would indicate a "1". If they were not equal, the I/O would indicate a "0". The WCBR cycle ($\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$) puts the device into test mode. To exit from test mode, a "$\overline{CAS}$ before $\overline{RAS}$ refresh", "$\overline{RAS}$ only refresh" or "Hidden refresh" can be used.Refresh during test mode operation can be performed by normal read cycles or by WCBR refresh cycles.

Row addresses A0 through A9 have to kept high to perform a testmode entry cycle. All other addresses are don't care.

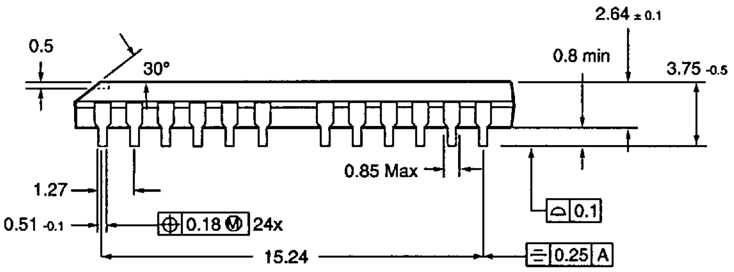
### *Block Diagram in Test Mode*

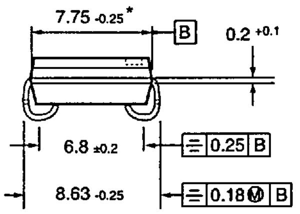


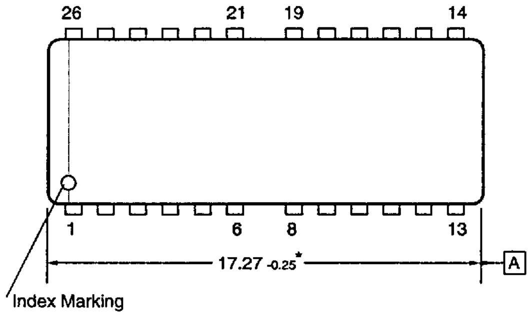
## *Package Diagrams*

### *24/26-pin 400 mil SOJ*

**Units in mm**



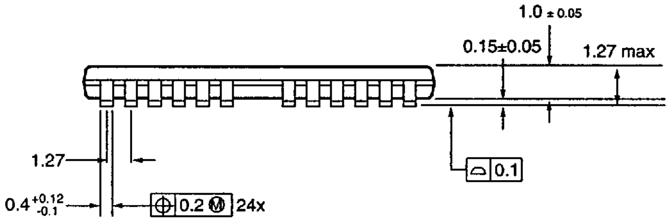


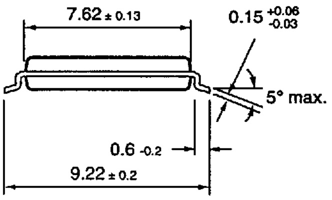


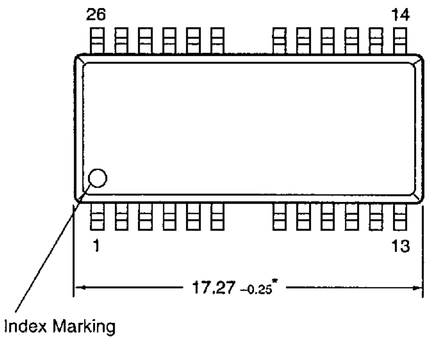
* Does not include plastic or metal protrusion of 0.15 max. per side

### *24/26-pin 400 mil TSOP-II*

**Units in mm**







* Does not include plastic or metal protrusion of 0.15 max. per side