MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

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1, 2, 4M x 64
5 V, EDO, Unbuffered

DRAM Dual-In-Line Memory Module (DIMM)
8, 16, and 32 Megabyte

- JEDEC–Standard 168–Lead Dual–In–Line Memory Module (DIMM)
- Single 5 V Power Supply, TTL–Compatible Inputs and Outputs
- Extended Data Out (EDO)
- $\overline{\text{RAS}}$–Only Refresh, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh, Hidden Refresh
- 8MB/16MB: 1024 Cycle Refresh: 16 ms (Max)
- 32MB: 2048 Cycle Refresh: 32 ms (Max)
- Keys Prevent Accidental Insertion into 3.3 V Systems
- Serial Presence Detect (SPD) Provides Module Configuration Information

PART NUMBERS (See Page 31 of Data Sheet for Definitions)

Organization	60	70
1M x 64	MB641BT08TADG60	MB641BT08TADG70
2M x 64	MB642BT08TADG60	MB642BT08TADG70
4M x 64	MB644CT00TADG60	MB644CT00TADG70

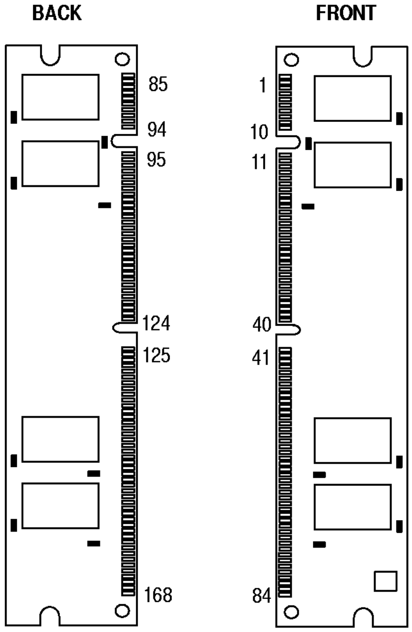
KEY TIMING PARAMETERS

Speed	t_{RC} (ns)	t_{RAC} (ns)	t_{CAC} (ns)	t_{AA} (ns)	t_{EPC} (ns)
60	104	60	17	30	25
70	124	70	20	35	30

ADDITIONAL PARAMETERS

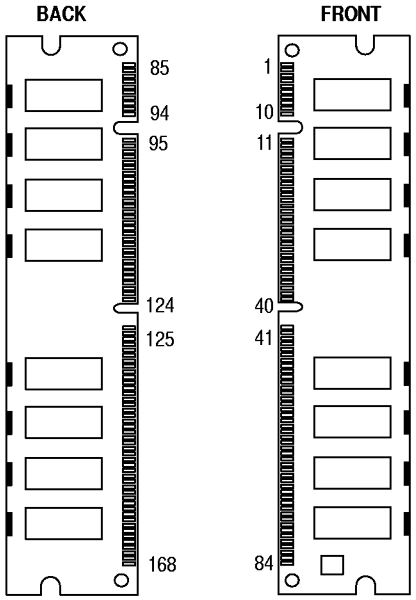
Configuration	Speed	Active Power Dissipation (mW) (Max)	Standby Power Dissipation (mW) (Max)	
			TTL	CMOS
8MB	60	4,070	44	22
	70	3,410		
16MB	60	4,114	88	44
	70	3,454		
32MB	60	9,680	176	88
	70	8,360		

**1M x 64 (8MB), 2M x 64 (16MB)
168–LEAD DIMM
CASE 1115A–01**



BACK NOT POPULATED ON 1M X 64 (8MB)

**4M x 64 (32MB)
168–LEAD DIMM
CASE 1115–01**



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PIN ASSIGNMENTS

Front Side								Back Side							
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	22	NC	43	V_{SS}	64	V_{SS}	85	V_{SS}	106	NC	127	V_{SS}	148	V_{SS}
2	DQ0	23	V_{SS}	44	$\overline{\mathrm{G2}}$	65	DQ21	86	DQ32	107	V_{SS}	128	NC	149	DQ53
3	DQ1	24	NC	45	$\overline{\mathrm{RAS2}}$	66	DQ22	87	DQ33	108	NC	129	$\overline{\mathrm{RAS3}}$*	150	DQ54
4	DQ2	25	NC	46	$\overline{\mathrm{CAS2}}$	67	DQ23	88	DQ34	109	NC	130	$\overline{\mathrm{CAS6}}$	151	DQ55
5	DQ3	26	V_{CC}	47	$\overline{\mathrm{CAS3}}$	68	V_{SS}	89	DQ35	110	V_{CC}	131	$\overline{\mathrm{CAS7}}$	152	V_{SS}
6	V_{CC}	27	$\overline{\mathrm{WE0}}$	48	$\overline{\mathrm{WE2}}$	69	DQ24	90	V_{CC}	111	NC	132	NC	153	DQ56
7	DQ4	28	$\overline{\mathrm{CAS0}}$	49	V_{CC}	70	DQ25	91	DQ36	112	$\overline{\mathrm{CAS4}}$	133	V_{CC}	154	DQ57
8	DQ5	29	$\overline{\mathrm{CAS1}}$	50	NC	71	DQ26	92	DQ37	113	$\overline{\mathrm{CAS5}}$	134	NC	155	DQ58
9	DQ6	30	$\overline{\mathrm{RAS0}}$	51	NC	72	DQ27	93	DQ38	114	$\overline{\mathrm{RAS1}}$*	135	NC	156	DQ59
10	DQ7	31	$\overline{\mathrm{G0}}$	52	NC	73	V_{CC}	94	DQ39	115	NC	136	NC	157	V_{CC}
11	DQ8	32	V_{SS}	53	NC	74	DQ28	95	DC40	116	V_{SS}	137	NC	158	DQ60
12	V_{SS}	33	A0	54	V_{SS}	75	DQ29	96	V_{SS}	117	A1	138	V_{SS}	159	DQ61
13	DQ9	34	A2	55	DQ16	76	DQ30	97	DQ41	118	A3	139	DQ48	160	DQ62
14	DQ10	35	A4	56	DQ17	77	DQ31	98	DQ42	119	A5	140	DQ49	161	DQ63
15	DQ11	36	A6	57	DQ18	78	V_{SS}	99	DQ43	120	A7	141	DQ50	162	V_{SS}
16	DQ12	37	A8	58	DQ19	79	NC	100	DQ44	121	A9	142	DQ51	163	NC
17	DQ13	38	A10**	59	V_{CC}	80	NC	101	DQ45	122	NC	143	V_{CC}	164	NC
18	V_{CC}	39	NC	60	DQ20	81	NC	102	V_{CC}	123	NC	144	DQ52	165	SA0
19	DQ14	40	V_{CC}	61	NC	82	SDA	103	DQ46	124	V_{CC}	145	NC	166	SA1
20	DQ15	41	V_{CC}	62	NC	83	SCL	104	DQ47	125	NC	146	NC	167	SA2
21	NC	42	NC	63	NC	84	V_{CC}	105	NC	126	NC	147	NC	168	V_{CC}

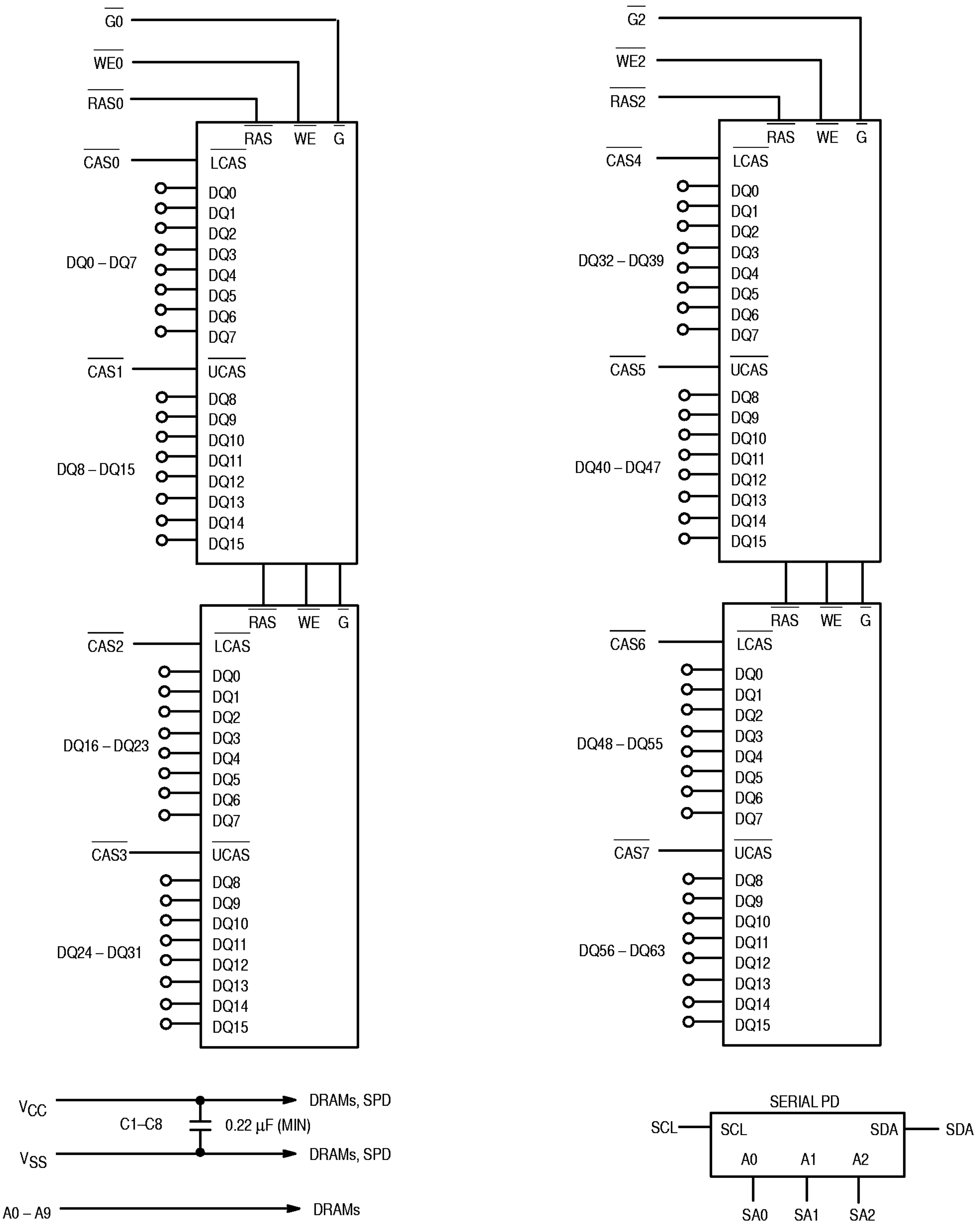
* NC on the 8MB and 32MB.

** NC on the 8MB and 16MB.

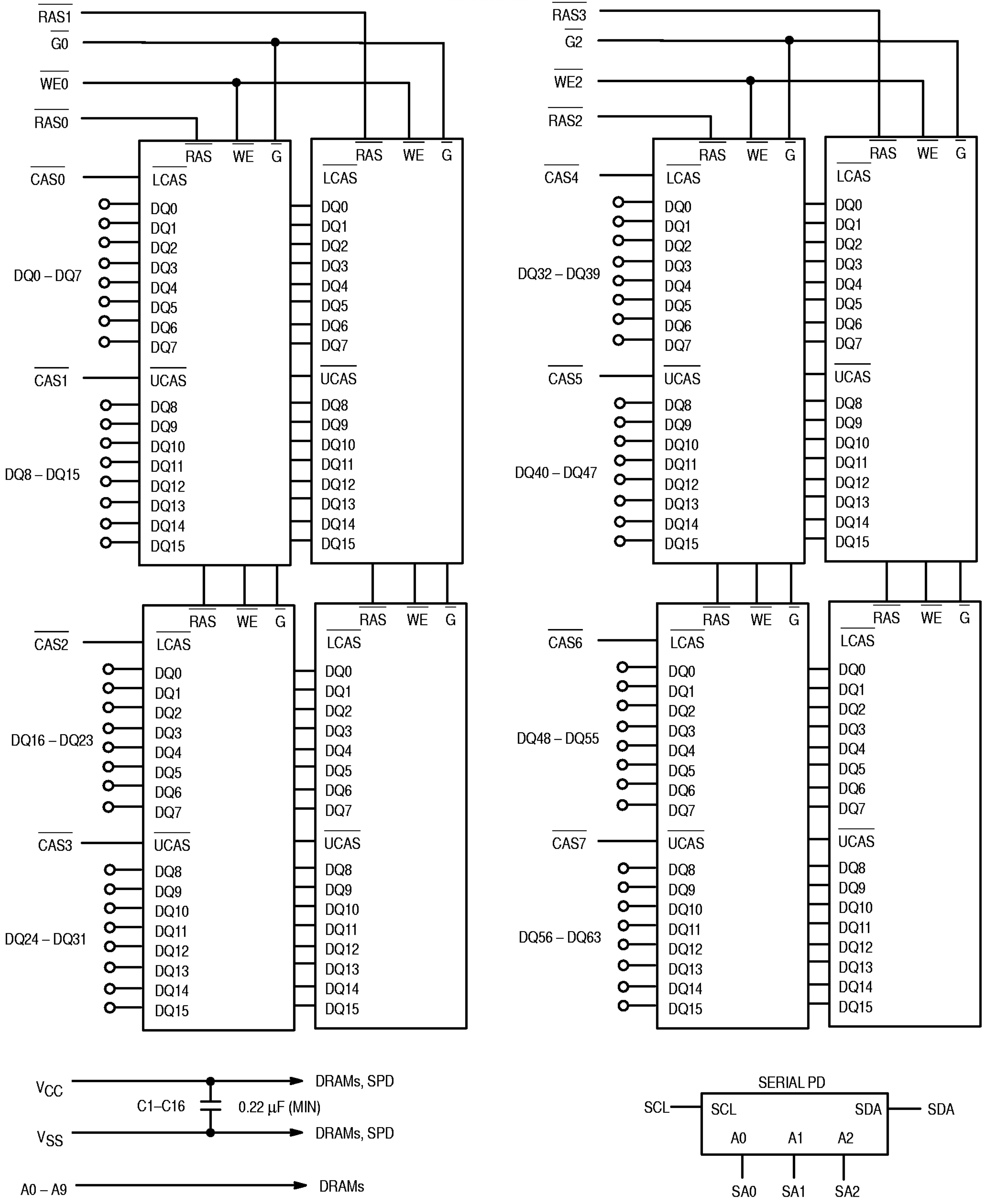
PIN NAMES			
A0 – A10	Address Inputs	DQ0 – DQ63	Data Input/Output
$\overline{\mathrm{CAS0}}$ – $\overline{\mathrm{CAS7}}$	Column Address Strobe	$\overline{\mathrm{RAS0}}$ – $\overline{\mathrm{RAS3}}$	Row Address Strobe
$\overline{\mathrm{WE0}}$, $\overline{\mathrm{WE2}}$	Write Enable	$\overline{\mathrm{G0}}$, $\overline{\mathrm{G2}}$	Output Enable
SA0 – SA2	SPD Address	SCL	SPD Clock
SDA	SPD Data I/O	V_{CC}	Power
V_{SS}	Ground	NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

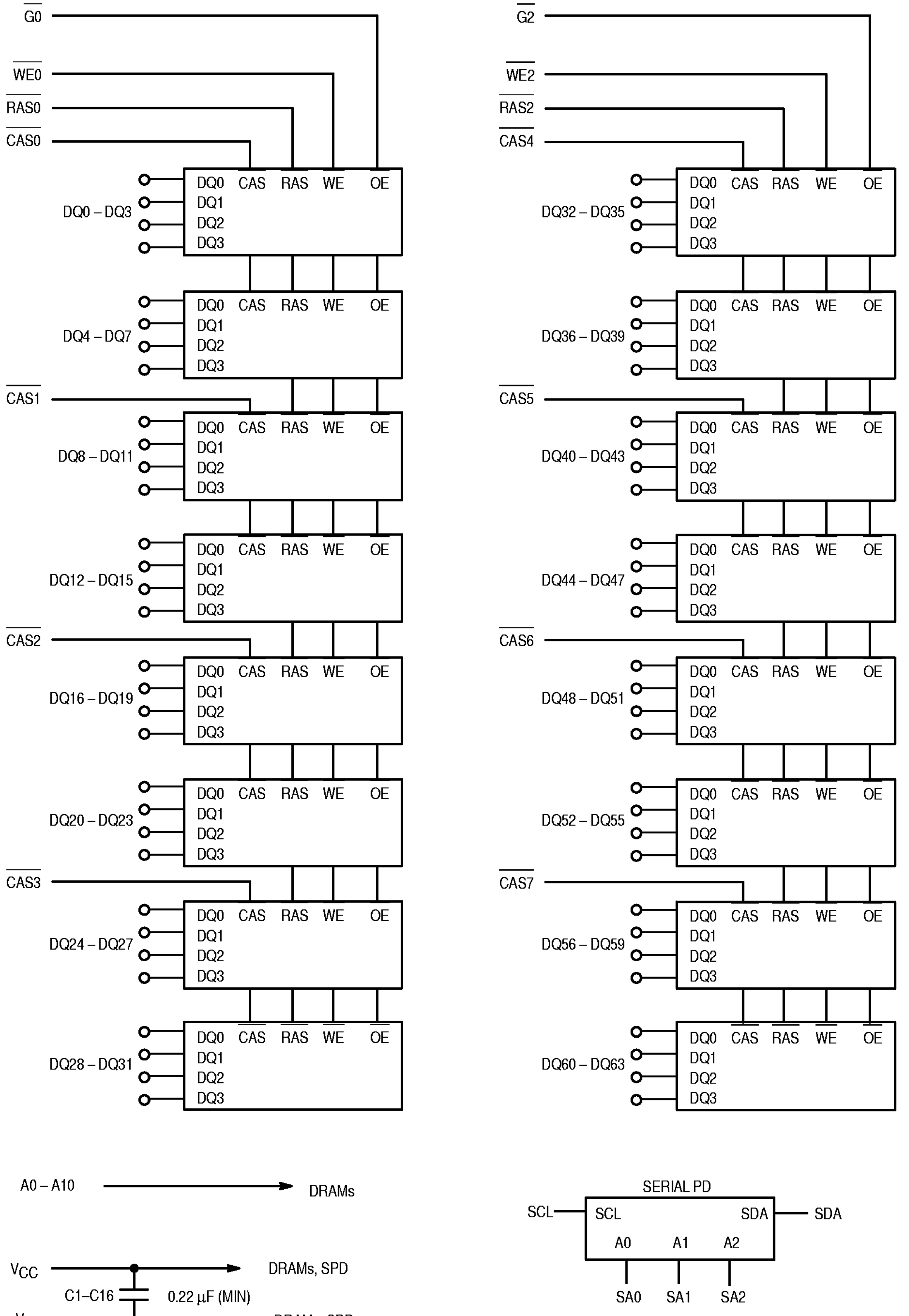
8MB BLOCK DIAGRAM



16MB BLOCK DIAGRAM



32MB BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7	V
Voltage Relative to V_{SS} (For Any Pin Except V_{CC})	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
SPD Pins	V_{in}, V_{out}	– 0.3 to 6.5	V
Data Output Current per DQ Pin	I_{out}	50	mA
Power Dissipation 8MB 16MB 32MB	P_D	5.2 10.4 14.4	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ± 10% V, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All Voltages Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	4	—	V_{CC} + 0.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 0.3*	—	0.8	V
SPD Pins	V_{IL}	– 0.3	—	V_{CC} + 0.3	V
SPD Pins	V_{IH}	V_{CC} x 0.7	—	V_{CC} + 0.5	V
SPD (I_{VOL} = 2.1 mA)	V_{OL}	—	—	0.4	V
Input Leakage Current ($V_{SS} \leq V_{in} \leq V_{CC}$)	$I_{lkg(I)}$	– 160	—	160	µA
Output Leakage Current (CAS at Logic 1, $V_{SS} \leq V_{out} \leq V_{CC}$)	$I_{lkg(O)}$	– 20	—	20	µA
Output High Voltage (I_{OH} = – 2 mA)	V_{OH}	2.4	—	—	V
Output Low Voltage (I_{OL} = 2 mA)	V_{OL}	—	—	0.4	V

* – 2.0 V at pulse widths ≤ 20 ns.

DC CHARACTERISTICS AND SUPPLY CURRENTS (All Voltages Referenced to V_{SS})

Characteristic		Symbol	8MB		16MB		32MB		Unit	Notes
			Min	Max	Min	Max	Min	Max		
V_{CC} Power Supply Current ($t_{RC} = t_{RC}$ MIN)	60 70	I_{CC1}	— —	740 620	— —	748 628	— —	1760 1520	mA	1, 2
V_{CC} Power Supply Current (Standby) (RAS = CAS = V_{IH})		I_{CC2}	—	8	—	16	—	32	mA	
V_{CC} Power Supply Current ($t_{RC} = t_{RC}$ MIN)	60 70	I_{CC3}	— —	740 620	— —	748 628	— —	1760 1520	mA	1, 2
V_{CC} Power Supply Current ($t_{EPC} = t_{EPC}$ MIN) During EDO Cycle	60 70	I_{CC4}	— —	480 440	— —	488 448	— —	1120 960	mA	1, 2
V_{CC} Power Supply Current (Standby) (RAS = CAS = V_{CC} – 0.2 V)		I_{CC5}	—	4	—	8	—	16	mA	
V_{CC} Power Supply Current ($t_{RC} = t_{RC}$ MIN) During CAS Before RAS Refresh Cycle	60 70	I_{CC6}	— —	740 620	— —	748 628	— —	1760 1520	mA	1

NOTES:
1. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
2. Column address can be changed once or less while RAS = V_{IL} and CAS = V_{IH}.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Input Capacitance	Symbol	8MB Max	16MB Max	32MB Max	Unit
Addresses	C_{in}	30	50	90	pF
WE, G	C_{in}	24	38	66	pF
RAS	C_{in}	24	24	66	pF
CAS	C_{in}	17	24	24	pF
SPD	C_{in}	18	18	18	pF
DQ	C_{out}	17	24	17	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\,\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

ALL DEVICES: READ, WRITE, AND READ–WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		60		70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	104	—	124	—	ns	5
Read–Write Cycle Time	t_{RELREL}	t_{RWC}	135	—	157	—	ns	5
Access Time from RAS	t_{RELQV}	t_{RAC}	—	60	—	70	ns	6, 7, 8, 9
Access Time from CAS	t_{CELQV}	t_{CAC}	—	17	—	20	ns	6, 8, 10
Access Time from Column Address	t_{AVQV}	t_{AA}	—	30	—	35	ns	6, 9, 11
Access Time from Precharge CAS	t_{CEHQV}	t_{CPA}	—	35	—	40	ns	6
CAS to Output in Low–Z	t_{CELQX}	t_{CLZ}	0	—	0	—	ns	
Output Buffer and Turn–Off Delay	t_{CEHQZ}	t_{OFF}	0	15	0	15	ns	12, 13
Transition Time (Rise and Fall)	t_T	t_T	1	50	1	50	ns	
RAS Precharge Time	t_{REHREL}	t_{RP}	40	—	50	—	ns	
RAS Pulse Width	t_{RELREH}	t_{RAS}	60	10 k	70	10 k	ns	
RAS Hold Time	t_{CELREH}	t_{RSH}	10	—	12	—	ns	
CAS Hold Time	t_{RELCEH}	t_{CSH}	40	—	50	—	ns	
CAS Pulse Width	t_{CELCEH}	t_{CAS}	10	10 k	12	10 k	ns	
RAS to CAS Delay Time	t_{RELCEL}	t_{RCD}	14	43	14	50	ns	8
RAS to Column Address Delay Time	t_{RELAV}	t_{RAD}	12	30	12	35	ns	9
CAS to RAS Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	ns	
CAS Precharge Time	t_{CEHCEL}	t_{CP}	10	—	12	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	10	—	12	—	ns	
Column Address to RAS Lead Time	t_{AVREH}	t_{RAL}	30	—	35	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	ns	

(continued)

NOTES:

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power–up followed by 8 RAS cycles before proper device operation is guaranteed. If using the internal refresh counter, a minimum of 8 CAS before RAS refresh cycles, instead of 8 RAS only refresh cyces are required.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specification for t_{RC} (min), t_{RWC} (min), and t_{EPC} (min) is used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.
10. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
11. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
12. t_{OFF} (max), t_{REZ} (max), t_{WEZ} (max), and t_{GZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
13. If RAS goes high before CAS goes high, the open circuit condition is controlled by CAS going high (t_{OFF}). If CAS goes high before RAS goes high, the open circuit condition is controlled by RAS going high (t_{REZ}).

ALL DEVICES: READ, WRITE, AND READ–WRITE CYCLES (continued)

Parameter	Symbol		60		70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Read Command Hold Time Referenced to CAS	t_{CEHWX}	t_{RCH}	0	—	0	—	ns	14
Read Command Hold Time Referenced to RAS	t_{REHWX}	t_{RRH}	0	—	0	—	ns	14
Write Command Hold Time Referenced to CAS	t_{CELWH}	t_{WCH}	10	—	12	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	12	—	ns	
Write Command to RAS Lead Time	t_{WLREH}	t_{RWL}	10	—	12	—	ns	
Write Command to CAS Lead Time	t_{WLCEH}	t_{CWL}	10	—	12	—	ns	
Data In Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	ns	15
Data In Hold Time	t_{CELDX}	t_{DH}	10	—	12	—	ns	15
Refresh Period 8MB, 16MB 32MB	t_{RVRV}	t_{RFSH}	—	16 32	—	16 32	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	ns	16
CAS to Write Delay	t_{CELWL}	t_{CWD}	36	—	39	—	ns	16
RAS to Write Delay	t_{RELWL}	t_{RWD}	79	—	89	—	ns	16
Column Address to Write Delay	t_{AVWL}	t_{AWD}	49	—	54	—	ns	16
CAS Precharge to Write Delay	t_{CEHWL}	t_{CPWD}	54	—	59	—	ns	16
CAS Setup Time for CAS Before RAS Refresh	t_{CELCEL}	t_{CSR}	5	—	5	—	ns	
CAS Hold Time for CAS Before RAS Refresh	t_{RELCEH}	t_{CHR}	10	—	15	—	ns	
RAS Precharge to CAS Active Time	t_{REHCEL}	t_{RPC}	5	—	5	—	ns	
CAS Precharge Time for CAS Before RAS Counter Test	t_{CEHCEL}	t_{CPT}	20	—	20	—	ns	
RAS Hold Time Referenced to G	t_{GLREH}	t_{ROH}	10	—	10	—	ns	
G Access Time	t_{GLQV}	t_{GA}	—	15	—	20	ns	6
G to Data Delay	t_{GLHDX}	t_{GD}	15	—	15	—	ns	
Output Buffer Turn–Off Delay from G	t_{GHQZ}	t_{GZ}	0	15	0	15	ns	12
G Command Hold Time	t_{WLGL}	t_{GH}	10	—	12	—	ns	
Output Disable Setup Time	t_{GHCEL}	t_{GDS}	0	—	0	—	ns	
RAS Hold Time from CAS Precharge (EDO)	t_{CEHREH}	t_{RHCP}	35	—	40	—	ns	
RAS Pulse Width (EDO)	t_{RELREH}	t_{RASP}	60	100 k	70	100 k	ns	
RAS to Next CAS Delay (EDO)	t_{RELCEL}	t_{RNCD}	60	—	70	—	ns	
EDO Cycle Time	t_{CELCEL}	t_{EPC}	25	—	30	—	ns	
EDO Read–Write Cycle Time	t_{CELCEL}	t_{ERWC}	68	—	75	—	ns	
Output Data Hold Time	t_{CELQZ}	t_{COH}	5	—	5	—	ns	
Output Buffer Turn–Off Delay from RAS	t_{REHQZ}	t_{REZ}	0	15	0	15	ns	12, 13
Output Buffer Turn–Off Delay from WE	t_{WLQZ}	t_{WEZ}	0	15	0	15	ns	12
WE to Data Delay	t_{WLDV}	t_{WED}	15	—	15	—	ns	
G to Pulse Width	t_{GLGH}	t_{G}	15	—	20	—	ns	
G Precharge Time	t_{GHGL}	t_{GP}	10	—	12	—	ns	
CAS to G Precharge Time	t_{CEHGL}	t_{CPG}	5	—	5	—	ns	

NOTES:

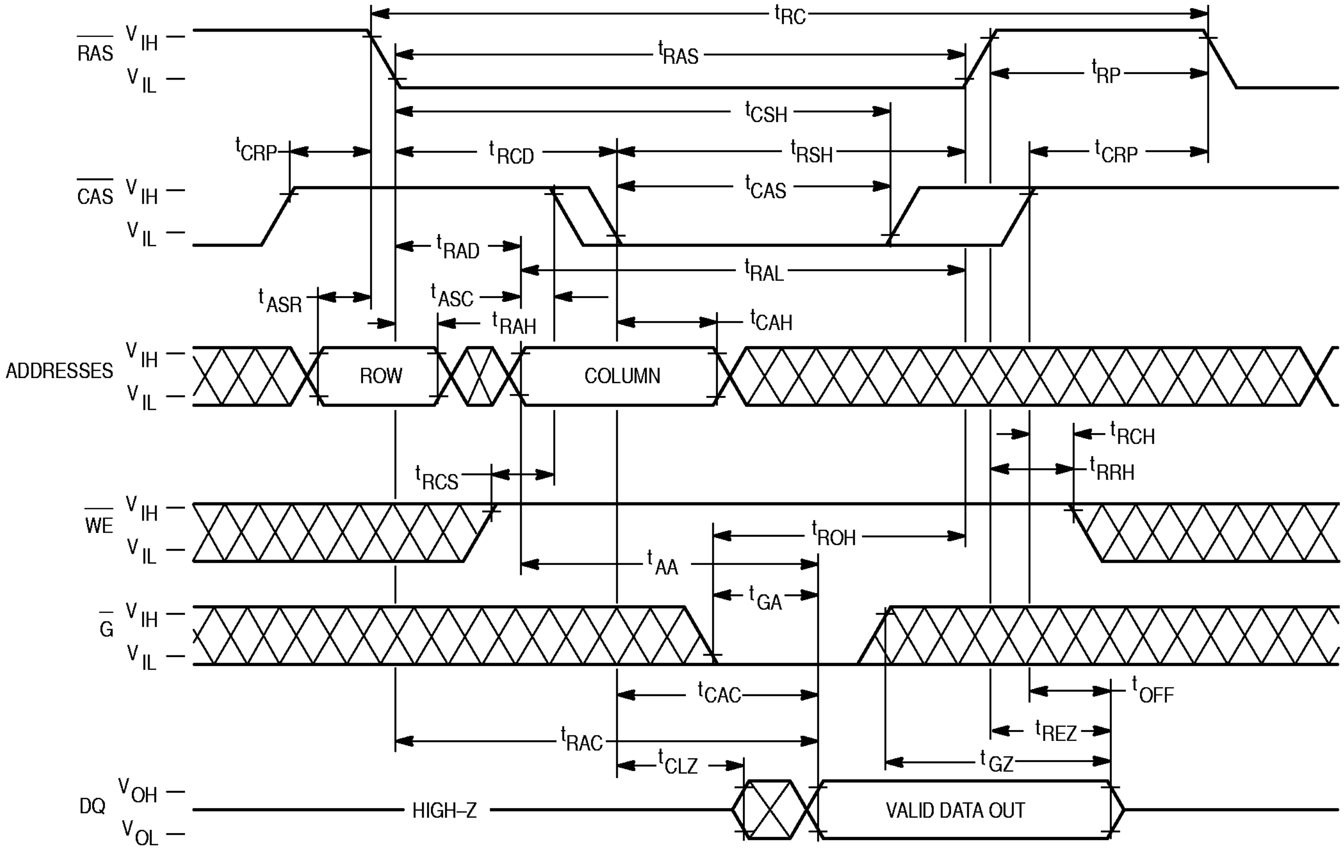
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. These parameters are referenced to UCAS or LCAS leading edge in early write cycles and to W leading edge in late write or read–write cycles.
16. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), $t_{CPWD} \geq t_{CPWD}$ (min), (extended data out), the cycle is a read–write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

SERIAL PRESENCE DETECT DATA

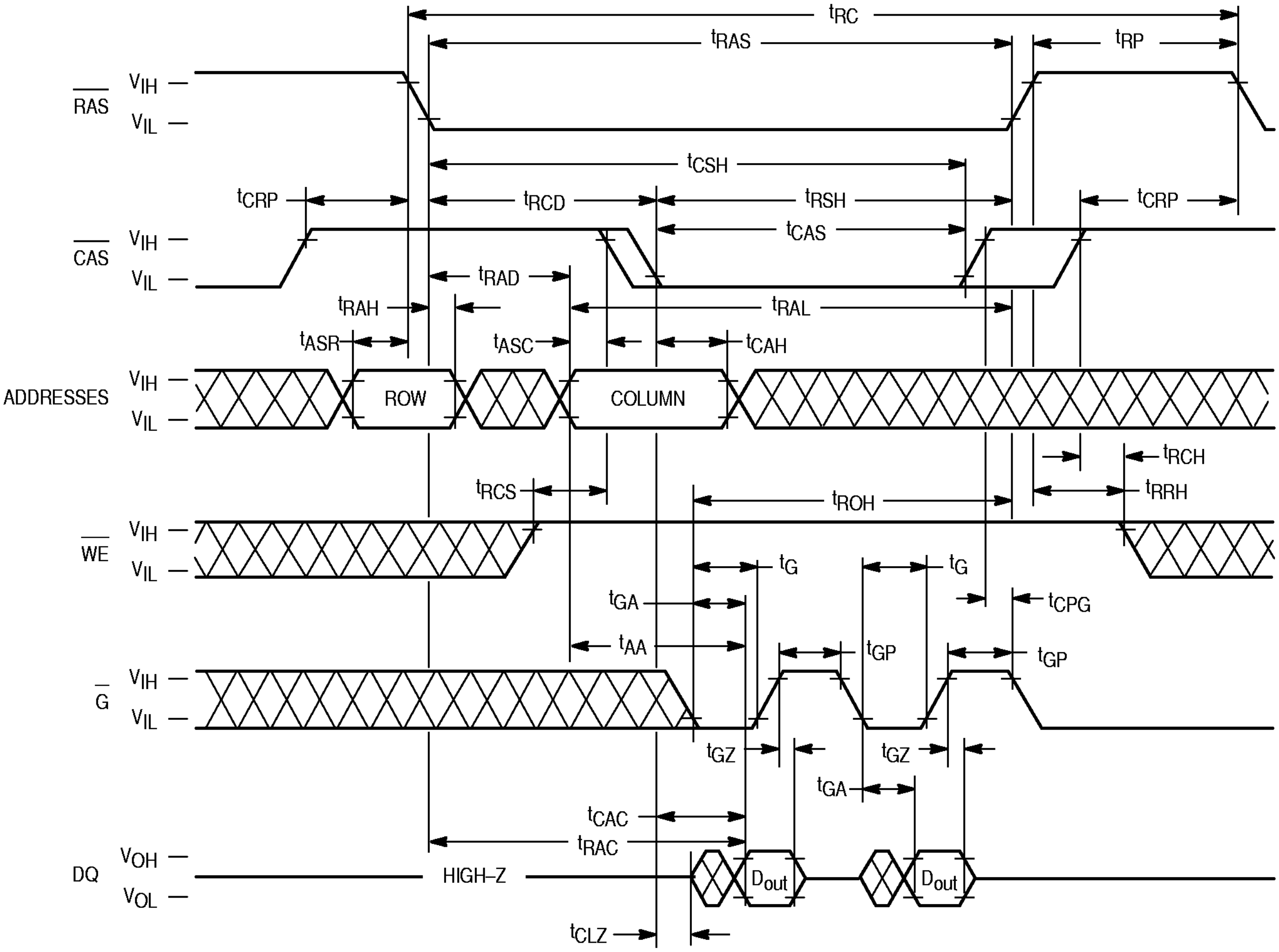
Field Description	Byte Number	Byte Value (Hex)	Byte Value Meaning
8MB			
SPD Size	0	80	128 bytes
Total SPD Memory Size	1	08	256 bytes
Fundamental Memory Type	2	02	EDO
Number of Rows	3	0A	10 rows
Number of Columns	4	0A	10 columns
Number of Banks	5	01	1 bank
Module Data Width	6	40	64 bits wide
Module Data Width (Continued)	7	00	None
Supply Voltage	8	00	5 V (TTL)
RAS Access Time 60/70	9	3C/46	60 ns/70 ns
CAS Access Time 60/70	10	11/14	17 ns/20 ns
Error Detection	11	00	None
Refresh Rates	12	00	15.625 µs
Primary DRAM Organization	13	10	x16 DRAMs
16MB			
SPD Size	0	80	128 bytes
Total SPD Memory Size	1	08	256 bytes
Fundamental Memory Type	2	02	EDO
Number of Rows	3	0A	10 rows
Number of Columns	4	0A	10 columns
Number of Banks	5	02	2 banks
Module Data Width	6	40	64 bits wide
Module Data Width (Continued)	7	00	None
Supply Voltage	8	00	5 V (TTL)
RAS Access Time 60/70	9	3C/46	60 ns/70 ns
CAS Access Time 60/70	10	11/14	17 ns/20 ns
Error Detection	11	00	None
Refresh Rates	12	00	15.625 µs
Primary DRAM Organization	13	10	x16 DRAMs
32MB			
SPD Size	0	80	128 bytes
Total SPD Memory Size	1	08	256 bytes
Fundamental Memory Type	2	02	EDO
Number of Rows	3	0B	11 rows
Number of Columns	4	0B	11 columns
Number of Banks	5	01	1 bank
Module Data Width	6	40	64 bits wide
Module Data Width (Continued)	7	00	None
Supply Voltage	8	00	5 V (TTL)
RAS Access Time 60/70	9	3C/46	60 ns/70 ns
CAS Access Time 60/70	10	11/14	17 ns/20 ns
Error Detection	11	00	None
Refresh Rates	12	00	15.625 µs
Primary DRAM Organization	13	04	x4 DRAMs

TIMING DIAGRAMS

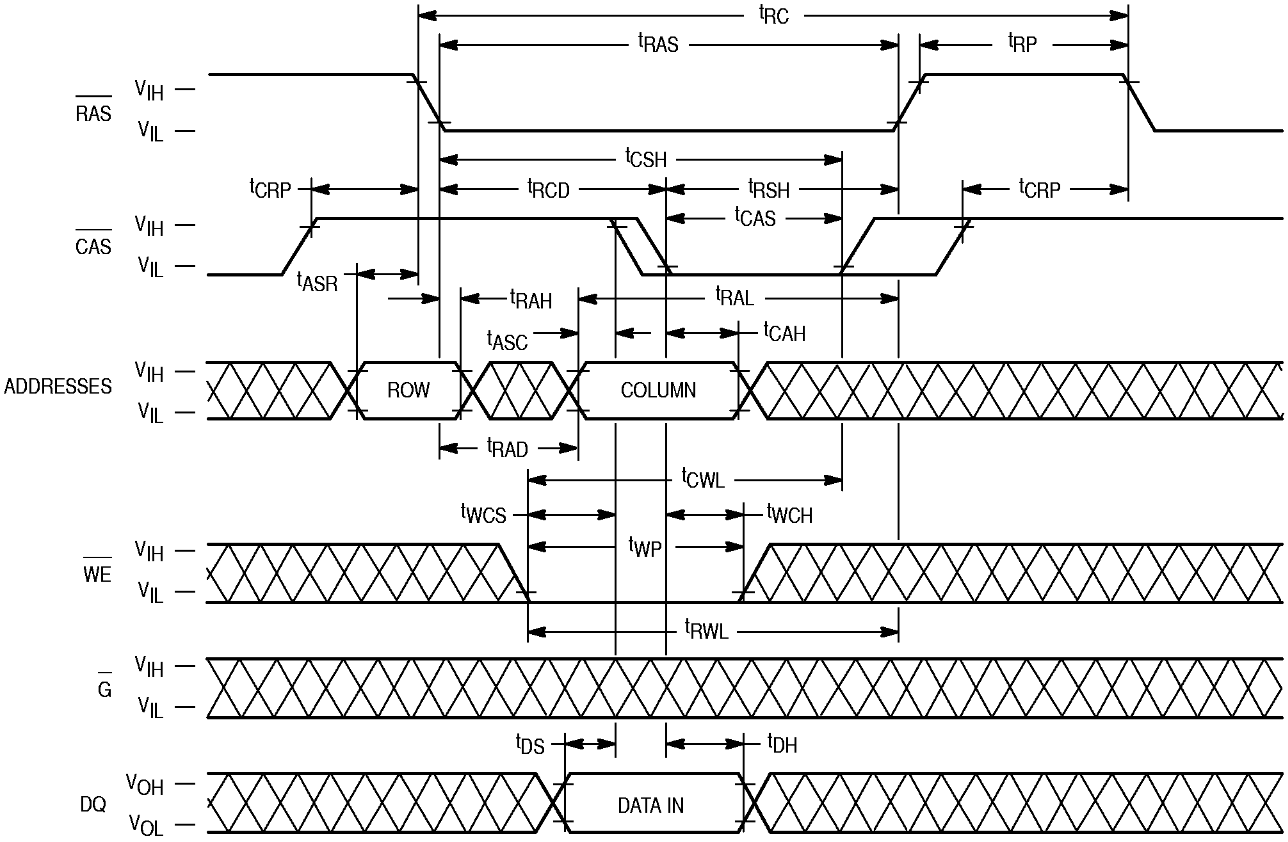
READ CYCLE



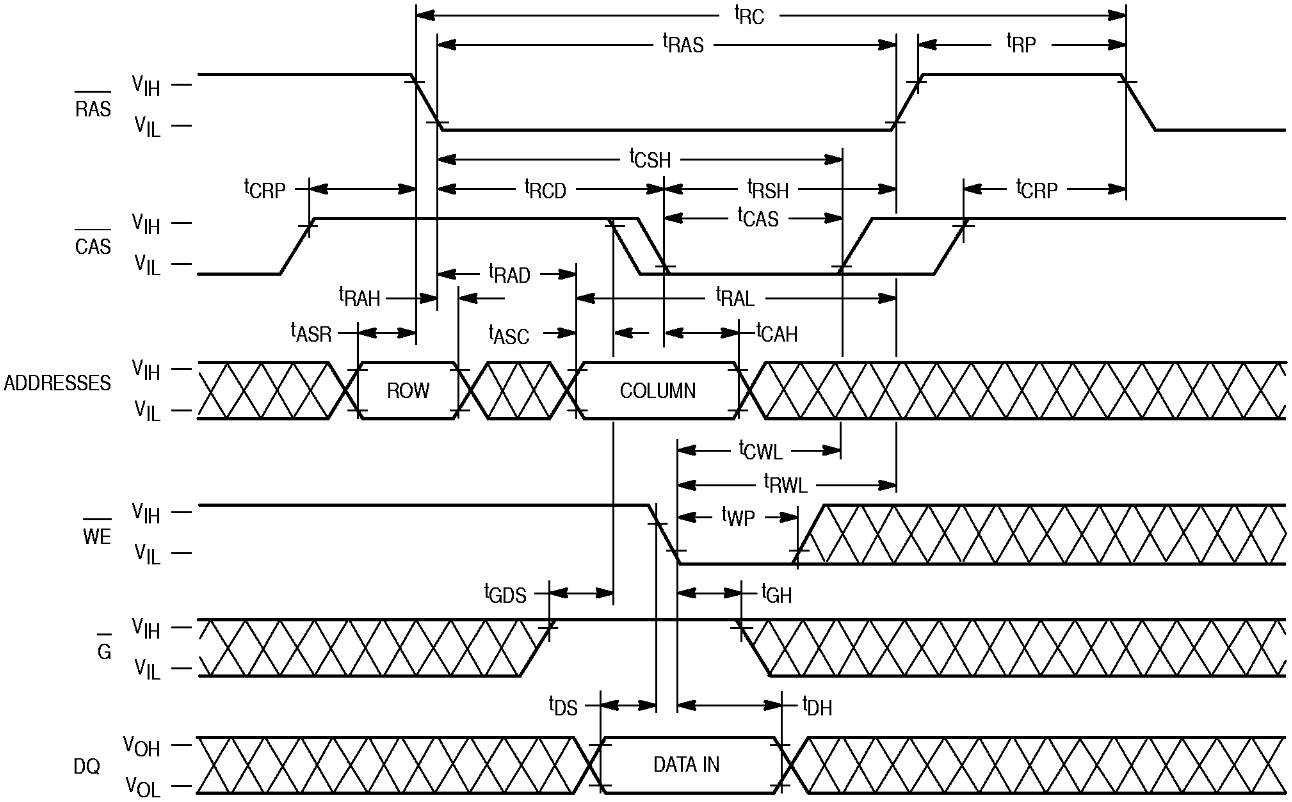
READ CYCLE ($\overline{G}$ CONTROLLED READ)



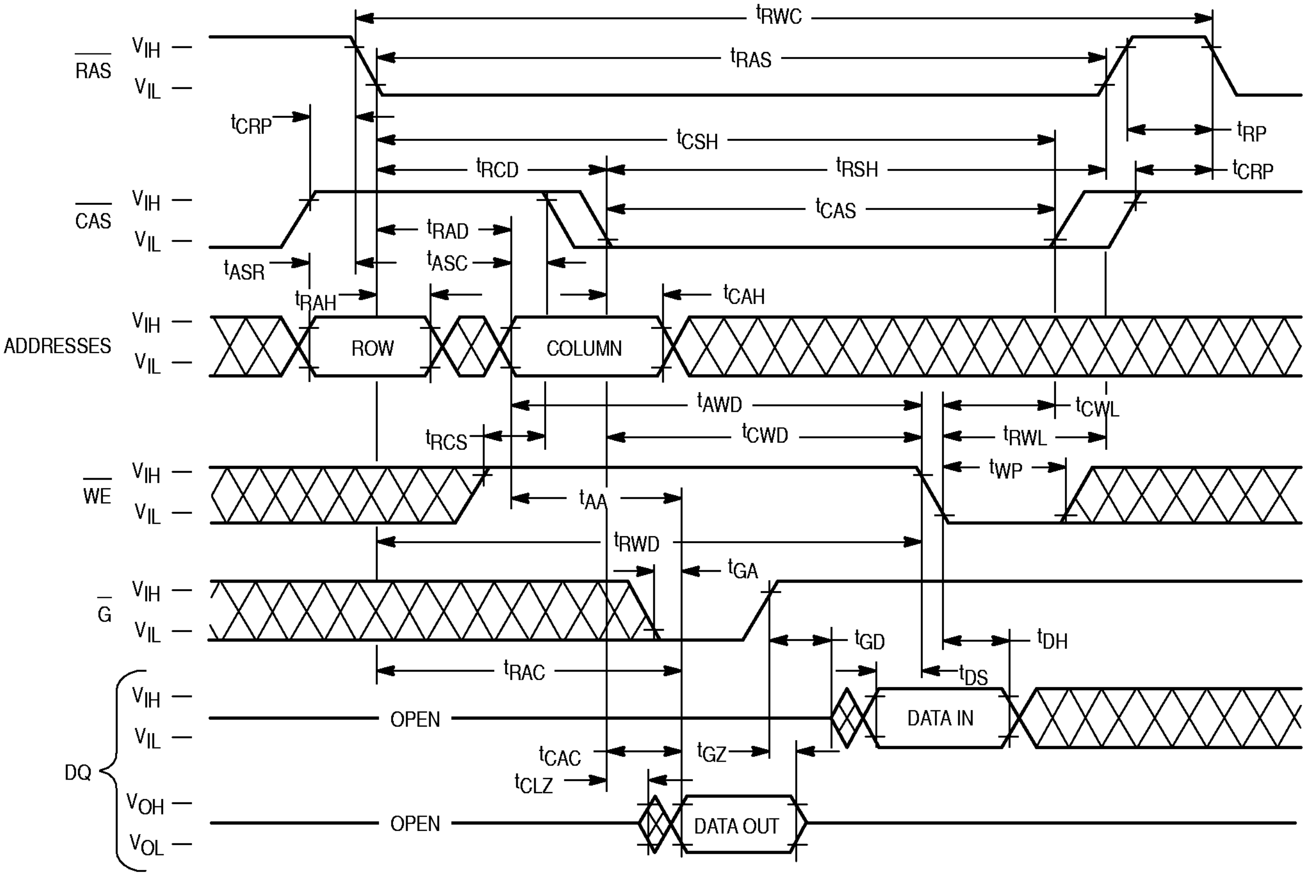
WRITE CYCLE (EARLY WRITE)



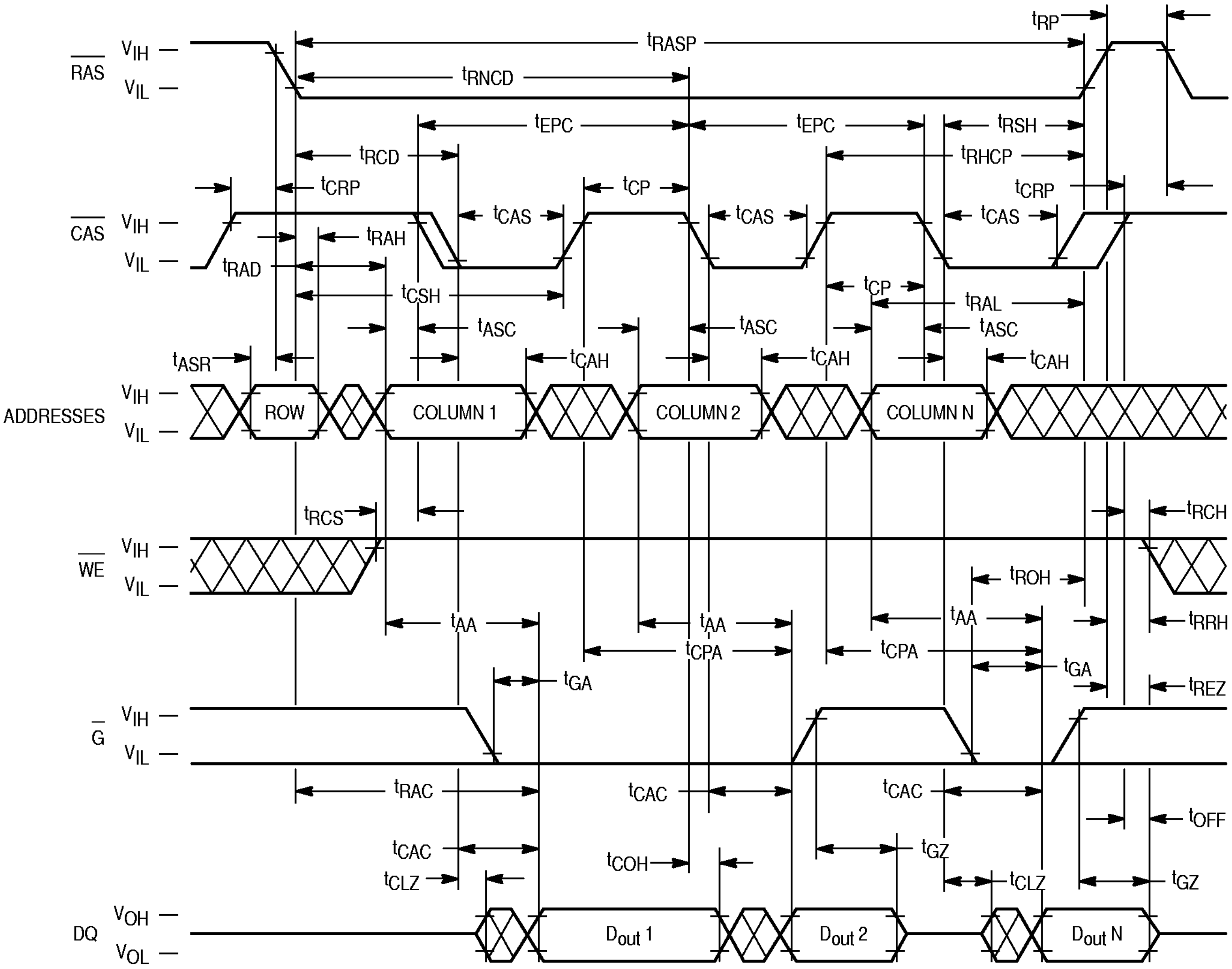
WRITE CYCLE ($\overline{G}$ CONTROLLED WRITE)



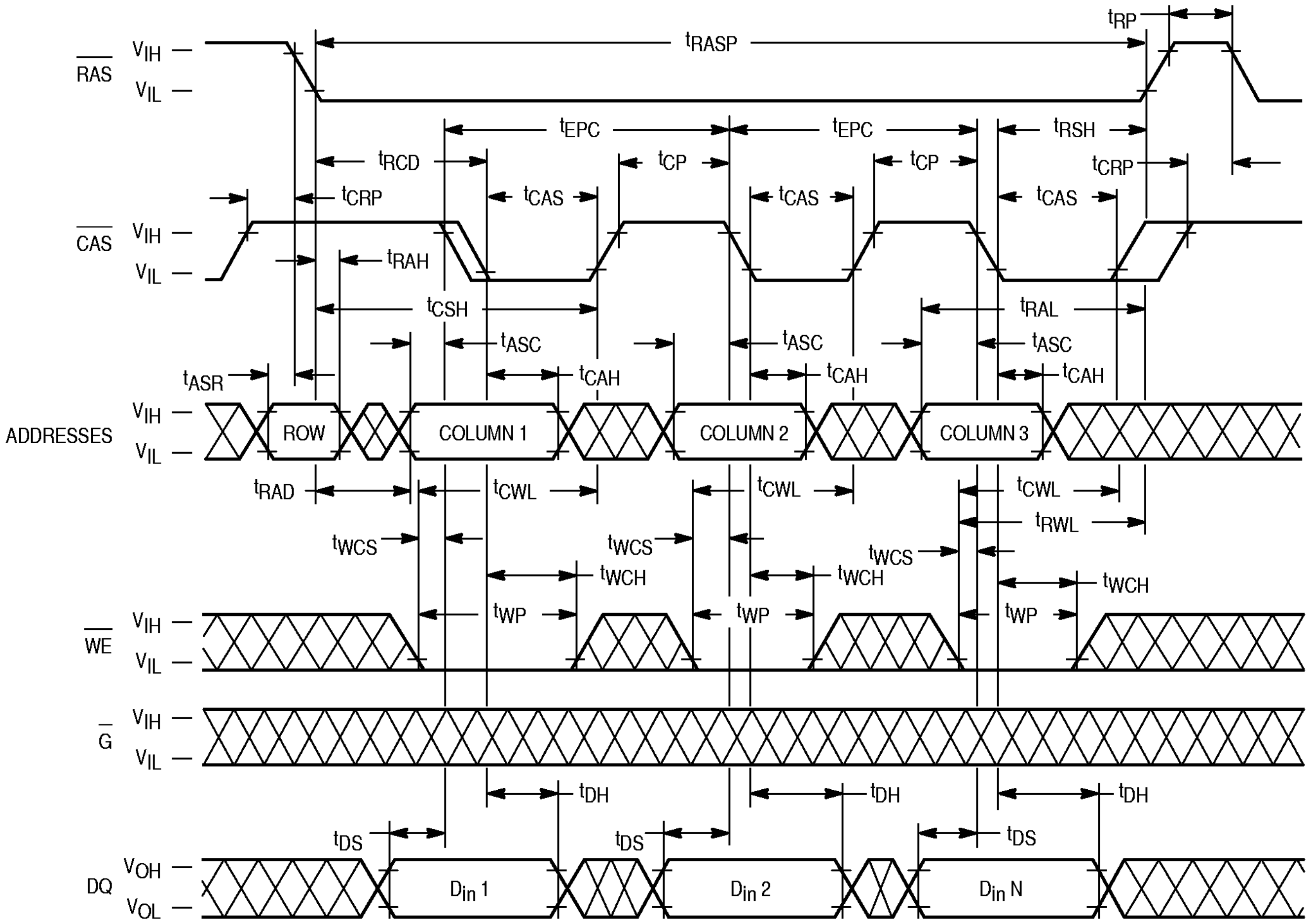
READ–WRITE CYCLE



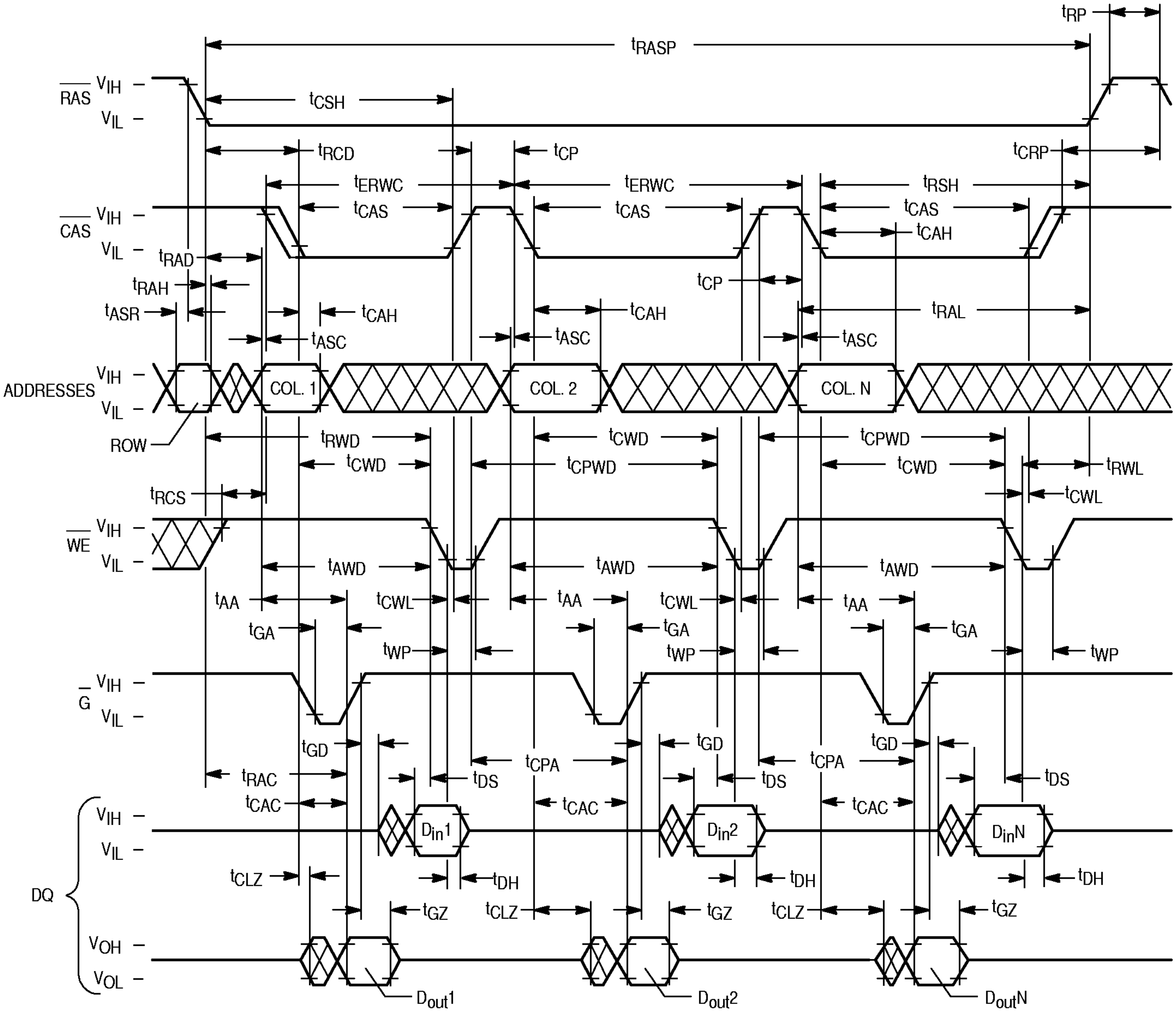
EXTENDED DATA OUT READ CYCLE



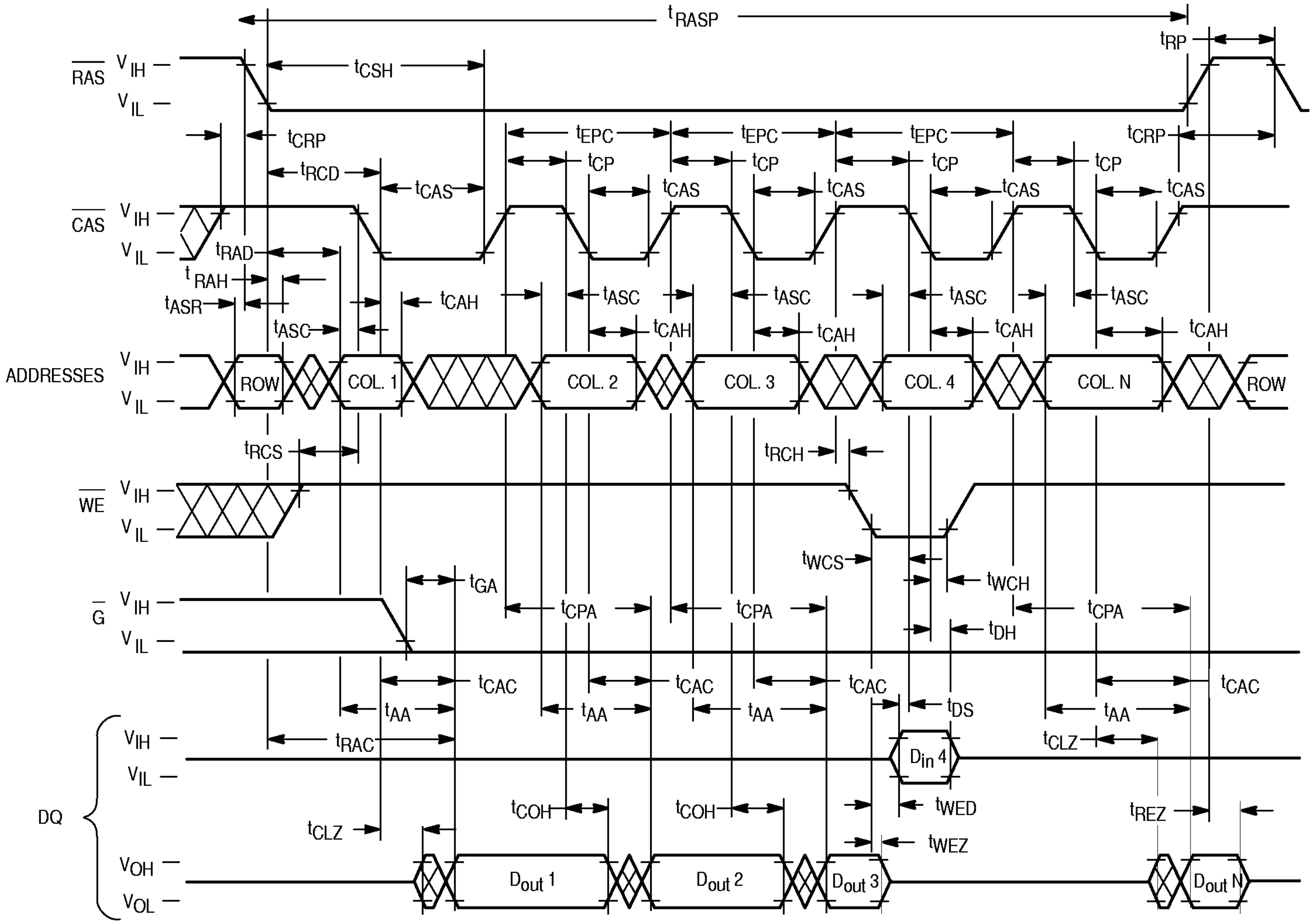
EXTENDED DATA OUT WRITE CYCLE (EARLY WRITE)



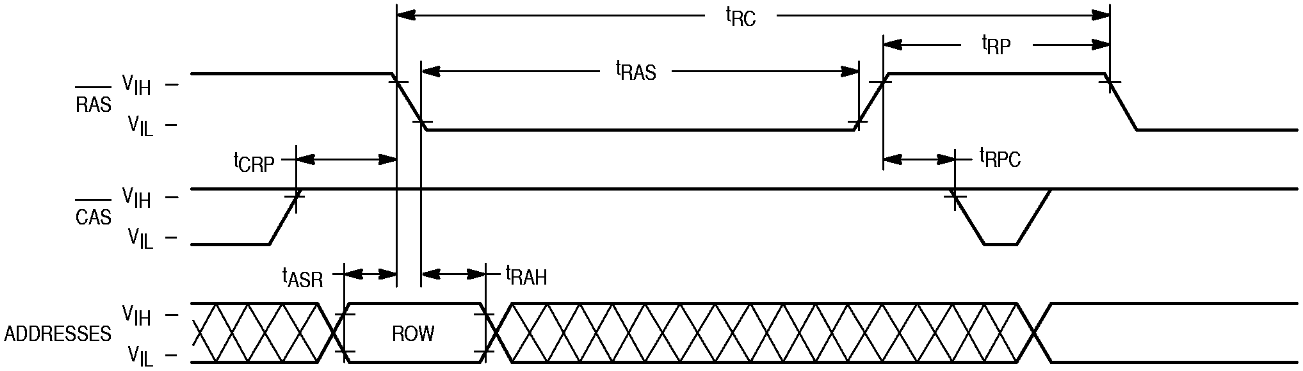
EXTENDED DATA OUT READ–WRITE CYCLE



EXTENDED DATA OUT READ–WRITE MIXED CYCLE

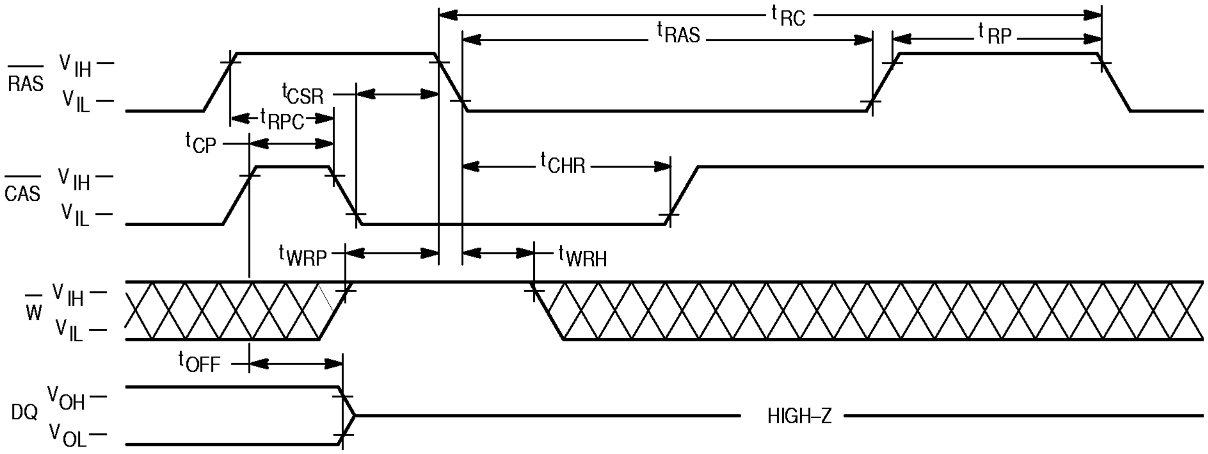


$\overline{\text{RAS}}$–ONLY REFRESH CYCLE



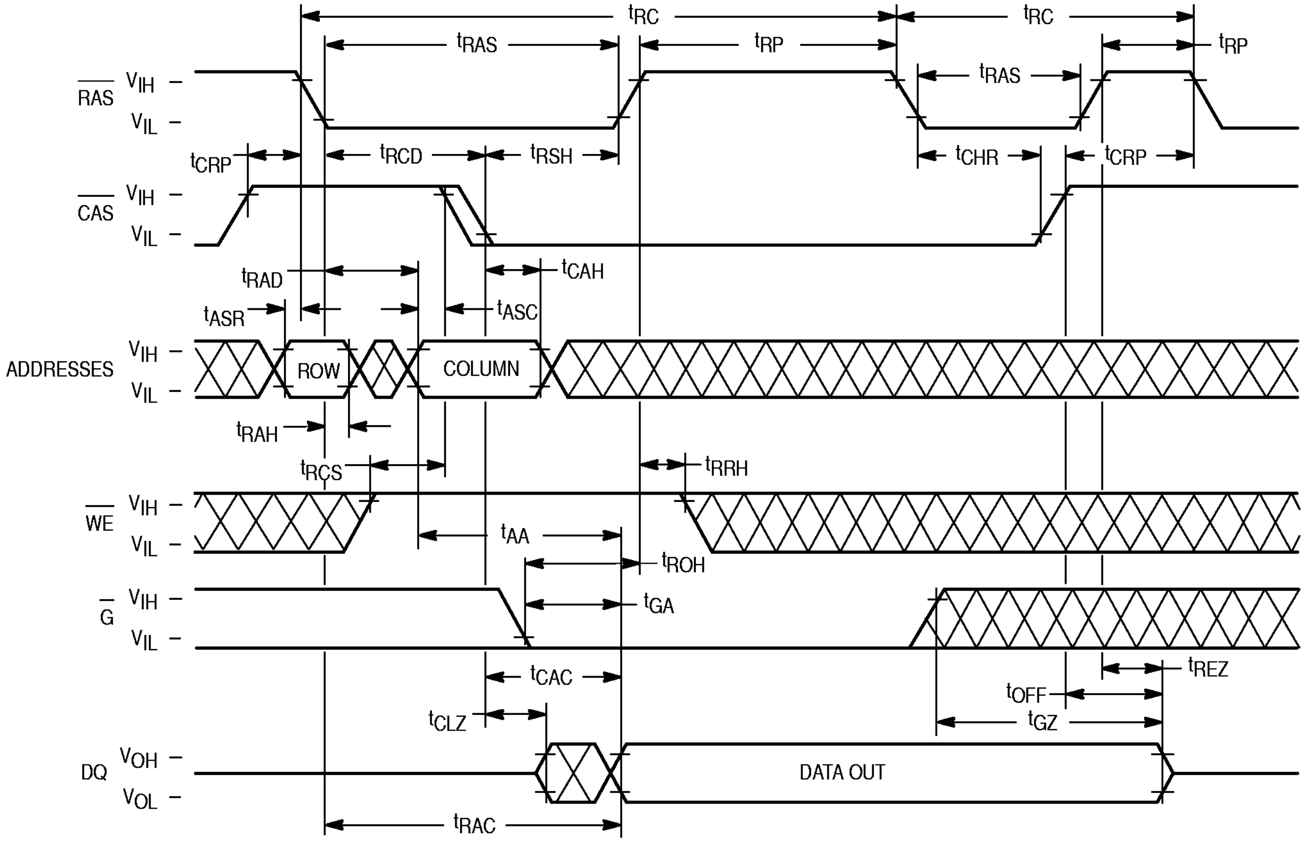
NOTE: $\overline{\text{WE}}$, $\overline{\text{G}}$ = H or L
DQ = Open

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

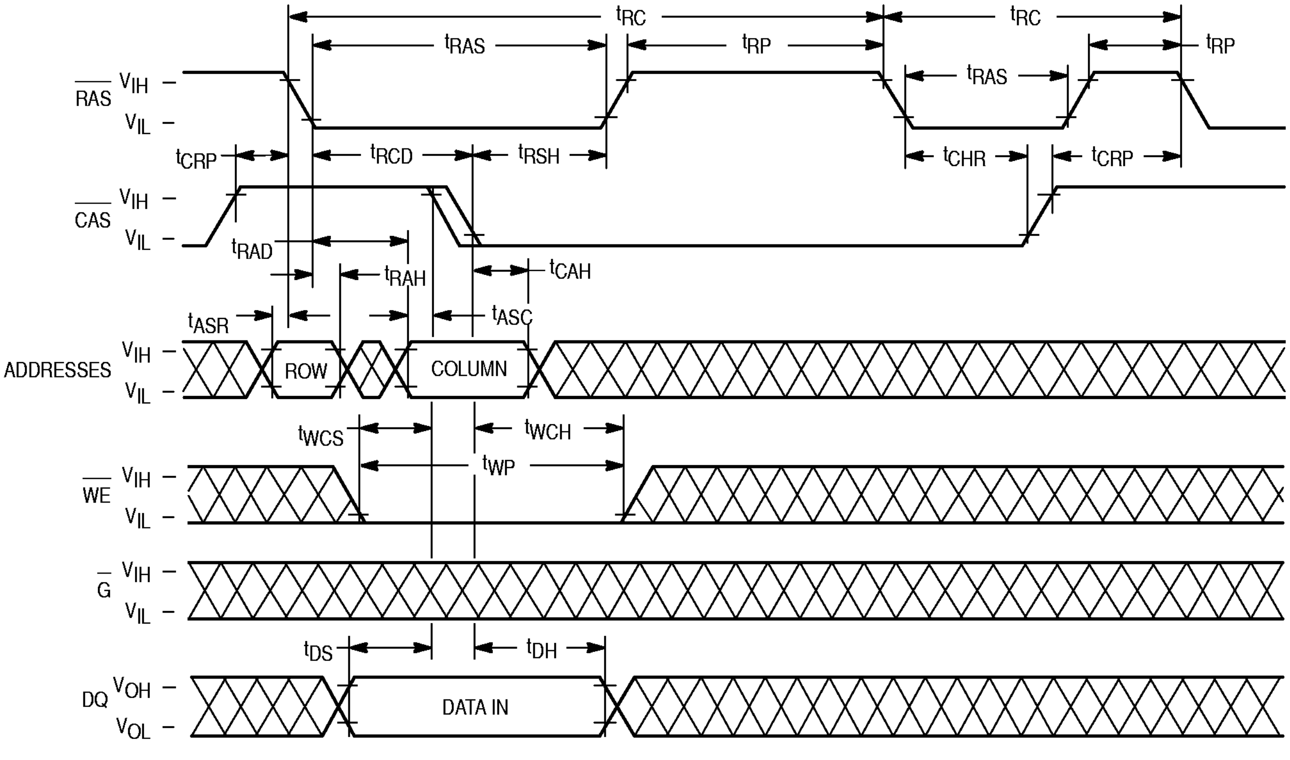


NOTE: Addresses = H or L.
8MB, 16MB: W = H or L.
32MB: W must be as shown to avoid switching into component test mode.
.

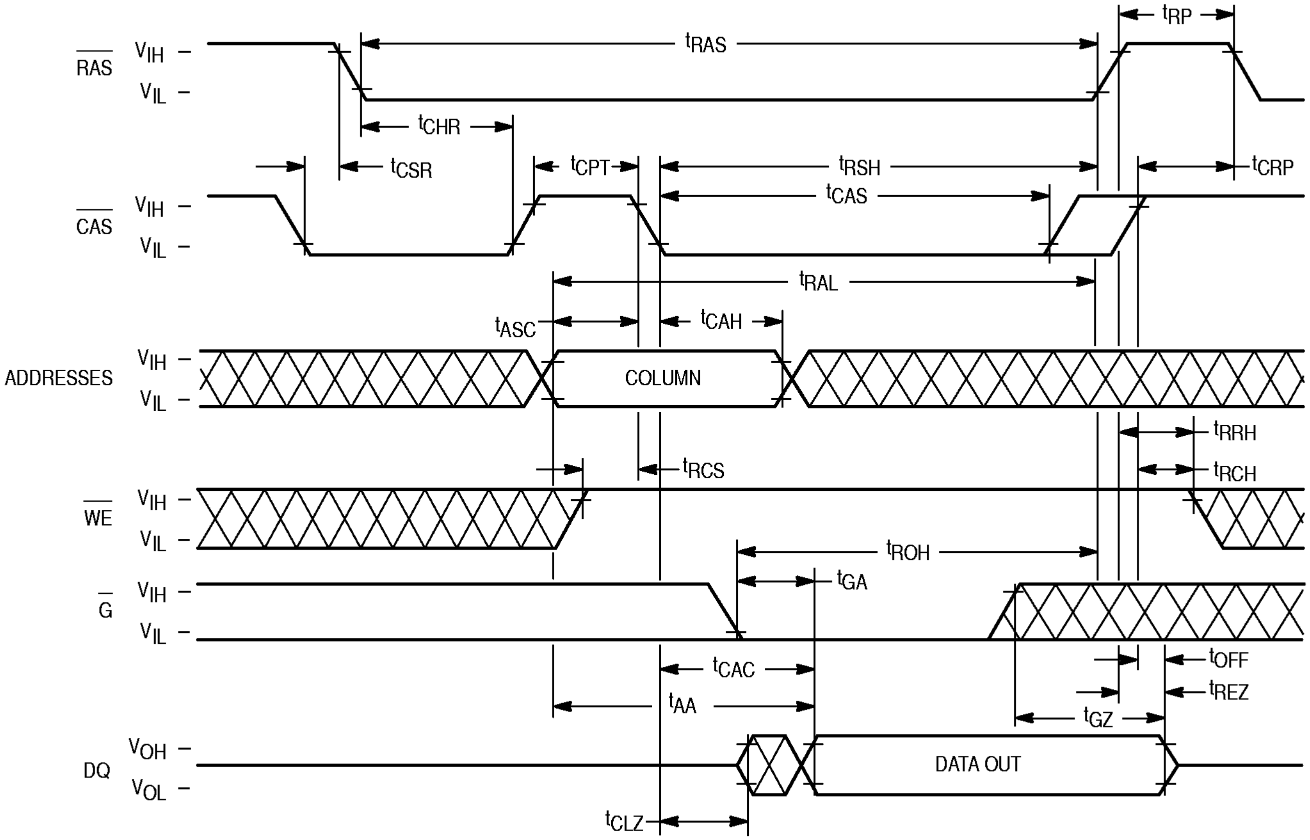
HIDDEN REFRESH CYCLE (READ)



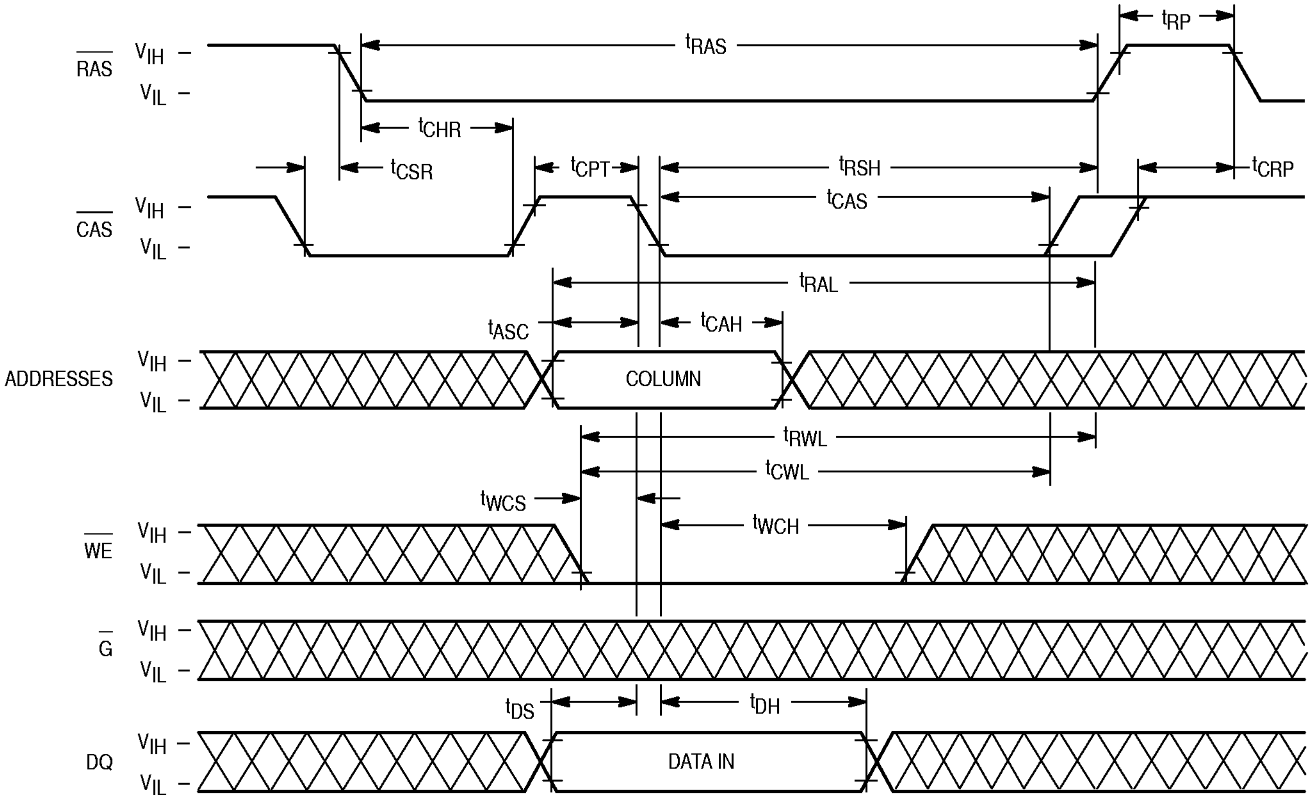
HIDDEN REFRESH CYCLE (WRITE)



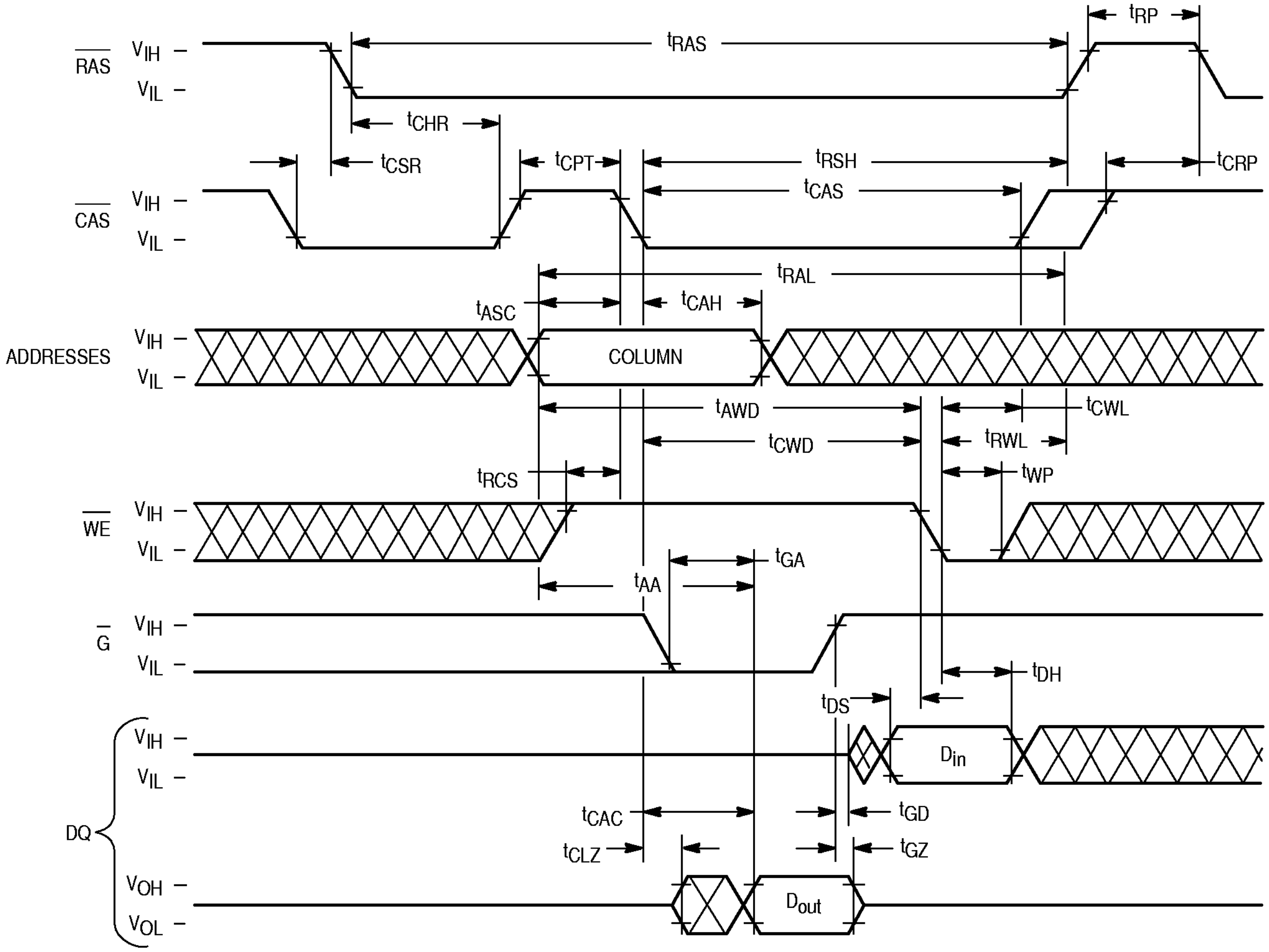
CAS BEFORE RAS REFRESH COUNTER TEST READ CYCLE



CAS BEFORE RAS REFRESH COUNTER TEST WRITE CYCLE



$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST READ–WRITE CYCLE



DEVICE INITIALIZATION

On power–up, an initial pause of 200 µs is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the module. During an extended inactive state (greater than 16 ms for the 8MB and 16MB, 32 ms for the 32MB with the device powered up), a wake up sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe (RAS) and column address strobe (CAS), into two separate address fields. For the 8MB and 16MB modules a total of 20 address bits, 10 rows and 10 columns, will decode one of the word locations in the device. For the 32MB module 22 address bits, 11 rows and 11 columns, decode one of the word locations in the device. RAS active transition is followed by CAS active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between RAS and CAS active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external CAS signal is ignored until an internal RAS signal is available. This "gate" feature on the external CAS clock enables the internal CAS line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the CAS clock.

There are three other variations in addressing the module: **RAS–only refresh cycle, CAS before RAS refresh cycle,** and **page mode**. All three are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, extended data out read cycle, read–write cycle, and extended data out read–write cycle. The normal read cycle is outlined here,while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with RAS and CAS active transitions latching the desired bit location. The write (W) input level must be high (V_{IH}), t_{RCS} (minimum) before the CAS or active transition, to enable read mode.

Both the RAS and CAS clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window.

Both CAS and output enable (G) control read access time: CAS must be active before or at t_{RCD} maximum and G must be active t_{RAC}–t_{GA} (both minimum) after RAS active transition to guarantee valid data out (Q) at t_{RAC}. If the t_{RCD} maximum is exceeded and/or G active transition does not occur in time, read access time is determined by either the CAS or G clock active transition (t_{CAC} or t_{GA}).

WRITE CYCLE

The user can write to the DRAM with any of four cycles: early write, late write, extended data out early write, and extended data out read–write. Early and late write modes are discussed here, while extended data out write operation is covered in a separate section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of W to active (V_{IL}). Early and late write modes are distinguished by the active transition of W, with respect to CAS. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP}, apply to write mode, as in the read mode.

An early write cycle is characterized by W active transition at minimum time t_{WCS} before CAS active transition. Column address setup and hold times (t_{ASC}, t_{CAH}) and data in (D) setup and hold times (t_{DS}, t_{DH}) are referenced to CAS in an early write cycle. RAS and CAS clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

A late–write cycle (referred to as G–controlled write) occurs when W active transition is made after CAS active transition. W active transition could be delayed for almost 10 µs after CAS active transition, ($t_{RCD} + t_{CWD} + t_{RWL} + 2t_T) \leq t_{RAS}$, if other timing minimums (t_{RCD}, t_{RWL}, and t_T) are maintained. D timing parameters are referenced to W active transition in a late write cycle. Output buffers are enabled by CAS active transition. Outputs are switched off by G inactive transition, which is required to write to the device. RAS and CAS must remain active for t_{RWL} and t_{CWL}, respectively, after W active transition to complete the write cycle. G devices must remain inactive for t_{GH} after W active transition to complete the write cycle.

READ–WRITE CYCLE

A read–write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except W must remain high for t_{CWD} and/or t_{AWD} minimum, to guarantee valid Q before writing the bit.

EDO MODE CYCLES

EDO mode allows fast successive data operations at all column locations on a selected row. Read access time in page mode (t_{CAC}) is typically half the regular RAS clock access time, t_{RAC}. EDO mode operation consists of keeping RAS active while toggling CAS between V_{IH} and V_{IL}. The row is latched by RAS active transition, while each CAS active transition allows selection of a new column location on the row.

An EDO mode cycle is initiated by a normal read, write, or read–write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, CAS transitions to inactive for minimum t_{CP}, while RAS remains low (V_{IL}). The second CAS active transition while RAS is low initiates the first EDO mode cycle (t_{EPC} or t_{ERWC}). Either a read, write, or read–write operation can be performed in an EDO mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive EDO mode cycles and performed in any order. The maximum number of consecutive EDO mode cycles is limited by t_{RASP}. EDO mode operation is ended when RAS transitions to inactive, coincident with or following CAS inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits require refresh every t_{RFSH}.

This is accomplished by cycling through the row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 µs. Burst refresh, a refresh of all rows consecutively, must be performed every t_{RFSH}.

A normal read, write, or read–write operation to the RAM will refresh all the bits associated with the particular row decodes. Three other methods of refresh, **RAS–only refresh, CAS before RAS refresh,** and **hidden refresh** are available on this device for greater system flexibility.

RAS–Only Refresh

RAS–only refresh consists of RAS transition to active, latching the row address to be refreshed, while CAS remains high (V_{IH}) throughout the cycle. An external counter should be employed to ensure that all rows are refreshed within the specified limit.

CAS Before RAS Refresh

CAS before RAS refresh is enabled by bringing CAS active before RAS. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh). W must be inactive for time t_{WRP} before and time t_{WRH} after RAS active transition to prevent switching the device into a **test mode cycle**.

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding CAS active at the end of a read or write cycle while RAS cycles inactive for t_{RP} and back to active starts the hidden refresh. This is essentially the execution of a CAS before RAS refresh from a cycle in progress (see Figure 1). W is subject to the same conditions with respect to RAS active transition (to prevent test mode entry) as in CAS before RAS refresh.

CAS BEFORE RAS REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **CAS before RAS refresh counter test**. This test is performed with a read–write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after completing one cycle for each column as indicated by the check data written in each row. See **CAS before RAS refresh counter test cycle** timing diagram.

The test can be performed after a minimum of eight **CAS before RAS** initialization cycles. Test procedure:

1. Write 0s into all memory cells with normal write mode.
2. Select a column address, read 0 out and write 1 into the cell by performing the **CAS before RAS refresh counter test, read–write cycle**. Repeat this operation for every column.
3. Read the 1s that were written in step two in normal read mode.
4. Using the same starting column address as in step two, read 1 out and write 0 into the cell by performing the **CAS before RAS refresh counter test, read–write cycle**. Repeat this operation for every column.
5. Read 0s which were written in step four in normal read mode.
6. Repeat steps one through five using complement data.

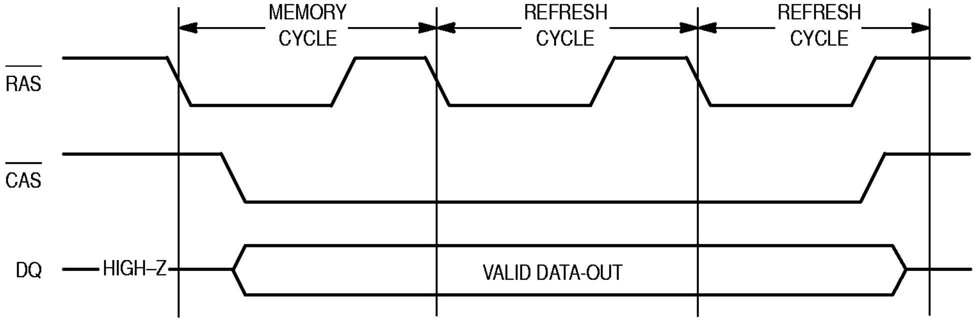


Figure 1. Hidden Refresh Cycle

PRESENCE DETECT OPERATION

LEXICON

This lexicon will describe some terms used in this serial interface description.

MASTER: The device that initiates the serial transmission is designated as master. In general, it is the device generating the clock. The SPD device can never function as a master.

SLAVE: The SPD device always operates as a slave.

TRANSMITTER: The device with its SDA pin in output is a data transmitter. In the case of multiple devices in output, the device sending a low level will win due to the Open–Drain connection.

RECEIVER: A device that has been properly selected by a chip address followed by a write bit is a receiver, and will shift data present on the SDA pin in internal registers.

MSB: The Most Significant Bit is the first bit transmitted and received.

START CONDITION: The start condition is defined as a 1 to 0 transition of SDA when SCL is high. The first byte of data following a start condition includes the chip address followed by the Read/Write bit. All devices connected on the same bus receive this data to check if they are addressed.

STOP CONDITION: The stop condition is defined as a 0 to 1 transition of SDA when SCL is high. In this circuit, the stop condition is never mandatory. An EEPROM programming can be initiated by the STOP or also by any following START condition.

A STOP after a serial read sequence will put the device in standby state.

CHIP ADDRESS: The first byte transmitted after a START contains the chip address followed by the Read/Write bit. The 7–bit chip address is formed of 4 fixed bits followed by 3 chip select bits.

Fixed bits are 1010 for this device. The 3 chip select bits must correspond to the 3 SA0–2 inputs for proper chip selection.

READ/WRITE BIT: The 8th bit transmitted by the master after the 7–bit chip address will indicate the direction of transfer for the next bytes (until a new start or stop). If low, the following bytes are transmitted by the master. If high, the following bytes are transmitted by the SPD device.

BYTE ADDRESS: The first byte of data received by the memory after the chip address, will be latched in the byte address register and is used to select one of the 256 EEPROM bytes.

ACKNOWLEDGE BIT: This bit is sent by the selected receiver on the data line after a byte reception. Due to the open drain structure, a valid acknowledge bit corresponds to a low level. While operating as a transmitter, sending a sequence of data bits, this device will check the acknowledge bit generated by the master. The absence of this bit will stop the transmission of data.

PROTOCOL

At the protocol level, the transmission of data is defined in the form of sequences of Start (STA), Stop (STO) conditions, and bytes followed by acknowledge bits.

Standby State

When no serial transmission and no programming are made, the SPD is in standby. A STOP condition following a read sequence or a write byte address sequence (without data write), will put the SPD in standby. A new START condition will wake up the SPD, to get the chip address. If the chip address is not valid, the SPD will return to standby.

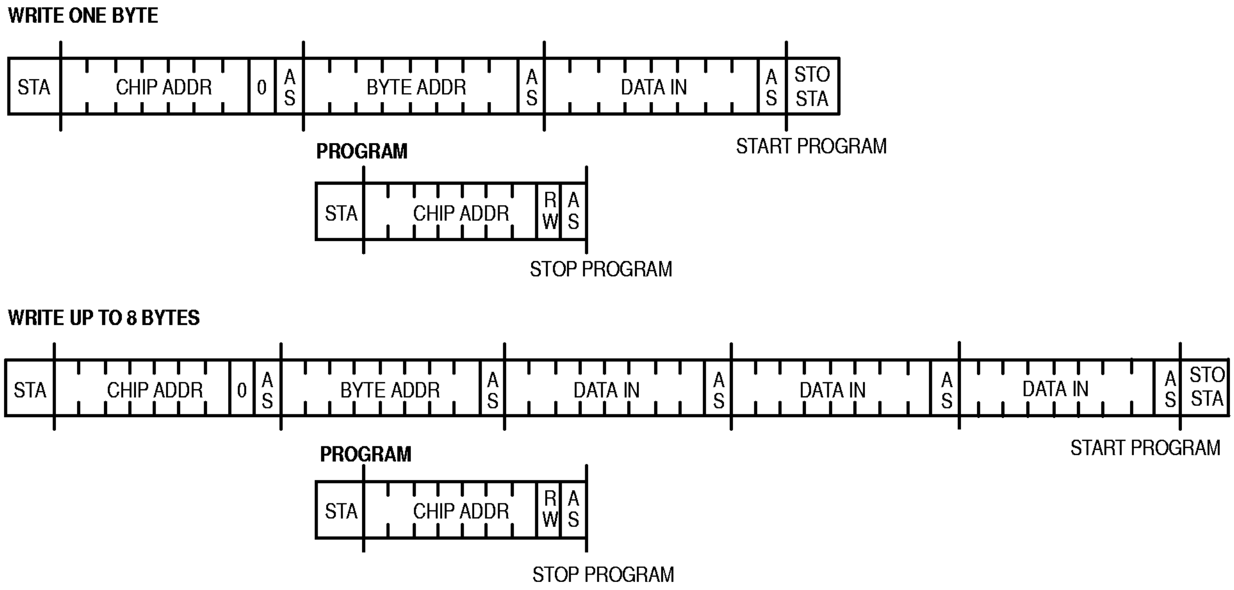
The power consumption is minimum in standby.

Write Sequence

The serial write to the memory includes a serial transmission of the byte address and the data to be written. When this is completed by a stop, the programming sequence is initiated.

During the write cycle, the SPD inputs and the SDA pin are disabled for the time t_{WR} and the SPD will not respond to any requests from the master.

It is possible to program simultaneously up to 8 bytes, provided the 5 most significant bits of their addresses are identical. The byte address is incremented after each new data byte shifted in.



STA: Start Condition
STO: Stop Condition

R/W Bit: 1 = Read/0 = Write
INC: Increment Byte Address

AS: Slave Acknowledge (SPD)
AM: Master Acknowledge

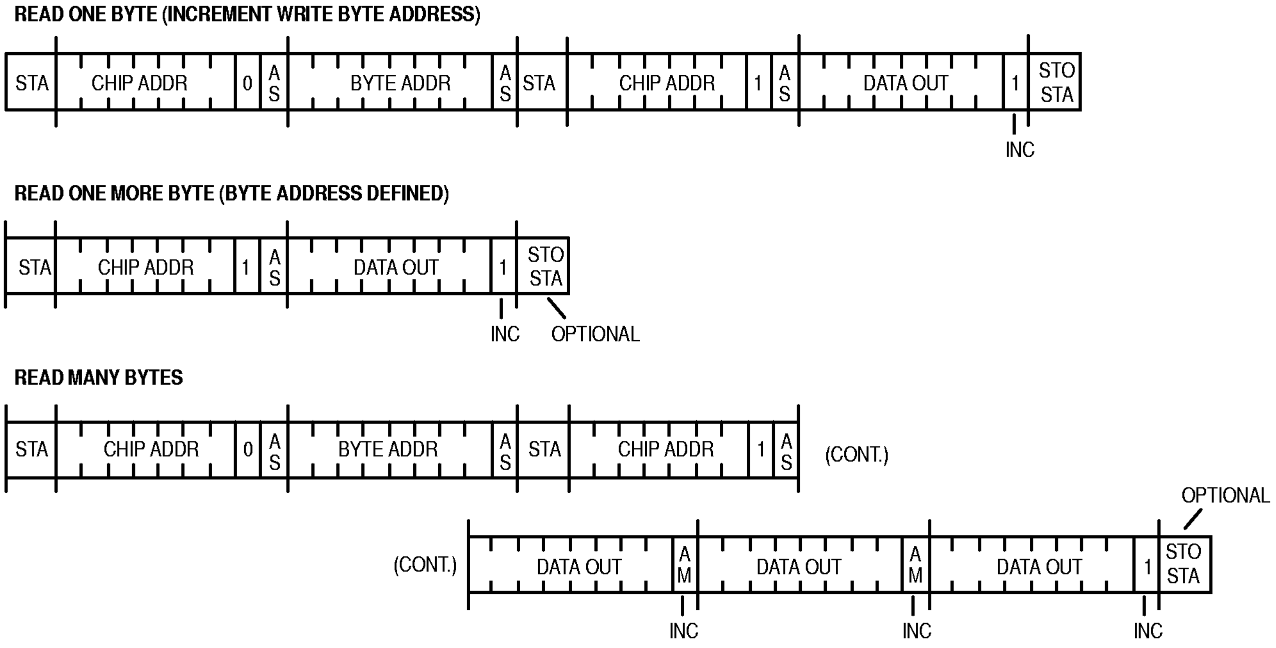
Figure 2. SPD Write Protocol

Read Sequence

Reading data from the memory is made in two steps. First the byte address must be loaded in the byte address register. Then data can be read out of the memory. The first step is only required to define the byte address. If this address was predefined from a previous read, this step can be skipped.

The byte address is automatically incremented after each data byte transmitted.

This is also valid after the last byte of a transmission. Therefore, the next read sequence without any byte address specified will transmit data of the next byte. A read sequence will transmit data bytes of successive addresses until the absence of the acknowledge bit from the master. In this case, the SDA output driver will switch off and the circuit will go to standby.



STA: Start Condition
STO: Stop Condition

R/W Bit: 1 = Read/0 = Write
INC: Increment Byte Address

AS: Slave Acknowledge (SPD)
AM: Master Acknowledge

Figure 3. SPD Read Protocol

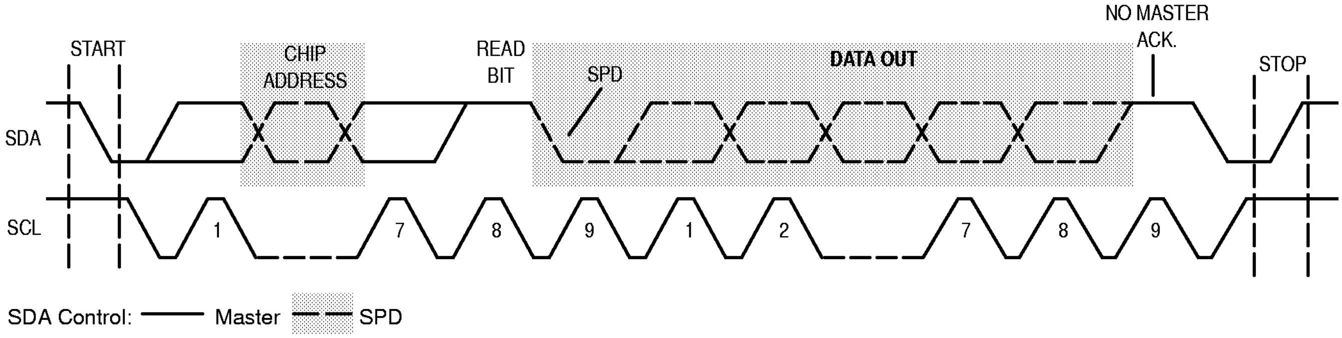


Figure 4. SPD Read Detail

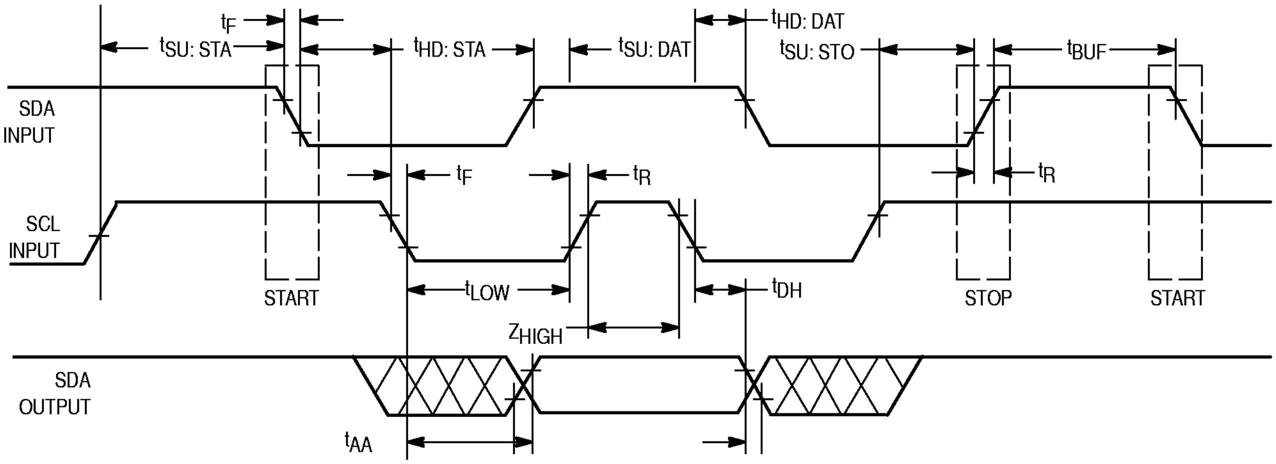


Figure 5. SPD Timings

PRESENCE DETECT READ AND WRITE CYCLE

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	F_{SCL}		100	kHz
Noise Suppression Time Constant at SCL, SDA Inputs	T_I		100	ns
SCL Low to SDA Data Out Valid	t_{AA}	0.1	4.5	µs
Time Bus Must be Free Before a New Transmission Can Start	t_{BUF}	4.7		µs
Start Condition Hold Time	$t_{HD:STA}$	4.0		µs
Clock Low Period	t_{LOW}	4.7		µs
Clock High Period	t_{HIGH}	4.0		µs
Start Condition Setup Time (for a Repeated Start Condition)	$t_{SU:STA}$	4.7		µs
Data In Hold Time	$t_{HD:DAT}$	0		µs
Data In Setup time	$t_{SU:STA}$	250		ns
SDA and SCL Rise Time	t_R		1	µs
SDA and SCL Fall Time	t_F		300	ns
Stop Condition Setup Time	$t_{SU:STO}$	4.7		µs
Data Out Hold Time	t_{DH}	100		ns
Write Cycle Time — NM24Cxx	t_{WR}*		10	ms

* The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle.

Signal Levels

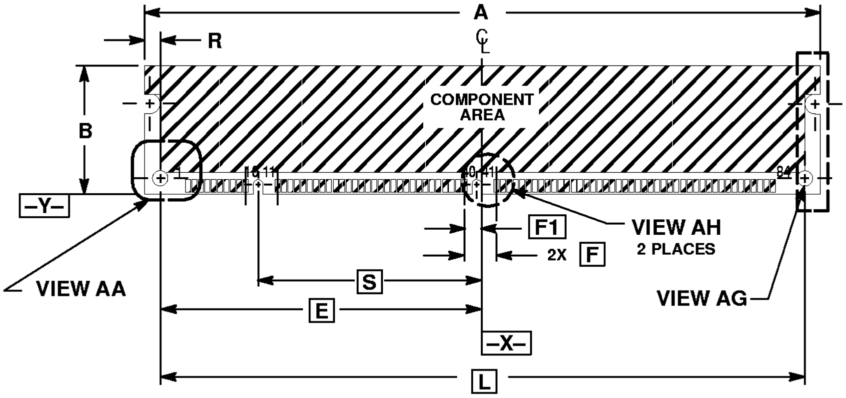
During a transmission, SDA line transitions must occur when SCL is low. A negative transition of SDA with SCL high is recognized as a START condition, the positive transition as a STOP condition.

The acknowledge bit is provided by the device receiving data. Therefore, during this time the data transmitter must leave the SDA line at high impedance.

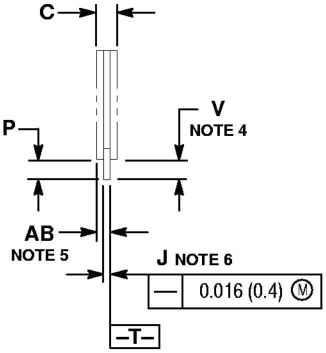
This memory has an open drain SDA output, so an external pull–up resistor to V_{CC} should be included on the SDA line.

PACKAGE DIMENSIONS

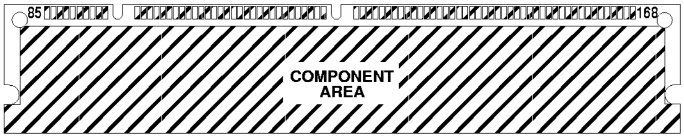
2M x 64 (16MB)
168–LEAD DIMM
CASE 1115A–01



FRONT VIEW



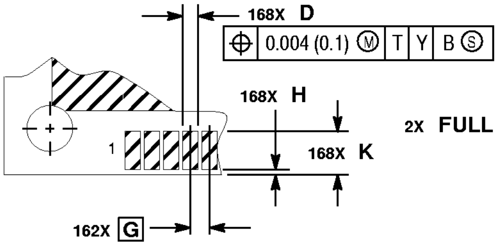
SIDE VIEW



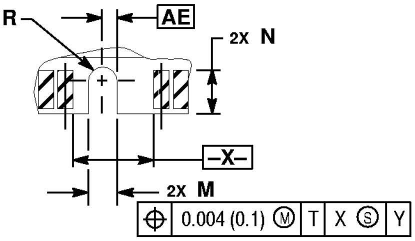
BACK VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALLIZATION.
4. DIMENSION C AND V DEFINE A DOUBLE–SIDED MODULE.
5. DIMENSION AB DEFINES OPTIONAL SINGLE–SIDED MODULE.
6. STRAIGHTNESS CALLOUT APPLIES TO TAB AREA ONLY.
7. R DIMENSION DEFINES SLOT END AND EDGE OF COMPONENT AREA.

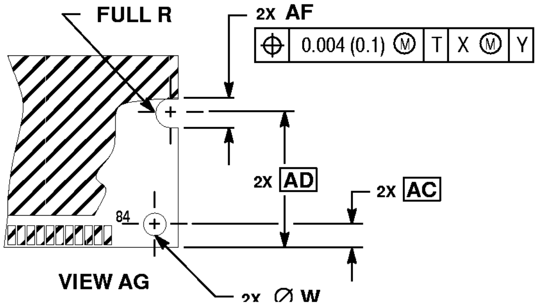
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	5.245	5.255	133.22	133.48
B	1.245	1.255	31.62	31.88
C	—	0.157	—	4.00
D	0.037	0.041	0.95	1.05
E	2.507 BSC		63.675 BSC	
F	0.250 BSC		6.35 BSC	
F1	0.125 BSC		3.175 BSC	
G	0.050 BSC		1.27 BSC	
H	—	0.010	—	0.25
J	0.046	0.054	1.17	1.37
K	0.100	—	2.54	—
L	5.014 BSC		127.35 BSC	
M	0.075	0.083	1.90	2.10
N	0.118	0.128	3.00	3.25
P	0.158	—	4.00	—
R	0.118	—	3.00	—
S	1.700 BSC		43.18 BSC	
V	0.158	—	4.00	—
W	0.114	0.122	2.90	3.10
AB	—	0.106	—	2.70
AC	0.118 BSC		3.00 BSC	
AD	0.700 BSC		17.78 BSC	
AE	0.039 BCS		1.00 BSC	
AF	0.154	0.161	3.90	4.10



VIEW AA

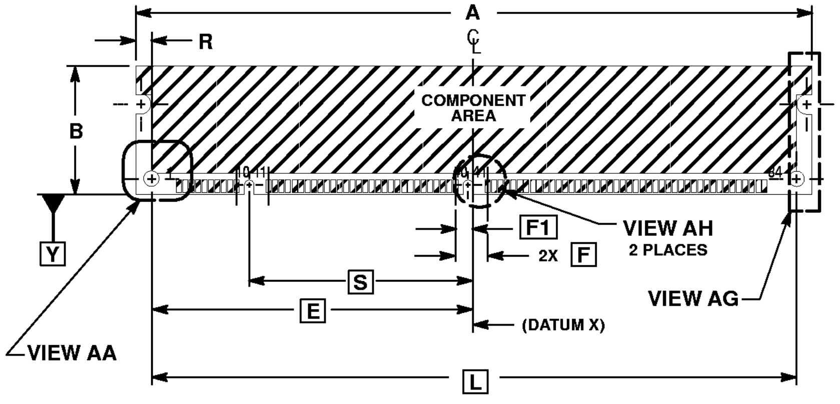


VIEW AH

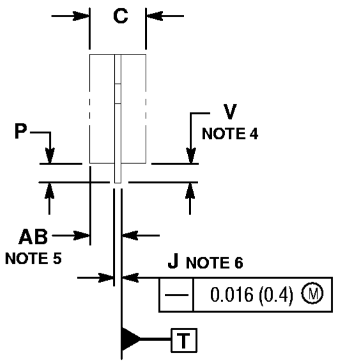


VIEW AG

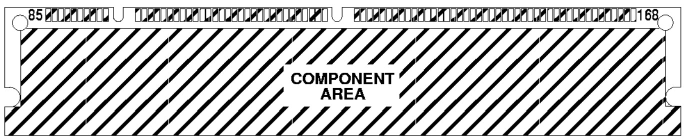
4M x 64 (32MB)
168–LEAD DIMM
CASE 1115–01



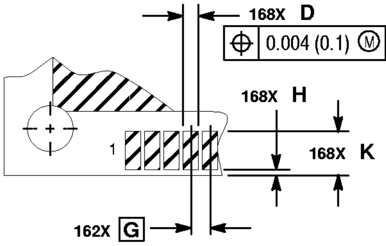
FRONT VIEW



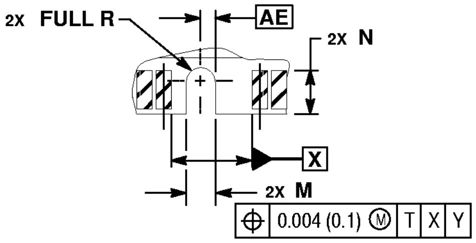
SIDE VIEW



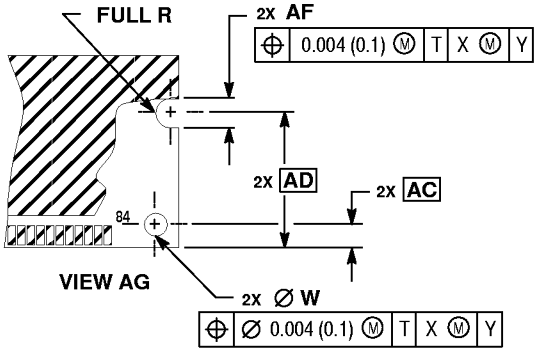
BACK VIEW



VIEW AA



VIEW AH



VIEW AG

NOTES:
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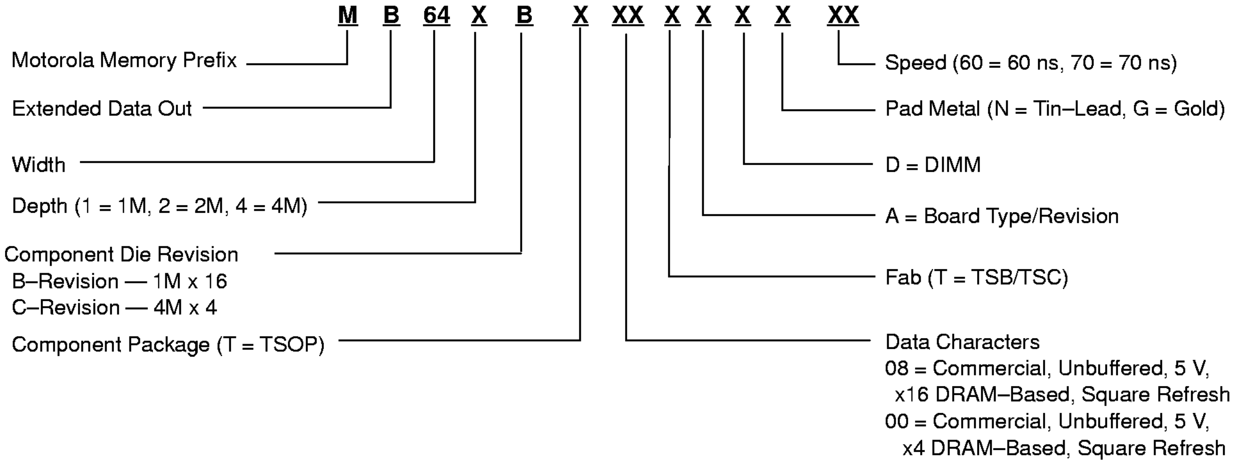
B	0.995	1.005	25.27	25.53
C	—	0.354	—	9.00
D	0.037	0.041	0.95	1.05
E	2.507 BSC		63.675 BSC	
F	0.250 BSC		6.35 BSC	
F1	0.125 BSC		3.175 BSC	
G	0.050 BSC		1.27 BSC	
H	—	0.010	—	0.25
J	0.046	0.054	1.17	1.37
K	0.100	—	2.54	—
L	5.014 BSC		127.35 BSC	
M	0.075	0.083	1.90	2.10
N	0.118	0.128	3.00	3.25
P	0.158	—	4.00	—
R	0.118	—	3.00	—
S	1.700 BSC		43.18 BSC	
V	0.158	—	4.00	—
W	0.114	0.122	2.90	3.10
AB	—	0.205	—	5.20
AC	0.118 BSC		3.00 BSC	
AD	0.700 BSC		17.78 BSC	
AE	0.039 BCS		1.00 BSC	
AF	0.154	0.161	3.90	4.10

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MB641BT08TADG60
MB641BT08TADG70

MB642BT08TADG60
MB642BT08TADG70

MB644CT00TADG60
MB644CT00TADG70