Integrated Device Technology, Inc.

RISC FLOATING POINT ACCELERATOR (FPA)

IDT79R3010A
IDT79R3010AE

FEATURES:

- Hardware Support of Single and Double-Precision Operations:
  - — Floating-Point Add
  - — Floating-Point Subtract
  - — Floating-Point Multiply
  - — Floating-Point Divide
  - — Floating-Point Comparisons
  - — Floating-Point Conversions
- Sustained performance:
  - — 11 MFLOPS single precision LINPACK
  - — 7.3 MFLOPS double precision LINPACK
- 16.7MHz through 40MHz operation
- Direct, high-speed interface with IDT79R3000A and IDT79R3001 Processor
- Supports Full Conformance With IEEE 754-1985 Floating-PointSpecification
- Full 64-bit operation using sixteen 64-bit data registers
- High-speed CMOS technology
- 32-bit status/control register providing access to all IEEE-Standard exception handling
- Load/store architecture allows data movement directly between FPA and memory or between CPU and FPA
- Overlapped operation of independent floating point ALUs

DESCRIPTION:

The IDT79R3010A Floating-Point Accelerator (FPA) operates in conjunction with the IDT79R3000A Processor and extends the IDT79R3000As instruction set to perform arithmetic operations on values in floating-point representations. The IDT79R3010A FPA, with associated system software, fully conforms to the requirements of ANSI/IEEE Standard 754-1985, "IEEE Standard for Binary Floating-Point Arithmetic." In addition, the architecture fully supports the standard's recomendations.

This data sheet provides an overview of the features and architecture of the 79R3010A FPA. A more detailed description of the operation of the device is incorporated in the *R3000A Family Hardware User's Manual*, available from IDT, and a more detailed architectural overview is provided in the *MIPS RISC Architecture* book, available from MIPS/SGI.

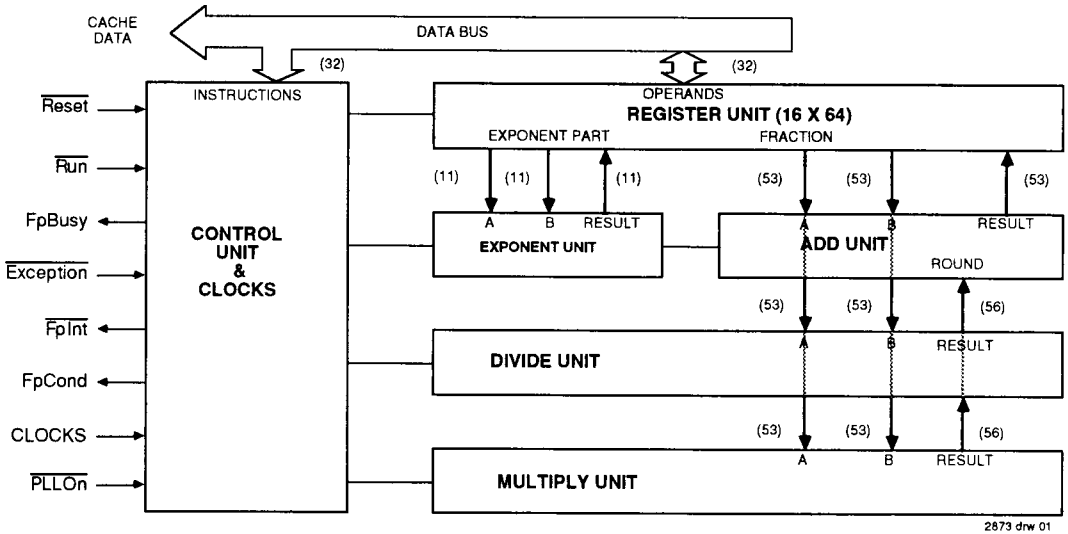

Figure 1. IDT79R3010A Functional Block Diagram

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IDT79R3010A FPA REGISTERS

The IDT79R3010A FPA provides 32 general purpose 32-bit registers, a Control/Status register, and a Revision Identification register. The tightly-coupled coprocessor interface causes the register resources of the FPA to appear to the systems programmers as an extension of the CPU internal registers. The FPA registers are shown in Figure 2.

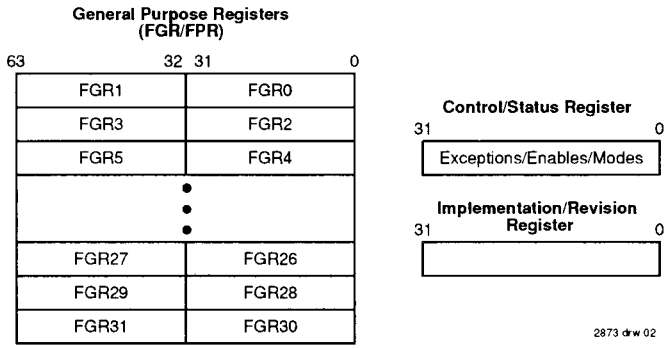

Figure 2. IDT79R3010A FPA Registers

Floating-point coprocessor operations reference three types of registers:

- Floating-Point Control Registers (FCR)
- Floating-Point General Registers (FGR)
- Floating-Point Registers (FPR)

Floating-Point General Registers (FGR)

There are 32 Floating-Point General Registers (FGR) on the FPA. They represent directly-addressable 32-bit registers, and can be accessed by Load, Store, or Move Operations.

Floating-Point Registers (FPR)

The 32 FGRs described in the preceding paragraph are also used to form sixteen 64-bit Floating-Point Registers (FPR). Pairs of general registers (FGRs), for example FGR0 and FGR1 (refer to Figure 2) are physically combined to form a single 64-bit FPR. The FPRs hold a value in either single- or double-precision floating-point format. Double-precision format FPRs are formed from two adjacent FGRs.

Floating-Point Control Registers (FCR)

There are 2 Floating-Point Control Registers (FCR) on the FPA. They can be accessed only by Move operations and include the following:

- Control/Status register, used to control and monitor exceptions, operating modes, and rounding modes;
- Revision register, containing revision information about the FPA.

COPROCESSOR OPERATION

The FPA continually monitors the IDT79R3000A processor instruction stream. If an instruction does not apply to the coprocessor, it is ignored; if an instruction does apply to the coprocessor, the FPA executes that instruction and transfers necessary result and exception data synchronously to the IDT79R3000A main processor.

The FPA performs three types of operations:

- Loads and Stores;
- Moves;
- Two- and three-register floating-point operations.

Load, Store, and Move Operations

Load, Store, and Move operations move data between memory or the IDT79R3000A Processor registers and the IDT79R3010A FPA registers. These operations perform no format conversions and cause no floating-point exceptions. Load, Store, and Move operations reference a single 32-bit word of either the Floating-Point General Registers (FGR) or the Floating-Point Control Registers (FCR).

Floating-Point Operations

The FPA supports the folowing single- and double-precision format floating-point operations:

- Add
- Subtract
- Multiply
- Divide
- Absolute Value
- Move
- Negate
- Compare

In addition, the FPA supports conversions between single- and double-precision floating-point formats and fixed-point formats.

The FPA incorporates separate Add/Subtract, Multiply, and Divide units, each capable of independent and concurrent operation. Thus, to achieve very high performance, floating point divides can be overlapped with floating point multiplies and floating point additions. These floating point operations occur independently of the actions of the CPU, allowing further overlap of integer and floating point operations. Figure 3 illustrates an example of the types of overlap permissible.

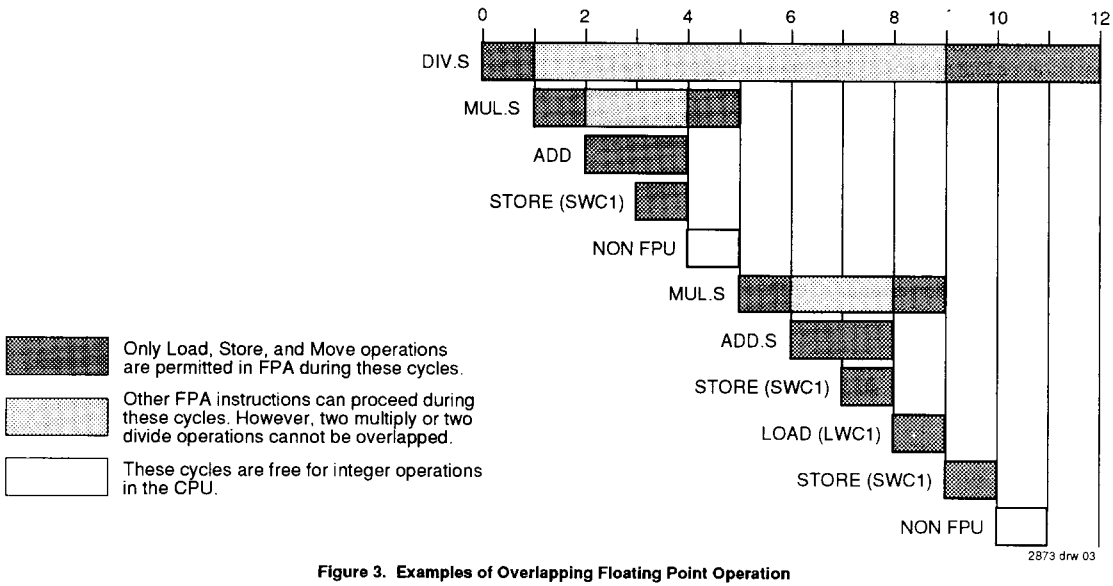

Figure 3. Examples of Overlapping Floating Point Operation

Exceptions

The IDT79R3010A FPA supports all five IEEE standard exceptions:

- Invalid Operation
- Inexact Operation
- Division by Zero
- Overflow
- Underflow

The FPA also supports the optional, Unimplemented Operation exception that allows unimplemented instructions to trap to software emulation routines.

The FPA provides precise exception capability to the CPU; that is, the execution of a floating point operation which generates an exception causes that exception to occur at the CPU instruction which caused the operation. This precise exception capability is a requirement in applications and languages which provide a mechanism for local software exception handlers within software modules.

INSTRUCTION SET OVERVIEW

All IDT79R3010A instructions are 32 bits long and they can be divided into the folowing groups:

- **Load/Store and Move** instructions move data between memory, the main processor and the FPA general registers.
- **Computational** instructions perform arithmetic operations on floating point values in the FPA registers.
- **Conversion** instructions perform conversion operations between the various data formats.
- **Compare** instructions perform comparisons of the contents of registers and set a condition bit based on the results. The result of the compare operation is output on the FpCond output of the FPA, which is typically used as CpCond1 on the CPU for use in coprocessor branch operations.

Table 1 lists the instruction set of the IDT79R3010A FPA.

OP	Description	OP	Description
	Load/Store/Move Instructions		**Computational Instructions**
LWC1	Load Word to FPA	**ADD.fmt**	Floating-point Add
SWC1	Store Word from FPA	**SUB.fmt**	Floating-point Subtract
MTC1	Move Word to FPA	**MUL. fmt**	Floating-point Multiply
MFC1	Move Word from FPA	**DIV.fmt**	Floating-point Divide
CTC1	Move Control word to FPA	**ABS.fmt**	Floating-point Absolute value
CFC1	Move Control word from FPA	**MOV.fmt**	Floating-point Move
		NEG.fmt	Floating-point Negate
	Conversion Instructions		**Compare Instructions**
CVT.S.fmt	Floating-point Convert to Single FP	**C.cond.fmt**	Floating-point Compare
CVT.D.fmt	Floating-point Convert to Double FP		
CVT.W.fmt	Floating-point Convert to fixed-point		

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Table 1. IDT79R3010A Instruction Summary

ID79R3010 PIPELINE ARCHITECTURE

The IDT79R3010A FPA provides an instruction pipeline that parallels that of the IDT79R3000A processor. The FPA, however, has a 6-stage pipeline instead of the 5-stage pipeline of the IDT79R3000: the additional FPA pipe stage is used to provide efficient coordination of exception responses between the FPA and main processor.

The execution of a single IDT79R3010A instruction consists of six primary steps:

1) **IF**—Instruction Fetch. The main processor calculates the insruction address required to read an instruction from the I-Cache. No action is required of the FPA during this pipe stage since the main processor is responsible for address generation.
2) **RD**—The instruction is present on the data bus during phase 1 of this pipe stage and the FPA decodes the instruction on the bus to determine if it is an instruction for the FPA.
3) **ALU**—If the instruction is an FPA instruction, instruction execution commences during this pipe stage.
4) **MEM**—If this is a coprocessor load or store instruction, the FPA presents or captures the data during phase 2 of this pipe stage.
5) **WB**—The FPA uses this pipe stage solely to deal with exceptions.
6) **FWB**—The FPA uses this stage to write back ALU results to its register file. This stage is the equivalent of the WB stage in the IDT79R3000A main processor.

Each of these steps requires approximately one FPA cycle as shown in Figure 3 (parts of some operations spill over into another cycle while other operations require only 1/2 cycle).

INSTRUCTION EXECUTION

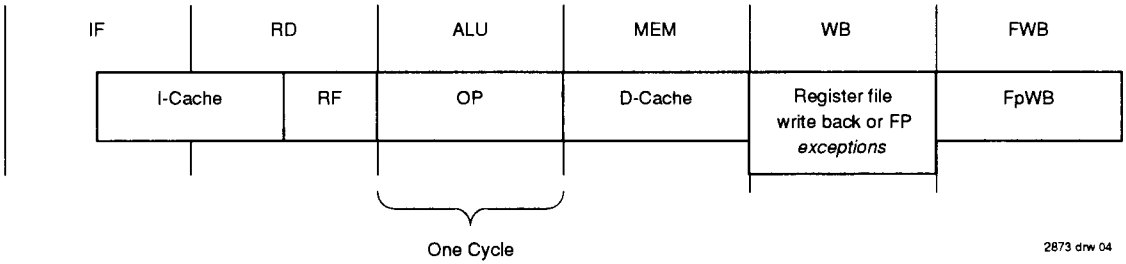

Figure 4. IDT79R3010A Instruction Summary

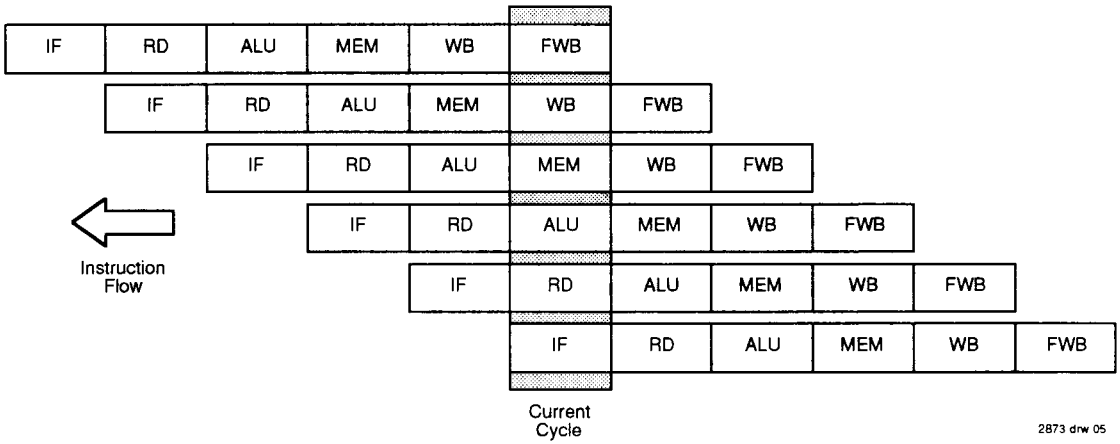

Figure 5. IDT79R3010A Instruction Pipeline

The IDT79R3010A uses a 6-stage pipeline to achieve an instruction execution rate approaching one instruction per FPA cycle. Thus, execution of six instructions at a time are overlapped as shown in Figure 5.

This pipeline operates efficiently because different FPA resources (address and data bus accesses, ALU operations. register accesses, and so on) are utilized on a non-interfering basis.

PACKAGE THERMAL SPECIFICATIONS

The IDT79R3010A utilizes special packaging techniques to improve both the thermal and electrical characteristics of the floating point accelerator.

In order to improve the electrical characteristics of the device, the package is constructed using multiple signal planes, including individual power planes and ground planes to reduce noise associated with high-frequency TTL parts.

In order to improve the thermal characteristics of the floating point accelerator, the device is housed using cavity down packaging for the flatpack and the PGA (the J-bend CerQuad is cavity up). In addition, these packages incorporate a copper-tungsten thermal slug designed to efficiently transfer heat from the die to the case of the package, and thus effectively lower the thermal resistance of the package. The use of an additional external heat sink affixed to the package thermal slug further decreases the effective thermal resistance of the package.

The case temperature may be measured in any environment to determine whether the device is within the specified operating range. The case temperature should be measured at the center of the top surface opposite the package cavity (the package cavity is the side where the package lid is mounted).

The equivalent allowable ambient temperature, T_A, can be calculated using the thermal resistance from case to ambient ($\varnothing ca$) for the given package. The following equation relates ambient and case temperature:

$$T_A = T_C - P * \varnothing ca$$

where P is the maximum power consumption, calculated by using the maximum Icc from the DC Electrical Characteristic section.

Typical values for $\varnothing ca$ at various airflows are shown in Table 2 for the various CPU packages.

	Airflow - (ft/min)					
	0	200	400	600	800	1000
$\varnothing ca$ (84-PGA)	22	8	3	2	1.5	1.0
$\varnothing ca$ (84-Flatpack)	22	9	4	3	2	1.5
$\varnothing ca$ (84-CerQuad)	25	17	12	8	7	6

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Table 2. Thermal Resistance (Oca) at Various Airflows

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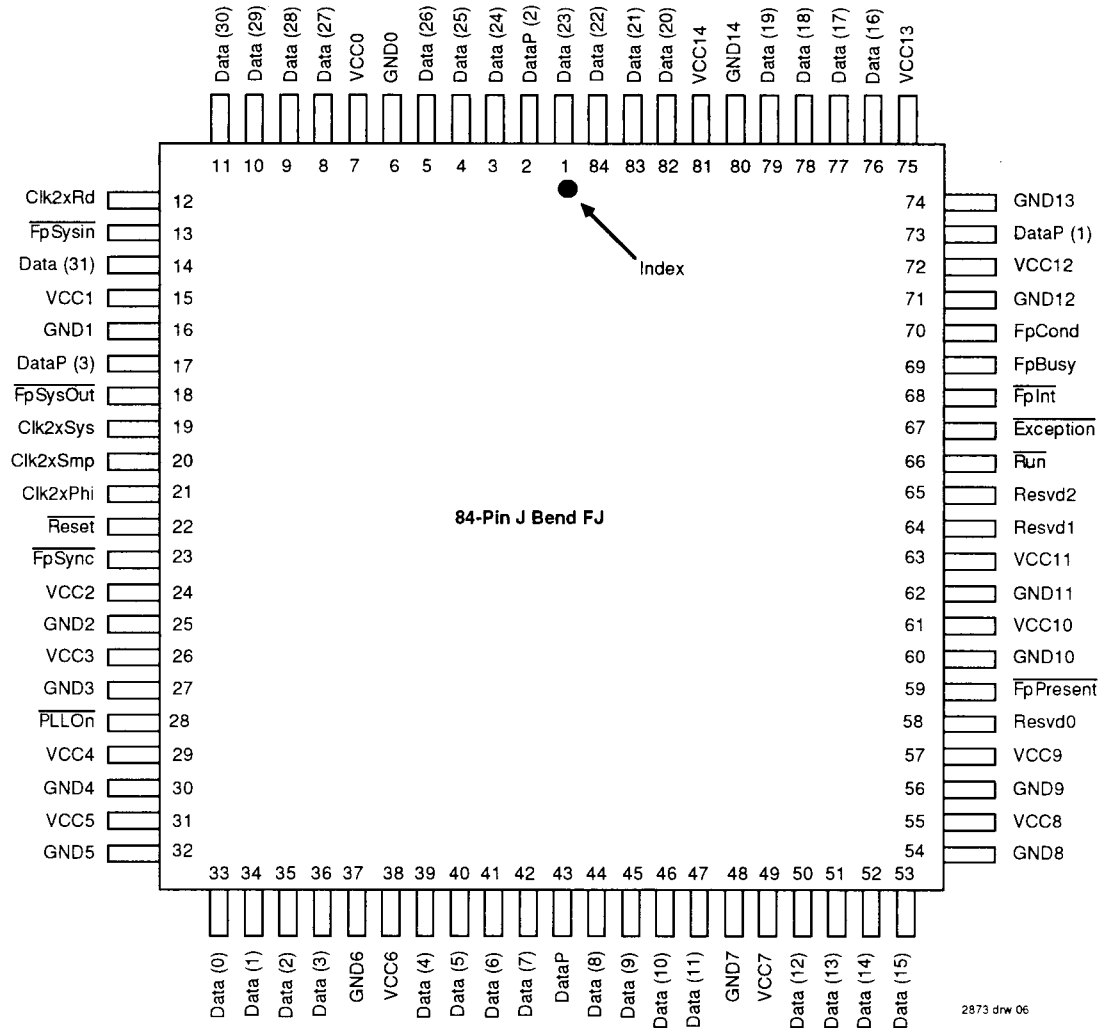
PIN CONFIGURATION[1]
(Top View)



NOTE:
1. Reserved pins must not be connected.

PIN CONFIGURATION[1]
(Ceramic, Cavity Down) – BOTTOM VIEW

	1	2	3	4	5	6	7	8	9	10	11	12
M	Vss	Vcc	Data 17	DataP 1	Vss	FP Cond	$\overline{\text{FPInt}}$	Vss	$\overline{\text{Run}}$	Rsrvd 1	Vcc	Vss
L	Data 21	Data 20	Data 18	Data 16	Vcc	FPBusy	Excep-tion	Vcc	Rsrvd 2	$\overline{\text{FP}}$ Present	Data 15	Data 14
K	Vss	Vcc	Data 19							Rsrvd 0	Vcc	Vss
J	Data 23	Data 22									Data 13	Data 12
H	Data 24	DataP 2									Data 11	Data 10
G	Data 26	Data 25				**84-Pin Ceramic Pin Grid Array**					Vcc	Vss
F	Vss	Vcc									Data 8	Data 9
E	Data 27	Data 28									Data 7	DataP 0
D	Data 29	Data 30									Data 5	Data 6
C	Vss	Vcc	Clk2x Rd							Data 2	Vcc	Vss
B	$\overline{\text{Fp}}$ SysIn	Data 31	DataP 3	Vcc	Clk2x Sys	Vcc	Clk2x Phi	Vcc	$\overline{\text{PllOn}}$	Data 1	Data 3	Data 4
A	Vss	Vcc	$\overline{\text{FpSys}}$ Out	Vss	Clk2x Smp	Vss	$\overline{\text{Reset}}$	Vss	$\overline{\text{FP}}$ Sync	Data 0	Vcc	Vss

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NOTE:
1. Reserved pins must not be connected.

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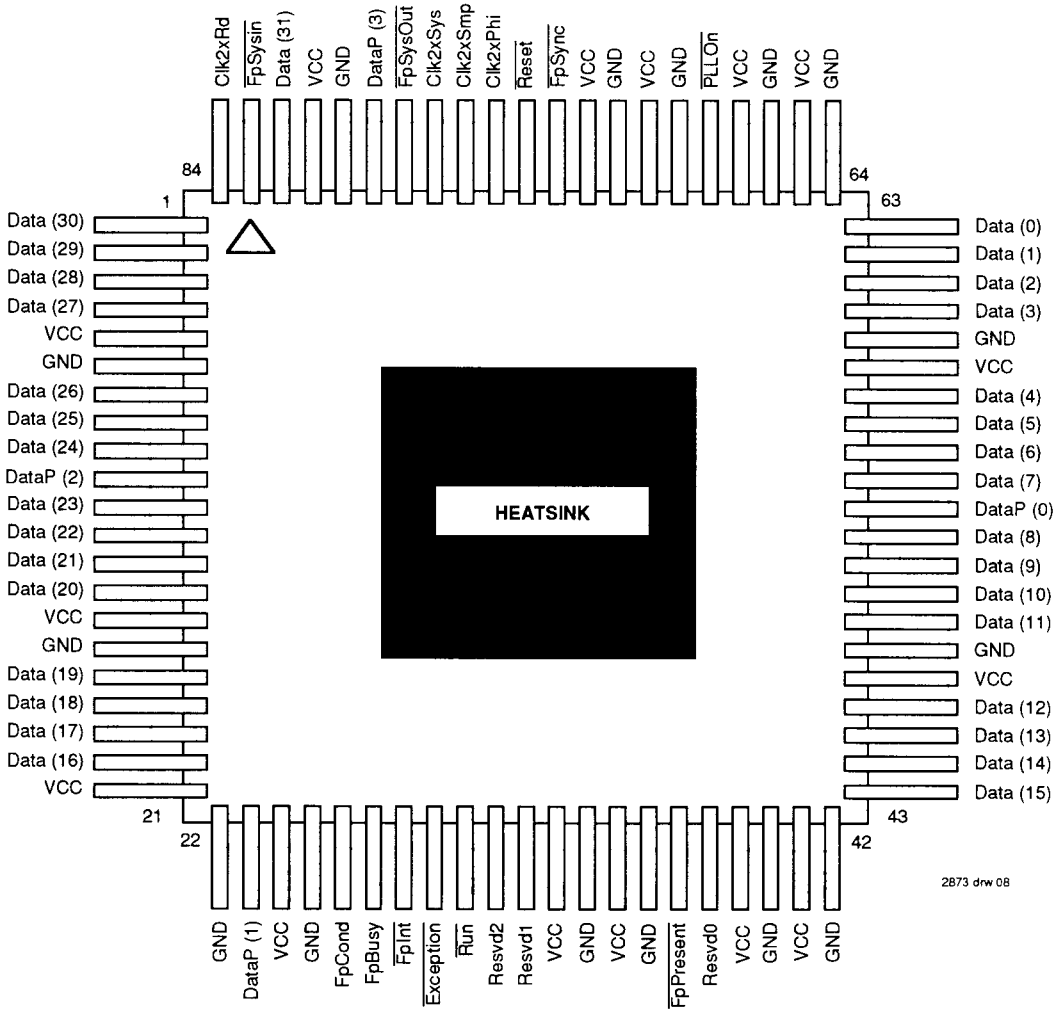
PIN CONFIGURATION[1]
84–L QUAD FLATPACK (CAVITY DOWN)
TOP VIEW



NOTE:
1. Reserved pins must not be connected.

PIN DESCRIPTIONS

Pin Name	I/O	Description
Data (0-31)	I/O	A multiplexed 32-bit bus used for instruction and data transfers on phase 1 and phase 2, respectively.
DataP (0-3)	O	A 4-bit bus containing even parity over the data bus. Parity is generated by the FPA on stores.
$\overline{\text{Run}}$	I	Input to the FPA which indicates whether the processor-coprocessor system is in the run or stall state.
$\overline{\text{Exception}}$	I	Input to the FPA which indicates exception related status information.
FpBusy	O	Signal to the CPU indicating a request for a coprocessor busy stall.
FpCond	O	Signal to the CPU indicating the result of the last comparision operation.
$\overline{\text{FpInt}}$	O	Signal to the CPU indicating that a floating-point exception has occured for the current FPA instruction.
$\overline{\text{Reset}}$	I	Synchronous initialization input used to distinguish the processor-FPA synchronization period from the execution period. $\overline{\text{Reset}}$ must be synchronized by the leading edge of $\overline{\text{SysOut}}$ from the CPU.
$\overline{\text{PllOn}}$	I	Input which during the reset period determines whether the phase lock mechanism is enabled and during the execution period determines the output timing model.
$\overline{\text{FpPresent}}$	O	Output which is pulled to ground through an impedance of approximately 0.5kΩ. By providing an external pullup on this line, an indication of the presence or absence of the FPA can be obtained.
Clk2xSys	I	A double frequency clock input used for generating $\overline{\text{FpSysOut}}$.
Clk2xSmp	I	A double frequency clock input used to determine the sample point for data coming in to the FPA.
Clk2xRd	I	A double frequency clock input used to determine the disable point for the data drivers.
Clk2xPhi	I	A double frequency clock input used to determine the position of the internal phases, phase 1 and phase 2.
$\overline{\text{FpSysOut}}$	O	Synchronization clock from the FPA.
$\overline{\text{FpSysIn}}$	I	Input used to receive the synchronization clock from the FPA.
$\overline{\text{FpSync}}$	I	Input used to receive the synchronization clock from the CPU.

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ABSOLUTE MAXIMUM RATINGS(1, 3)

Symbol	Rating	Commercial	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
TA, TC	Operating Temperature	0 to +70(4) (Ambient) 0 to +90(5) (Case)	°C
TBIAS	Case Temperature Under Bias	–55 to +125(4) 0 to +90(5)	°C
TSTG	Storage Temperature	–55 to +125	°C
IIN	Input Voltage	–0.5 to +7.0	V

2873 tbl 04

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VIN minimum = –3.0V for pulse width less than 15ns. VIN should not exceed VCC +0.5 Volts.
3. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.
4. 16-33MHz only.
5. 40MHz only.

AC TEST CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
VIH	Input HIGH Voltage	3.0	—	V
VIL	Input LOW Voltage	—	0.4	V
VIHS	Input HIGH Voltage	3.5	—	V
VILS	Input LOW Voltage	—	0.4	V
VIHC	Input HIGH Voltage	4.0	—	V
VILC	Input LOW Voltage	—	0.4	V

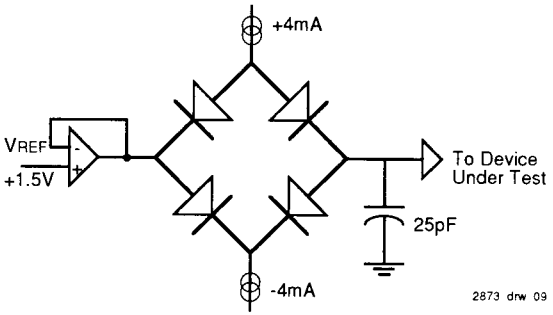
2873 tbl 05

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Commercial 16-33MHz	0°C to +70°C (Ambient)	0V	5.0 ±5%
Commercial 40MHz	0°C to +90°C (Case)	0V	5.0 ±5%

2873 tbl 06

OUTPUT LOADING FOR AC TESTING



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DC ELECTRICAL CHARACTERISTICS FOR IDT79R3010A COMMERCIAL TEMPERATURE RANGE (T_A = 0°C to + 70°C, V_{CC} = + 5.0 V ± 5%)

Symbol	Parameter	Test Conditions	16.67 MHz		20.0 MHz		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = –4mA	3.5	—	3.5	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OLFP}	Output LOW Voltage(5)	V_{CC} = Min, I_{OL} = 1.5mA	—	0.5	—	0.5	V
V_{IH}	Input HIGH Voltage(6)		2.0	—	2.0	—	V
V_{IL}	Input LOW Voltage(1)		—	0.8	—	0.8	V
V_{IHS}	Input HIGH Voltage(2,6)		3.0	—	3.0	—	V
V_{ILS}	Input LOW Voltage(1,2)		—	0.4	—	0.4	V
V_{IHC}	Input HIGH Voltage(4,6)		4.0	—	4.0	—	V
V_{ILC}	Input LOW Voltage(1,4)		—	0.4	—	0.4	V
C_{IN}	Input Capacitance(7)		—	10	—	10	pF
C_{OUT}	Output Capacitance(7)		—	10	—	10	pF
I_{CC}	Operating Current	V_{CC} = 5.0V, T_A = 70°C	—	525	—	600	mA
I_{IH}	Input HIGH Leakage(3)	V_{IH} = V_{CC}	—	100	—	100	µA
I_{IL}	Input LOW Leakage(3)	V_{IL} = GND	–100	—	–100	—	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	–100	100	–100	100	µA

2873 tbl 07

DC ELECTRICAL CHARACTERISTICS FOR IDT79R3010AE COMMERCIAL TEMPERATURE RANGE (T_A = 0°C to + 70°C, V_{CC} = + 5.0 V ± 5%)

Symbol	Parameter	Test Conditions	25.0 MHz		33.33 MHz		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = –4mA	3.5	—	3.5	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OLFP}	Output LOW Voltage(5)	V_{CC} = Min, I_{OL} = 1.5mA	—	0.5	—	0.5	V
V_{IH}	Input HIGH Voltage(6)		2.0	—	2.0	—	V
V_{IL}	Input LOW Voltage(1)		—	0.8	—	0.8	V
V_{IHS}	Input HIGH Voltage(2,6)		3.0	—	3.0	—	V
V_{ILS}	Input LOW Voltage(1,2)		—	0.4	—	0.4	V
V_{IHC}	Input HIGH Voltage(4,6)		4.0	—	4.0	—	V
V_{ILC}	Input LOW Voltage(1,4)		—	0.4	—	0.4	V
C_{IN}	Input Capacitance(7)		—	10	—	10	pF
C_{OUT}	Output Capacitance(7)		—	10	—	10	pF
I_{CC}	Operating Current	V_{CC} = 5.0V, T_A = 70°C	—	650	—	700	mA
I_{IH}	Input HIGH Leakage(3)	V_{IH} = V_{CC}	—	100	—	100	µA
I_{IL}	Input LOW Leakage(3)	V_{IL} = GND	–100	—	–100	—	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	–100	100	–100	100	µA

2873 tbl 08

NOTES:

1. V_{IL} Min. = –3.0V for pulse width less than 15ns. V_{IL} should not fall below –0.5V for larger periods.
2. V_{IHS} and V_{ILS} apply to Clk2xSys, Clk2xSmp, Clk2xRd, Clk2xPhi, $\overline{\text{FpSysin}}$, $\overline{\text{FpSync}}$ and $\overline{\text{Reset}}$.
3. These parameters do not apply to the clock inputs.
4. V_{IHC} and V_{ILC} apply to $\overline{\text{Run}}$, $\overline{\text{PllOn}}$ and $\overline{\text{Exception}}$.
5. V_{OLFP} applies to the $\overline{\text{FPPresent}}$ pin only.
6. V_{IH} and V_{IHS} should not be held above V_{CC} + 0.5V.
7. Guaranteed by design.

DC ELECTRICAL CHARACTERISTICS FOR IDT79R3010AE
COMMERCIAL TEMPERATURE RANGE (T_C = 0°C to + 90°C, V_{CC} = + 5.0 V ± 5%)

Symbol	Parameter	Test Conditions	40 MHz		Unit
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = –4mA	3.5	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 4mA	—	0.4	V
V_{OLFP}	Output LOW Voltage(5)	V_{CC} = Min, I_{OL} = 1.5mA	—	0.5	V
V_{IH}	Input HIGH Voltage(6)		2.0	—	V
V_{IL}	Input LOW Voltage(1)		—	0.8	V
V_{IHS}	Input HIGH Voltage(2,6)		3.0	—	V
V_{ILS}	Input LOW Voltage(1,2)		—	0.4	V
V_{IHC}	Input HIGH Voltage(4,6)		4.0	—	V
V_{ILC}	Input LOW Voltage(1,4)		—	0.4	V
C_{IN}	Input Capacitance(7)		—	10	pF
C_{OUT}	Output Capacitance(7)		—	10	pF
I_{CC}	Operating Current	V_{CC} = 5.0V, T_C = 90°C	—	750	mA
I_{IH}	Input HIGH Leakage(3)	V_{IH} = V_{CC}	—	100	µA
I_{IL}	Input LOW Leakage(3)	V_{IL} = GND	–100	—	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	–100	100	µA

2873 tbl 09

NOTES:

1. V_{IL} Min. = –3.0V for pulse width less than 15ns. V_{IL} should not fall below –0.5V for larger periods.
2. V_{IHS} and V_{ILS} apply to Clk2xSys, Clk2xSmp, Clk2xRd, Clk2xPhi, $\overline{\text{FpSysIn}}$, $\overline{\text{FpSync}}$ and $\overline{\text{Reset}}$.
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5. V_{OLFP} applies to the $\overline{\text{FPPresent}}$ pin only.
6. V_{IH} and V_{IHS} should not be held above V_{CC} + 0.5V.
7. Guaranteed by design.

AC ELECTRICAL CHARACTERISTICS FOR IDT79R3010A(1, 3)
COMMERCIAL TEMPERATURE RANGE (T_A = 0°C to +70°C, V_{CC} = +5.0V ± 5%)

Symbol	Parameter	Test Conditions	16.67 MHz		20.0 MHz		Unit
			Min.	Max.	Min.	Max.	
Clock							
TckHigh	Input Clock HIGH(2)	Note 7	12	—	10	—	ns
TckLow	Input Clock LOW(2)	Note 7	12	—	10	—	ns
TckP	Input Clock Period		30	1000	25	1000	ns
	Clk2xSys to Clk2xSmp(5)		0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xRd(5)		0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xPhi(5)		9.0	tcyc/4	7.0	tcyc/4	ns
Timing Paramters							
TDEn	Data Enable(3)		—	-2.0	—	-2.0	ns
TDDis	Data Disable(3)		—	-1.0	—	-1.0	ns
TDVal	Data Valid	Load= 25pF	—	3.0	—	3.0	ns
TRSDS	Reset Set-up		15	—	15	—	ns
TDS	Data Set-up		9.0	—	8.0	—	ns
TDH	Data Hold(3)		-2.5	—	-2.5	—	ns
TFpCond	Fp Condition		—	35	—	30	ns
TFpBusy	Fp Busy		—	15	—	13	ns
TFpInt	Fp Interrupt		—	40	—	35	ns
TFpMov	Fp Move To		—	35	—	30	ns
TRExS	Exception Set-up (Run Cycle)		14	—	12	—	ns
TSExS	Exception Set-up (Stall Cycle)		12	—	10	—	ns
TExH	Exception Hold		0	—	0	—	ns
TRunS	Run Set-up		17	—	15	—	ns
TRunH	Run Hold		-2.0	—	-2.0	—	ns
TStallS	Stall Set-up		10	—	10	—	ns
TStallH	Stall Hold		-2.0	—	-2.0	—	ns
Reset Initialization							
TrstPLL	Reset Timing, Phase-lock on(4, 5)		3000	—	3000	—	Tcyc
Trst	Reset Timing, Phase-lock off(5)		128	—	128	—	Tcyc
Capacitive Load Deration							
CLD	Load Derate(6)		0.5	2.0	0.5	1.0	ns/25pF

2873 tbl 12

NOTES:
1. All timings are referenced to 1.5V.
2. The clock parameters apply to all four 2xClocks: Clk2xSys, Clk2xSmp, Clk2xRd, and Clk2xPhi.
3. This parameter is guaranteed by design.
4. With $\overline{\text{PllOn}}$ asserted, $\overline{\text{Reset}}$ must be asserted for the longer of 3000 clock cycles or 200 microseconds.
5. Tcyc is one CPU clock cycle (two cycles of a 2x clock).
6. No two signals on a given device will derate for a given load by a difference greater than 15%.
7. Clock transition time < 5ns.

6

AC ELECTRICAL CHARACTERISTICS FOR IDT79R3010AE(1, 3)
COMMERCIAL TEMPERATURE RANGE (T_A = 0°C to +70°C, V_{CC} = +5.0V ± 5%)

Symbol	Parameter	Test Conditions	25.0 MHz		33.33 MHz		Unit
			Min.	Max.	Min.	Max.	
Clock							
TCkHigh	Input Clock High(2)	Note 7	8.0	—	6.0	—	ns
TCkLow	Input Clock Low(2)	Note 7	8.0	—	6.0	—	ns
TCkP	Input Clock Period		20	1000	15	1000	ns
	Clk2xSys to Clk2XSmp(5)		0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xRd(5)		0	tcyc/4	0	tcyc/4	ns
	Clk2xSmp to Clk2xPhi(5)		5.0	tcyc/4	3.5	tcyc/4	ns
Timing Paramters							
TDEn	Data Enable(3)		—	–1.5	—	–1.0	ns
TDDis	Data Disable(3)		—	–0.5	—	–0.5	ns
TDVal	Data Valid	Load= 25pF	—	2.0	—	2.0	ns
TRSDS	Reset Set-up		10	—	10	—	ns
TDS	Data Set-up		6.0	—	4.5	—	ns
TDH	Data Hold(3)		–2.5	—	–2.5	—	ns
TFpCond	Fp Condition		—	25	—	17	ns
TFpBusy	Fp Busy		—	10	—	7.0	ns
TFpInt	Fp Interrupt		—	25	—	18	ns
TFpMov	Fp Move To		—	25	—	16	ns
TRExS	Exception Set-up (Run Cycle)		11	—	9.0	—	ns
TSExS	Exception Set-up (Stall Cycle)		8.0	—	6.5	—	ns
TExH	Exception Hold		0	—	0	—	ns
TRunS	Run Set-up		15	—	12.5	—	ns
TRunH	Run Hold		–2.0	—	–1.5	—	ns
TStallS	Stall Set-up		9.0	—	7.0	—	ns
TStallH	Stall Hold		–2.0	—	–2.0	—	ns
Reset Initialization							
TrstPLL	Reset Timing, Phase-lock on(4, 5)		3000	—	3000	—	Tcyc
Trst	Reset Timing, Phase-lock off(5)		128	—	128	—	Tcyc
Capacitive Load Deration							
CLD	Load Derate(6)		0.5	1.0	0.5	1.0	ns/25pF

2873 tbl 13

NOTES:
1. All timings are referenced to 1.5V.
2. The clock parameters apply to all four 2xClocks: Clk2xSys, Clk2xSmp, Clk2xRd, and Clk2xPhi.
3. This parameter is guaranteed by design.
4. With $\overline{\text{PllOn}}$ asserted, $\overline{\text{Reset}}$ must be asserted for the longer of 3000 clock cycles or 200 microseconds.
5. Tcyc is one CPU clock cycle (two cycles of a 2x clock).
6. No two signals on a given device will derate for a given load by a difference greater than 15%.
7. Clock transition time < 2.5ns for 33MHz; clock transition time < 5ns for all other speeds.

AC ELECTRICAL CHARACTERISTICS FOR IDT79R3010AE(1, 3)
COMMERCIAL TEMPERATURE RANGE (Tc = 0°C to +90°C, Vcc = +5.0V ± 5%)

Symbol	Parameter	Test Conditions	40.0 MHz		Unit
			Min.	Max.	
Clock					
TckHigh	Input Clock HIGH(2)	Note 7	5.5	—	ns
TckLow	Input Clock LOW(2)	Note 7	5.5	—	ns
TckP	Input Clock Period		12.5	1000	ns
	Clk2xSys to Clk2XSmp(5)		0	tcyc/4	ns
	Clk2xSmp to Clk2xRd(5)		0	tcyc/4	ns
	Clk2xSmp to Clk2xPhi(5)		3.0	tcyc/4	ns
Timing Paramters					
TDEn	Data Enable(3)		—	–1.0	ns
TDDis	Data Disable(3)		—	–0.5	ns
TDVal	Data Valid	Load= 25pF	—	2.0	ns
TRSDS	Reset Set-up		8.0	—	ns
TDS	Data Set-up		4.0	—	ns
TDH	Data Hold(3)		–2.5	—	ns
TFpCond	Fp Condition		—	16	ns
TFpBusy	Fp Busy		—	6.0	ns
TFpInt	Fp Interrupt		—	17	ns
TFpMov	Fp Move To		—	16	ns
TRExS	Exception Set-up (Run Cycle)		8.5	—	ns
TSExS	Exception Set-up (Stall Cycle)		5.5	—	ns
TExH	Exception Hold		0	—	ns
TRunS	Run Set-up		9.0	—	ns
TRunH	Run Hold		–1.5	—	ns
TStallS	Stall Set-up		6.0	—	ns
TStallH	Stall Hold		–2.0	—	ns
Reset Initialization					
TrstPLL	Reset Timing, Phase-lock on(4, 5)		3000	—	Tcyc
Trst	Reset Timing, Phase-lock off(5)		128	—	Tcyc
Capacitive Load Deration					
CLD	Load Derate(6)		0.5	1.0	ns/25pF

2873 tbl 14

NOTES:
1. All timings are referenced to 1.5V.
2. The clock parameters apply to all four 2xClocks: Clk2xSys, Clk2xSmp, Clk2xRd, and Clk2xPhi.
3. This parameter is guaranteed by design.
4. With $\overline{\text{PllOn}}$ asserted, $\overline{\text{Reset}}$ must be asserted for the longer of 3000 clock cycles or 200 microseconds.
5. Tcyc is one CPU clock cycle (two cycles of a 2x clock).
6. No two signals on a given device will derate for a given load by a difference greater than 15%.
7. Clock transition time < 2.5ns.

6

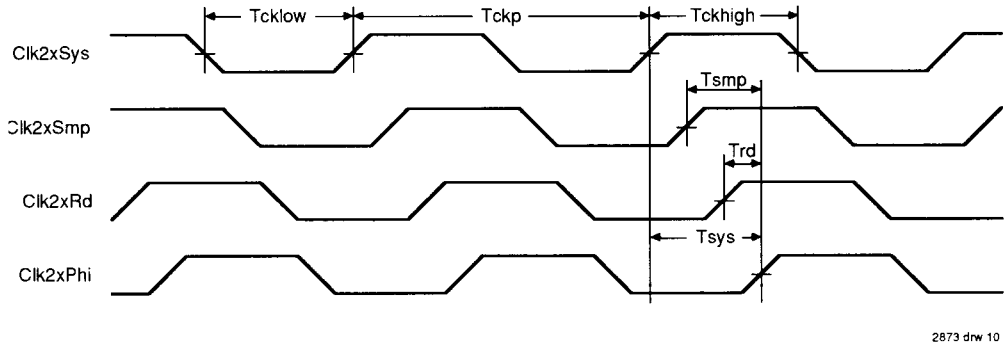


Figure 6. Input "2x" Clock Timing

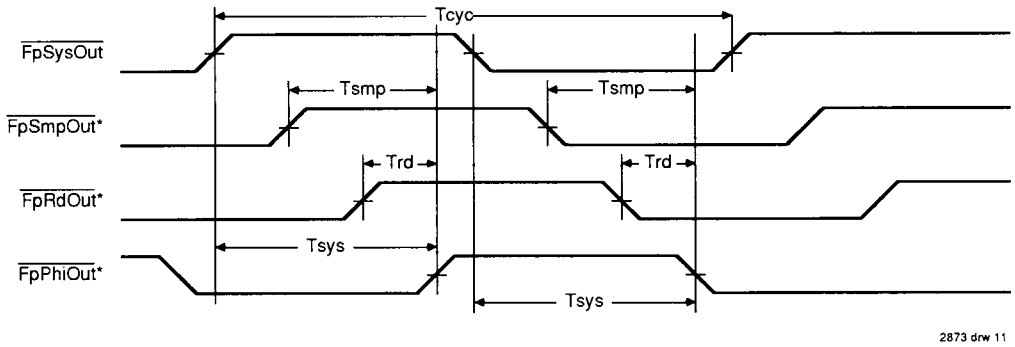


Figure 7. Processor Reference Clock

* These signals are not actually output from the floating point processor. They are drawn to provide a reference for other timing diagrams.

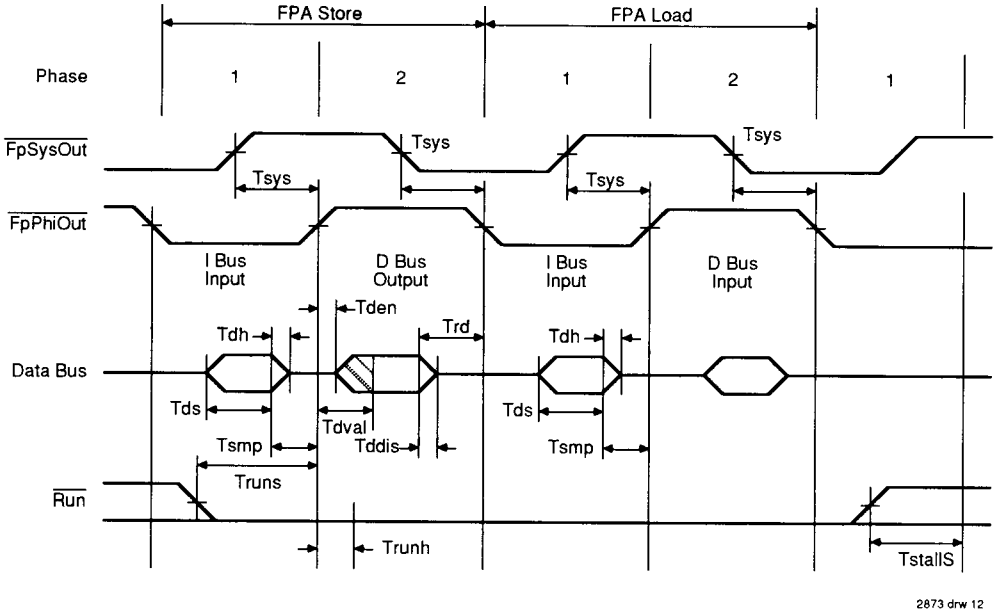


Figure 8. Floating Point Load/Store Timing

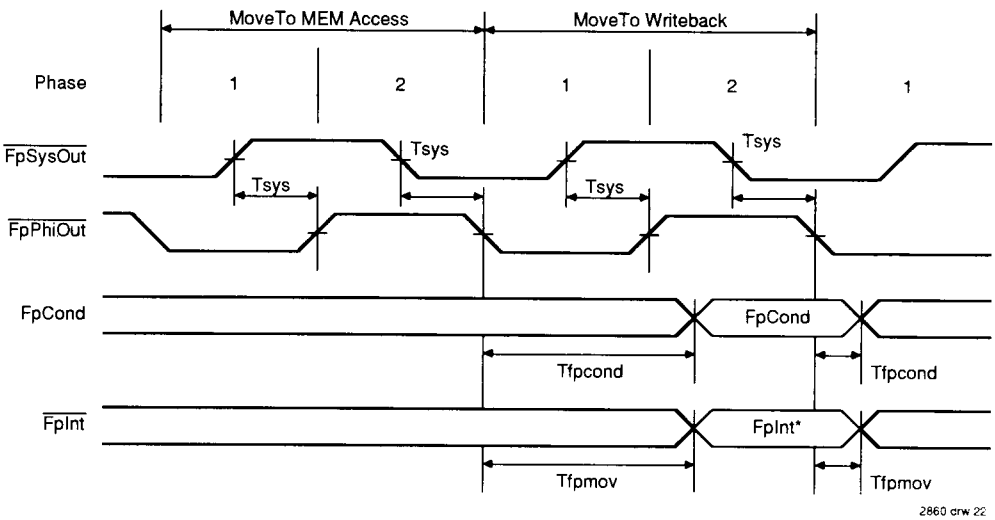


Figure 9. Move to FPC Status Timing

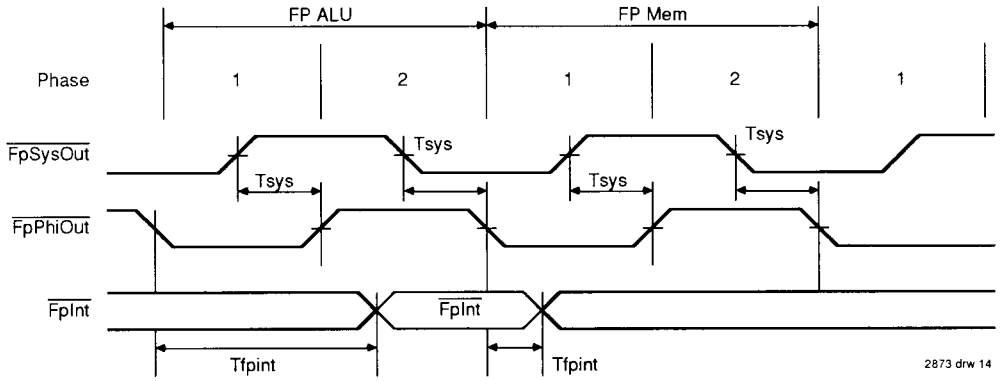


Figure 10. Floating Point Interrupt Timing

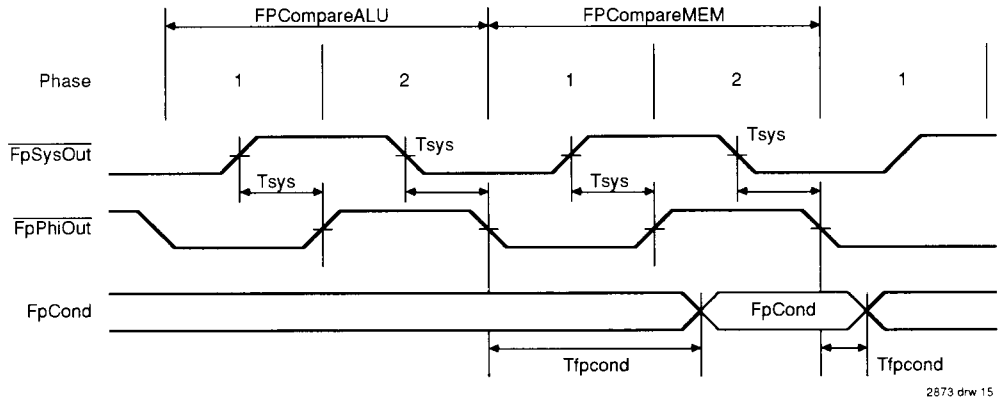


Figure 11. Floating Point Condition Timing

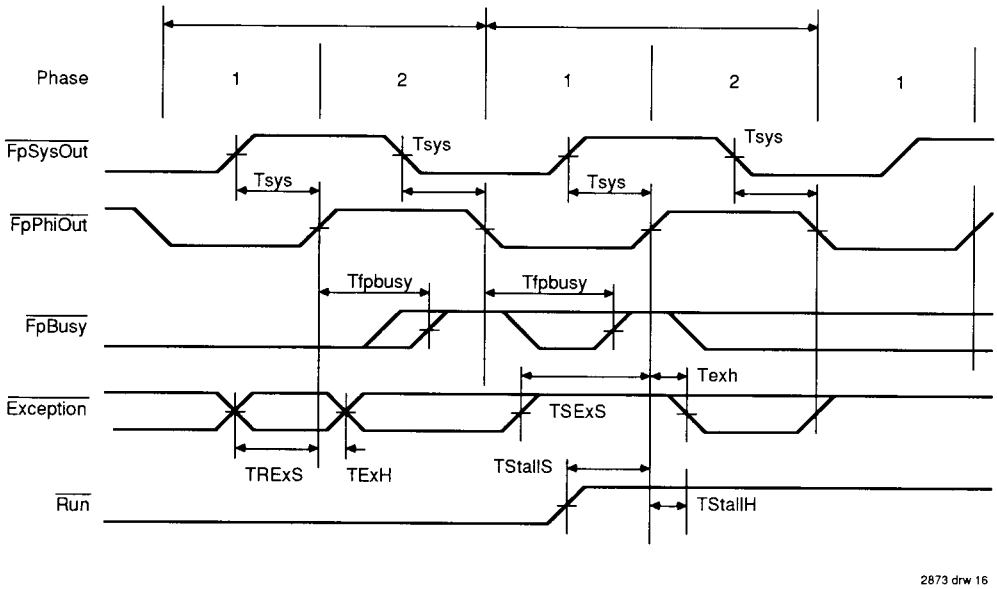


Figure 12. Floating Point Busy, Exception Timing

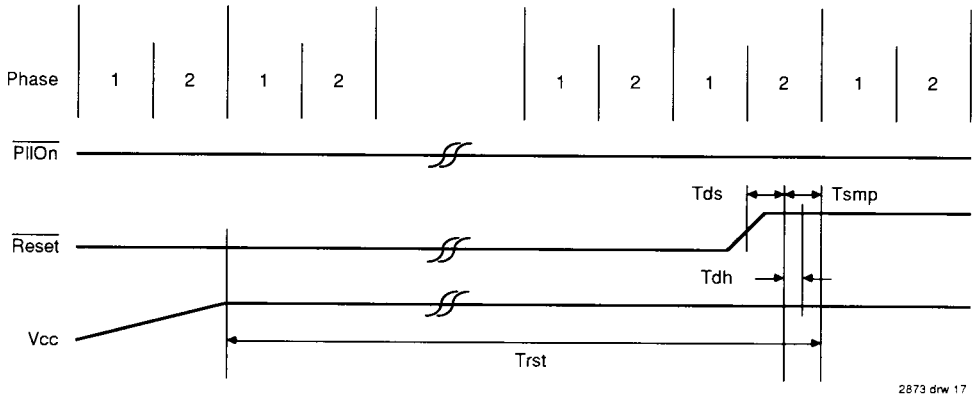
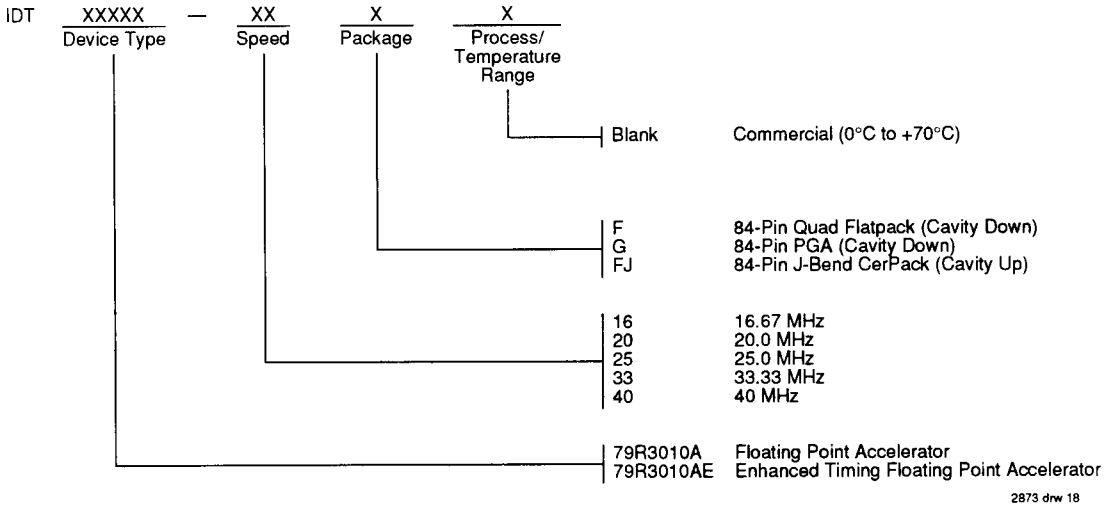


Figure 13. Power-On Reset Timing

6

ORDERING INFORMATION



VALID COMBINATIONS

IDT	79R3010A - 16, 20	All packages
	79R3010AE - 25, 33, 40	G