

# Horizontal and vertical deflection controller for VGA/XGA and autosync monitors

TDA4851

## FEATURES

- VGA operation fully implemented including alignment-free vertical and E/W amplitude presettings
- 4th VGA mode easy applicable (XGA, Super VGA)
- Autosync operation externally selectable
- Low jitter
- All adjustments DC-controllable
- Alignment-free oscillators
- Sync separators for video or horizontal and vertical TTL sync levels regardless of polarity
- Horizontal oscillator with PLL1 for sync and PLL2 for flyback
- Constant vertical and E/W amplitude in autosync operation
- DC-coupling to vertical power amplifier
- Internal supply voltage stabilization with excellent ripple rejection to ensure stable geometrical adjustments

## QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_P$	positive supply voltage (pin 1)	9.2	12	16	V
$I_P$	supply current	–	40	–	mA
$V_{i\ sync}$	AC-coupled composite video signal with negative-going sync (peak-to-peak value, pin 9)	–	1	–	V
	sync slicing level	–	120	–	mV
	DC-coupled TTL-compatible horizontal sync signal (peak-to-peak value, pin 9)	1.7	–	–	V
	slicing level	1.2	1.4	1.6	V
	DC-coupled TTL-compatible vertical sync signal (peak-to-peak value, pin 10)	1.7	–	–	V
	slicing level	1.2	1.4	1.6	V
$I_{oV}$	vertical differential output current (peak-to-peak value, pins 5 and 6)	–	1	–	mA
$I_{oH}$	horizontal sink output current on pin 3	–	–	60	mA
$T_{amb}$	operating ambient temperature range	0	–	+70	°C

## GENERAL DESCRIPTION

The TDA4851 is a monolithic integrated circuit for economical solutions in VGA/XGA and autosync monitors. The IC incorporates the complete horizontal and vertical small signal processing.

VGA-dependent mode detection and settings are performed on chip. In conjunction with TDA4860/61/65, or TDA8351 (vertical output circuits) the ICs offer an extremely advanced system solution.

## ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4851	20	DIL	plastic	SOT146

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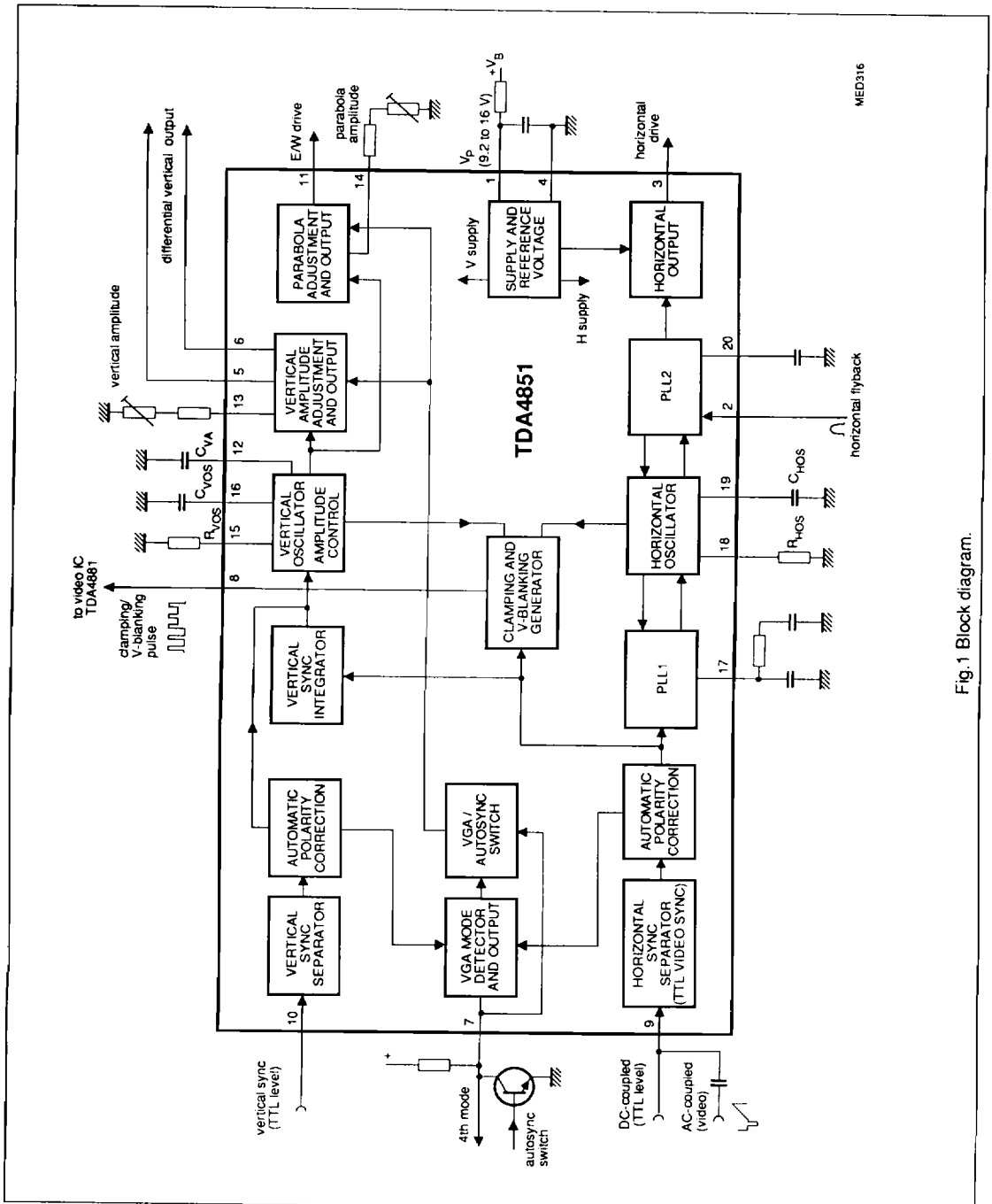


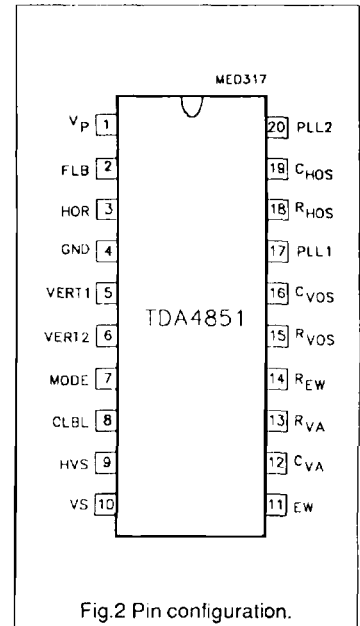
Fig. 1 Block diagram.

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## PINNING

SYMBOL	PIN	DESCRIPTION
V <sub>P</sub>	1	positive supply voltage
FLB	2	horizontal flyback input
HOR	3	horizontal output
GND	4	ground (0 V)
VERT1	5	vertical output 1; negative-going sawtooth
VERT2	6	vertical output 2; positive-going sawtooth
MODE	7	4th mode output and autosync input
CLBL	8	clamping/blanking pulse output
HVS	9	horizontal sync/video input
VS	10	vertical sync input
EW	11	E/W output (parabola to driver stage)
C <sub>V</sub> A	12	capacitor for amplitude control
R <sub>V</sub> A	13	vertical amplitude adjustment input
R <sub>EW</sub>	14	E/W amplitude adjustment input (parabola)
R <sub>V</sub> OS	15	vertical oscillator resistor
C <sub>V</sub> OS	16	vertical oscillator capacitor
PLL1	17	PLL1 phase
R <sub>H</sub> OS	18	horizontal oscillator resistor
C <sub>H</sub> OS	19	horizontal oscillator capacitor
PLL2	20	PLL2 phase



## FUNCTIONAL DESCRIPTION

### Horizontal sync separator and polarity correction

An AC-coupled video signal or a DC-coupled TTL sync signal (H only or composite sync) is input on pin 9. Video signals are clamped with top sync on 1.28 V, and are sliced at 1.4 V. This results in a fixed absolute slicing level of 120 mV related to top sync. DC-coupled TTL sync signals are also sliced at 1.4 V, however with the clamping circuit in current limitation. The polarity of the separated sync is detected by internal integration of the signal, then the polarity is corrected. The polarity information is fed to the VGA mode detector. The corrected sync is input signal for the vertical sync integrator and the PLL1 stage.

### Vertical sync separator, polarity correction and vertical sync integrator

DC-coupled vertical TTL sync signals may be applied to pin 10. They are sliced at 1.4 V. The polarity of the separated sync is detected by internal integration, then the polarity is corrected. The polarity information is fed to the VGA mode detector. If pin 10 is not used, it must be connected to ground. The separated  $V_{i\text{ sync}}$  signal from pin 10, or the integrated composite sync signal from pin 9 (TTL or video) triggers directly the vertical oscillator.

### VGA mode detector and mode output

The three standard VGA modes and a 4th not fixed mode are decoded by the polarities of the horizontal and the vertical sync input signals. An external resistor (from V<sub>P</sub> to pin 7) is necessary to match this function. In

all three VGA modes the correct amplitudes are activated. The presence of the 4th mode is indicated by a HIGH on pin 7. This signal can be used externally to switch any horizontal or vertical parameters.

### VGA mode detector input

For autosync operation the voltage on pin 7 must be externally forced to a level of < 50 mV. Vertical amplitude pre-settings for VGA are then inhibited. The delay time between vertical trigger pulse and the start of vertical deflection changes from 575  $\mu\text{s}$  to 300  $\mu\text{s}$  (575  $\mu\text{s}$  is needed for VGA). The vertical amplitude then remains constant in a frequency range from 50 Hz up to 110 Hz.

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## Clamping and V-blanking generator

A combined clamping and V-blanking pulse is available on pin 8 (suitable for the video pre-amplifier TDA4881). The lower level of 1.9 V is the blanking signal derived from the vertical blanking pulse from the internal vertical oscillator.

Vertical blanking equals the delay between vertical sync and start of vertical scan. By this, an optimum blanking is achieved for VGA/XGA and autosync operation (selectable via pin 7).

The upper level of 5.4 V is the horizontal clamping pulse with an internally fixed pulse width of 0.8  $\mu$ s.

A monoflop, which is triggered by the trailing edge of the horizontal sync pulse, generates this pulse. If composite sync is applied, one clamping pulse per H-period is generated during V-sync. The phase of the clamping pulse may change during V-sync (see Fig.8).

## PLL1 phase detector

The phase detector is a standard type using switched current sources. The middle of the sync is compared with a fixed point of the oscillator sawtooth voltage. The PLL filter is connected to pin 17. If composite sync is applied, the disturbed control voltage is corrected during V-sync (see Fig.8).

## Horizontal oscillator

This oscillator is of the relaxation type and requires a fixed capacitor of 10 nF at pin 19. By changing the current into pin 18 the whole frequency range from 13 to 100 kHz can be covered.

The current can be generated either by a frequency to voltage converter or by a resistor. A frequency adjustment may also be added if necessary.

The PLL1 control voltage at pin 17 modulates via a buffer stage the oscillator thresholds. A high DC-loop gain ensures a stable phase relationship between horizontal sync and line flyback pulses.

## PLL2 phase detector

This phase detector is similar to the PLL1 phase detector. Line flyback signals (pin 2) are compared with a fixed point of the oscillator sawtooth voltage. Delays in the horizontal deflection circuit are compensated by adjusting the phase relationship between horizontal sync and horizontal output pulses.

A certain amount of phase adjustment is possible by injecting a DC current from an external source into the PLL2 filter capacitor at pin 20.

## Horizontal driver

This open-collector output stage (pin 3) can directly drive an external driver transistor. The saturation voltage is less than 300 mV at 20 mA.

To protect the line deflection transistor, the horizontal output stage does not conduct for  $V_P < 6.4$  V (pin 1).

## Vertical oscillator and amplitude control

This stage is designed for fast stabilization of the vertical amplitude after changes in sync conditions. The free-running frequency  $f_0$  is determined by the values of  $R_{vos}$  and  $C_{vos}$ . The recommended values should be altered marginally only to preserve the excellent linearity and noise performance. The vertical drive currents  $I_5$  and  $I_6$  are in relation to the value of  $R_{vos}$ . Therefore, the oscillator frequency must be determined only by  $C_{vos}$  on pin 16.

$$f_0 = \frac{1}{10.8 \times R_{vos} \times C_{vos}}$$

To achieve a stabilized amplitude the free-running frequency  $f_0$  (without adjustment) must be lower than the lowest occurring sync frequency. The following contributions can be assumed:

minimum frequency offset between $f_0$ and the lowest trigger frequency	10%
spread of IC	$\pm 3\%$
spread of R (22 k $\Omega$ )	$\pm 1\%$
spread of C (0.1 $\mu$ F)	$\pm 5\%$
	19%

$$\text{Result: } f_0 = \frac{50}{1.19} \text{ Hz} = 42 \text{ Hz}$$

(for 50 to 110 Hz application)

Table 1 VGA modes

MODE	H / V SYNC POLARITY	FREQUENCY H (kHz)	FREQUENCY V (Hz)	NUMBER OF ACTIVE LINES	MODE OUTPUT PIN 7
1	+ / -	31.45	70	350	LOW
2	- / +	31.45	70	400	LOW
3	- / -	31.45	60	480	LOW
4	+ / +	fixed by external circuitry	-	-	HIGH
autosync	*/*	fixed by external circuitry	-	-	forced to GND

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## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V <sub>P</sub>	supply voltage (pin 1)	-0.5	16	V
V <sub>3,7</sub>	voltage on pins 3 and 7	-0.5	16	V
V <sub>8</sub>	voltage on pin 8	-0.5	7	V
V <sub>n</sub>	voltage on pins 5, 6, 9, 10, 13, 14 and 18	-0.5	6.5	V
I <sub>2</sub>	current on pin 2	-	±10	mA
I <sub>3</sub>	current on pin 3	-	100	mA
I <sub>7</sub>	current on pin 7	-	20	mA
I <sub>8</sub>	current on pin 8	-	-10	mA
T <sub>stg</sub>	storage temperature range	-55	+150	°C
T <sub>amb</sub>	operating ambient temperature range	0	70	°C
T <sub>j</sub>	maximum junction temperature	0	+150	°C
V <sub>ESD</sub>	electrostatic handling for all pins (note 1)	-	±400	V

### Note to the Limiting Values

1. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

## THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
R <sub>thj-a</sub>	from junction to ambient in free air	65 K/W

## CHARACTERISTICS

V<sub>P</sub> = 12 V; T<sub>amb</sub> = +25 °C; measurements taken in Fig.3 unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V <sub>P</sub>	positive supply voltage (pin 1)		9.2	12	16	V
I <sub>P</sub>	supply current	I <sub>18</sub> = -1.05 mA	-	36	44	mA
		I <sub>18</sub> = -3.388 mA	-	40	49	mA
<b>Internal reference voltage</b>						
V <sub>ref</sub>	internal reference voltage		6.0	6.25	6.5	V
TC	temperature coefficient	T <sub>amb</sub> = +20 to +100 °C	-	-	±90	10 <sup>-6</sup> /K
PSRR	power supply ripple rejection	f = 1 kHz sinewave	60	75	-	dB
		f = 1 MHz sinewave	25	35	-	dB
V <sub>P</sub>	supply voltage (pin 1) to ensure all internal reference voltages		9.2	-	16	V
<b>Composite sync input (AC-coupled)</b>		V <sub>10</sub> = 5 V				
V <sub>i sync</sub>	sync amplitude of video input signal (pin 9)	sync on green	-	300	-	mV
	top sync clamping level		1.1	1.28	1.5	V
	slicing level above top sync level	R <sub>S</sub> = 50 Ω	90	120	150	mV
R <sub>S</sub>	allowed source resistance for 7% duty factor	V <sub>i sync</sub> > 200 mV	-	-	1.5	kΩ
r <sub>g</sub>	differential input resistance	during sync	-	80	-	Ω
I <sub>g</sub>	charging current of coupling capacitor	V <sub>g</sub> > 1.5 V	1.3	2	3	μA

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{int}$	vertical sync integration time to generate vertical trigger pulse	$f_H = 31 \text{ kHz};$ $I_{18} = -1.050 \text{ mA}$	7	10	13	$\mu\text{s}$
		$f_H = 64 \text{ kHz};$ $I_{18} = -2.169 \text{ mA}$	3.5	5	6.5	$\mu\text{s}$
		$f_H = 100 \text{ kHz};$ $I_{18} = -3.388 \text{ mA}$	2.5	3.4	4.5	$\mu\text{s}$
<b>Horizontal sync input (DC-coupled, TTL-compatible)</b>						
$V_{i \text{ sync}}$	sync input signal (peak-to-peak value, pin 9)		1.7	–	–	V
	slicing level		1.2	1.4	1.6	V
$t_p$	minimum pulse width		700	–	–	ns
$t_r, t_f$	rise time and fall time		10	–	500	ns
$I_9$	input current	$V_9 = 0.8 \text{ V}$	–	–	–200	$\mu\text{A}$
		$V_9 = 5.5 \text{ V}$	–	–	10	$\mu\text{A}$
<b>Automatic horizontal polarity switch</b>		H-sync on pin 9				
$t_p H/t_H$	horizontal sync pulse width related to $t_H$ (duty factor for automatic polarity correction)		–	–	30	%
$t_p$	delay time for changing sync polarity		0.3	–	1.8	ms
<b>Vertical sync input (DC-coupled, TTL-compatible)</b>		V-sync on pin 10				
$V_{i \text{ sync}}$	sync input signal (peak-to-peak value, pin 10)		1.7	–	–	V
	slicing level		1.2	1.4	1.6	V
$I_{10}$	input current	$0 < V_{10} < 5.5 \text{ V}$	–	–	$\pm 10$	$\mu\text{A}$
$t_{pV}$	maximum vertical sync pulse width for automatic vertical polarity switch		–	–	300	$\mu\text{s}$
<b>Horizontal mode detector output</b>		VGA mode				
$V_7$	output saturation voltage LOW (for Modes 1, 2 and 3)	$I_7 = 6 \text{ mA}$	–	0.275	0.33	V
	output voltage HIGH	mode 4	–	–	$V_P$	V
$I_7$	load current range to force VGA mode-dependent vertical and parabola amplitudes	modes 1, 2 and 3	2	–	6	mA
	output current	mode 4	–	0	–	mA
<b>VGA / autosync mode switch</b>						
$V_7$	input voltage LOW to force autosync mode		0	–	50	mV
<b>Horizontal clamping / blanking generator output</b>		Fig. 6				
$V_8$	output voltage LOW		–	–	0.9	V
	blanking output voltage	internal V blanking	1.6	1.9	2.2	V
	clamping output voltage	H-sync on pin 9	5.15	5.4	5.65	V
$I_8$	internal sink current for all output levels	H and V scanning	2.3	2.9	3.5	mA
	external load current		–	–	–3.0	mA
$t_8$	clamping pulse start		with end of H-sync			
$t_{clp}$	clamping pulse width	$V_8 = 3 \text{ V}$	0.6	0.8	1.0	$\mu\text{s}$
S	steepness of rise and fall times		–	60	75	ns/V

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Vertical oscillator</b>		$V_{ref} = 6.25\text{ V}$				
$f_0$	vertical free-running frequency	$R_{15} = 22\text{ k}\Omega$ ; $C_{16} = 0.1\text{ }\mu\text{F}$	–	42	–	Hz
$f_v$	nominal vertical sync range	no $f_0$ adjustment	50	–	110	Hz
$V_{15}$	voltage on pin 15	$R_{15} = 22\text{ k}\Omega$	2.8	3.0	3.2	V
$t_d$	delay between sync pulse and start of vertical scan	measured on pin 8				
	in VGA/XGA mode, activated by an external resistor on pin 7		500	575	650	$\mu\text{s}$
	in autosync mode	$V_7 < 50\text{ mV}$	240	300	360	$\mu\text{s}$
$I_{12}$	control current for amplitude control		–	$\pm 200$	–	$\mu\text{A}$
$C_{12}$	capacitor for amplitude control		–	–	0.18	$\mu\text{F}$
<b>Vertical differential output</b>		Fig.7				
$I_o$	differential output current between pins 5 and 6 (peak-to-peak value)	mode 3; $I_{13} > -135\text{ }\mu\text{A}$ ; $R_{15} = 22\text{ k}\Omega$	0.9	1.0	1.1	mA
	maximum offset-current error	$I_o = 1\text{ mA}$	–	–	$\pm 2.5$	%
	maximum linearity error		–	–	$\pm 1.5$	%
<b>Vertical amplitude adjustment</b> (in percentage of output signal)						
$V_{13}$	input voltage		–	5.0	–	V
$I_{13}$	adjustment current	$I_o\text{ max}$ (100%)	–110	–120	–135	$\mu\text{A}$
		$I_o\text{ min}$ (typically 58%)	–	0	–	$\mu\text{A}$
$\Delta I_o/\Delta t$	VGA mode-dependent pre-settings activated by an external resistor on pin 7	Table 1; note 1				
	Mode 1		116.2	116.8	117.4	%
	Mode 2		101.6	102.2	102.8	%
	Mode 3		–	100	–	%
	Mode 4		–	100	–	%
	autosync operation (VGA operation disabled)	$V_7 < 50\text{ mV}$	–	100	–	%
<b>Horizontal comparator PLL1</b>						
$V_{17}$	upper control voltage limitation		–	5.9	–	V
	lower control voltage limitation		–	5.1	–	V
$I_{17}$	control current	Fig.6	–	$\pm 0.083I_{18}$	–	mA
<b>Horizontal oscillator</b>						
$f_{osc}$	centre frequency	$R_{18} = 2.4\text{ k}\Omega$ (pin 18); $C_{19} = 10\text{ nF}$ (pin 19)	–	31.45	–	kHz
	deviation of centre frequency		–	–	$\pm 3$	%
	temperature coefficient		0	+200	+300	$10^{-6}/\text{K}$
$\Phi_H/\Delta H$	relative holding/catching range		$\pm 6$	$\pm 6.5$	$\pm 7.3$	%
$I_{18}$	external oscillator current		–0.5	–	–4.3	mA
$V_{18}$	voltage at reference current input (pin 18)		2.35	2.5	2.65	V

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Horizontal PLL2</b>		Fig.6				
V <sub>2</sub>	upper clamping level of flyback input	I <sub>2</sub> = 6 mA	–	5.5	–	V
	lower clamping level of flyback input	I <sub>2</sub> = –1 mA	–	–0.75	–	V
	H-flyback slicing level		–	3.0	–	V
t <sub>d</sub> /t <sub>H</sub>	delay between middle of sync and middle of H-flyback related to t <sub>H</sub>		–	3.0	–	%
V <sub>20</sub>	upper control voltage limitation		–	6.2	–	V
	lower control voltage limitation		–	4.8	–	V
I <sub>20</sub>	control current		–	±0.083I <sub>18</sub>	–	μA
Δt/t <sub>H</sub>	PLL2 control range related to t <sub>H</sub>		30	–	–	%
<b>Horizontal output (open-collector)</b>		Fig.6				
V <sub>3</sub>	output voltage LOW	I <sub>3</sub> = 20 mA	–	–	0.3	V
		I <sub>3</sub> = 60 mA	–	–	0.8	V
t <sub>p</sub> /t <sub>H</sub>	t <sub>H</sub> duty factor		42	45	48	%
V <sub>P</sub>	threshold to activate under voltage protection	horizontal output off	–	5.6	–	V
		horizontal output on	–	5.8	–	V
Δt <sub>H</sub>	jitter of horizontal output	f = 31 kHz	–	–	3.5	ns
		f = 64 kHz	–	–	1.9	ns
		f = 100 kHz	–	–	1.2	ns
<b>E/W output</b>		note 2				
V <sub>11</sub>	bottom output signal during mid-scan (pin 11)	internally stabilized	1.05	1.2	1.35	V
	top output signal during flyback		4.2	4.5	4.8	V
	temperature coefficient of output signal		–	–	250	10 <sup>–6</sup> /K
<b>E/W amplitude adjustment (parabola)</b>		Fig.7				
V <sub>14</sub>	input voltage (pin 14)		–	5.0	–	V
I <sub>14</sub>	adjustment current	100% parabola	–110	–120	–135	μA
		typically 28% parabola	–	0	–	μA

### Notes to the characteristics

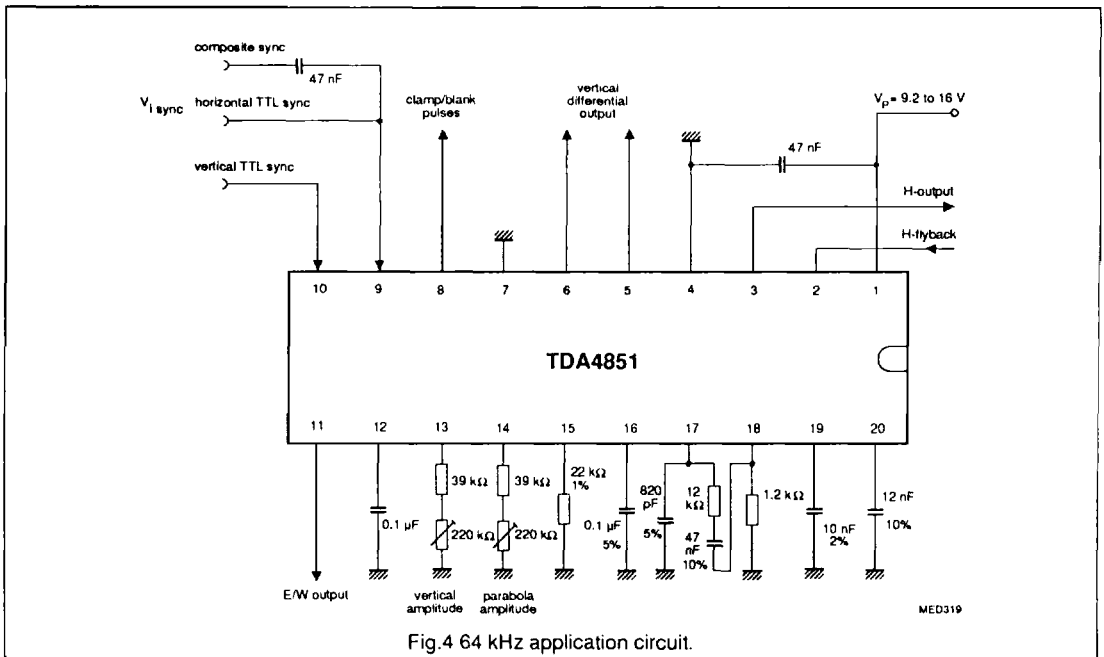
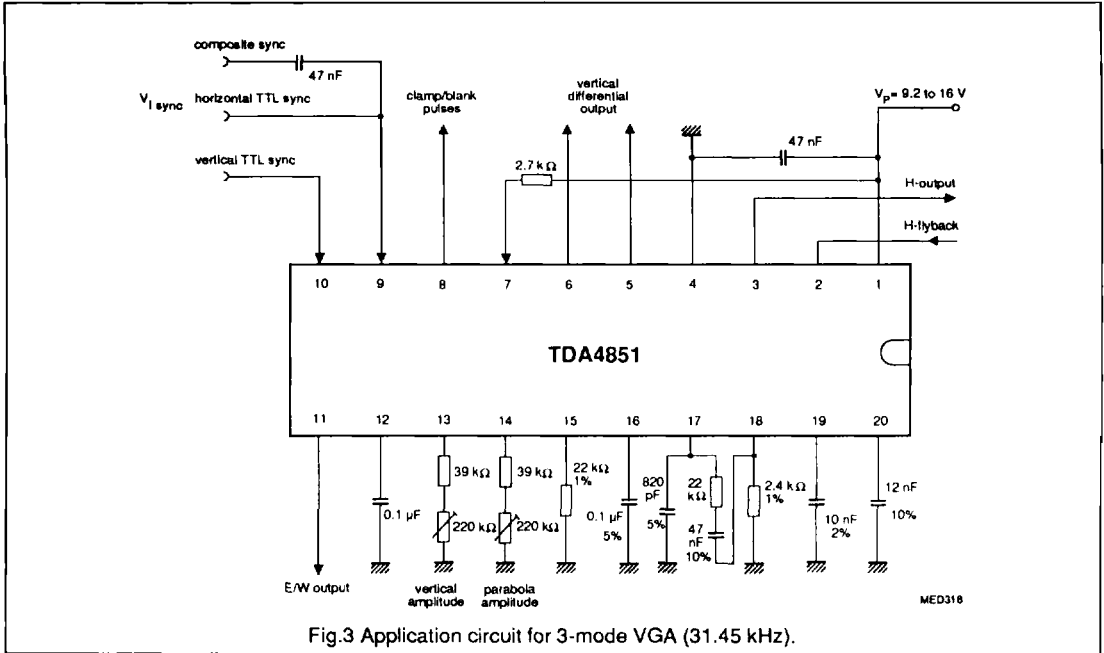
1. ΔI<sub>2</sub>/Δt relative to value of Mode 3.
2. Parabola amplitude tracks with mode-dependent vertical amplitude but not with vertical amplitude adjustment. Tracking can be achieved by a resistor from vertical amplitude potentiometer to pin 14.



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## APPLICATION INFORMATION



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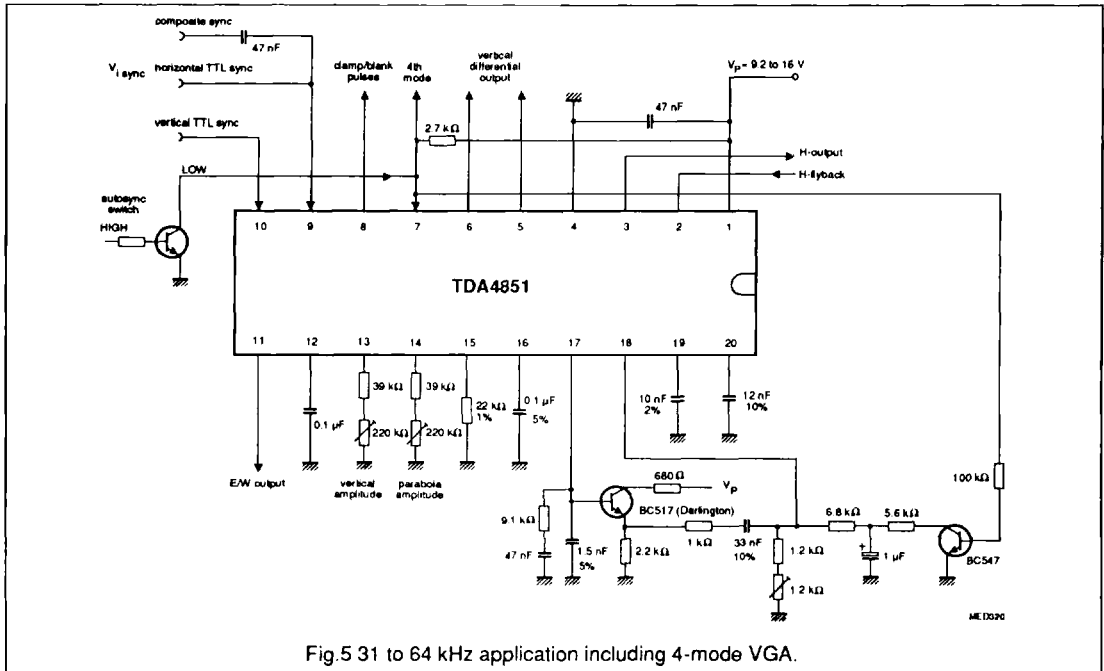


Fig.5 31 to 64 kHz application including 4-mode VGA.

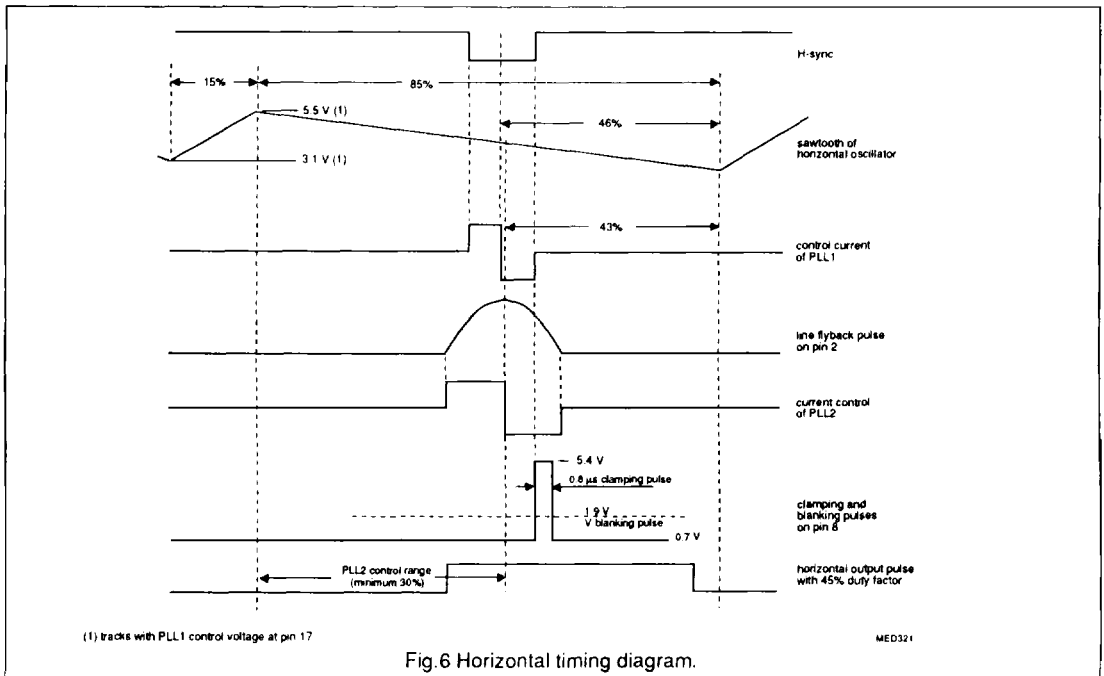
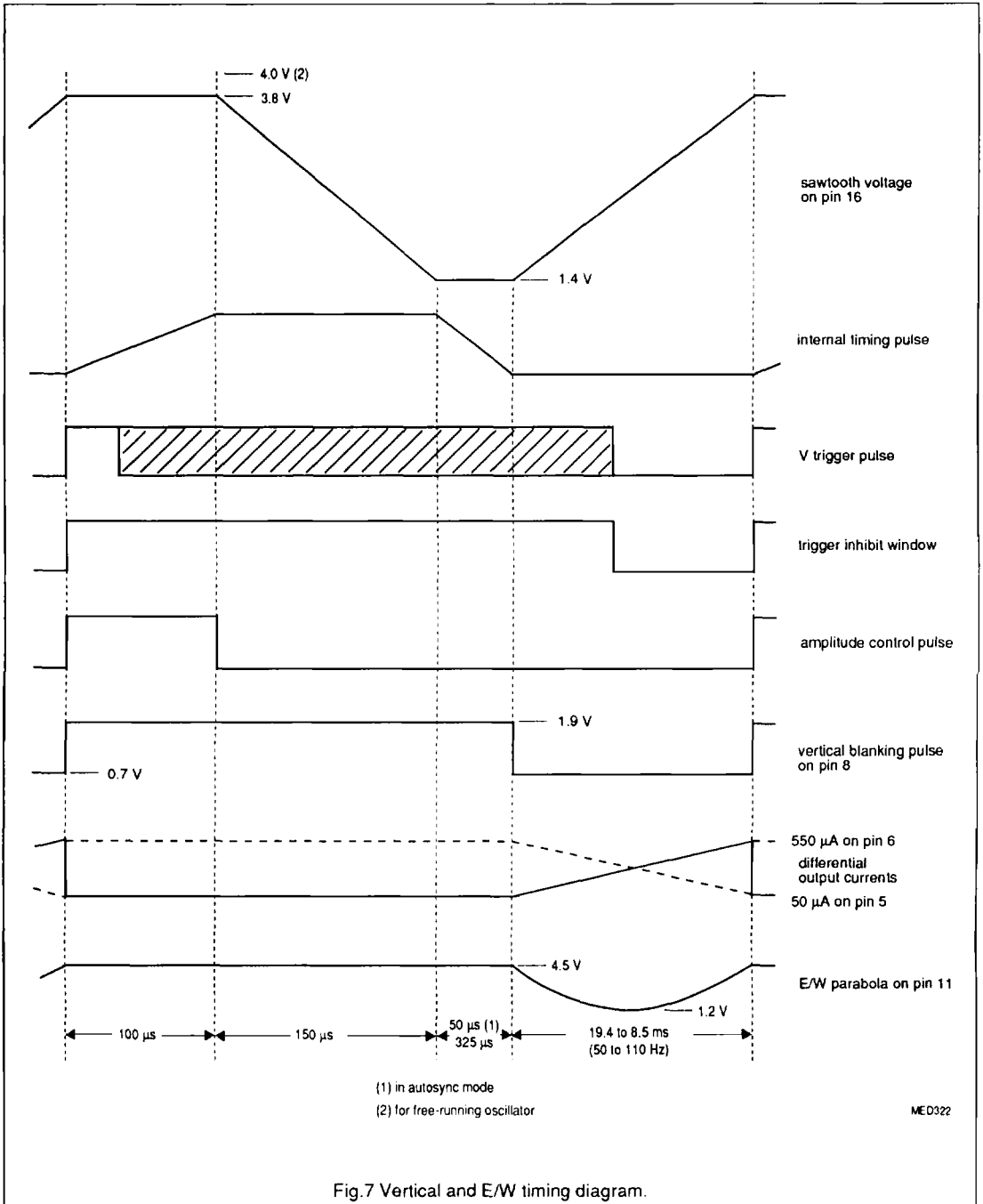


Fig.6 Horizontal timing diagram.

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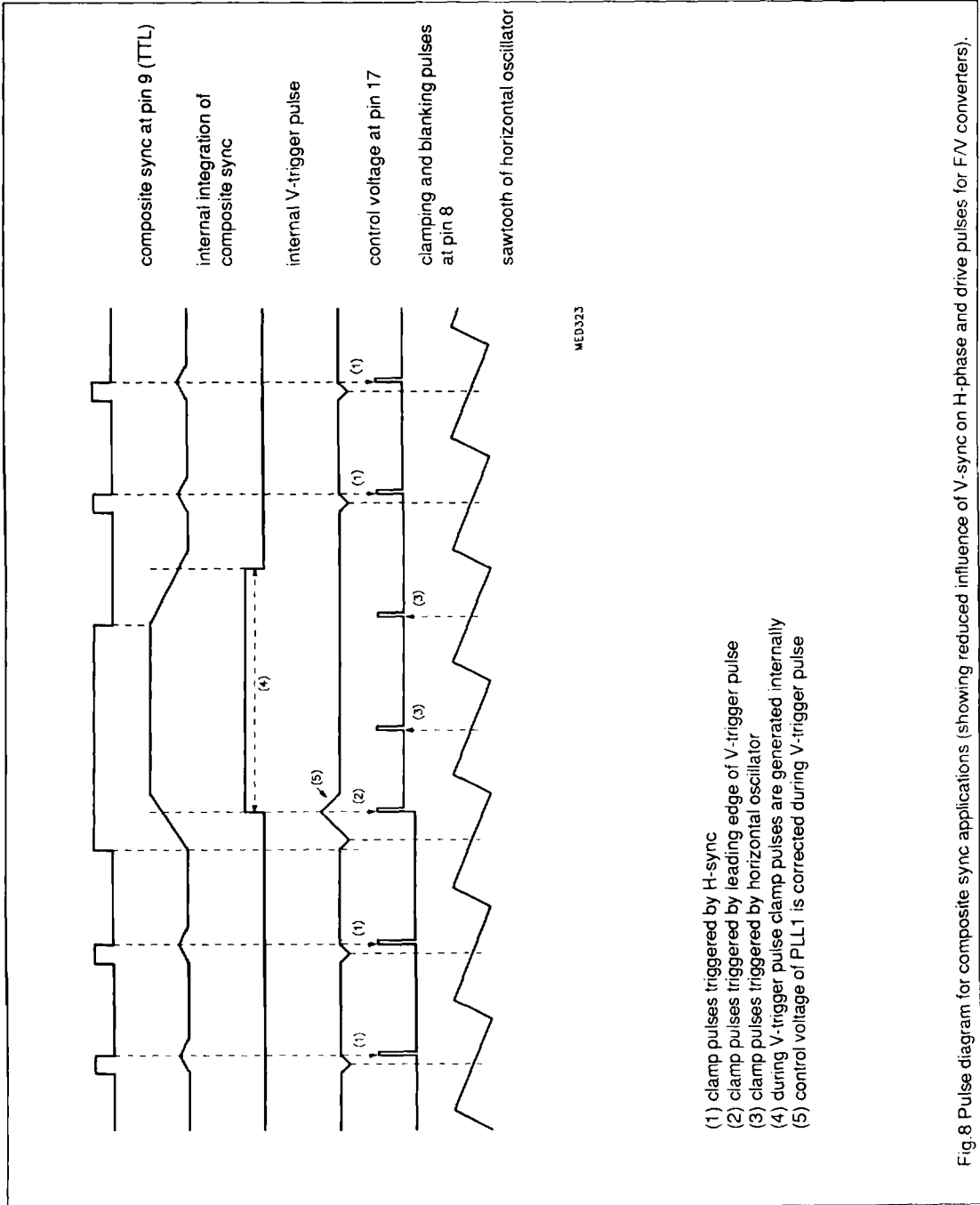


Fig. 8 Pulse diagram for composite sync applications (showing reduced influence of V-sync on H-phase and drive pulses for F/V converters).

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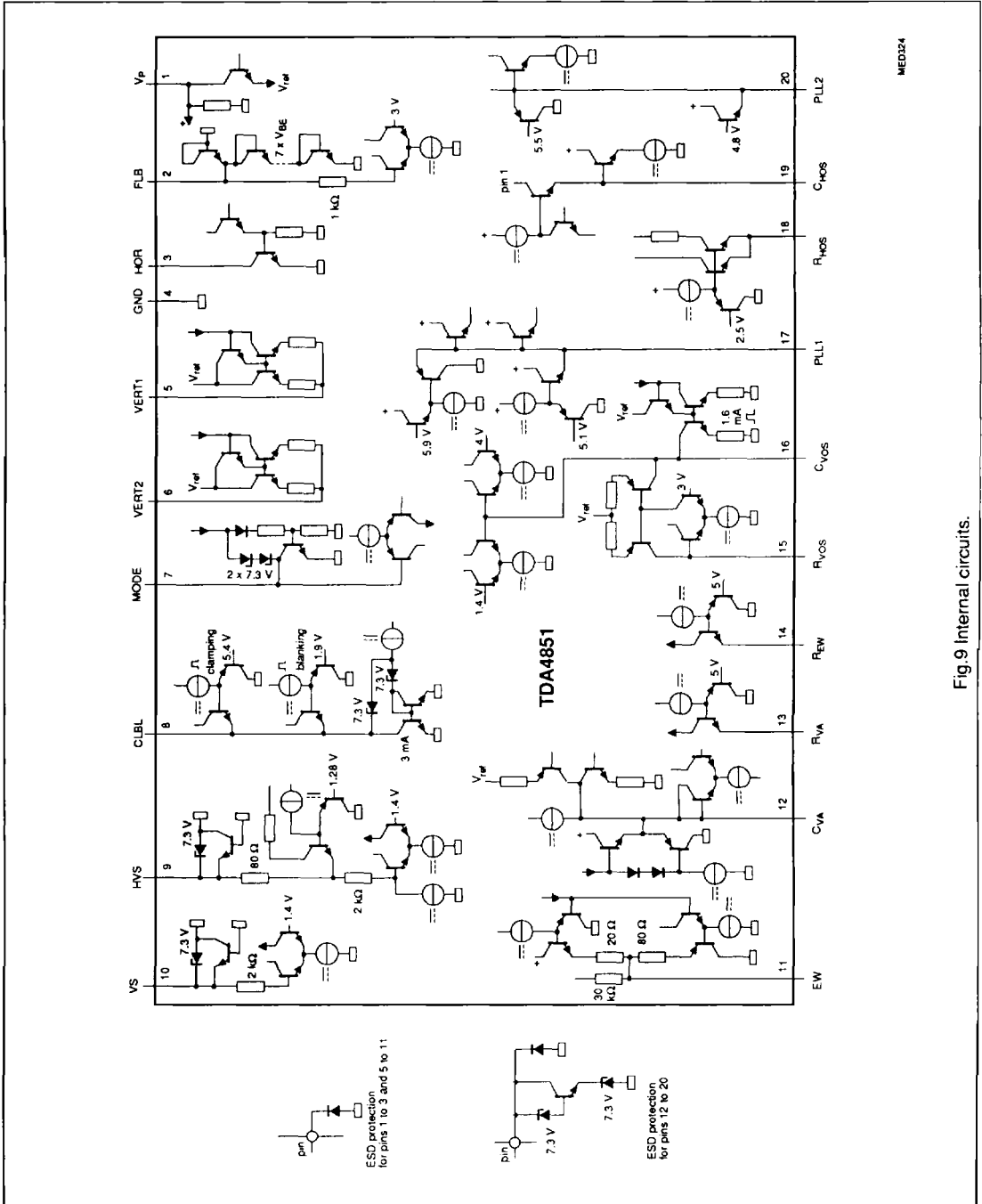


Fig.9 Internal circuits.