Absolute Maximum Ratings

Supply Voltage, V_{DD} . . . . . -0.5V to +7V
Input Voltage, V_{IN} . . . . . V_{SS} - 0.3V to V_{DD} + 0.3V
Self-Check Mode (IRQ Pin Only), V_{IN} . V_{SS} - 0.3V to 2 x V_{DD} + 0.3V
Current Drain Per Pin Excluding V_{DD} and V_{SS}, I 25mA

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range . . . . . -55°C to 125°C
CDP68HC05C16B . . . . . -40°C to 85°C
CDP68HCL05C16B . . . . . 0°C to 70°C
CDP68HSC05C16B . . . . . 0°C to 85°C
Input Low Voltage . . . . . 0V to +0.8V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SPDIP Package	55	N/A
PDIP Package	55	N/A
PLCC Package	45	N/A
MQFP Package	70	N/A
SBDIP Package	60	18

Maximum Junction Temperature (Hermetic Package) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(PLCC, MQFP - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications HC Product Type

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CDP68HC05C16B V_{DD} = 5V ±10%, V_{SS} = 0V, T_A = -40°C to 85°C (Note 2)						
Output Voltage	V_{OL}	I_{LOAD} < 10µA	-	-	0.1	V
	V_{OH}		V_{DD} - 0.1	-	-	V
Output High Voltage						
PA0-7, PB0-7, PC0-6, TCMP, PD7, PD0	V_{OH}	I_{LOAD} = -0.8mA	V_{DD} - 0.8	-	-	V
PD1-5	V_{OH}	I_{LOAD} = -1.6mA	V_{DD} - 0.8	-	-	V
PC7	V_{OH}	I_{LOAD} = -5.0mA	V_{DD} - 0.8	-	-	V
Output Low Voltage						
PA0-7, PB0-7, PC0-6, PD0-5, PD7, TCMP	V_{OL}	I_{LOAD} = 1.6mA	-	-	0.4	V
PC7	V_{OL}	I_{LOAD} = 10.0mA	-	-	0.4	V
Input High Voltage, PA0-7, PB0-7, PC0-7, PD0-5, PD7, TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IH}		0.7 x V_{DD}	-	V_{DD}	V
Input Low Voltage, PA0-7, PB0-7, PC0-7, PD0-5, PD7, TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IL}		V_{SS}	-	0.2 x V_{DD}	V
Data Retention Mode	V_{RM}	T_A = 0°C to 70°C	1.5	-	-	V
Wake Up Timer Oscillator Frequency	f_{RCO}	T_A = 25°C	-	13	-	kHz
Supply Current (f_{OSC} = 4.2MHz)						
Run (Note 6)	I_{DD}		-	3.5	5.25	mA
WAIT (Notes 5, 6, 7, 9)	I_{DD}		-	1.0	3.25	mA
STOP (Notes 7, 8)	I_{DD}	T_A = 25°C	-	1.0	20	µA
		T_A = 0°C to 70°C	-	2.0	40	µA
		T_A = -40°C to 85°C	-	7.0	50	µA
STOP with Wake Up Timer Enabled	I_{DD}	T_A = 25°C	-	10.0	-	µA
I/O Ports Hi-Z Leakage Current - $\overline{RESET}$, PA0-7, PB0-7 (without Pullups), PC0-7, PD0-5, PD7	I_{IL}		-10	-	+10	µA
Pullup Current PB0-7 (with Pullups, Note 10)	I_{IN}		60	140	300	µA
Input Current, $\overline{IRQ}$, TCAP, OSC1	I_{IN}		-1	-	+1	µA
Capacitance Ports (As Input or Output) $\overline{RESET}$, $\overline{IRQ}$, TCAP, OSC1, PD0-5, PD7	C_{OUT}		-	-	12	pF
	C_{IN}		-	-	8	pF

DC Electrical Specifications HC Product Type (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CDP68HC05C16B V_{DD} = 3.3V ±10%, V_{SS} = 0V, T_A = -40°C to 85°C						
Output Voltage	V_{OL}	$I_{LOAD} \leq 10\mu A$	-	-	0.1	V
	V_{OH}		V_{DD} - 0.1	-	-	V
Output High Voltage PA0-7, PB0-7, PC0-6, TCMP, PD0, PD7	V_{OH}	I_{LOAD} = -0.2mA	V_{DD} - 0.3	-	-	V
PD1-5	V_{OH}	I_{LOAD} = -0.4mA	V_{DD} - 0.3	-	-	V
PC7	V_{OH}	I_{LOAD} = -1.5mA	V_{DD} - 0.3	-	-	V
Output Low Voltage PA0-7, PB0-7, PC0-6, PD0-5, TCMP, PD7	V_{OL}	I_{LOAD} = 0.4mA	-	-	0.3	V
PC7	V_{OL}	I_{LOAD} = 6.0mA	-	-	0.3	V
Input High Voltage, PA0-7, PB0-7, PC0-7, PD0-5, PD7, TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IH}		0.7 x V_{DD}	-	V_{DD}	V
Input Low Voltage, PA0-7, PB0-7, PC0-7, PD0-5, PD7, TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IL}		V_{SS}	-	0.2 x V_{DD}	V
Data Retention Mode	V_{RM}	T_A = 0°C to 70°C	1.5	-	-	V
Wake Up Timer Oscillator Frequency	f_{RCO}	T_A = 25°C	-	13	-	kHz
Supply Current (f_{OSC} = 2.0MHz) Run (Note 6)	I_{DD}		-	1	1.6	mA
WAIT (Notes 5, 6, 7, 9)	I_{DD}		-	0.5	0.9	mA
STOP (Notes 7, 9)	I_{DD}	T_A = 25°C	-	1	8	µA
		T_A = 0°C to 70°C	-	-	16	µA
		T_A = -40°C to 85°C	-	-	20	µA
STOP with Wake Up Timer Enabled	I_{DD}	T_A = 25°C	-	10.0	-	µA
I/O Ports Hi-Z Leakage Current - $\overline{RESET}$, PA0-7, PB0-7 (without Pullups), PC0-7, PD0-5, PD7	I_{IL}		-10	-	+10	µA
Pullup Current PB0-7 (with Pullups, Note 10)	I_{IN}		25	65	140	µA
Input Current - $\overline{IRQ}$, TCAP, OSC1	I_{IN}		-1	-	+1	µA
Capacitance Ports (As Input or Output) $\overline{RESET}$, $\overline{IRQ}$, TCAP, OSC1, PD0-5, PD7	C_{OUT}		-	-	12	pF
	C_{IN}		-	-	8	pF

NOTES:

2. This device contains circuitry to protect the inputs against damage due to high static voltages of electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to the range $V_{SS}<(V_{IN}$ or $V_{OUT})<V_{DD}$. Reliability of operation is enhanced if unused inputs except OSC2 are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).
3. All values shown reflect average measurement.
4. Typical values at midpoint of voltage range, 25°C only.
5. Wait I_{DD}: Only timer system active (SPE = TE = RE = 0). If SPI, SCI active (SPE = TE = RE = 1) add 10% current draw.
6. Run (Operating) I_{DD}, Wait I_{DD}: Measured using external square-wave clock source, all inputs 0.2V from rail, no DC loads, less than 50pF on all outputs, C_L = 20pF on OSC2.
7. Wait, Stop I_{DD}: All ports configured as inputs, V_{IL} = 0.2V, V_{IH} = V_{DD} -0.2V.
8. Stop I_{DD} measured with OSC1 = V_{SS}.
9. Wait I_{DD} is affected linearly by the OSC2 capacitance.
10. Input pullup current measured with V_{IL} = 0.2V.

Control Timing HC Product Type

PARAMETER	SYMBOL	MIN	MAX	UNITS
CDP68HC05C16B V_{DD} = 5V ±10%, V_{SS} = 0V, T_A = -40°C to 85°C				
Frequency Of Operation				
Crystal Option	f_{OSC}	-	4.2	MHz
External Clock Option	f_{OSC}	DC	4.2	MHz
Internal Operating Frequency				
Crystal (f_{OSC} + 2)	f_{OP}	-	2.1	MHz
External Clock (f_{OSC} + 2)	f_{OP}	DC	2.1	MHz
Cycle Time (See Figure 11)	t_{CYC}	480	-	ns
Crystal Oscillator Start Up Time for AT-cut Crystal (See Figure 11)	t_{OXOV}	-	100	ms
Stop Recovery Start Up Time (AT-cut Crystal Oscillator) (See Figure 2)	t_{ILCH}	-	100	ms
$\overline{\text{RESET}}$ Pulse Width (See Figure 11)	t_{RL}	1.5	-	t_{CYC}
Timer				
Resolution (Note 12)	t_{RES}	4	-	t_{CYC}
Input Capture Pulse Width (See Figure 3)	t_{TH}, t_{TL}	125	-	ns
Input Capture Pulse Period (See Figure 3)	t_{TLTL}	(Note 13)	-	t_{CYC}
Interrupt Pulse Width Low (Edge-Triggered) (See Figure 15)	t_{ILIH}	125	-	ns
Interrupt Pulse Period (See Figure 15)	t_{ILIL}	(Note 11)	-	t_{CYC}
OSC1 Pulse Width	t_{OH}, t_{OL}	90	-	ns
CDP68HC05C16B V_{DD} = 3.3V ±10%, V_{SS} = 0V, T_A = -40°C to 85°C				
Frequency Of Operation				
Crystal Option	f_{OSC}	-	2.0	MHz
External Clock Option	f_{OSC}	DC	2.0	MHz
Internal Operating Frequency				
Crystal (f_{OSC} + 2)	f_{OP}	-	1.0	MHz
External Clock (f_{OSC} + 2)	f_{OP}	DC	1.0	MHz
Cycle Time (See Figure 11)	t_{CYC}	1000	-	ns
Crystal Oscillator Start Up Time for AT-cut Crystal (See Figure 11)	t_{OXOV}	-	100	ms
Stop Recovery Start Up Time (AT-cut Crystal Oscillator) (See Figure 2)	t_{ILCH}	-	100	ms
$\overline{\text{RESET}}$ Pulse Width (See Figure 11)	t_{RL}	1.5	-	t_{CYC}
Timer				
Resolution (Note 12)	t_{RES}	4	-	t_{CYC}
Input Capture Pulse Width (See Figure 3)	t_{TH}, t_{TL}	250	-	ns
Input Capture Pulse Period (See Figure 3)	t_{TLTL}	(Note 13)	-	t_{CYC}
Interrupt Pulse Width Low (Edge-Triggered) (See Figure 15)	t_{ILIH}	250	-	ns
Interrupt Pulse Period (See Figure 15)	t_{ILIL}	(Note 11)	-	t_{CYC}
OSC1 Pulse Width	t_{OH}, t_{OL}	200	-	ns

NOTES:

11. The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{CYC}.
12. Since a 2-bit prescaler in the timer must count four internal cycles (t_{CYC}), this is the limiting minimum factor in determining the timer resolution.
13. The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{CYC}.

Serial Peripheral Interface (SPI) Timing (See Figure 4) HC Product Type

LEAD	PARAMETER	SYMBOL	MIN	MAX	UNITS
CDP68HC05C16B V_{DD} = 5V ±10%, V_{SS} = 0V, T_A = -40°C to 85°C Unless Otherwise Specified					
	Operating Frequency				
	Master	$f_{OP(M)}$	DC	0.5	f_{OP} (Note 16)
	Slave	$f_{OP(S)}$	DC	2.1	MHz
1	Cycle Time				
	Master	$t_{CYC(M)}$	2.0	-	t_{CYC}
	Slave	$t_{CYC(S)}$	480	-	ns
2	Enable Lead Time				
	Master	$t_{LEAD(M)}$	(Note 14)	-	-
	Slave	$t_{LEAD(S)}$	240	-	ns
3	Enable Lag Time				
	Master	$t_{LAG(M)}$	(Note 14)	-	-
	Slave	$t_{LAG(S)}$	720	-	ns
4	Clock (SCK) High Time				
	Master	$t_{W(SCKH)M}$	340	-	ns
	Slave	$t_{W(SCKH)S}$	190	-	ns
5	Clock (SCK) Low Time				
	Master	$t_{W(SCKL)M}$	340	-	ns
	Slave	$t_{W(SCKL)S}$	190	-	ns
6	Data Setup Time (Inputs)				
	Master	$t_{SU(M)}$	100	-	ns
	Slave	$t_{SU(S)}$	100	-	ns
7	Data Hold Time (Inputs)				
	Master	$t_{H(M)}$	100	-	ns
	Slave	$t_{H(S)}$	100	-	ns
8	Access Time (Time to Data Active from High Impedance State)				
	Slave	t_A	0	120	ns
9	Disable Time (Hold Time to High Impedance State)				
	Slave	t_{DIS}	-	240	ns
10	Data Valid Time				
	Master (Before Capture Edge)	$t_{V(M)}$	0.25	-	$t_{CYC(M)}$
	Slave (After Enable Edge) (Note 15)	$t_{V(S)}$	-	240	ns
11	Data Hold Time (Outputs)				
	Master (After Capture Edge)	$t_{HO(M)}$	0.25	-	$t_{CYC(M)}$
	Slave (After Enable Edge)	$t_{HO(S)}$	0	-	ns
12	Rise Time (V_{DD} = 20% to 70%, C_L = 200pF)				
	SPI Outputs (SCK, MOSI, MISO)	$t_{r(M)}$	-	100	ns
	SPI Inputs (SCK, MOSI, MISO, $\overline{SS}$)	$t_{r(S)}$	-	2.0	µs
13	Fall Time (V_{DD} = 20% to 70%, C_L = 200pF)				
	SPI Outputs (SCK, MOSI, MISO)	$t_{f(M)}$	-	100	ns
	SPI Inputs (SCK, MOSI, MISO, $\overline{SS}$)	$t_{f(S)}$	-	2.0	µs
CDP68HC05C16B V_{DD} = 3.3V ±10%, V_{SS} = 0V, T_A = -40°C to 85°C Unless Otherwise Specified					
	Operating Frequency				
	Master	$f_{OP(M)}$	DC	0.5	f_{OP} (Note 16)
	Slave	$f_{OP(S)}$	DC	1.0	MHz

Serial Peripheral Interface (SPI) Timing (See Figure 4) **HC Product Type (Continued)**

LEAD	PARAMETER	SYMBOL	MIN	MAX	UNITS
1	Cycle Time				
	Master	$t_{CYC(M)}$	2.0	-	t_{CYC}
	Slave	$t_{CYC(S)}$	1.0	-	µs
2	Enable Lead Time				
	Master	$t_{LEAD(M)}$	(Note 14)	-	-
	Slave	$t_{LEAD(S)}$	500	-	ns
3	Enable Lag Time				
	Master	$t_{LAG(M)}$	(Note 14)	-	-
	Slave	$t_{LAG(S)}$	1.5	-	µs
4	Clock (SCK) High Time				
	Master	$t_{W(SCKH)M}$	720	-	ns
	Slave	$t_{W(SCKH)S}$	400	-	ns
5	Clock (SCK) Low Time				
	Master	$t_{W(SCKL)M}$	720	-	ns
	Slave	$t_{W(SCKL)S}$	400	-	ns
6	Data Setup Time (Inputs)				
	Master	$t_{SU(M)}$	200	-	ns
	Slave	$t_{SU(S)}$	200	-	ns
7	Data Hold Time (Inputs)				
	Master	$t_{H(M)}$	200	-	ns
	Slave	$t_{H(S)}$	200	-	ns
8	Access Time (Time to Data Active from High Impedance State)				
	Slave	t_A	0	250	ns
9	Disable Time (Hold Time to High Impedance State)				
	Slave	t_{DIS}	-	500	ns
10	Data Valid Time				
	Master (Before Capture Edge)	$t_{V(M)}$	0.25	-	$t_{CYC(M)}$
	Slave (After Enable Edge) (Note 15)	$t_{V(S)}$	-	500	ns
11	Data Hold Time (Outputs)				
	Master (After Capture Edge)	$t_{HO(M)}$	0.25	-	$t_{CYC(M)}$
	Slave (After Enable Edge)	$t_{HO(S)}$	0	-	ns
12	Rise Time (V_{DD} = 20% to 70%, C_L = 200pF)				
	SPI Outputs (SCK, MOSI, MISO)	$t_{r(M)}$	-	200	ns
	SPI Inputs (SCK, MOSI, MISO, $\overline{SS}$)	$t_{r(S)}$	-	2.0	µs
13	Fall Time (V_{DD} = 20% to 70%, C_L = 200pF)				
	SPI Outputs (SCK, MOSI, MISO)	$t_{f(M)}$	-	200	ns
	SPI Inputs (SCK, MOSI, MISO, $\overline{SS}$)	$t_{f(S)}$	-	2.0	µs

NOTES:

14. Signal Production depends on software.
15. Assumes 200pF load on all SPI leads.
16. Note that the units this specification uses is f_{OP} (internal operating frequency), not MHz! In the master mode the SPI bus is capable of running at one-half of the devices's internal operating frequency, therefore 5V: 1.05MHz and 3.3V: 0.05MHz maximum.

DC Electrical Specifications HCL Product Type

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CDP68HCL05C16B V_{DD} = 5V ±10%, V_{SS} = 0V, T_A = 0°C to 70°C (Note 17)						
Output Voltage	V_{OL}	I_{LOAD} ≤10µA	-	-	0.1	V
	V_{OH}		V_{DD} - 0.1	-	-	V
Output High Voltage						
PA0-7, PB0-7, PC0-6, TCMP, PD0, PD7	V_{OH}	I_{LOAD} = -0.8mA	V_{DD} - 0.8	-	-	V
PD1-5	V_{OH}	I_{LOAD} = -1.6mA	V_{DD} - 0.8	-	-	V
PC7	V_{OH}	I_{LOAD} = -5.0mA	V_{DD} - 0.8	-	-	V
Output Low Voltage						
PA0-7, PB0-7, PC0-6, PD0-5, PD7, TCMP	V_{OL}	I_{LOAD} = 1.6mA	-	-	0.4	V
PC7	V_{OL}	I_{LOAD} = 10.0mA	-	-	0.4	V
Input High Voltage, PA0-7, PB0-7, PC0-7, PD0-5, PD7, TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IH}		0.7 x V_{DD}	-	V_{DD}	V
Input Low Voltage, PA0-7, PB0-7, PC0-7, PD0-5, PD7, TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IL}		V_{SS}	-	0.2 x V_{DD}	V
Data Retention Mode	V_{RM}	T_A = 0°C to 70°C	1.5	-	-	V
Wake Up Timer Oscillator Frequency	f_{RCO}	T_A = 25°C	-	13	-	kHz
Supply Current (f_{OSC} = 4.2MHz)						
Run (Note 20)	I_{DD}		-	3.5	4.25	mA
WAIT (Notes 19, 20, 21, 23)	I_{DD}		-	1.6	2.25	mA
STOP (Notes 21, 22)	I_{DD}	T_A = 25°C	-	1	15	µA
		T_A = 0°C to 70°C	-	-	25	µA
STOP with Wake Up Timer Enabled	I_{DD}	T_A = 25°C	-	10.0	-	µA
I/O Ports Hi-Z Leakage Current - $\overline{RESET}$, PA0-7, PB0-7 (without pullups), PC0-7, PD0-5, PD7	I_{IL}		-10	-	+10	µA
Pullup Current PB0-7 (with pullups, Note 24)	I_{IN}		60	140	300	µA
Input Current - $\overline{IRQ}$, TCAP, OSC1	I_{IN}		-1	-	+1	µA
Capacitance Ports (As Input or Output) $\overline{RESET}$, $\overline{IRQ}$, TCAP, OSC1, PD0-5, PD7	C_{OUT}		-	-	12	pF
	C_{IN}		-	-	8	pF
CDP68HCL05C16B V_{DD} = 2.5V - 3.6V, V_{SS} = 0V, T_A = 0°C to 70°C						
Output Voltage	V_{OL}	I_{LOAD} ≤ 10µA	-	-	0.1	V
	V_{OH}		V_{DD} - 0.1	-	-	V
Output High Voltage						
PA0-7, PB0-7, PC0-6, TCMP, PD0, PD7	V_{OH}	I_{LOAD} = -0.2mA	V_{DD} - 0.3	-	-	V
PD1-5	V_{OH}	I_{LOAD} = -0.4mA	V_{DD} - 0.3	-	-	V
PC7	V_{OH}	I_{LOAD} = -1.5mA	V_{DD} - 0.3	-	-	V

DC Electrical Specifications HCL Product Type (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Low Voltage						
PA0-7, PB0-7, PC0-6, PD0-5, PD7, TCMP	V_{OL}	I_{LOAD} = 0.4mA	-	-	0.3	V
PC7	V_{OL}	I_{LOAD} = 5.0mA	-	-	0.3	V
Input High Voltage, PA0-7, PB0-7, PC0-7, PD0-5, PD7, TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IH}		0.7 x V_{DD}	-	V_{DD}	V
Input Low Voltage, PA0-7, PB0-7, PC0-7, PD0-5, PD7, TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IL}		V_{SS}	-	0.2 x V_{DD}	V
Data Retention Mode	V_{RM}	T_A = 0°C to 70°C	1.5	-	-	V
Wake Up Timer Oscillator Frequency	f_{RCO}	T_A = 25°C	-	13	-	kHz
Supply Current (f_{OSC} = 2MHz)						
Run (Note 20)	I_{DD}		-	1.0	1.4	mA
WAIT (Notes 19, 20, 21, 23)	I_{DD}		-	0.7	1.0	mA
STOP (Notes 21, 22)	I_{DD}	T_A = 25°C	-	1.0	5.0	µA
		T_A = 0°C to 70°C	-	-	10	µA
STOP with Wake Up Timer Enabled	I_{DD}	T_A = 25°C	-	10.0	-	µA
Supply Current (f_{OSC} = 1MHz)						
Run (Note 20)	I_{DD}		-	500	750	µA
WAIT (Notes 19, 20, 21, 23)	I_{DD}		-	300	500	µA
STOP (Notes 21, 22)	I_{DD}	T_A = 25°C	-	1.0	5.0	µA
		T_A = 0°C to 70°C	-	-	10	µA
I/O Ports Hi-Z Leakage Current - $\overline{RESET}$, PA0-7, PB0-7 (without Pullups), PC0-7, PD0-5, PD7	I_{IL}		-10	-	+10	µA
Pullup Current PB0-7 (with Pullups, Note 24)	I_{IN}		20	55	120	µA
Input Current - $\overline{IRQ}$, TCAP, OSC1	I_{IN}		-1	-	-1	µA
Capacitance Ports (As Input or Output) $\overline{RESET}$, $\overline{IRQ}$, TCAP, OSC1, PD0-5, PD7	C_{OUT}		-	-	12	pF
	C_{IN}		-	-	8	pF
CDP68HCL05C16B V_{DD} = 1.8V - 2.4V, V_{SS} = 0V, T_A = 0°C to 70°C (Note 17)						
Output Voltage	V_{OL}	$I_{LOAD} \leq 10\mu A$	-	-	0.1	V
	V_{OH}		V_{DD} - 0.1	-	-	V
Output High Voltage						
PA0-7, PB0-7, PC0-6, TCMP, PD0, PD7	V_{OH}	I_{LOAD} = -0.1mA	V_{DD} - 0.3	-	-	V
PD1-5	V_{OH}	I_{LOAD} = -0.2mA	V_{DD} - 0.3	-	-	V
PC7	V_{OH}	I_{LOAD} = -0.75mA	V_{DD} - 0.3	-	-	V
Output Low Voltage						
PA0-7, PB0-7, PC0-6, PD0-5, PD7, TCMP	V_{OL}	I_{LOAD} = 0.2mA	-	-	0.3	V
PC7	V_{OL}	I_{LOAD} = 2.0mA	-	-	0.3	V
Input High Voltage, PA0-7, PB0-7, PC0-7, PD0-5, PD7, TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IH}		0.7 x V_{DD}	-	V_{DD}	V

DC Electrical Specifications HCL Product Type (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage, PA0-7, PB0-7, PC0-7, PD0-5, PD7, TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IL}		V_{SS}	-	0.2 x V_{DD}	V
Data Retention Mode	V_{RM}	T_A = 0°C to 70°C	1.5	-	-	V
Wake Up Timer Oscillator Frequency	f_{RCO}	T_A = 25°C	-	13	-	kHz
Supply Current (f_{OSC} = 1MHz)						
Run (Note 20)	I_{DD}		-	300	600	µA
WAIT (Notes 19, 20, 21, 23)	I_{DD}		-	250	400	µA
STOP (Notes 21, 22)	I_{DD}	T_A = 25°C	-	1.0	2.0	µA
		T_A = 0°C to 70°C	-	-	5.0	µA
STOP with Wake Up Timer Enabled	I_{DD}	T_A = 25°C	-	10.0	-	µA
I/O Ports Hi-Z Leakage Current - $\overline{RESET}$, PA0-7, PB0-7 (without Pullups), PC0-7, PD0-5, PD7	I_{IL}		-10	-	+10	µA
Pullup Current PB0-7 (with Pullups, Note 24)	I_{IN}		20	45	75	µA
Input Current - $\overline{IRQ}$, TCAP, OSC1	I_{IN}		-1	-	+1	µA
Capacitance Ports (As Input or Output) $\overline{RESET}$, $\overline{IRQ}$, TCAP, OSC1, PD0-5, PD7	C_{OUT}		-	-	12	pF
	C_{IN}		-	-	8	pF

NOTES:

17. All values shown reflect average measurement.
18. Typical values at midpoint of voltage range, 25°C only.
19. Wait I_{DD}: Only timer system active (SPE = TE = RE = 0). If SPI, SCI active (SPE = TE = RE = 1) add 10% current draw.
20. Run (Operating) I_{DD}, Wait I_{DD}: Measured using external square-wave clock source, all inputs 0.2V from rail, no DC loads, less than 50pF on all outputs, C_L = 20pF on OSC2.
21. Wait, Stop I_{DD}: All ports configured as inputs, V_{IL} = 0.2V, V_{IH} = V_{DD} - 0.2V.
22. Stop I_{DD} measured with OSC1 = V_{SS}.
23. Wait I_{DD} is affected linearly by the OSC2 capacitance.
24. Input pullup current measured with V_{IL} = 0.2V.

Control Timing HCL Product Type

PARAMETER	SYMBOL	MIN	MAX	UNITS
CDP68HCL05C16B V_{DD} = 5V 10%, V_{SS} = 0V, T_A = 0°C to 70°C				
Frequency Of Operation				
Crystal Option	f_{OSC}	-	4.2	MHz
External Clock Option	f_{OSC}	DC	4.2	MHz
Internal Operating Frequency				
Crystal (f_{OSC} + 2)	f_{OP}	-	2.1	MHz
External Clock (f_{OSC} + 2)	f_{OP}	DC	2.1	MHz
Cycle Time (See Figure 11)	t_{CYC}	480	-	ns
Crystal Oscillator Start Up Time for AT-cut Crystal (See Figure 11)	t_{OXOV}	-	100	ms
Stop Recovery Start Up Time (AT-cut Crystal Oscillator) (See Figure 2)	t_{ILCH}	-	100	ms
$\overline{RESET}$ Pulse Width (See Figure 11)	t_{RL}	1.5	-	t_{CYC}

Control Timing HCL Product Type (Continued)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Timer				
Resolution (Note 26)	t_{RES}	4	-	t_{CYC}
Input Capture Pulse Width (See Figure 3)	t_{TH}, t_{TL}	125	-	ns
Input Capture Pulse Period (See Figure 3)	t_{TLTL}	(Note 27)	-	t_{CYC}
Interrupt Pulse Width Low (Edge-Triggered) (See Figure 15)	t_{ILIH}	125	-	ns
Interrupt Pulse Period (See Figure 15)	t_{ILIL}	(Note 25)	-	t_{CYC}
OSC1 Pulse Width	t_{OH}, t_{OL}	90	-	ns
CDP68HCL05C16B V_{DD} = 2.4V to 3.6V, V_{SS} = 0V, T_A = 0°C to 70°C (V_{DC} = 3.6)				
Frequency Of Operation				
Crystal Option	f_{OSC}	-	2.0	MHz
External Clock Option	f_{OSC}	DC	2.0	MHz
Internal Operating Frequency				
Crystal (f_{OSC} ÷ 2)	f_{OP}	-	1.0	MHz
External Clock (f_{OSC} ÷ 2)	f_{OP}	DC	1.0	MHz
Cycle Time (See Figure 11)	t_{CYC}	1000	-	ns
Crystal Oscillator Start Up Time for AT-cut Crystal (See Figure 11)	t_{OXOV}	-	100	ms
Stop Recovery Start Up Time (AT-cut Crystal Oscillator) (See Figure 2)	t_{ILCH}	-	100	ms
$\overline{\text{RESET}}$ Pulse Width (See Figure 11)	t_{RL}	1.5	-	t_{CYC}
Timer				
Resolution (Note 26)	t_{RES}	4.0	-	t_{CYC}
Input Capture Pulse Width (See Figure 3)	t_{TH}, t_{TL}	250	-	ns
Input Capture Pulse Period (See Figure 3)	t_{TLTL}	(Note 27)	-	t_{CYC}
Interrupt Pulse Width Low (Edge-Triggered) (See Figure 15)	t_{ILIH}	250	-	ns
Interrupt Pulse Period (See Figure 15)	t_{ILIL}	(Note 25)	-	t_{CYC}
OSC1 Pulse Width	t_{OH}, t_{OL}	200	-	ns
CDP68HCL05C16B V_{DD} = 2.4V to 3.6V, V_{SS} = 0V, T_A = 0°C to 70°C (V_{DC} = 2.4)				
Frequency Of Operation				
Crystal Option	f_{OSC}	-	1.0	MHz
External Clock Option	f_{OSC}	DC	1.0	MHz
Internal Operating Frequency				
Crystal (f_{OSC} ÷ 2)	f_{OP}	-	0.5	MHz
External Clock (f_{OSC} ÷ 2)	f_{OP}	DC	0.5	MHz
Cycle Time (See Figure 11)	t_{CYC}	2000	-	ns
Crystal Oscillator Start Up Time for AT-cut Crystal (See Figure 11)	t_{OXOV}	-	100	ms
Stop Recovery Start Up Time (AT-cut Crystal Oscillator) (See Figure 2)	t_{ILCH}	-	100	ms
$\overline{\text{RESET}}$ Pulse Width (See Figure 11)	t_{RL}	1.5	-	t_{CYC}

Control Timing HCL Product Type (Continued)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Timer				
Resolution (Note 26)	t_{RES}	4.0	-	t_{CYC}
Input Capture Pulse Width (See Figure 3)	t_{TH}, t_{TL}	500	-	ns
Input Capture Pulse Period (See Figure 3)	t_{TLTL}	(Note 27)	-	t_{CYC}
Interrupt Pulse Width Low (Edge-Triggered) (See Figure 15)	t_{ILIH}	500	-	ns
Interrupt Pulse Period (See Figure 15)	t_{ILIL}	(Note 25)	-	t_{CYC}
OSC1 Pulse Width	t_{OH}, t_{OL}	400	-	ns

NOTES:

25. The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{CYC}.
26. Since a 2-bit prescaler in the timer must count four internal cycles (t_{CYC}), this is the limiting minimum factor in determining the timer resolution.
27. The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{CYC}.

Serial Peripheral Interface (SPI) Timing (See Figure 4) HCL Product Type

LEAD	PARAMETER	SYMBOL	MIN	MAX	UNITS
CDP68HCL05C16B V_{DD} = 5V ±10%, V_{SS} = 0V, T_A = 0°C to 70°C Unless Otherwise Specified					
	Operating Frequency				
	Master	$f_{OP(M)}$	DC	0.5	f_{OP} (Note 30)
	Slave	$f_{OP(S)}$	DC	2.1	MHz
1	Cycle Time				
	Master	$t_{CYC(M)}$	2.0	-	t_{CYC}
	Slave	$t_{CYC(S)}$	480	-	ns
2	Enable Lead Time				
	Master	$t_{LEAD(M)}$	(Note 28)	-	-
	Slave	$t_{LEAD(S)}$	240	-	ns
3	Enable Lag Time				
	Master	$t_{LAG(M)}$	(Note 28)	-	-
	Slave	$t_{LAG(S)}$	720	-	ns
4	Clock (SCK) High Time				
	Master	$t_{W(SCKH)M}$	340	-	ns
	Slave	$t_{W(SCKH)S}$	190	-	ns
5	Clock (SCK) Low Time				
	Master	$t_{W(SCKL)M}$	340	-	ns
	Slave	$t_{W(SCKL)S}$	190	-	ns
6	Data Setup Time (Inputs)				
	Master	$t_{SU(M)}$	100	-	ns
	Slave	$t_{SU(S)}$	100	-	ns
7	Data Hold Time (Inputs)				
	Master	$t_{H(M)}$	100	-	ns
	Slave	$t_{H(S)}$	100	-	ns

Serial Peripheral Interface (SPI) Timing (See Figure 4) HCL Product Type (Continued)

LEAD	PARAMETER	SYMBOL	MIN	MAX	UNITS
8	Access Time (Time to Data Active from High Impedance State) Slave	t_A	0	120	ns
9	Disable Time (Hold Time to High Impedance State) Slave	t_{DIS}	-	240	ns
10	Data Valid Time Master (Before Capture Edge)	$t_{V(M)}$	0.25	-	$t_{CYC(M)}$
	Slave (After Enable Edge) (Note 29)	$t_{V(S)}$	-	240	ns
11	Data Hold Time (Outputs) Master (After Capture Edge)	$t_{HO(M)}$	0.25	-	$t_{CYC(M)}$
	Slave (After Enable Edge)	$t_{HO(S)}$	0	-	ns
12	Rise Time (V_{DD} = 20% to 70%, C_L = 200pF) SPI Outputs (SCK, MOSI, MISO)	$t_{r(M)}$	-	100	ns
	SPI Inputs (SCK, MOSI, MISO, $\overline{SS}$)	$t_{r(S)}$	-	2.0	µs
13	Fall Time (V_{DD} = 20% to 70%, C_L = 200pF) SPI Outputs (SCK, MOSI, MISO)	$t_{f(M)}$	-	100	ns
	SPI Inputs (SCK, MOSI, MISO, $\overline{SS}$)	$t_{f(S)}$	-	2.0	µs
CDP68HCL05C16B V_{DD} = 2.5V - 3.6V$_{DC}$, V_{SS} = 0V, T_A = 0°C to 70°C Unless Otherwise Specified					
	Operating Frequency Master	$f_{OP(M)}$	DC	0.5	f_{OP} (Note 30)
	Slave	$f_{OP(S)}$	DC	2.1	MHz
1	Cycle Time Master	$t_{CYC(M)}$	2.0	-	t_{CYC}
	Slave	$t_{CYC(S)}$	480	-	ns
2	Enable Lead Time Master	$t_{LEAD(M)}$	(Note 28)	-	-
	Slave	$t_{LEAD(S)}$	240	-	ns
3	Enable Lag Time Master	$t_{LAG(M)}$	(Note 28)	-	-
	Slave	$t_{LAG(S)}$	720	-	ns
4	Clock (SCK) High Time Master	$t_{W(SCKH)M}$	340	-	ns
	Slave	$t_{W(SCKH)S}$	190	-	ns
5	Clock (SCK) Low Time Master	$t_{W(SCKL)M}$	340	-	ns
	Slave	$t_{W(SCKL)S}$	190	-	ns
6	Data Setup Time (Inputs) Master	$t_{SU(M)}$	100	-	ns
	Slave	$t_{SU(S)}$	100	-	ns

Serial Peripheral Interface (SPI) Timing (See Figure 4) HCL Product Type (Continued)

LEAD	PARAMETER	SYMBOL	MIN	MAX	UNITS
7	Data Hold Time (Inputs)				
	Master	$t_{H(M)}$	100	-	ns
	Slave	$t_{H(S)}$	100	-	ns
8	Access Time (Time to Data Active from High Impedance State)				
	Slave	t_A	0	120	ns
9	Disable Time (Hold Time to High Impedance State)				
	Slave	t_{DIS}	-	240	ns
10	Data Valid Time				
	Master (Before Capture Edge)	$t_{V(M)}$	0.25	-	$t_{CYC(M)}$
	Slave (After Enable Edge) (Note 29)	$t_{V(S)}$	-	240	ns
11	Data Hold Time (Outputs)				
	Master (After Capture Edge)	$t_{HO(M)}$	0.25	-	$t_{CYC(M)}$
	Slave (After Enable Edge)	$t_{HO(S)}$	0	-	ns
12	Rise Time (V_{DD} = 20% to 70%, C_L = 200pF)				
	SPI Outputs (SCK, MOSI, MISO)	$t_{r(M)}$	-	100	ns
	SPI Inputs (SCK, MOSI, MISO, $\overline{SS}$)	$t_{r(S)}$	-	2.0	µs
13	Fall Time (V_{DD} = 20% to 70%, C_L = 200pF)				
	SPI Outputs (SCK, MOSI, MISO)	$t_{f(M)}$	-	100	ns
	SPI Inputs (SCK, MOSI, MISO, $\overline{SS}$)	$t_{f(S)}$	-	2.0	µs

NOTES:

28. Signal Production depends on software.
29. Assumes 200pF load on all SPI pins.
30. Note that the units this specification uses is f_{OP} (internal operating frequency), not MHz! In the master mode the SPI bus is capable of running at one-half of the devices's internal operating frequency, therefore 5V: 1.05MHz maximum.

DC Electrical Specifications HSC Product Type

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CDP68HSC05C16B V_{DD} = 5V ±10%, V_{SS} = 0V, T_A = 0°C to 85°C (Notes 31, 32)						
Output Voltage	V_{OL}	I_{LOAD} ≤10µA	-	-	0.1	V
	V_{OH}		V_{DD} - 0.1	-	-	V
Output High Voltage						
PA0-7, PB0-7, PC0-6, TCMP, PD0, PD7	V_{OH}	I_{LOAD} = -0.8mA	V_{DD} - 0.8	-	-	V
PD1-5	V_{OH}	I_{LOAD} = -1.6mA	V_{DD} - 0.8	-	-	V
PC7	V_{OH}	I_{LOAD} = -5.0mA	V_{DD} - 0.8	-	-	V
Output Low Voltage						
PA0-7, PB0-7, PC0-6, PD0-5, PD7, TCMP	V_{OL}	I_{LOAD} = 1.6mA	-	-	0.4	V
PC7	V_{OL}	I_{LOAD} = 10.0mA	-	-	0.4	V
Input High Voltage, PA0-7, PB0-7, PC0-7, PD0-5, PD7, TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IH}		0.7 x V_{DD}	-	V_{DD}	V
Input Low Voltage, PA0-7, PB0-7, PC0-7, PD0-5, PD7, TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IL}		V_{SS}	-	0.2 x V_{DD}	V

DC Electrical Specifications HSC Product Type (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Retention Mode	V_{RM}	T_A = 0°C to 70°C	1.5	-	-	V
Supply Current (f_{OSC} = 8.0MHz) Run (Note 34)	I_{DD}		-	7	11	mA
WAIT (Notes 33, 34, 35, 37)	I_{DD}		-	2	6.5	mA
STOP (Notes 35, 36)	I_{DD}	T_A = 25°C	-	1	20	µA
		T_A = 0°C to 70°C	-	-	40	µA
		T_A = -40°C to 85°C	-	-	50	µA
STOP with Wake Up Timer Enabled	I_{DD}	T_A = 25°C	-	10.0	-	µA
Wake Up Timer Oscillator Frequency	f_{RCO}	T_A = 25°C	-	13	-	kHz
I/O Ports Hi-Z Leakage Current - $\overline{RESET}$, PA0-7, PB0-7 (without pullups), PC0-7, PD0-5, PD7	I_{IL}		-10	-	+10	µA
Pullup Current PB0-7 (with pullups)	I_{IN}		60	140	300	µA
Input Current - $\overline{IRQ}$, TCAP, OSC1	I_{IN}		-1	-	+1	µA
Capacitance Ports (As Input or Output) $\overline{RESET}$, $\overline{IRQ}$, TCAP, OSC1, PD0-5, PD7	C_{OUT}		-	-	12	pF
	C_{IN}		-	-	8	pF
CDP68HSC05C16B V_{DD} = 2.4V - 3.6V, V_{SS} = 0V, T_A = 0°C to 85°C, Unless Otherwise Specified						
Output Voltage	V_{OL}	I_{LOAD} ≤10µA	-	-	0.1	V
	V_{OH}		V_{DD} - 0.1	-	-	V
Output High Voltage PA0-7, PB0-7, PC0-6, TCMP, PD0, PD7	V_{OH}	I_{LOAD} = -0.2mA	V_{DD} - 0.3	-	-	V
PD1-5	V_{OH}	I_{LOAD} = -0.4mA	V_{DD} - 0.3	-	-	V
PC7	V_{OH}	I_{LOAD} = -1.5mA	V_{DD} - 0.3	-	-	V
Output Low Voltage PA0-7, PB0-7, PC0-6, PD0-5, PD7, TCMP	V_{OL}	I_{LOAD} = 0.4mA	-	-	0.3	V
PC7	V_{OL}	I_{LOAD} = 6.0mA	-	-	0.3	V
Input High Voltage, PA0-7, PB0-7, PC0-7, PD0-5, PD7, TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IH}		0.7 x V_{DD}	-	V_{DD}	V
Input Low Voltage, PA0-7, PB0-7, PC0-7, PD0-5, PD7, TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IL}		V_{SS}	-	0.2 x V_{DD}	V
Data Retention Mode	V_{RM}	T_A = 0°C to 70°C	1.5	-	-	V
Supply Current (f_{OSC} = 4.0MHz) Run (Note 34)	I_{DD}		-	2.5	4	mA
WAIT (Notes 33, 34, 35, 37)	I_{DD}		-	1	2	mA
STOP (Notes 35, 36)	I_{DD}	T_A = 25°C	-	1	8	µA
		T_A = 0°C to 70°C	-	-	16	µA
		T_A = -40°C to 85°C	-	-	20	µA
STOP with Wake Up Timer Enabled	I_{DD}	T_A = 25°C	-	10.0	-	µA
Wake Up Timer Oscillator Frequency	f_{RCO}	T_A = 25°C	-	13	-	kHz

DC Electrical Specifications HSC Product Type (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O Ports Hi-Z Leakage Current - $\overline{RESET}$, PA0-7, PB0-7 (without Pullups), PC0-7, PD0-5, PD7	I_{IL}		-10	-	+10	µA
Pullup Current PB0-7 (with Pullups)	I_{IN}		25	65	140	µA
Input Current - $\overline{IRQ}$, TCAP, OSC1	I_{IN}		-	-	±1	µA
Capacitance Ports (As Input or Output) $\overline{RESET}$, $\overline{IRQ}$, TCAP, OSC1, PD0-5, PD7	C_{OUT}		-	-	12	pF
	C_{IN}		-	-	8	pF

NOTES:

31. All values shown reflect average measurement.
32. Typical values at midpoint of voltage range, 25°C only.
33. Wait I_{DD}: Only timer system active (SPE = TE = RE = 0). If SPI, SCI active (SPE = TE = RE = 1) add 10% current draw.
34. Run (Operating) I_{DD}, Wait I_{DD}: Measured using external square-wave clock source, all inputs 0.2V from rail, no DC loads, less than 50pF on all outputs, C_L = 20pF on OSC2.
35. Wait, Stop I_{DD}: All ports configured as inputs, V_{IL} = 0.2V, V_{IH} = V_{DD} - 0.2V.
36. Stop I_{DD} measured with OSC1 = V_{SS}.
37. Wait I_{DD} is affected linearly by the OSC2 capacitance.

Control Timing HSC Product Type

PARAMETER	SYMBOL	MIN	MAX	UNITS
CDP68HSC05C16B V_{DD} = 5V ±10%, V_{SS} = 0V, T_A = 0°C to 85°C, Unless Otherwise Specified				
Frequency Of Operation				
Crystal Option	f_{OSC}	-	8.2	MHz
External Clock Option	f_{OSC}	DC	8.2	MHz
Internal Operating Frequency				
Crystal (f_{OSC} + 2)	f_{OP}	-	4.1	MHz
External Clock (f_{OSC} + 2)	f_{OP}	DC	4.1	MHz
Cycle Time (See Figure 11)	t_{CYC}	250	-	ns
Crystal Oscillator Start Up Time for AT-cut Crystal (See Figure 11)	t_{OXOV}	-	100	ms
Stop Recovery Start Up Time (AT-cut Crystal Oscillator) (See Figure 2)	t_{ILCH}	-	100	ms
$\overline{RESET}$ Pulse Width (See Figure 11)	t_{RL}	1.5	-	t_{CYC}
Timer				
Resolution (Note 39)	t_{RES}	4	-	t_{CYC}
Input Capture Pulse Width (See Figure 3)	t_{TH}, t_{TL}	64	-	ns
Input Capture Pulse Period (See Figure 3)	t_{TLTL}	(Note 40)	-	t_{CYC}
Interrupt Pulse Width Low (Edge-Triggered) (See Figure 15)	t_{ILIH}	64	-	ns
Interrupt Pulse Period (See Figure 15)	t_{ILIL}	(Note 38)	-	t_{CYC}
OSC1 Pulse Width	t_{OH}, t_{OL}	50	-	ns
CDP68HSC05C16B V_{DD} = 2.4V - 3.6V, V_{SS} = 0V, T_A = 0°C to 85°C, Unless Otherwise Specified				
Frequency Of Operation				
Crystal Option	f_{OSC}	-	4.2	MHz
External Clock Option	f_{OSC}	DC	4.2	MHz

Control Timing HSC Product Type (Continued)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Internal Operating Frequency				
Crystal (f_{OSC} + 2)	f_{OP}	-	2.1	MHz
External Clock (f_{OSC} + 2)	f_{OP}	DC	2.1	MHz
Cycle Time (See Figure 11)	t_{CYC}	1000	-	ns
Crystal Oscillator Start Up Time for AT-cut Crystal (See Figure 11)	t_{OXOV}	-	100	ms
Stop Recovery Start Up Time (AT-cut Crystal Oscillator) (See Figure 2)	t_{ILCH}	-	100	ms
$\overline{\text{RESET}}$ Pulse Width (See Figure 11)	t_{RL}	1.5	-	t_{CYC}
Timer				
Resolution (Note 39)	t_{RES}	4	-	t_{CYC}
Input Capture Pulse Width (See Figure 3)	t_{TH}, t_{TL}	125	-	ns
Input Capture Pulse Period (See Figure 3)	t_{TLTL}	(Note 40)	-	t_{CYC}
Interrupt Pulse Width Low (Edge-Triggered) (See Figure 15)	t_{ILIH}	125	-	ns
Interrupt Pulse Period (See Figure 15)	t_{ILIL}	(Note 38)	-	t_{CYC}
OSC1 Pulse Width	t_{OH}, t_{OL}	90	-	ns

NOTES:

38. The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{CYC}.
39. Since a 2-bit prescaler in the timer must count four internal cycles (t_{CYC}), this is the limiting minimum factor in determining the timer resolution.
40. The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{CYC}.

Serial Peripheral Interface (SPI) Timing (See Figure 4) HSC Product Type

LEAD	PARAMETER	SYMBOL	MIN	MAX	UNITS
CDP68HSC05C16B V_{DD} = 5V ±10%, V_{SS} = 0V, T_A = 0°C to 85°C Unless Otherwise Specified					
	Operating Frequency				
	Master	$f_{OP(M)}$	DC	0.5	f_{OP} (Note 43)
	Slave	$f_{OP(S)}$	DC	4.1	MHz
1	Cycle Time				
	Master	$t_{CYC(M)}$	2.0	-	t_{CYC}
	Slave	$t_{CYC(S)}$	244	-	ns
2	Enable Lead Time				
	Master	$t_{LEAD(M)}$	(Note 41)	-	-
	Slave	$t_{LEAD(S)}$	122	-	ns
3	Enable Lag Time				
	Master	$t_{LAG(M)}$	(Note 41)	-	-
	Slave	$t_{LAG(S)}$	366	-	ns
4	Clock (SCK) High Time				
	Master	$t_{W(SCKH)M}$	166	-	ns
	Slave	$t_{W(SCKH)S}$	93	-	ns
5	Clock (SCK) Low Time				
	Master	$t_{W(SCKL)M}$	166	-	ns
	Slave	$t_{W(SCKL)S}$	93	-	ns

Serial Peripheral Interface (SPI) Timing (See Figure 4) **HSC Product Type (Continued)**

LEAD	PARAMETER	SYMBOL	MIN	MAX	UNITS
6	Data Setup Time (Inputs)				
	Master	$t_{SU(M)}$	49	-	ns
	Slave	$t_{SU(S)}$	49	-	ns
7	Data Hold Time (Inputs)				
	Master	$t_{H(M)}$	49	-	ns
	Slave	$t_{H(S)}$	49	-	ns
8	Access Time (Time to Data Active from High Impedance State)				
	Slave	t_A	0	61	ns
9	Disable Time (Hold Time to High Impedance State)				
	Slave	t_{DIS}	-	122	ns
10	Data Valid Time				
	Master (Before Capture Edge)	$t_{V(M)}$	0.25	-	$t_{CYC(M)}$
	Slave (After Enable Edge) (Note 42)	$t_{V(S)}$	-	122	ns
11	Data Hold Time (Outputs)				
	Master (After Capture Edge)	$t_{HO(M)}$	0.25	-	$t_{CYC(M)}$
	Slave (After Enable Edge)	$t_{HO(S)}$	0	-	ns
12	Rise Time (V_{DD} = 20% to 70%, C_L = 200pF)				
	SPI Outputs (SCK, MOSI, MISO)	$t_{r(M)}$	-	50	ns
	SPI Inputs (SCK, MOSI, MISO, $\overline{SS}$)	$t_{r(S)}$	-	1.0	µs
13	Fall Time (V_{DD} = 20% to 70%, C_L = 200pF)				
	SPI Outputs (SCK, MOSI, MISO)	$t_{f(M)}$	-	50	ns
	SPI Inputs (SCK, MOSI, MISO, $\overline{SS}$)	$t_{f(S)}$	-	1.0	µs
CDP68HSC05C16B V_{DD} = 2.4V to 3.6V, V_{SS} = 0V, T_A = 0°C to 85°C Unless Otherwise Specified					
	Operating Frequency				
	Master	$f_{OP(M)}$	DC	0.5	f_{OP} (Note 43)
	Slave	$f_{OP(S)}$	DC	2.1	MHz
1	Cycle Time				
	Master	$t_{CYC(M)}$	2.0	-	t_{CYC}
	Slave	$t_{CYC(S)}$	480	-	ns
2	Enable Lead Time				
	Master	$t_{LEAD(M)}$	(Note 41)	-	-
	Slave	$t_{LEAD(S)}$	240	-	ns
3	Enable Lag Time				
	Master	$t_{LAG(M)}$	(Note 41)	-	-
	Slave	$t_{LAG(S)}$	720	-	ns
4	Clock (SCK) High Time				
	Master	$t_{W(SCKH)M}$	340	-	ns
	Slave	$t_{W(SCKH)S}$	190	-	ns
5	Clock (SCK) Low Time				
	Master	$t_{W(SCKL)M}$	340	-	ns
	Slave	$t_{W(SCKL)S}$	190	-	ns
6	Data Setup Time (Inputs)				
	Master	$t_{SU(M)}$	100	-	ns
	Slave	$t_{SU(S)}$	100	-	ns

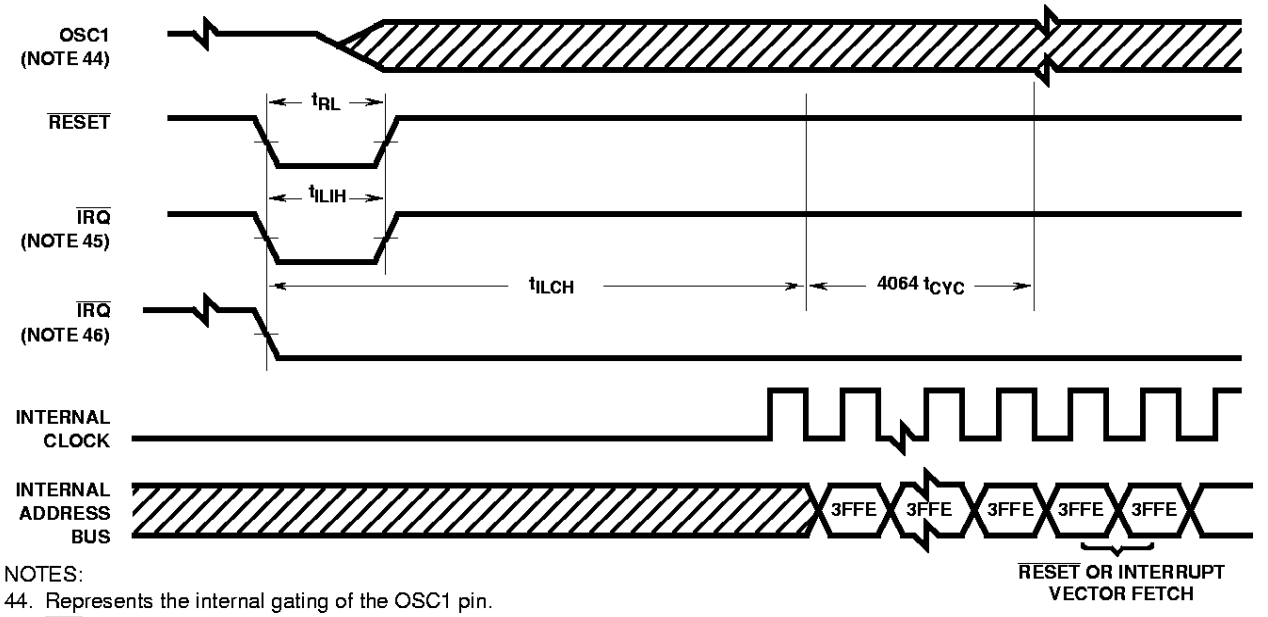
Serial Peripheral Interface (SPI) Timing (See Figure 4) **HSC Product Type (Continued)**

LEAD	PARAMETER	SYMBOL	MIN	MAX	UNITS
7	Data Hold Time (Inputs)				
	Master	$t_{H(M)}$	100	-	ns
	Slave	$t_{H(S)}$	100	-	ns
8	Access Time (Time to Data Active from High Impedance State)				
	Slave	t_A	0	120	ns
9	Disable Time (Hold Time to High Impedance State)				
	Slave	t_{DIS}	-	240	ns
10	Data Valid Time				
	Master (Before Capture Edge)	$t_{V(M)}$	0.25	-	$t_{CYC(M)}$
	Slave (After Enable Edge) (Note 42)	$t_{V(S)}$	-	240	ns
11	Data Hold Time (Outputs)				
	Master (After Capture Edge)	$t_{HO(M)}$	0.25	-	$t_{CYC(M)}$
	Slave (After Enable Edge)	$t_{HO(S)}$	0	-	ns
12	Rise Time (V_{DD} = 20% to 70%, C_L = 200pF)				
	SPI Outputs (SCK, MOSI, MISO)	$t_{r(M)}$	-	100	ns
	SPI Inputs (SCK, MOSI, MISO, $\overline{SS}$)	$t_{r(S)}$	-	2.0	µs
13	Fall Time (V_{DD} = 20% to 70%, C_L = 200pF)				
	SPI Outputs (SCK, MOSI, MISO)	$t_{f(M)}$	-	100	ns
	SPI Inputs (SCK, MOSI, MISO, $\overline{SS}$)	$t_{f(S)}$	-	2.0	µs

NOTES:

41. Signal Production depends on software.
42. Assumes 200pF load on all SPI pins.
43. Note that the units this specification uses is f_{OP} (internal operating frequency), not MHz! In the master mode the SPI bus is capable of running at one-half of the devices's internal operating frequency, therefore 5V: 2.0MHz and 2.4V to 3.6V: 500kHz maximum.

Waveforms



NOTES:

44. Represents the internal gating of the OSC1 pin.
45. $\overline{IRQ}$ pin edge-sensitive mask option.
46. $\overline{IRQ}$ pin level and edge-sensitive mask option.

FIGURE 2. STOP RECOVERY TIMING DIAGRAM

Waveforms (Continued)

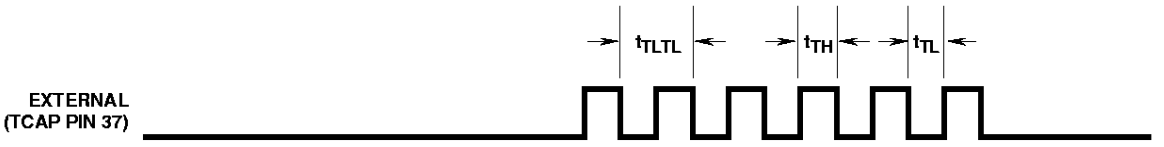


FIGURE 3. TIMER RELATIONSHIPS

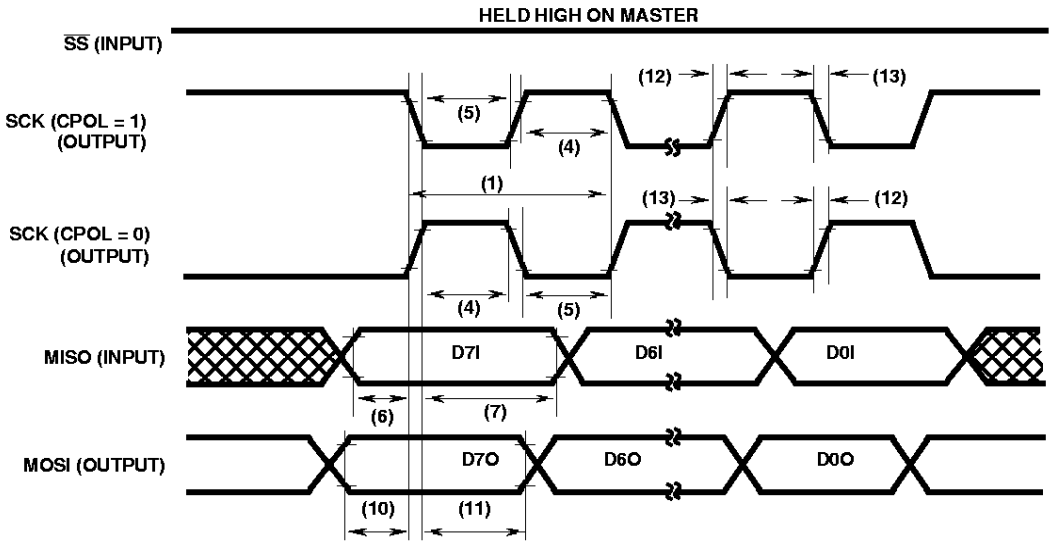


FIGURE 4A. SPI MASTER TIMING CPHA = 0

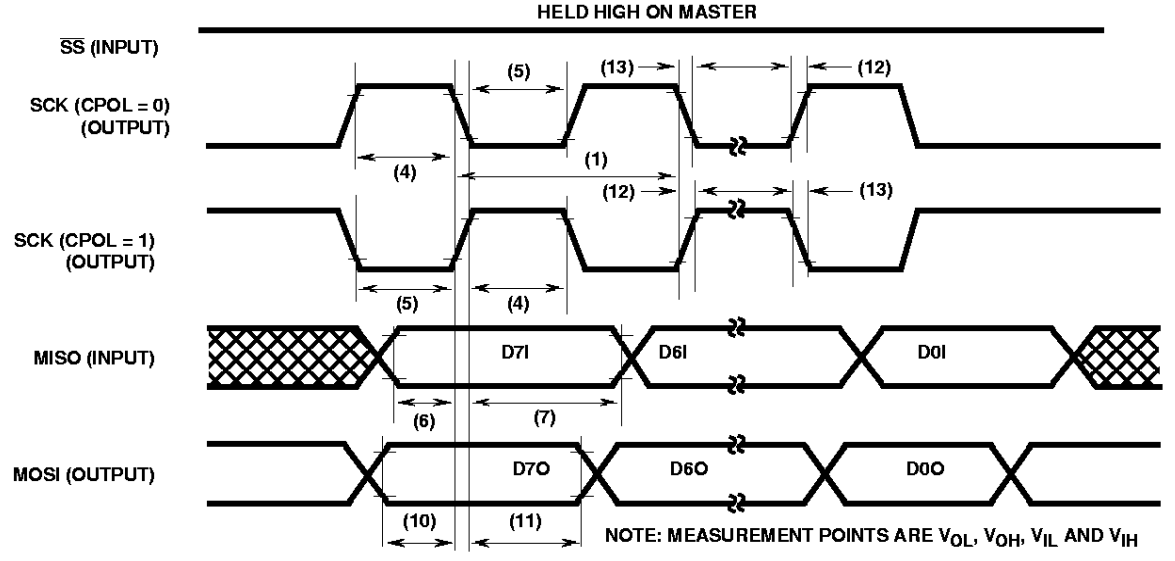


FIGURE 4B. SPI MASTER TIMING CPHA = 1

Waveforms (Continued)

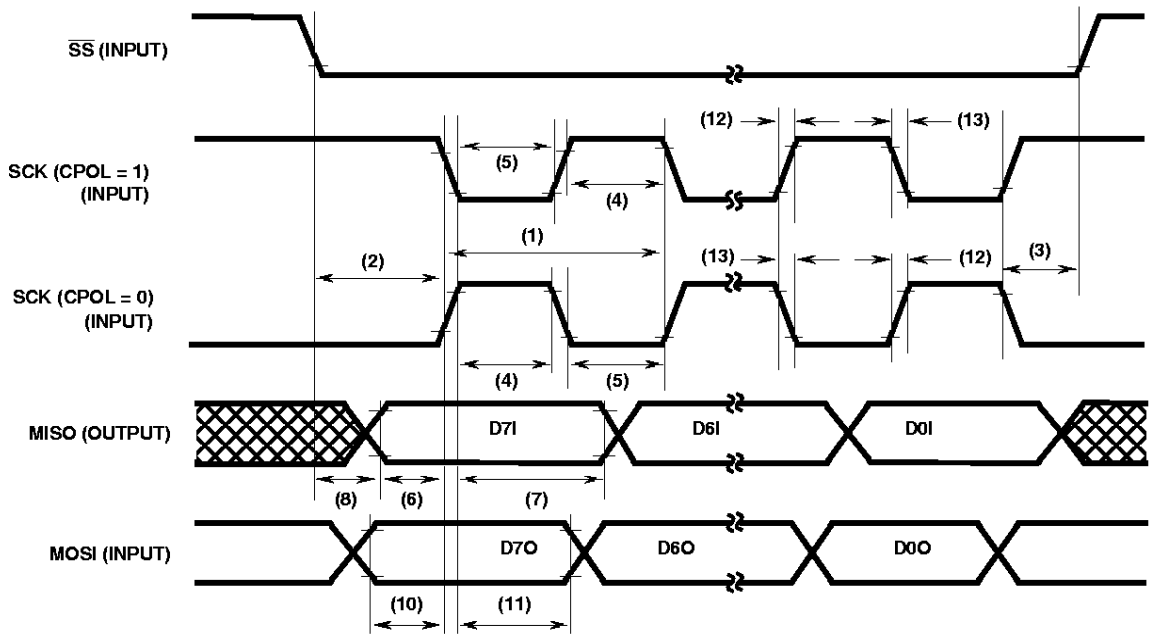


FIGURE 4C. SPI SLAVE TIMING CPHA = 0

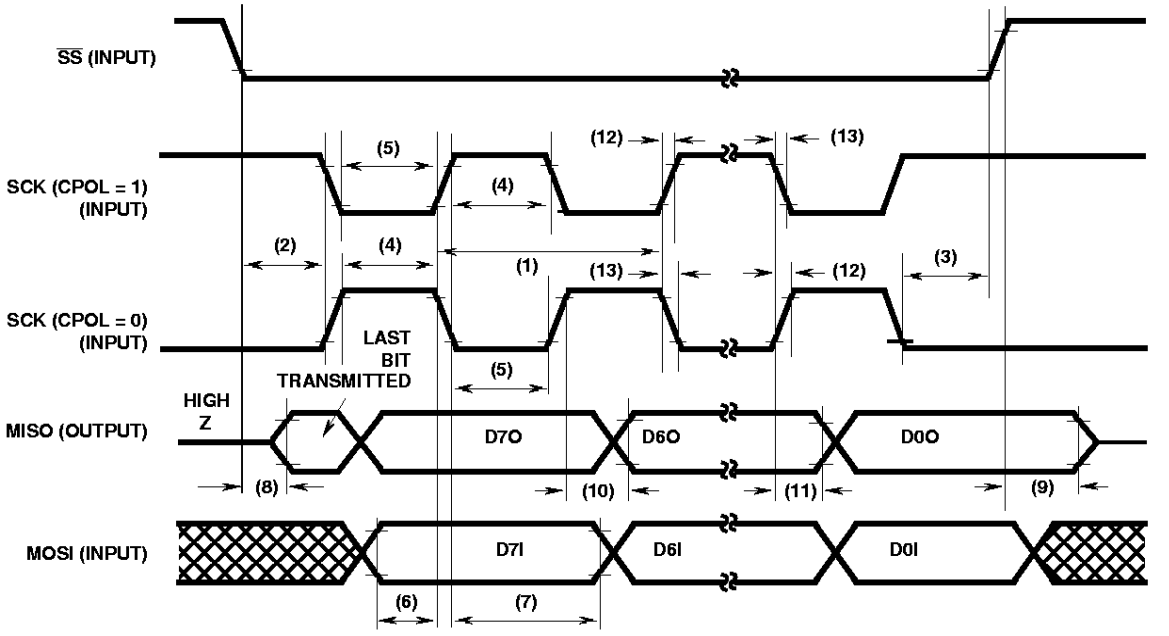


FIGURE 4D. SPI SLAVE TIMING CPHA = 1

The following sections provide a description of the functional pins, Input/Output programming, software programmable options, memory, CPU registers and self check mode for the Harris CDP68HC05C16B microcontroller. See pages 2 and 67 for ordering information.

Functional Pin Description

V_{DD} and V_{SS}

Power is supplied to the MCU using these two pins. V_{DD} is power and V_{SS} is ground.

$\overline{IRQ}$ (Maskable Interrupt Request)

IRQ is an external maskable interrupt which can force the MCU into an interrupt service routine. The IRQ pin on the C16B has a software programmable option which provides two different choices of interrupt triggering sensitivity. The options that can be chosen are: 1.) Negative edge-sensitive triggering only, or 2.) Both negative edge-sensitive and level-sensitive triggering. The IRQ options are chosen by either setting or clearing the IRQ bit in the OPTION register (See ***Software Programmable Options*** for details). In the latter case, either type of input to the IRQ pin will produce the interrupt. The MCU completes the current instruction before it responds to the interrupt request. When the IRQ pin goes low for at least one t_{ILIH}, a logic one is latched internally to signify an interrupt has been requested. When the MCU completes its current instruction, the interrupt latch is tested. If the interrupt latch contains a logic one, and the interrupt mask bit (I bit) in the condition code register is clear, the MCU then begins the interrupt sequence.

If the option is selected to include level-sensitive triggering, then the $\overline{IRQ}$ input requires an external resistor to V_{DD} for "wire-OR" operation. See **INTERRUPTS** for more detail concerning interrupts.

$\overline{RESET}$

The RESET input is not required for start up but can be used to reset the MCU internal state and provide an orderly software start up procedure. Refer to RESETS for a detailed description.

TCAP

The TCAP input controls the input capture feature for the on-chip programmable timer system. Refer to Input Capture Register for additional information.

TCMP

The TCMP pin (35) provides an output for the output compare feature of the on-chip timer system. Refer to Output Compare Register for additional information.

OSC1, OSC2

The CDP68HC05C16B family of MCUs can be configured to accept either a crystal input or an RC network to control the internal oscillator. The internal clocks are derived by a divide-by-two of the internal oscillator frequency (f_{OSC}).

Crystal

The circuit shown in Figure 5B is recommended when using a crystal. The internal oscillator is designed to interface with an AT-cut parallel resonant quartz-crystal resonator in the frequency range specified for f_{OSC} in Control Timing. Use of an external CMOS oscillator is recommended when crystals outside the specified ranges are to be used. The crystal and components should be mounted as close as possible to the input pins to minimize output distortion and start up stabilization time. Refer to DC Electrical Specifications for V_{DD} specifications.

Ceramic Resonator

A ceramic resonator may be used in place of the crystal in cost-sensitive applications. The circuit in Figure 5B is recommended when using a ceramic resonator. Figure 5A lists the recommended capacitance and feedback resistance values. The manufacturer of the particular ceramic resonator being considered should be consulted for specific information.

RC

If the RC oscillator option is selected, then a resistor is connected to the oscillator pins as shown in Figure 5D.

External Clock

An external clock should be applied to the OSC1 input with the OSC2 input not connected, as shown in Figure 5E. An external clock may be used with either the RC or crystal oscillator option. The t_{OXOV} or t_{ILCH} specifications do not apply when using an external clock input. The equivalent specification of the external clock source should be used in lieu of t_{OXOV} or t_{ILCH}.

PA0 - PA7

These eight I/O lines comprise port A. The state of any pin is software programmable and all port A lines are configured as inputs during power-on or reset. Port A pins PA7 - PA4 are mask programmable to provide fixed tone/simple PWM outputs. The port A data register (PORTA) is at location $0000 and the port A data direction register (DDRA) is at location $0004. Refer to ***Input/Output Programming*** paragraph for a detailed description of I/O programming.

PB0 - PB7

These eight lines comprise port B. The state of any pin is software programmable and all port B lines are configured as inputs during power-on or reset. Each of the port B pins has a mask programmable interrupt and pullup option. This makes port B ideal for keyboard scanning. The port B data register (PORTB) is at location $0001 and the port B data direction register (DDRB) is at location $0005. Refer to ***Input/Output Programming*** paragraph for a detailed description of I/O programming.

PC0 - PC7

These eight lines comprise port C. The state of any pin is software programmable and all port C lines are configured as inputs during power-on reset. PC7 has a high current sink and source output stage. The port C data register (PORTC) is at location $0002 and the port C data direction register (DDRC) is at location $0006. Refer to ***Input/Output Programming*** paragraph for a detailed description of I/O programming.

CRYSTAL

	2MHz	4MHz	UNITS
R_{SMAX}	400	75	Ω
C_0	5	7	pF
C_1	0.008	0.012	pF
C_{OSC1}	15 - 40	15 - 30	pF
C_{OSC2}	15 - 30	15 - 25	pF
R_P	10	10	MΩ
Q	30	40	K

CERAMIC RESONATOR

	2MHz - 4MHz	UNITS
R_S (Typical)	10	Ω
C_0	40	pF
C_1	4.3	pF
C_{OSC1}	30	pF
C_{OSC2}	30	pF
R_P	1 - 10	MΩ
Q	1250	-

FIGURE 5A. CRYSTAL/CERAMIC RESONATOR PARAMETERS

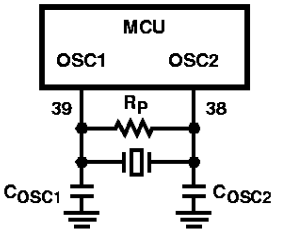


FIGURE 5B. CRYSTAL OSCILLATOR CONNECTIONS

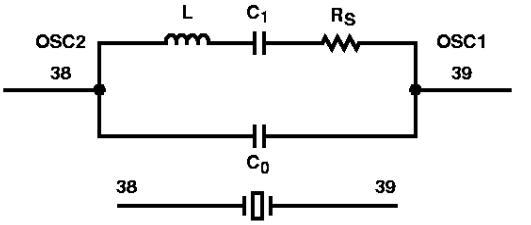


FIGURE 5C. EQUIVALENT CRYSTAL CIRCUIT

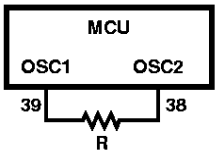


FIGURE 5D. RC OSCILLATOR CONNECTIONS

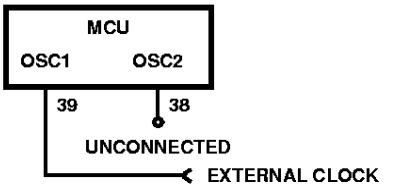


FIGURE 5E. EXTERNAL CLOCK SOURCE CONNECTIONS

PD0 - PD5, PD7

These seven lines comprise port D. The state of each port pin is software programmable and all Port D pins are configured as inputs during reset. Two of the CDP68HC05C16B's subblocks make use of the pins on this port. Four of the lines, PD2/MISO, PD3/MOSI, PD4/SCK, and PD5/$\overline{SS}$, are used for the serial peripheral interface (SPI). Two of these lines, PD0/RDI and PD1/TD0, are used for the serial communications interface (SCI). Both the SCI and the SPI systems are disabled during power-on or reset configuring all pins as inputs. The port D data register (PORTD) is at location $0003 and the Port D data direction register (DDRD) is located at $0007. Refer to ***Input/Output Programming*** for a detailed description of I/O programming.

Input/Output Programming

Bidirectional Parallel Ports A, B, C and D

Each I/O pin of ports A, B, C and D can be programmed as an input or an output under software control. Each port has an data register (PORTn) and an associated data direction register (DDRn). All registers are 8 bits wide except for the port D data and data direction which are 7 bits wide. The direction of the pins is determined by the state of the corresponding bit in the DDRn.

TABLE 1. I/O PIN FUNCTIONS

(NOTE) R/$\overline{W}$	DDRn BIT	I/O PIN FUNCTION
0	0	The I/O pin is in input mode. Data is written into the output data latch.
0	1	Data is written into the output data latch and output to the I/O pin.
1	0	The state of the I/O pin is read.
1	1	The I/O pin is in an output mode. The output data latch is read.

NOTE: R/$\overline{W}$ is an internal signal.

The data direction registers are capable of being written to or read by the processor. Refer to Figure 6 and Table 1. Any port A, port B, port C, or port D pin is configured as an output if its corresponding DDRn bit is set to a logic one. When configured as an output, the pin will be driven to V_{DD} if the associated PORTn bit is a 1 and it will be driven to V_{SS} if the associated PORTn bit is a 0. During the programmed output state, a read of the data register actually reads the value of the output data latch and not the I/O pin (see Figure 6A). At power-on or reset, all DDR bits are cleared, which configures all port A, B, C, and D pins as inputs.

Port A4 - A7 Tone/Simple PWM Output Option

In addition to being a standard bidirectional port, four bits of Port A (PA4 - PA7) have a mask option to connect an internal "tone" signal to the output (see Figure 6D). When the option is selected a fixed frequency will appear on the output pin whenever the appropriate PORTA and DDRA bits are set. A second mask option disables the output NMOS device allowing wire-ORing of the pins to produce various duty cycle outputs creating a simple PWM (see Figure 6D). Refer to ***Port A Tone and Simple PWM Circuitry*** for a detailed explanation.

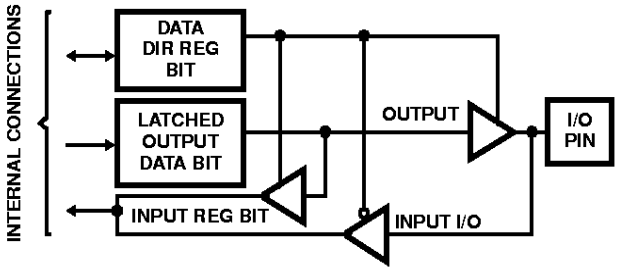
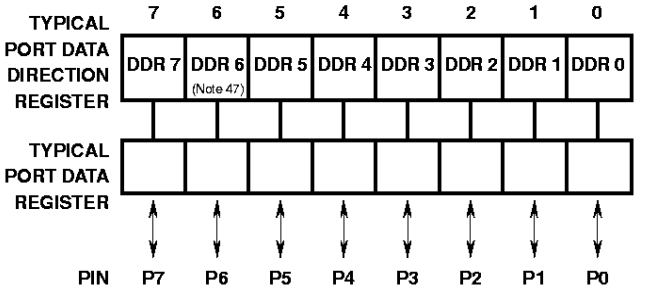


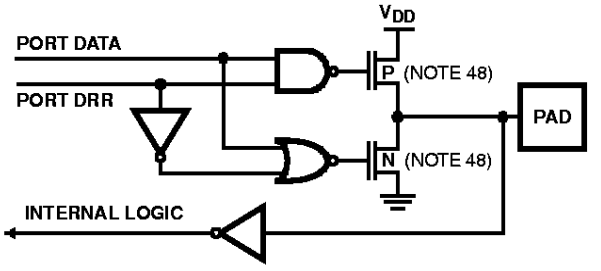
FIGURE 6A. TYPICAL PARALLEL PORT I/O CIRCUITRY



NOTE:

47. DDR6 not available on port D.

FIGURE 6B. TYPICAL PARALLEL PORT I/O CIRCUITRY



NOTES:

48. Denotes devices are enhancement type.
49. Input Protection and Latch-up protection not shown.

FIGURE 6C. TYPICAL PARALLEL PORT I/O CIRCUITRY

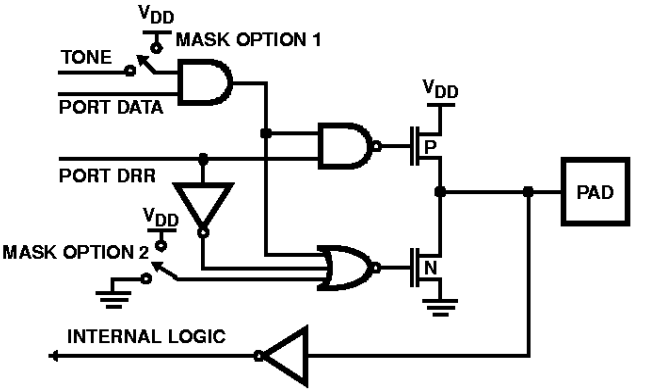


FIGURE 6D. PORT A7 - A4 TONE OUTPUT MASK OPTION

Port B Interrupts and Pullups

In addition to being a standard bidirectional port, each bit of Port B has a mask option to connect a pullup device to the I/O pad and to simultaneously feed the input to the internal interrupt logic. When the mask option is not selected, each Port B pin behaves as a standard bidirectional port pin.

When the mask option is selected, a pullup PMOS device with an impedance of approximately 20kΩ is connected between the pad and V_{DD} (see Pullup Current, I_{IN}, in the DC Electrical Specifications tables for more details) and the input signal is inverted and internally ORed with the $\overline{IRQ}$ signal (refer to Figure 6E).

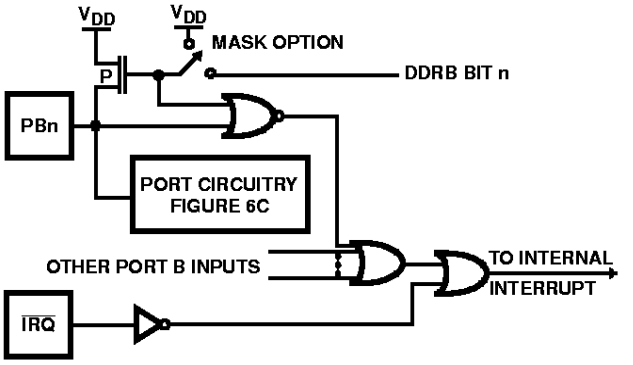


FIGURE 6E. PORT B INTERRUPT AND PULLUP MASK OPTION

The interrupt behavior of any port B pin which has the pullup/interrupt mask option activated is identical to the results one would achieve by externally ORing (active low) the signal with the $\overline{IRQ}$ signal.

NOTE: The BIH and BIL instructions apply to the output of the logic OR of the Port B $\overline{IRQ}$, $\overline{IRQ}$ pin and Wake Up Timer $\overline{IRQ}$ signals and can not be used to test the IRQ pin exclusively.

If the IRQ bit in the OPTION register is clear (the external interrupt will sense only edges, see ***Software Programmable Options*****, External Interrupts** and Figure 15 for details) when any one of the interrupt sources (port B inputs or $\overline{IRQ}$) goes low an interrupt will be generated. A second interrupt will not be generated until all of the interrupt lines go high and one or more again goes low.

If the IRQ bit in the OPTION register is set (the external interrupt will sense both level and edges, see ***Software Programmable Options*, External Interrupts** and Figure 15 for details) when any one of the interrupt sources (port B inputs or $\overline{IRQ}$) goes low an interrupt will be generated. Interrupts will continue to be generated until all of the interrupt lines go high.

The pullup device and the interrupt function are disabled when the associated DDRB bit is set high. When its DDRB bit is a 1, each port B pin acts as a normal output regardless of whether or not the pullup/interrupt mask option has been selected. Thus the DDRB bit can be used as an interrupt enable for the interruptible port B pins. Care should be taken when re-enabling a port B interrupt to avoid false interrupts. False interrupts can be avoided by first driving the PORTB bit high before clearing the DDRB bit. Further note, that all DDRB bits are cleared by reset, thus enabling port B interrupts (no interrupt will be recognized until execution of the first CLI instruction following reset).

Bidirectional I/O Port C

Port C is an 8-bit general purpose bidirectional input/output ports located at $0002. The data direction register for port C is located at $0006. The contents of the port C data register are indeterminate at initial power up and must be initialized by user software. Reset does not affect the data register itself, but does however clear the data direction register (DDRC), setting the port to input. Bit 7 of port C (PC7) is a high current sink and source output. Refer to the DC Electrical Specifications table for details.

Bidirectional I/O Port D

Port D is a 7-bit bidirectional port located at $0003 with a data direction register (DDRD) located at $0007. Four of it's pins are with the SPI subsystem and two more are shared with the SCI subsystem. Refer to ***Serial Communications Interface*** and ***Serial Peripheral Interface*** for more detailed information. When these systems are disabled the port D lines serve as general purpose bidirectional port lines. During power-on reset or external reset both the SPI and SCI modules are disabled and all of the bits in DDRD are cleared, setting port D as an input port. When reading Port D, bit 6 returns the state of the TCMP pin. This bit is read only and can not be used to set the TCMP high or low. There is no DDR associated with bit 6. Bits being used for the serial ports should not be used as general I/O as they do not return valid data.

NOTE: It is recommended that all unused inputs, except OSC2, and I/O ports (configured as outputs) be tied to an appropriate logic level (e.g. either V_{DD} or V_{SS}).

Software Programmable Options

The CDP68HC05C16B has several software programmable options that are controlled by the Option register (OR), located at memory address $3FDF. The Option register contains control bits for the following options:

- Memory mapping of shared RAM/ROM areas from $20 to $4F and from $100 to $17F
- Edge triggered only or edge and level-triggered external interrupt ($\overline{IRQ}$ or any port B pin configured as an interrupt)

This register must be configured by the user software and all bits except for the IRQ bit can be read or written any time the CPU is operational.

7	6	5	4	3	2	1	0	
RAM0	RAM1	0	0	0	0	IRQ	0	$3FDF

B7, RAM0 RAM0 is the Random Access Memory Control Bit 0. This bit is used to control which memory type (RAM/user ROM) is mapped between $20 and $4F. If RAM0=0, then the ROM is selected. If RAM0=1 then the RAM is selected.

B6, RAM1 RAM1 is the Random Access Memory Control Bit 1. This bit is used to control which memory type (RAM/user ROM) is mapped between $100 and $17F. If RAM1=0, then the ROM is selected. If RAM1=1 then the RAM is selected.

B5-B2, B0 Not implemented, always read as 0.

B1, IRQ The IRQ edge level bit is used to select what type of signal will trigger an external interrupt. If this bit is set (1) then the edge and level interrupt option is selected. If this bit is clear (0), the edge only option is selected. This bit is set by reset but can be cleared by software. This bit can only be written once.