Advance Information

This document contains information on a product under development. The parametric and functional information are target parameters and are subject to change without notice.

Bt494

160 MHz
Monolithic CMOS
RAMDAC™

Distinguishing Features

- 160 MHz, 110 MHz Operation
- 1:1, 2:1, or 4:1 Multiplexed Pixel Ports
- Pseudo Color or True Color Support
- Double-Buffered Pseudo Color Support
- Three 256 x 8 Color Palette RAMs
- Programmable Setup (0 or 7.5 IRE)
- 2 Overlay Planes
- 2 Cursor Planes
- Input and Output Signature Registers
- JTAG Support
- 169-pin PGA Package

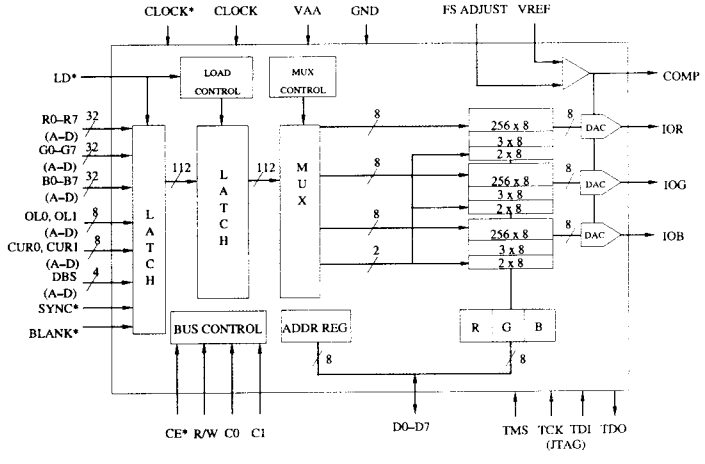
Applications

- High-Resolution Color Graphics
- Medical Imaging
- Visualization
- CAE/CAD/CAM
- Image Processing
- Video Reconstruction

Related Products

- Bt431, Bt438, Bt463

Functional Block Diagram



Product Description

The Bt494 is a high-performance RAMDAC designed for high-resolution, true-color graphics. It has three 256 x 8 lookup tables with triple 8-bit D/A converters to support 24-bit true color for monitors with up to 1600 x 1280 resolution. The Bt494 also supports single- or double-buffered 8-bit pseudo color. The Bt494 contains two overlay planes and a dedicated two-plane cursor port.

On-chip features include programmable 1:1, 2:1, or 4:1 input multiplexing of the pixels, bit plane masking, and a programmable setup (0 or 7.5 IRE).

The Bt494 supports double-buffered pseudo color by using the DBS input pin to switch on a pixel- by-pixel basis from the red port to the green port.

The Bt494 has significant testability features, including input and output signature analysis registers, and fully supports the Joint Test Action Group (JTAG) specification.

The Bt494 is pin and software compatible to the Bt463 and is offered in a pin grid array package.

5

Brooktree Corporation • 9950 Barnes Canyon Rd. • San Diego, CA 92121
(619) 452-7580 • (800) VIDEO IC • TLX: 383 596 • FAX: (619) 452-1249
L494001 Rev. A

Brooktree®

5-419

Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt494 supports a standard MPU bus interface, allowing the MPU direct access to the internal control registers and color palettes. The dual-port color palette RAMs allow color updating without contention with the display refresh process.

The C0 and C1 control inputs, in conjunction with the internal address register, specify which control register or color palette location will be accessed by the MPU (Table 1). The 12-bit address register eliminates the requirement for external address multiplexers. ADDR0 is the least significant bit. ADDR0 and ADDR8 correspond to data bus bit D0. ADDR12–ADDR15 are ignored during MPU write cycles and return logical zeroes when read by the MPU.

The control registers are also accessed through the address register in conjunction with the C0 and C1 inputs, as shown in Table 1. All control registers may be written to or read by the MPU at any time. When the control registers and the color palette RAM are accessed, the address register increments following a read or write cycle.

Writing/Reading Color Palette RAM

To write color data, the MPU loads the address register with the address of the color palette, overlay palette, or cursor color register to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using C0 and C1 to select the color palette RAM or cursor color register. After the blue write cycle, the address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data.

To read the color palette RAM or cursor color register, the MPU loads the address register with the address of the color palette RAM location or cursor color register to be read. Reading color data is similar to writing it, except the MPU executes read cycles.

When accessing the cursor color registers, the address register increments to $0102 following a blue read or write cycle. The color palette RAM does not have a wraparound feature after the last valid address. However, any attempt to write past $020F does not affect previous data load cycles. The address register will reset to $0000 after incrementing past $0FFF.

ADDR0–16	C1, C0	Addressed by MPU
$xxxx	00	address register (ADDR0–7)
$xxxx	01	address register (ADDR8–11)
$0100	10	cursor color 0 (Note 1)
$0101	10	cursor color 1 (Note 1)
$0200	10	ID register ($2C)
$0201	10	command register_0
$0203	10	command register_2
$0205	10	R0–R7 read mask register
$0206	10	G0–G7 read mask register
$0207	10	B0–B7 read mask register
$0208	10	CUR and OL read mask register
$0209	10	R0–R7 blink mask register
$020A	10	G0–G7 blink mask register
$020B	10	B0–B7 blink mask register
$020C	10	CUR and OL blink mask register
$020D	10	test register
$020E	10	input signature register (Note 2)
$020F	10	output signature register (Note 1)
$0220	10	revision register ($A)
$0000–$00FF	11	color palette RAM (Note 1)
$0201	11	overlay color 1 (Note 1)
$0202	11	overlay color 2 (Note 1)
$0203	11	overlay color 3 (Note 1)

Note 1: Requires three read/write cycles.
Note 2: Two out of three valid read/write cycles.

Table 1. Address Register (ADDR) Operation.

Circuit Description (continued)

Additional Information

When accessing the color palette RAM, overlay palette RAM, signature analysis registers, or cursor color registers, the address register increments after every third read/write cycle for each addressable location. To keep track of the red, green, and blue read/write cycles, the address register has 2 additional bits (ADDRa and ADDRb) that count modulo three. They are reset to zero when the MPU reads or writes to the address register. The MPU does not have access to these bits. The other 12 bits of the address register (ADDR0–11) are accessible to the MPU.

If an invalid address is loaded into the address register, data written to the device will be ignored and invalid data will be read by the MPU.

For 8-bit registers, the address increments after every read/write cycle.

Figure 1 illustrates the MPU read/write timing of the Bt494.

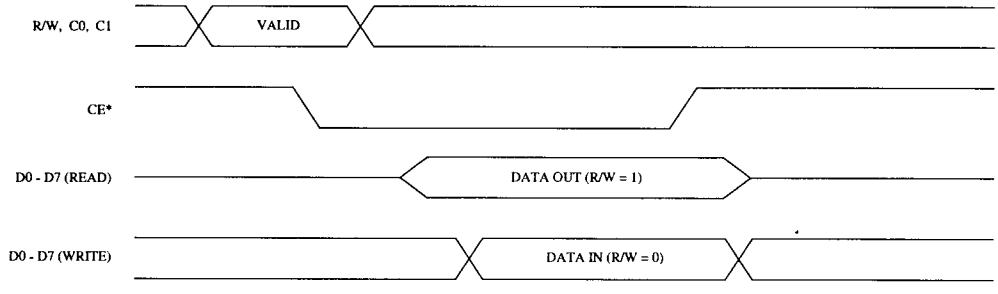


Figure 1. MPU Read/Write Timing.

Circuit Description (continued)

Frame Buffer Interface

To enable transfer of pixel data from the frame buffer at TTL data rates, the Bt494 incorporates internal latches and multiplexers. As illustrated in Figure 2, on the rising edge of LD*, sync and blank information, color, and overlay information for either 1, 2, or 4 consecutive pixels are latched into the device. With this configuration, the sync and blank timing will be recognized only with 1-, 2-, or 4-pixel resolution. Typically, the LD* signal is used to clock external circuitry, generating the basic video timing, and to clock the video DRAMs.

For 1:1, 2:1, or 4:1 input multiplexing, the Bt494 outputs color information each clock cycle based on the {A} inputs, followed by the {B} inputs, then the {C} inputs, etc., until 1, 2, or 4 pixels have been output, at which point the cycle repeats.

To simplify the frame buffer interface timing, LD* may be phase shifted in any amount relative to CLOCK. This enables computation of the LD* signal by externally dividing CLOCK by 2 or 4, independent of the propagation delays of the LD* generation logic. As a result, the pixel, overlay, and cursor data are latched on the rising edge of LD*, independent of the clock phase.

Internal logic maintains an internal LOAD signal synchronous to CLOCK and is guaranteed to follow the LD* signal by at least one, but not more than three (in 4:1 mode), clock cycles. This LOAD signal transfers the latched pixel, overlay, and cursor data into a second set of latches, which are then internally multiplexed at the pixel clock rate.

If 1:1 multiplexing is specified, the CLOCK and CLOCK* signals are ignored and pixel data is latched on the rising edge of LD*. If 2:1 multiplexing is specified, only one rising edge of LD* should occur every two clock cycles. If 4:1 multiplexing is specified, only one rising edge of LD* should occur every four clock cycles. Otherwise, the internal LOAD generation circuitry assumes it is not locked onto the LD* signal and will continuously attempt to resynchronize itself to LD*.

Color Palette RAM

The color lookup table consists of three independent 256-entry RAMs.

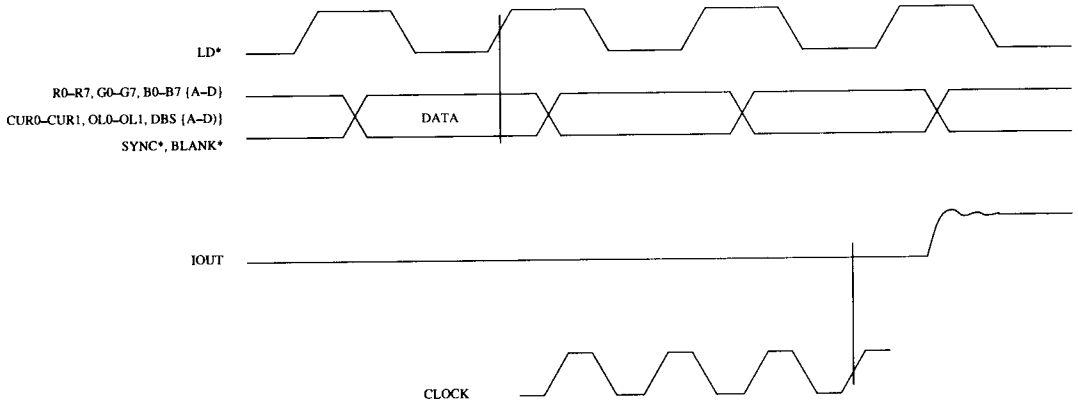


Figure 2. Video Input/Output Timing.

Circuit Description (continued)

Video Generation

Every clock cycle, up to 24 bits of color information are presented to the three 8-bit D/A converters.

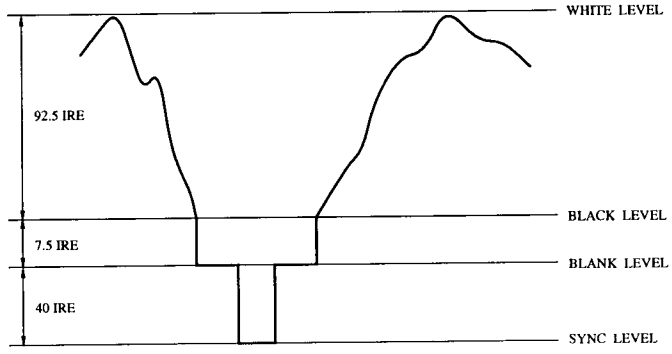
The SYNC* and BLANK* inputs are pipelined to maintain synchronization with the pixel data. They add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 3 and 4. Command register_2 specifies whether a 0 IRE or 7.5 IRE blanking pedestal is to be generated and whether sync information is to be encoded on the video output. A 0 IRE pedestal will force the black level and the blank level to be the same.

The varying output current from the D/A converters produces a corresponding voltage level, which is used to drive the CRT monitor. Tables 2 and 3 detail how the SYNC* and BLANK* inputs modify the output levels.

The D/A converters on the Bt494 use a segmented architecture in which bit currents are routed to either the current output or GND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

Circuit Description (continued)

SYNC DISABLED		SYNC ENABLED	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75 Ω doubly-terminated load, RSET = 523 Ω, and VREF = 1.235 V. Blank pedestal = 7.5 IRE. RS-343A levels and tolerances are assumed on all levels.

Figure 3. Composite Video Output Waveform (SETUP = 7.5 IRE).

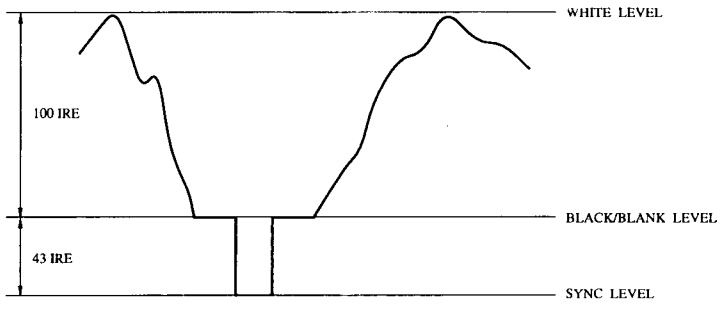
Description	Sync Iout (mA)	No Sync Iout (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	$FF
DATA	data + 9.05	data + 1.44	1	1	data
DATA–SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	9.05	1.44	1	1	$00
BLACK–SYNC	1.44	1.44	0	1	$00
BLANK	7.62	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with RSET = 523 Ω and VREF = 1.235 V. Blank pedestal = 7.5 IRE.

Table 2. Video Output Truth Table (SETUP = 7.5 IRE).

Circuit Description (continued)

SYNC DISABLED		SYNC ENABLED	
MA	V	MA	V
18.60	0.698	26.67	1.000
0.00	0.000	8.05	0.302
		0.00	0.000



Note: 75 Ω doubly-terminated load, RSET = 495 Ω and VREF = 1.235 V. Blank pedestal = 0 IRE. RS-343A levels and tolerances are assumed on all levels.

Figure 4. Composite Video Output Waveform (SETUP = 0 IRE).

Description	Sync Iout (mA)	No Sync Iout (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	18.60	1	1	$FF
DATA	data + 8.05	data	1	1	data
DATA–SYNC	data	data	0	1	data
BLACK	8.05	0	1	1	$00
BLACK–SYNC	0	0	0	1	$00
BLANK	8.05	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with RSET = 495 Ω and VREF = 1.235 V. Blank pedestal = 0 IRE.

Table 3. Video Output Truth Table (SETUP = 0 IRE).

Circuit Description (continued)

Hardware Cursor Interface

Pins CUR0 and CUR1 (A–D) can be used to interface the Bt494 with one or two Bt431 hardware cursor chips. Table 4 contains more details.

CUR1	CUR0	CURSOR COLOR
0	0	RAM Palette or Overlays
0	1	0
1	0	1
1	1	1

Table 4. Cursor Interface Operation.

Overlay Operation

Pins OL0 and OL1 (A–D) provide two-plane normal overlay inputs. Three overlay colors are available. These must be in CLUT RAM address locations: $0201, $0202, and $0203. Refer to Table 5.

OL0	OL1	Overlay Color	RAM Address Location
0	0	—	—
0	1	1	$0201
1	0	2	$0202
1	1	3	$0203

Table 5. Overlay Interface Operation.

Boundary-Scan Testability Structures

As the complexity of RAMDACs increases, the need to easily access the RAMDAC for functional verification is becoming vital. The Bt494 has incorporated special circuitry that allows it to be accessed in full compliance with standards set by the JTAG. Conforming to the IEEE P1149.1 *Standard Test Access Port and Boundary Scan Architecture*, the Bt494 has dedicated pins that are used for testability purposes only.

JTAG's approach to testability uses boundary-scan cells placed at each digital pin, both inputs and outputs. All scan cells are interconnected into a Boundary-Scan Register (BSR), which applies or captures test data used for functional verification of the RAMDAC. The JTAG approach is particularly useful for board testers that use functional testing methods.

JTAG consists of four dedicated pins comprising the Test Access Port (TAP). These pins are TMS (Test Mode Select), TCK (Test Clock), TDI (Test Data Input), and TDO (Test Data Out). These four TAP pins can completely verify the RAMDAC. With boundary-scan cells at each digital pin, the Bt494 can apply and capture the logic level. Since all of the digital pins are interconnected as a long shift register, the TAP logic has access to and control of all the necessary pins to verify functionality. The TAP controller can shift in any number of test vectors through the TDI input and apply them to the internal circuitry.

The output result is scanned out on the TDO pin and externally checked. The Timing Waveform section contains timing information. While isolating the Bt494 from the other components on the board, the user has easy access to all Bt494 digital pins through the TAP and can perform complete functionality tests without expensive testers.

The bidirectional MPU port is given special attention with respect to JTAG. Because JTAG requires control over each digital pin, an additional Output Enable (OE) function is included in the BSR for the MPU pins. In conjunction with the JTAG instruction, the OE will configure the MPU port as an input or output.

With the JTAG bus, users also have access to a vital portion of the Bt494, the Output Signature Analysis Register (OSAR). See Figure 5. With access to this register, users can easily verify expected video data serially through the JTAG port. The OSAR is located between the lookup table and the inputs to the DACs.

The Power-On Reset (POR) circuitry ensures that the Bt494 initializes each pin to operate in a RAM-DAC mode instead of a JTAG test mode during power-up sequence.

A variety of verification procedures can be performed through the TAP controller. Through a set of eight instructions, the Bt494 can verify board connectivity at all digital pins, generate artificial pixel vectors on chip, check signatures on system pixel streams, and scan vectors in and out of the pixel shifter and signature analysis register. The instructions are accessible through a simple state machine.

Note: Since the boundary scan (JTAG) circuitry is intended for gross functional verification, it is tested and guaranteed operational at VAA >= 5.0 volts and VIL on JTAG pins at 0.6 volts max. Maximum JTAG clock speed (TCK) is 50 MHz.

5

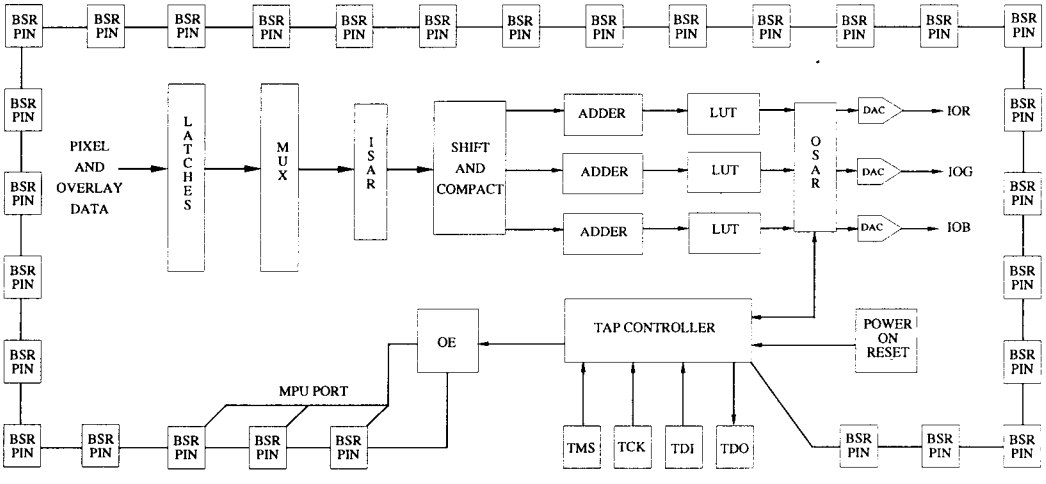


Figure 5. JTAG Block Diagram.

Command Register_0

This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power up. CR00 corresponds to data bus bit D0.

CR07, CR06 Multiplex select

(00) reserved
(01) 4:1 multiplexing
(10) 1:1 multiplexing
(11) 2:1 multiplexing

These bits specify whether 1:1, 2:1, or 4:1 multiplexing is to be used for the pixel and overlay inputs. If 2:1 is specified, the {C} and {D} pixel and overlay inputs are ignored and should be connected to GND, and the LD* input should be one half the CLOCK rate. If 4:1 is specified, all of the pixel and overlay inputs are used, and the LD* input should be one fourth the CLOCK rate. If 1:1 is specified, the {B}, {C}, and {D} inputs are ignored.

In the 1:1 multiplex mode, the maximum clock rate is 66 MHz. LD* is used for the pixel clock. Although CLOCK is ignored in the 1:1 mode, it must remain running.

The pipeline delay of the Bt494 can be reset to a fixed 13 clock cycles. In this instance, each time the input multiplexing is changed, the Bt494 must be reset again to a fixed pipeline delay.

CR05 Mode select

(0) True color
(1) Pseudo color

This bit specifies whether the chip is operating in true color or pseudo-color mode. When in PC mode, the DBS pin selects either R7–R0 pins (DBS = 0) or B7–B0 pins (DBS = 1) as the pseudo-color pixel port.

CR04 reserved (logical zero)

CR03, CR02 Blink rate selection

(00) 16 on, 48 off (25/75)
(01) 16 on, 16 off (50/50)
(10) 32 on, 32 off (50/50)
(11) 64 on, 64 off (50/50)

These two bits control the blink rate cycle time and duty cycle, and are specified as the number of vertical retrace intervals. The numbers in parentheses specify the duty cycle (percent on/off). The counters that determine the blink rate are reset when writing to command register_0. For the blink function to operate properly, SYNC* must toggle only once on horizontal retrace and two times or more on vertical retrace.

CR01, CR00 reserved (logical zero)

Internal Registers (continued)

Command Register_2

This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power up. CR20 corresponds to data bus bit D0.

CR27	Sync enable (0) disable sync (1) enable sync	This bit specifies whether sync information is to be output onto IOG (logical one) or not (logical zero).
CR26	Pedestal enable (0) 0 IRE pedestal (1) 7.5 IRE pedestal	This bit specifies whether a 0 or 7.5 IRE blanking pedestal is to be generated on the video outputs. A 0 IRE specifies that the black and blank levels are the same.
CR25–CR23	reserved (logical zero)	
CR22	Input SAR capture selection (0) lower 16 bits (1) upper 16 bits	This bit specifies whether the 16-bit input signature analysis register (SAR) should capture the lower or upper 16 bits of the pixel path. When CR22 is selected as a logical one, 3 of the upper 16 bits will be ground. The input SAR is guaranteed operational only for the 110 MHz speed grade on the current revision.
CR21	Analysis register clock control (0) every LD* cycle (1) every CLOCK cycle	This bit controls the rate of operation of all signature analysis register (SAR) clocking. Logical zero is the normal mode with pixel position (A, B, C, or D) determined by the test register. Logical one is a special mode for chip testing. (In this instance, SAR operation is not guaranteed for clock rates above 30 MHz.)
CR20	Test mode select (0) signature analysis test (1) data strobe test	This bit determines the method of high-speed test used. The SARs are used to hold the test result for both test methods.

Internal Registers (continued)

ID Register

This 8-bit register may be read by the MPU to determine the type of RAMDAC being used in the system. The value is different for each RAMDAC. For the Bt494, the value read by the MPU will be $2C. Data written to this register is ignored.

Pixel Read Mask Register

The 24-bit pixel read mask register is used to enable (logical one) or disable (logical zero) a bit plane from addressing the color palette RAM. Each register bit is logically ANDed with the corresponding bit plane input. This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power up. D0 corresponds to R0, B0, G0, and CUR0.

Pixel Blink Mask Register

The 24-bit pixel blink mask register is used to enable (logical one) or disable (logical zero) a bit plane from blinking at the blink rate and duty cycle specified by command register_0. This register may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power up. D0 corresponds to R0, B0, G0, and CUR0. For the blink function to operate properly, SYNC* must toggle no more than once on horizontal retrace and more than once on vertical retrace.

Revision Register

This 8-bit register is a read-only register, specifying the revision of the Bt494. The 4 most significant bits signify the revision letter in hexadecimal form. The 4 least significant bits do not represent any value and should be ignored.

Internal Registers (continued)

Red, Green, and Blue Output Signature Analysis Registers (OSAR)

Signature Operation

These three 8-bit signature analysis registers may be read by the MPU while BLANK* is a logical zero. While BLANK* is a logical one, the signatures are being acquired. The MPU may write to the OSARs while BLANK* is a logical zero to load the seed value. The OSARs use data loading into the output DACs to calculate the signatures. JTAG logic can access the OSAR independently of the MPU operation. MPU accesses to the OSARs require one address register load to address $020F, followed by three reads or writes to the red, green, and blue signature registers. D0 corresponds to R0, G0, and B0.

When a test display is loaded into the frame buffer, a given value for the red, green, and blue signature registers will be returned if all circuitry is working properly.

Data-Strobe Operation

If command bit CR20 selects "data strobe testing," the operation of the signature registers changes slightly. Rather than determining the signature, they capture red, green, and blue data being presented to the three DACs.

Each LD* cycle, the three signature registers capture the color values being presented to the DACs. As only one of the (A–D) pixels can be captured each LD* cycle, D0–D2 of the test register are used to specify which pixel (A–D) is to be captured.

Input Signature Analysis Registers (ISAR)

Signature Operation

This 16-bit signature analysis register may be read by the MPU while BLANK* is a logical zero. While BLANK* is a logical one, the signatures are being acquired. The MPU may write to the ISAR while BLANK* is a logical zero to load the seed value. The ISAR uses R0–R7, G0–G7, B0–B7, CUR0–CUR1, OL0–OL1, and DBS (selected by command bit CR22) to calculate the signatures. When CR22 is a logical one, the upper 16 bits are used. B0–B7, CUR0–CUR1, OL0–OL1, DBS, and the remaining 3 bits are ground (logical zero). The 16 bits of data latched in the ISAR may be masked (forced low) by the read mask registers. MPU accesses to the ISAR require one address register load to $020E, followed by three reads or writes to lower byte, upper byte, and dummy access. D0 corresponds to R0, B0, G0, and CUR0.

When a test display is loaded into the frame buffer, a given value for the ISAR will be returned if all circuitry is working properly.

Note: The input signature analysis register is operational at frequencies < 120 MHz only.

Data-Strobe Operation

If command bit CR20 selects "data strobe testing," the operation of the ISAR changes slightly. Rather than determining the signature, it just captures and holds the 16 bits of pixel data addressing the color palette RAM.

Each LD* cycle, the ISAR captures the 16 bits of pixel data addressing the color palette RAM. As only 1 of the (A–D) pixels can be captured each LD* cycle, D0–D2 of the test register are used to specify which pixel (A–D) is to be captured.

Internal Registers (continued)

Test Register

This 8-bit register is used for testing the Bt494. If 1:1 pixel multiplexing is specified, signature analysis is done on every pixel; if 2:1 pixel multiplexing is specified, signature analysis is done on every second pixel; if 4:1 pixel multiplexing is specified, signature analysis is done on every fourth pixel. D0–D2 are used for 2:1 and 4:1 multiplexing to specify whether to use the A, B, C, or D pixel inputs, as follows:

D2–D0	Selection
000	pixel A
001	pixel B
010	pixel C
011	pixel D
100	reserved
101	reserved
110	reserved
111	reserved

In 1:1 multiplexing mode, D0–D2 should select pixel A.

D3–D7 are used to compare the analog RGB outputs to each other and to a 145 mV reference. This enables the MPU to determine whether the CRT monitor is connected to the analog RGB outputs and whether the DACs are functional.

D7	D6	D5	D4	D3
red select	green select	blue select	145 mV ref. select	result

D7–D4		If D3 = 1	If D3 = 0
0000	normal operation	—	—
1010	red DAC compared to blue DAC	red > blue	blue > red
1001	red DAC compared to 145 mV reference	red > 145 mV	red < 145 mV
0110	green DAC compared to blue DAC	green > blue	blue > green
0101	green DAC compared to 145 mV reference	green > 145 mV	green < 145 mV

The table above lists the valid comparison combinations. A logical one enables comparison of that function; the result is D3. The output levels of the DACs should be constant for 5 µs to allow enough time for detection. The capture occurs over one LD* period set by a logical one at any of the pixel pins B0A, B0B, B0C, or B0D.

For normal operation, D4–D7 must be logical zeroes.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the analog output to the blanking level, as detailed in Tables 2 and 3. It is latched on the rising edge of LD*. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*	Composite sync control inputs (TTL compatible). A logical zero typically switches off a 40 IRE current source on the IOG output (see Figures 3 and 4). SYNC* does not override any other control or data input, as shown in Tables 2 and 3; therefore, it should be asserted only during the blanking interval. SYNC* is latched on the rising edge of LD*.
LD*	Load control input (TTL compatible). The R0–R7 {A–D}, G0–G7 {A–D}, OL0–OL1 {A–D}, CUR0–CUR1 {A–D}, BLANK*, and SYNC* inputs are latched on the rising edge of LD*. While LD* is the output clock (1:1 multiplex mode) or is one half or one fourth of CLOCK, it may be phase independent of the CLOCK and CLOCK* inputs. LD* may have any duty cycle within the limits specified in the AC Characteristics section.
R0-R7, G0-G7, B0-B7 {A–D}	Red, green, and blue pixel select inputs (TTL compatible). If nonzero data exists in the assigned overlay input port, then pixel data inputs are ignored. Either 1, 2, or 4 consecutive pixels (up to 24 bits per pixel) are input through this port. All 4 pixels (96 bits) are latched on the rising edge of LD*. Unused inputs should be connected to GND. Typically, the {A} pixel is output first, followed by the {B} pixel, then the {C} pixel, etc., until all 1, 2, or 4 pixels have been output, at which point the cycle repeats.
OL0, OL1 {A–D}	Overlay select inputs (TTL compatible). These inputs are latched on the rising edge of LD*. When they are nonzero, the overlay palette RAM is accessed and the R0–R7, G0–G7, and B0–B7 {A–D} inputs are ignored. Overlay information (up to 2 bits per pixel) for either 1, 2, or 4 consecutive pixels is input through this port. Unused inputs should be connected to GND. If nonzero data exists on CUR0 and CUR1, overlay input pixels will be ignored.
CUR0, CUR1 {A–D}	Cursor inputs (TTL compatible). If these inputs are nonzero, the color and overlay input pixels are ignored; one of two cursor colors is selected. Unused inputs should be connected to GND.
DBS{A–D}	Double buffer select (TTL compatible). If the Bt494 is in pseudo-color mode, a zero value causes the R7–R0 pins to act as the pixel input. If a one value, G7–G0 pins act as the pixel input. This pin allows double-buffered pseudo-color operation on a pixel-by-pixel basis.
IOR, IOG, IOB	Red, green, and blue current outputs. These high-impedance current sources can directly drive a doubly-terminated 75 Ω coaxial cable (see the PC Board Layout Considerations section). All outputs, whether used or not, should have the same output load.
TCK	Test Clock (TTL compatible). It is used to synchronize all JTAG test structures. Maximum clock rate for this pin is 50 MHz. When JTAG operations are not being performed, this pin is pulled low by internal circuitry.
TMS	Test Mode Select (TTL compatible). It is a JTAG input pin whose transitions drive the JTAG state machine through its sequences. When JTAG operations are not being performed, this pin is pulled high by internal circuitry.
TDI	Test Data Input (TTL compatible). It is a JTAG input pin used for loading instructions to the TAP controller or for loading test vector data for boundary scan operation. When JTAG operations are not being performed, this pin is pulled high by internal circuitry.
TDO	Test Data Output (TTL compatible). It is a JTAG output pin used to verify test results of all JTAG sampling operations. This output pin is active for certain JTAG sequences, and will be three-stated at all other times. When JTAG operations are not being performed, this pin should be left floating.
VAA	Analog power. All VAA pins must be connected together on the same PCB plane to prevent latchup. Refer to the PC Board Layout Considerations section for critical layout criteria.

Pin Descriptions (continued)

<table>
<tr><th>Pin Name</th><th>Description</th></tr>
<tr><td>GND</td><td>Analog ground. All GND pins must be connected together on the same PCB plane to prevent latchup. Refer to the PC Board Layout Considerations section for critical layout criteria.</td></tr>
<tr><td>COMP</td><td>Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between this pin and VAA (see Figure 6 in the PC Board Layout Considerations section). Connecting the capacitor to VAA rather than to GND provides the highest possible power supply noise rejection. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. Refer to the PC Board Layout Considerations section for critical layout criteria.</td></tr>
<tr><td>FS ADJUST</td><td>Full-scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal (see Figure 6). The IRE relationships in Figures 3 and 4 are maintained, regardless of the full-scale output current.

The relationship between RSET and the full-scale output current on IOG is:

RSET (Ω) = K1 * VREF (V) / IOG (mA)

The full-scale output current on IOR and IOB for a given RSET is:

IOR, IOB (mA) = K2 * VREF (V) / RSET (Ω)

where K1 and K2 are defined as:

<table>
<tr><th>Setup</th><th>IOG</th><th>IOR, IOB</th></tr>
<tr><td>7.5 IRE</td><td>K1 = 11,294</td><td>K2 = 8,067</td></tr>
<tr><td>0 IRE</td><td>K1 = 10,684</td><td>K2 = 7,457</td></tr>
</table>
</td></tr>
<tr><td>VREF</td><td>Voltage reference input. An external voltage reference circuit, such as the one shown in Figure 6, must supply this input with a 1.235 V (typical) reference. The use of a resistor network to generate the reference is not recommended, as any low-frequency power supply noise on VREF will be directly coupled onto the analog outputs. A 0.1 µF ceramic capacitor is used to decouple this input to VAA. If VAA is excessively noisy, better performance may be obtained by decoupling VREF to GND. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. Refer to the PC Board Layout Considerations section for critical layout criteria.</td></tr>
<tr><td>CLOCK,
CLOCK*</td><td>Clock inputs. These differential clock inputs are designed to be driven by ECL logic configured for single-supply (+5 V) operation. The clock rate is typically the pixel clock rate of the system. Refer to the PC Board Layout Considerations section for critical layout criteria.</td></tr>
<tr><td>CE*</td><td>Chip enable control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. During write operations, data is internally latched on the rising edge of CE*. Glitches must be avoided on this edge-triggered input.</td></tr>
<tr><td>R/W</td><td>Read/write control input (TTL compatible). To write data to the device, both CE* and R/W must be a logical zero. To read data from the device, CE* must be a logical zero and R/W must be a logical one. R/W is latched on the falling edge of CE*.</td></tr>
<tr><td>C0, C1</td><td>Command control inputs (TTL compatible). C0 and C1 specify the type of read or write operation being performed, as shown in Table 1. They are latched on the falling edge of CE*.</td></tr>
<tr><td>D0–D7</td><td>Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.</td></tr>
</table>

Pin Descriptions (continued)—169-pin PGA Package

Signal	Pin Number
BLANK*	J1
SYNC*	H1
LD*	H3
CLOCK*	J3
CLOCK	J2
R0A	F2
R0B	G3
R0C	F1
R0D	G1
R1A	F3
R1B	D1
R1C	E2
R1D	E1
R2A	C2
R2B	B1
R2C	D2
R2D	C1
R3A	C3
R3B	D3
R3C	E3
R3D	B2
R4A	A1
R4B	B3
R4C	C4
R4D	D4
R5A	A3
R5B	C5
R5C	A2
R5D	B4
R6A	A5
R6B	B6
R6C	A4
R6D	B5
R7A	A7
R7B	C7
R7C	A6
R7D	C6
G0A	A9
G0B	B8
G0C	A8
G0D	B7

Signal	Pin Number
G1A	A10
G1B	B10
G1C	B9
G1D	C10
G2A	A12
G2B	C11
G2C	A11
G2D	B11
G3A	A14
G3B	B12
G3C	A13
G3D	C12
G4A	A16
G4B	C13
G4C	A15
G4D	B13
G5A	C14
G5B	B15
G5C	A17
G5D	B14
G6A	D15
G6B	B16
G6C	E15
G6D	C15
G7A	D16
G7B	C17
G7C	C16
G7D	B17
B0A	T16
B0B	T17
B0C	R16
B0D	R17
B1A	R15
B1B	R14
B1C	P15
B1D	U17
B2A	T14
B2B	U15
B2C	T15
B2D	U16

Signal	Pin Number
B3A	T13
B3B	U13
B3C	R13
B3D	U14
B4A	R12
B4B	U11
B4C	T12
B4D	U12
B5A	T11
B5B	U9
B5C	R11
B5D	U10
B6A	R10
B6B	U8
B6C	T10
B6D	T9
B7A	T7
B7B	U6
B7C	T8
B7D	U7
CUR0A	R6
CUR0B	U4
CUR0C	R7
CUR0D	U5
CUR1A	T5
CUR1B	U2
CUR1C	T6
CUR1D	U3
OL0A	T4
OL0B	R4
OL0C	R5
OL0D	U1
OL1A	R3
OL1B	N3
OL1C	T3
OL1D	T1
TMS	D17
TCK	E16
TDI	E17
TDO	F17

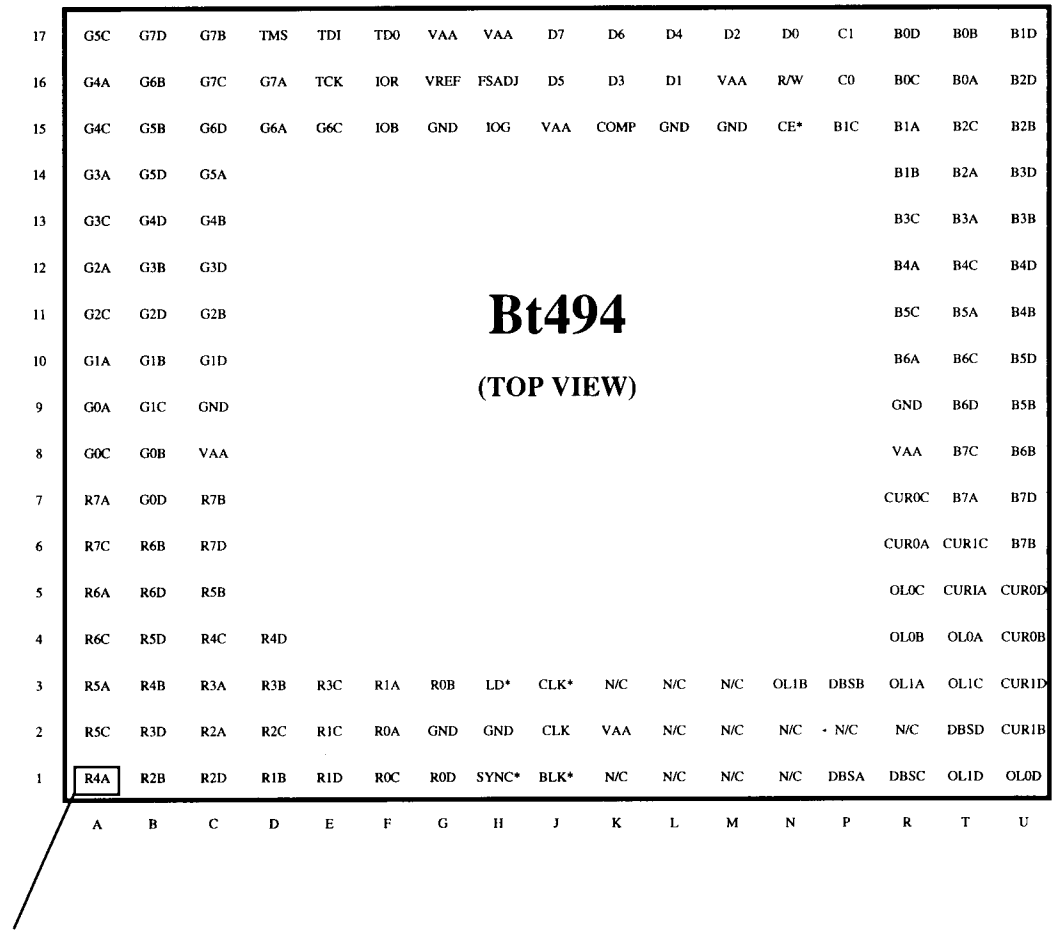
Pin Descriptions (continued)—169-pin PGA Package

Signal	Pin Number
DBSA	P1
DBSB	P3
DBSC	R1
DBSD	T2
D0	N17
D1	L16
D2	M17
D3	K16
D4	L17
D5	J16
D6	K17
D7	J17

Signal	Pin Number
IOR	F16
IOG	H15
IOB	F15
COMP	K15
FS ADJUST	H16
VREF	G16
CE*	N15
R/W	N16
C1	P17
C0	P16

Signal	Pin Number
VAA	C8
VAA	G17
VAA	H17
VAA	J15
VAA	K2
VAA	R8
VAA	M16
GND	C9
GND	G2
GND	G15
GND	H2
GND	L15
GND	M15
GND	R9
N/C	M1
N/C	P2
N/C	N1
N/C	R2
N/C	L1
N/C	N2
N/C	L3
N/C	M3
N/C	K1
N/C	L2
N/C	K3
N/C	M2

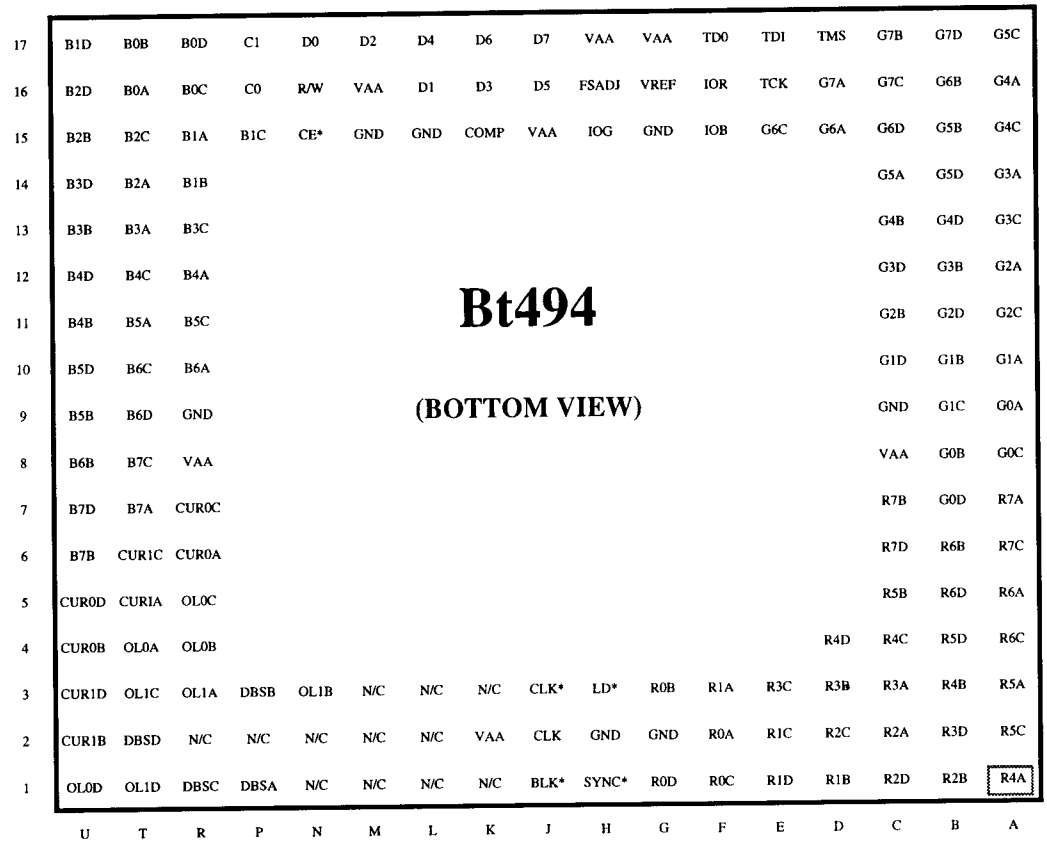
Pin Descriptions (continued)—169-pin PGA Package



	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U
17	G5C	G7D	G7B	TMS	TDI	TD0	VAA	VAA	D7	D6	D4	D2	D0	C1	B0D	B0B	B1D
16	G4A	G6B	G7C	G7A	TCK	IOR	VREF	FSADJ	D5	D3	D1	VAA	R/W	C0	B0C	B0A	B2D
15	G4C	G5B	G6D	G6A	G6C	IOB	GND	IOG	VAA	COMP	GND	GND	CE*	B1C	B1A	B2C	B2B
14	G3A	G5D	G5A												B1B	B2A	B3D
13	G3C	G4D	G4B												B3C	B3A	B3B
12	G2A	G3B	G3D												B4A	B4C	B4D
11	G2C	G2D	G2B												B5C	B5A	B4B
10	G1A	G1B	G1D												B6A	B6C	B5D
9	G0A	G1C	GND												GND	B6D	B5B
8	G0C	G0B	VAA												VAA	B7C	B6B
7	R7A	G0D	R7B												CUR0C	B7A	B7D
6	R7C	R6B	R7D												CUR0A	CUR1C	B7B
5	R6A	R6D	R5B												OL0C	CURIA	CUR0D
4	R6C	R5D	R4C	R4D											OL0B	OL0A	CUR0B
3	R5A	R4B	R3A	R3B	R3C	R1A	R0B	LD*	CLK*	N/C	N/C	N/C	OL1B	DBSB	OL1A	OL1C	CUR1D
2	R5C	R3D	R2A	R2C	R1C	R0A	GND	GND	CLK	VAA	N/C	N/C	N/C	N/C	N/C	DBSD	CUR1B
1	R4A	R2B	R2D	R1B	R1D	R0C	R0D	SYNC*	BLK*	N/C	N/C	N/C	N/C	DBSA	DBSC	OL1D	OL0D

5

Pin Descriptions (continued)—169-pin PGA Package



	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A
17	B1D	B0B	B0D	C1	D0	D2	D4	D6	D7	VAA	VAA	TD0	TDI	TMS	G7B	G7D	G5C
16	B2D	B0A	B0C	C0	R/W	VAA	D1	D3	D5	FSADJ	VREF	IOR	TCK	G7A	G7C	G6B	G4A
15	B2B	B2C	B1A	B1C	CE*	GND	GND	COMP	VAA	IOG	GND	IOB	G6C	G6A	G6D	G5B	G4C
14	B3D	B2A	B1B												G5A	G5D	G3A
13	B3B	B3A	B3C												G4B	G4D	G3C
12	B4D	B4C	B4A												G3D	G3B	G2A
11	B4B	B5A	B5C												G2B	G2D	G2C
10	B5D	B6C	B6A												G1D	G1B	G1A
9	B5B	B6D	GND												GND	G1C	G0A
8	B6B	B7C	VAA												VAA	G0B	G0C
7	B7D	B7A	CUR0C												R7B	G0D	R7A
6	B7B	CUR1C	CUR0A												R7D	R6B	R7C
5	CUR0D	CUR1A	OL0C												R5B	R6D	R6A
4	CUR0B	OL0A	OL0B											R4D	R4C	R5D	R6C
3	CUR1D	OL1C	OL1A	DBSB	OL1B	N/C	N/C	N/C	CLK*	LD*	R0B	R1A	R3C	R3B	R3A	R4B	R5A
2	CUR1B	DBSD	N/C	N/C	N/C	N/C	N/C	VAA	CLK	GND	GND	R0A	R1C	R2C	R2A	R3D	R5C
1	OL0D	OL1D	DBSC	DBSA	N/C	N/C	N/C	N/C	BLK*	SYNC*	R0D	R0C	R1D	R1B	R2D	R2B	R4A

PC Board Layout Considerations

PC Board Considerations

For optimum performance of the Bt494, proper CMOS RAMDAC layout techniques should be studied in the Bt451/7/8 Evaluation Module Operation and Measurements, Application Note (AN-16). This application note can be found in Brooktree's *Applications Handbook*.

The layout should be optimized for lowest noise on the Bt494 power and ground planes by providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of six layers is recommended. The ground layer should be used as a shield to isolate noise from the analog traces with layer 1 (top) for the analog traces, layer 2 for the ground plane, layer 3 for the analog power plane, and the remaining layers used for digital traces and digital power supplies.

Component Placement

Components should be placed as close as possible to the associated RAMDAC pin. Whenever possiple, components should be placed so traces can be connected point to point.

The optimum layout enables the Bt494 to be located as close as possible to the power supply connector and the video output connector.

Ground Planes

For optimum performance, a common digital and analog ground plane is recommended.

Power Planes

Separate digital and analog power planes are recommended. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt494 power pins, VREF circuitry, and COMP and VREF decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 6. This bead should be located within 3 inches of the Bt494. The bead provides resistance to switching currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device, and the shortest possible leads (consistent with reliable operation) should be used to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

The best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor in parallel with a 0.01 µF chip capacitor, decoupling each of the four groups of VAA pins to GND. The capacitors should be placed as close as possible to the device VAA and GND pins and connected with short, wide traces.

The 10 µF capacitor shown in Figure 6 is for low-frequency power supply ripple; the 0.1 µF and 0.01-µF capacitors are for high-frequency power supply noise rejection.

When a linear regulator is used, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than or equal to 200 mV. This is especially important when a switching power supply is used, and the switching frequency is close to the raster scan frequency. About 10 percent of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically with a 0.1 µF ceramic capacitor. Low-frequency supply noise will require a larger value. The COMP capacitor must be as close as possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance. Lead inductance degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

If the display has a ghosting problem, additional capacitance in parallel with the COMP capacitor may help.

PC Board Layout Considerations (continued)

VREF Decoupling

A 0.1 µF ceramic capacitor should be used to decouple this input to VAA. If VAA is excessively noisy, better performance may be obtained by decoupling VREF to GND. Providing alternate PCB pads (one to VAA and one to GND) is recommended for the VREF decoupling capacitor.

Digital Signal Interconnect

The digital inputs to the Bt494 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and output signals.

Most noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should not be faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower-speed applications will benefit from using lower-speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one fourth the signal edge time (refer to Brooktree Application Notes AN-11 and AN-12). Line termination or line-length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without use of termination. Ringing may be reduced by damping the line with a series resistor (30–300 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing the digital signals at a 90 degree angle to any analog signals.

The clock driver and all other digital devices must be adequately decoupled to prevent noise generated by the digital devices from coupling into the analog circuitry.

Analog Signal Interconnect

The Bt494 should be located as close as possible to the output connectors to minimize noise pickup and reflections caused by impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

To maximize the high-frequency power supply rejection, the video output signals should not overlay the analog power plane.

For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same. The load resistor connection between the video outputs and GND should be as close as possible to the Bt494 to minimize reflections. Unused analog outputs should be connected to GND.

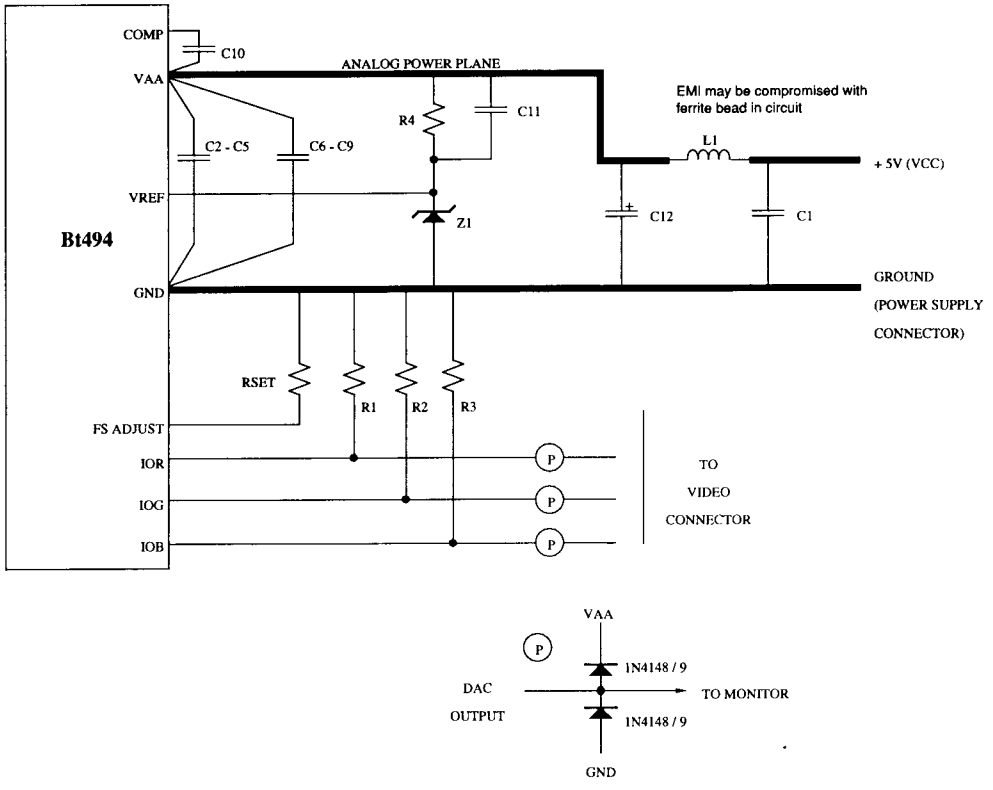
Analog output video edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise. The filter impedance must match the line impedance.

Analog Output Protection

The Bt494 analog output should be protected against high-energy discharges, such as those from monitor arc-over or from hot-switching AC-coupled monitors.

The diode protection circuit shown in Figure 6 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations (continued)



Note: Each pair of device VAA and GND pins must be separately decoupled with 0.1 µF and 0.01 µF capacitors.

Location	Description	Vendor Part Number
C1–C5, C10, C11	0.1 µF ceramic capacitor	Erie RPE110Z5U104M50V
C6–C9	0.01 µF ceramic chip capacitor	AVX 12102T103QA1018
C12	10 µF tantalum capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111 (Note 1)
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	1000 Ω 1% metal film resistor	Dale CMF-55C
RSET	523 Ω 1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385Z-1.2

The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt494.

Note 1: Or equivalent only.

Figure 6. Typical Connection Diagram and Parts List.

Application Information

Clock Interfacing

Because of the high clock rates at which the Bt494 may operate, it is designed to accept differential clock signals (CLOCK and CLOCK*). These clock inputs are generated by ECL logic operating at +5 V. The CLOCK and CLOCK* inputs require termination resistors (220 Ω to GND) that should be located as close as possible to the clock driver. A 150 Ω chip resistor connected between the RAMDAC's CLOCK and CLOCK* pins is also required to ensure proper termination. It should be located as close as possible to the RAMDAC. (See Figure 7.)

The CLOCK and CLOCK* inputs must be differential signals and greater than 0.6 V peak-to-peak due to the noise margins of the CMOS process. The Bt494 will not function using a single-ended clock with CLOCK* connected to ground.

Typically, LD* is generated by dividing CLOCK by two or four (depending on whether 2:1 or 4:1 multiplexing was specified) and translating it to TTL levels. As LD* may be phase-shifted relative to CLOCK, the designer need not worry about propagation delays in deriving the LD* signal only if fixed pipeline is not required. LD* may be used as the shift clock for the video DRAMs and to generate the fundamental video timing of the system (SYNC*, BLANK*, etc.).

For display applications where a single Bt494 is being used, it is recommended that the Bt438 or Bt440 Clock Generator Chip be used to generate the clock and load signals. It supports 4:1 input multiplexing of the Bt494 and will also optionally set the pipeline delay of the Bt494 to 9 clock cycles. The Bt438 may also be used to interface the Bt494 to a TTL clock. Figure 7 illustrates use of the Bt438 with the Bt494.

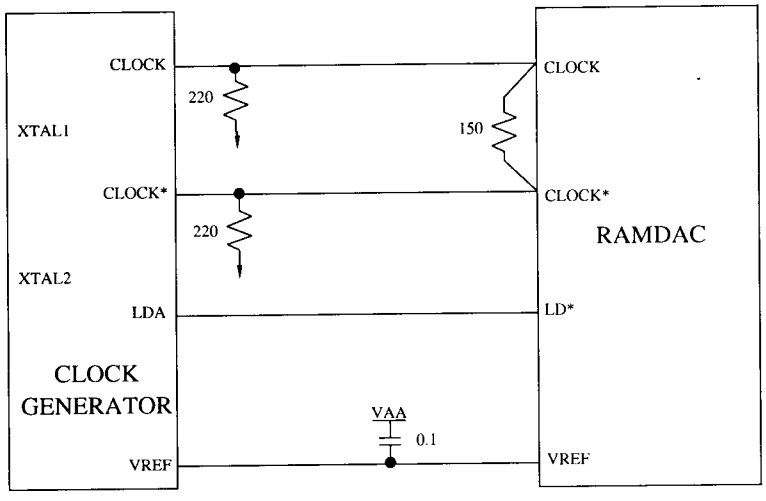


Figure 7. Generating the Bt494 Clock Signals.

Application Information (continued)

Setting the Pipeline Delay

The pipeline delay of the Bt494, although fixed after a power-up condition, may be anywhere from 7–11 clock cycles. The Bt494 contains additional circuitry enabling the pipeline delay to be fixed at 9 clock cycles. The Bt438 Clock Generator Chip supports this mode of operation when used with the Bt494.

To reset the Bt494, it should be powered-up with LD*, CLOCK, and CLOCK* running. Stop the CLOCK and CLOCK* signals with CLOCK high and CLOCK* low for *at least* three rising edges of LD*. There is no upper limit on how long the device can be held with CLOCK and CLOCK* stopped.

Restart CLOCK and CLOCK* so that the first edge of the signals is as close as possible to the rising edge of LD* (the falling edge of CLOCK leads the rising edge of LD* by no more than 1 clock cycle or follows the rising edge of LD* by no more than 1.5 clock cycles). When restarting the clocks, care must be taken to ensure that the minimum clock pulse width is not violated.

Resetting the Bt494 to a 9-clock cycle pipeline delay does not reset the blink counter circuitry. Therefore, if multiple Bt494s are used in parallel, the on-chip blink counters may not be synchronized. In this instance, the blink mask registers should be $00. Blinking may be done under software control via the read mask registers.

ESD and Latchup Considerations

ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Avoid DAC power decoupling networks with large time constants, which could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by ensuring all VAA pins are at the same potential, and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Test Features of the Bt494

The Bt494 contains two dedicated test registers and an analog output comparator that assist the user in evaluating the performance and functionality of the part. This section is intended to explain the operating usage of these test features.

Signature Registers (Signature Mode)

The input signature register is 16 bits wide, capturing pixel information prior to the lookup tables. Since the pixel path is 24 bits wide, the lower or upper 16 bits are selected for capture via command bit CR22.

The output signature register, in the active mode, operates with the 24 bits of data that are output from the color palette RAM. These 24-bit vectors represent a single pixel color, and are presented as inputs simultaneously to the red, green, and blue signature analysis registers (SARs), as well as the three on-chip DACs.

The SARs act as a 16-bit or 24-bit wide linear feedback shift register on each succeeding pixel that is latched. It is important to note that in either the 2:1 or 4:1 multiplexed modes, the SARs latch only one pixel per "load group." Thus, the SARs are operating only on every second or fourth pixel in the multiplexed modes. The user determines which pixel phase (A, B, C, or D) is latched for generating new signatures by setting bits D0–D2 in the test register.

In 1:1 mux mode, the SARs will generate signatures on each succeeding pixel in the input stream. In this case, the user should always select pixel "A" (test register D0, D1, and D2 = 000) when in the 1:1 mode, since the "A" pixel pins are the only active pixel inputs.

The Bt494 will only generate signatures while in "active-display" (BLANK* negated). The SARs are available for reading and writing via the MPU port when the Bt494 is in a blanking state (BLANK* asserted). Specifically, it is safe to access the SARs after the DAC outputs are in the blanking state (up to 15 pixel clock periods after BLANK* is asserted).

Typically, the user will write a specific 16-bit or 24-bit "seed" value into the SARs. Then, a known pixel stream will be input to the chip, for example, one scan-line or one frame buffer's worth of pixels. Then, at the succeeding blank state, the resultant 16-bit or 24-bit signature canbe read out by the MPU. The 24-bit signature register data is a result of the

5

Application Information (continued)

same captured data that is fed to the DACs. Thus, overlay and cursor data validity is also tested using the signature registers.

Assuming the chip is running 2:1 or 4:1 mux modes, the above process would be repeated with all different pixel phases—A, B, C, or D—being selected.

It is not simple to describe algorithmically the specific linear feedback shift operation used in the Bt494. The linear feedback configurations are shown in Figures 8 and 9.

Experienced users have developed tables of specific seeds and pixel streams and recorded the signatures that result from those inputs applied to "known-good" parts. Note that a good signature from one given pixel stream can be used as the seed for the succeeding stream to be tested. Any signature is deterministically created from a starting seed and the succeeding pixel stream fed to the SARs.

Signature Registers (Data Strobe Mode)

Setting command bit CR20 to a logic one puts the SARs into data strobe mode. In this instance, the linear feedback circuits of the SARs are disabled, which stops the SARs from generating signatures. Instead, the SARs simply capture and hold the respective pixel phase selected.

Any MPU data written to the SARs is ignored. One use, however, is to directly check each pixel color value that is strobed into the SARs. To read out values captured in the middle of a pixel stream, the user should first freeze all inputs to the Bt494. The levels of most inputs do not matter *except* that CLOCK should be high, and CLOCK* should be low. Then, the user may read out the pixel color by doing three successive MPU reads from the red, green, and blue SARs. Likewise, the input SAR may be read with 2 MPU reads.

In general, the color read-out will correspond to a pixel latched on the previous load. However, due to the pipelined data path, the color may come from an earlier load cycle. To read successive pixels, toggle LD*, pulse the CLOCK pins according to the mux state (1, 2, or 4 periods), then hold all pixel-related inputs and perform the three MPU reads as described. This process is best done on a sophisticated VLSI semiconductor tester.

Analog Comparator

The other dedicated test structure in the Bt494 is the analog comparator. It allows the user to measure the DACs against each other, as well as against a specific reference voltage.

Four combinations of tests are selected via the test register. With a given setting, the respective signals (DAC outputs or the 145 mV reference) will be continuously input to the comparator. The result of the comparator is latched into the test register. The capture occurs over one LD* period set by a logic one at pixel port B0 (A–D).

Due to the simple design of the comparator, it is recommended that the DAC outputs be stable for 5 µs before capture. At a display rate of 100 MHz, 5 µs corresponds to 500 pixels. Furthermore, either the color palette RAM or the pixel inputs (or both) should be configured to guarantee a single continuous output from the DACs under test, up until capture.

Application Information (continued)

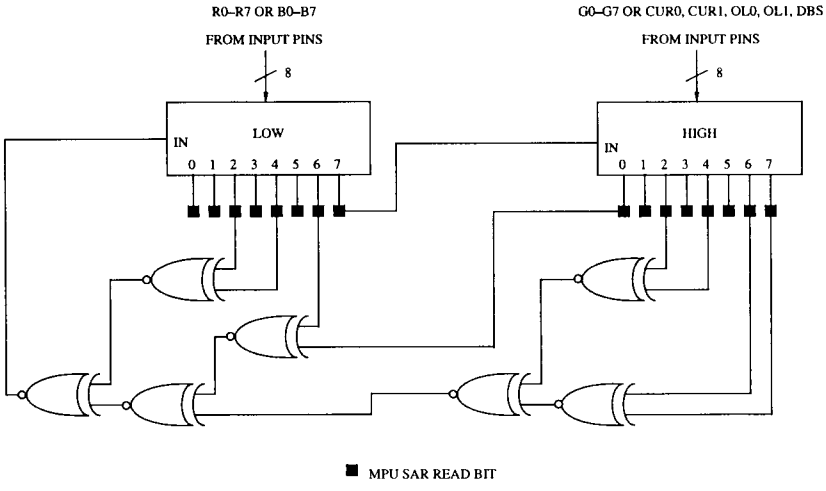


Figure 8. Input Signature Analysis Register Circuit.

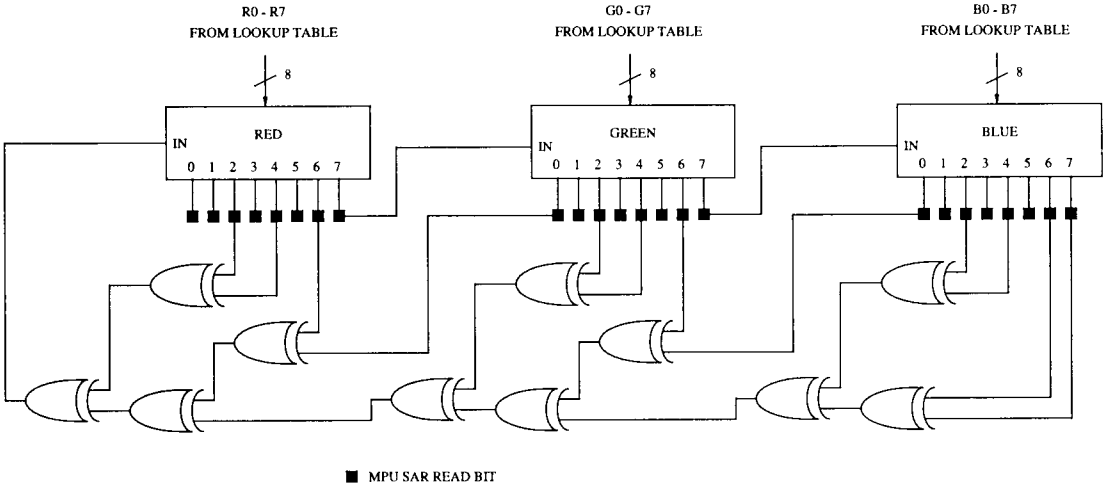


Figure 9. Output Signature Analysis Register Circuit.

Application Information (continued)

Initializing the Bt494

Following a power-on sequence, the Bt494 must be initialized. This sequence will configure it as follows:

- 4:1 multiplexed true-color operation
- 2 overlay planes on OL0, OL1
- sync enabled on IOG, 7.5 IRE blanking pedestal
- 2 cursor planes on CUR0, CUR1

Control Register Initialization

	C1, C0
Write $01 to address register low	00
Write $02 to address register high	01
Write $40 to command register 0	10
Write $00 to reserved location	10
Write $C0 to command register 2	10
Write $00 to reserved location	10
Write $FF to pixel read mask register R0- R7	10
Write $FF to pixel read mask register G0–G7	10
Write $FF to pixel read mask register B0–B7	10
Write $FF to pixel read mask register CUR & OL	10
Write $00 to pixel blink mask register R0- R7	10
Write $00 to pixel blink mask register G0–G7	10
Write $00 to pixel blink mask register B0–B7	10
Write $00 to pixel blink mask register CUR & OL	10
Write $00 to test register	10

Color Palette RAM Initialization

Write $00 to address register low	00
Write $00 to address register high	01
Write red data to RAM (location $000)	11
Write green data to RAM (location $000)	11
Write blue data to RAM (location $000)	11
Write red data to RAM (location $001)	11
Write green data to RAM (location $001)	11
Write blue data to RAM (location $001)	11
:	:
Write red data to RAM (location $0FF)	11
Write green data to RAM (location $0FF)	11
Write blue data to RAM (location $0FF)	11

Cursor Color Palette Initialization

Write $00 to address register low	00
Write $01 to address register high	01
Write red data to cursor (location $0)	10
Write green data to cursor (location $0)	10
Write blue data to cursor (location $0)	10
Write red data to cursor (location $1)	10
Write green data to cursor (location $1)	10
Write blue data to cursor (location $1)	10
Write red data to cursor (location $2)	10

Overlay Palette RAM Initialization (Note 1)

Write $00 to address register low	00
Write $00 to address register high	01
Write red data to RAM (location $201)	11
Write green data to RAM (location $201)	11
Write blue data to RAM (location $201)	11
Write red data to RAM (location $202)	11
Write green data to RAM (location $202)	11
Write blue data to RAM (location $202)	11
Write red data to RAM (location $203)	11
Write green data to RAM (location $203)	11
Write blue data to RAM (location $203)	

Note 1: The unused overlay palette locations are: $204–$20F.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ω
Reference Voltage	VREF	1.20	1.235	1.26	V
FS ADJUST Resistor	RSET		523		Ω

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				6.5	V
Voltage on Any Signal Pin (Note 1)		GND–0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
PGA	TJ			+170	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray-Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs (except CLOCK, CLOCK*)					
Input High Voltage	VIH	2.0		VAA + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			80	µA
Input Low Current (Vin = 0.4 V)	IIL			–80	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		4	15	pF
Clock Inputs (CLOCK, CLOCK*)				6	
Differential Input Voltage	ΔVIN	0.6		1	V
Input High Current (Vin = 4.0V)	IKIH			–1	µA
Input Low Current (Vin = 0.4 V)	IKIL			15	µA
Input Capacitance (f = 1 MHz, Vin = 4.0V)	CKIN		4		pF
Digital Outputs (D0–D7)					
Output High Voltage (IOH = 400 µA)	VOH	2.4		0.4	V
Output Low Voltage (IOL = 3.2 mA)	VOL			10	V
3-state Current	IOZ				µA
Output Capacitance	CDOUT		10		pF

See test conditions on next page.

DC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank					
SETUP = 7.5 IRE		0.95	1.44	1.90	mA
SETUP = 0 IRE		0	5	50	µA
Blank Level on IOG		6.29	7.62	8.96	mA
Blank Level on IOR, IOB		0	5	50	µA
Sync Level on IOG		0	5	50	µA
LSB Size			69.1		µA
DAC-to-DAC Matching			2	5	%
Output Compliance	VOC	–0.5		+1.2	V
Output Impedance	RAOUT		50		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT		13	20	pF
Voltage Reference Input Current	IREF		90		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 kHz)	PSRR		0.5		% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω and VREF = 1.235 V. SETUP = 7.5 IRE. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note: All JTAG DC parameters are tested to a minimum VAA = 5.0 volts wth VIL on JTAG pins at 0.6 volts max.

A C Characteristics

Parameter	Symbol	Min/Typ/ Max	160 MHz	135 MHz	110 MHz	Units
Clock Rate	Fmax	max	160	135	110	MHz
LD* Rate	LDmax					
1:1 multiplexing		max	67.5	67.5	55	MHz
2:1 multiplexing		max	67.5	67.5	55	MHz
4:1 multiplexing		max	40	33.75	27.5	MHz
R/W, C0, C1 Setup Time	1	min	0	0	0	ns
R/W, C0, C1 Hold Time	2	min	15	15	15	ns
CE* Low Time	3	min	50	50	50	ns
CE* High Time	4	min	25	25	25	ns
CE* Asserted to Data Bus Driven	5	min	7	7	7	ns
CE* Asserted to Data Valid	6	max	75	75	75	ns
CE* Negated to Data Bus 3-Stated	7	max	20	20	20	ns
Write Data Setup Time	8	min	35	35	35	ns
Write Data Hold Time	9	min	3	3	3	ns
TMS, TDI Setup Time	10	min	8	8	8	ns
TMS, TDI Hold Time	11	min	6	6	6	ns
TCK Low Time	12	min	10	10	10	ns
TCK High Time	13	min	10	10	10	ns
TCK Asserted to TDO Driven	14	min	5	5	5	ns
TCK Asserted to TDO Valid	15	max	20	20	20	ns
TCK Negated to TDO 3-Stated	16	max	20	20	20	ns
Pixel and Control Setup Time	17	min	3	3	3	ns
Pixel and Control Hold Time	18	min	2	2	2	ns
Clock Cycle Time	19	min	6.25	7.4	9.09	ns
Clock Pulse Width High Time	20	min	2.8	3.2	4	ns
Clock Pulse Width Low Time	21	min	2.8	3.2	4	ns
LD* Cycle Time	22					
1:1 multiplexing		min	14.81	14.81	18.18	ns
2:1 multiplexing		min	14.81	14.81	18.18	ns
4:1 multiplexing		min	25	29.63	36.36	ns
LD* Pulse Width High Time	23					
1:1 multiplexing		min	6	6	7	ns
2:1 multiplexing		min	6	6	8	ns
4:1 multiplexing		min	10	12	15	ns
LD* Pulse Width Low Time	24					
1:1 multiplexing		min	6	6	7	ns
2:1 multiplexing		min	6	6	8	ns
4:1 multiplexing		min	10	12	15	ns

See test conditions on next page.

AC Characteristics (continued)

Parameter	Symbol	Min/Typ/ Max	160 MHz	135 MHz	110 MHz	Units
Analog Output Delay	25	typ	25	25	25	ns
Analog Output Rise/Fall Time	26	typ	1.5	1.5	1.5	ns
Analog Output Settling Time	27	max	8	8	8	ns
Clock and Data Feedthrough		typ	tbd	tbd	tbd	dB
Glitch Impulse (Note 1)		typ	50	50	50	pV – sec
DAC-to-DAC Crosstalk		typ	tbd	tbd	tbd	dB
Analog Output Skew		typ	0	0	0	ns
		max	2	2	2	ns
Pipeline Delay		min	7	7	7	Clocks
		max	11	11	11	Clocks
VAA Supply Current (Note 1)	IAA	typ	400	380	365	mA
		max	tbd	tbd	tbd	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω and VREF = 1.235 V. TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10-percent and 90-percent points. ECL input values are VAA–0.8 to VAA–1.8 V, with input rise/fall times ≤2 ns, measured between the 20-percent and 80-percent points. Timing reference points at 50 percent for inputs and outputs. Analog output load ≤10 pF, D0–D7 output load ≤75 pF. See the timing dimensions and notes in Figures 10–12. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Glitch impulse includes clock and data feedthrough, and –3 dB test bandwidth = 2x clock rate.

Note 1: At Fmax. IAA (typ) at VAA = 5.0 V, TA = 20° C. IAA (max) at VAA = 5.25 V, TA = 0° C.
Note 2: All JTAG AC parameters are tested to a minimum VAA = 5.0 volts withVIL on JTAG pins at 0.6 volts max.

Timing Waveforms

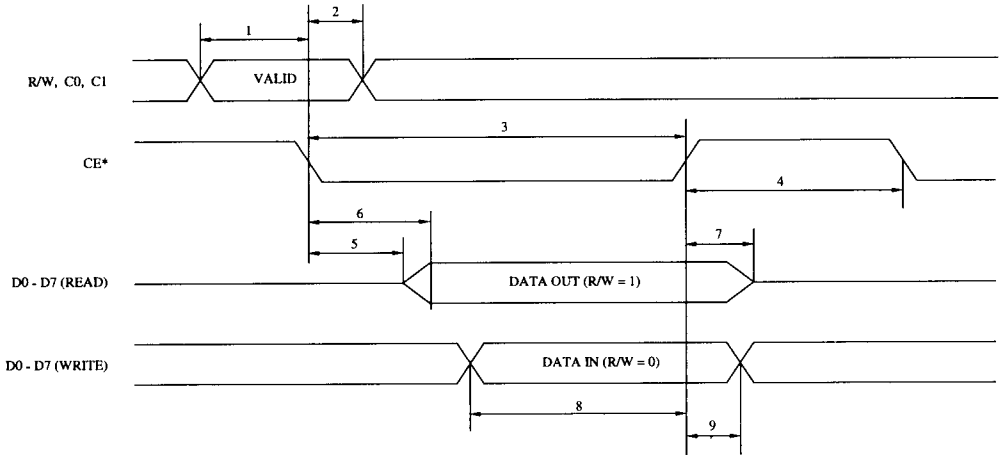
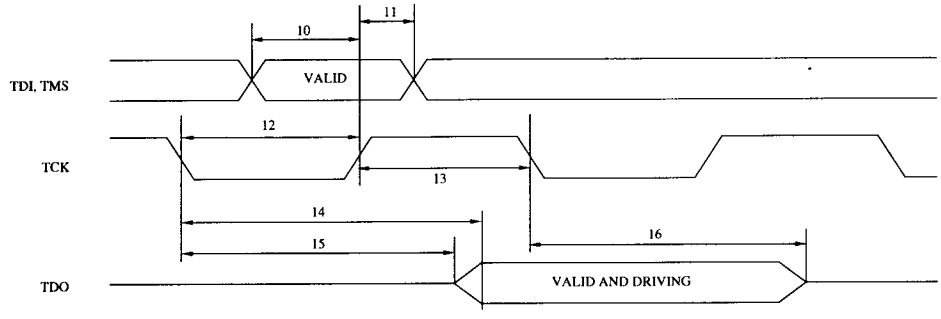


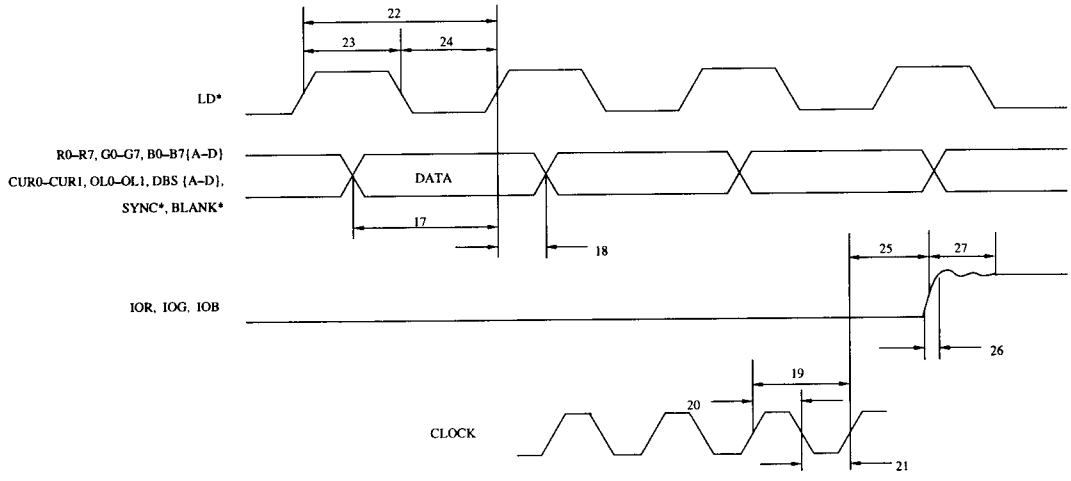
Figure 10. MPU Read/Write Timing Dimensions.



Note 1: TMS and TDI are sampled on the rising edge of TCK.
Note 2: TDO changes after the falling edge of TCK.

Figure 11. JTAG Timing.

Timing Waveforms



Note 1: Output delay time is measured from the 50-percent point of the rising clock edge to the 50-percent point of full-scale transition.

Note 2: Output settling time is measured from the 50-percent point of full-scale transition to output settling within ±1LSB.

Note 3: Output rise/fall time is measured between 10 percent and 90 percent points of full-scale transition.

Figure 12. Video Input/Output Timing.

5

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt494KG135	135 MHz	169-pin PGA	0° to +70° C
Bt494KG110	110 MHz	169-pin PGA	0° to +70° C
Bt494KG160	160 MHz	169-pin PGA	0° to +70° C