LXP302

T1/ESF Digital Trunk Interface Circuit

General Description

The LXP302 is one of a famly of Level One T1 interface solutions. The device interfaces to the DS1 1.544 Mbps digital trunk. Pin compatible with the Mitel MT8976, the LXP302 provides all formatting necessary for transmission on the T1 link.

The LXP302 meets the Extended Super Frame format (ESF) and D3/D4 format, and is compatible with SLC-96 systems.

The chip includes a full two-frame elastic buffer, ensuring superior jitter and wander suppression. Zero-code suppression schemes such as B8ZS and jammed-bit enhance the flexibility of this device.

The LXP302 provides a full range of maintenance and diagnostic features, allowing reliable performance measurement.

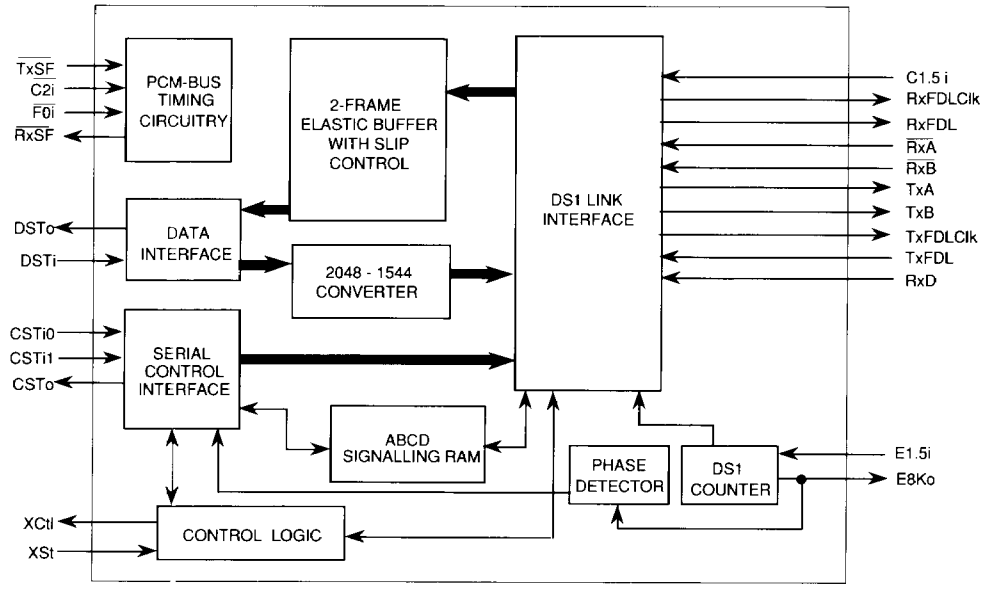
Applications

- DS1/ESF digital trunk interfaces
- Computer to PBX interfaces (DMI and CPI)
- High speed computer to computer data links
- Digital cross-connect interface

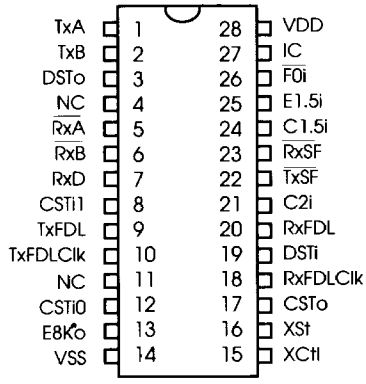
Features

- D3/D4 or ESF framing and SLC-96 compatible
- 2 frame elastic buffer with 32 µsec jitter buffer
- Insertion and detection of A, B, C, D bits. Signalling freeze, optional debounce.
- Selectable B8ZS/jammed-bit (ZCS) or transparent zero code replacement
- Yellow alarm and blue alarm signal capabilities
- Bipolar violation count, FT error count, CRC error count
- Selectable robbed-bit signalling
- Frame and superframe sync. signals, Tx and Rx
- AMI encoding and decoding
- Per channel, overall, and remote loop-around
- Digital phase detector between T1 line & PCM-BUS
- One uncommitted scan point and drive point
- Pin-compatible with LXP303 CEPT interface circuit
- Pin-compatible with MT8976
- ST-BUS™ compatible

Figure 1: Block Diagram



LEVEL ONE



Pin Descriptions

Pin #	Sym	I/O	Name	Description
1	TxA	O	Transmit A	Unipolar output that can be used in conjunction with TxB and external line driver circuitry to generate the bipolar DS1 signal
2	TxB	O	Transmit B	Unipolar output that can be used in conjunction with TxA and external line driver circuitry to generate the bipolar DS1 signal
3	DSTo	O	Data PCM-BUS	A 2048 kbps serial output stream which contains the 24 PCM or data channels received from the DS1 line
4	NC			No connection
5	$\overline{\text{RxA}}$	I	Receive A Complementary	Accepts a unipolar split-phase signal decoded externally from the received DS1 bipolar signal. This input, in conjunction with RxB, detects bipolar violations in the received signal
6	$\overline{\text{RxB}}$	I	Receive B Complementary	Accepts a unipolar split-phase signal decoded externally from the received DS1 bipolar signal. This input, in conjunction with $\overline{\text{RxA}}$, detects bipolar violations in the received signal
7	RxD	I	Receive Data	Unipolar RZ data signal decoded from the received DS1 signal. Generally the signals input at $\overline{\text{RxA}}$ and $\overline{\text{RxB}}$ are combined externally with a NAND gate and the resulting composite signal is input at this pin
8	CSTi1	I	Control PCM-BUS Input #1	A 2048 kbps serial control stream which carries 24 per-channel control words
9	TxFDL	I	Transmit Facility Data Link	A 4 kHz serial input stream that is multiplexed into the FDL position in the ESF mode, or the F_s pattern when in SLC-96 mode. It is clocked in on the rising edge of TxFDLClk
10	TxFDLClk	O	Transmit Facility Data Link Clock	A 4 kHz clock used to clock in the FDL data
11	NC			No connection
12	CSTi0	I	Control PCM-BUS Input #0	A 2048 kbps serial control stream that contains 24 per-channel control words and two master control words

Pin Descriptions continued

Pin #	Sym	I/O	Name	Description
13	E8Ko	O	Extracted 8 kHz Clock	The E1.5i clock is internally divided by 193 to produce an 8 kHz clock which is aligned with the received DS1 frame and output at this pin
14	V_{SS}		Ground	System Ground
15	XCtl	O	External Control	This is an uncommitted external output pin which is set or reset via bit 3 in Master Control Word 1 on CSTi0. The state of XCtl is updated once per frame
16	XSt	I	External Status	The state of this Schmitt trigger input pin is sampled once per frame and the status is reported in bit 4 of Master Status Word 1 on CSTo
17	CSTo	O	Control PCM-BUS	This is a 2048 kbps serial control stream which provides the 24 per-channel status words, and two master status words
18	RxFDLClk	O	Rcv Facility Data Link Clock	A 4 kHz clock signal used to clock out FDL information. The data is clocked out on the rising edge of RxFDLClk
19	DSTi	I	Data PCM-BUS	This pin accepts a 2048 kbps serial stream which contains the 24 PCM or data channels to be transmitted on the T1 trunk
20	RxFDL	O	Rcv Facility Data Link	A 4 kHz serial output stream that is demultiplexed from the FDL in ESF mode, or the received F_s bit pattern in SLC-96 mode. Clocked out on the rising edge of RxFDLClk
21	C2i	I	2.048 MHz Clock	This is the master clock used for clocking serial data into DSTi, CSTiO and CSTi1. It is also used to clock serial data out of CSTo
22	$\overline{\text{TxSF}}$	I	Transmit Superframe Pulse	A low-going pulse applied at this pin will set the transmit superframe to 1. The device will free run if this pin is held high
23	$\overline{\text{RxSF}}$	O	Received Superframe Pulse	A pulse output on this pin designates that the next frame of data on the PCM-BUS is from frame 1 of the received superframe. The period is 12 frames long in D3/D4 modes and 24 frames in ESF mode
24	C1.5i	I	1.544 MHz Clock	This is the DS1 transmit clock and is used to output data on TxA and TxB. It must be phase-locked to C2i. Data is clocked out on the rising edge of C1.5i
25	E1.5i	I	1.544 MHz Extracted Clock	This clock which is extracted from the received data is used to clock in data at $\overline{\text{RxA}}$, $\overline{\text{RxB}}$ and RxD. The falling edge of the clock is nominally aligned with the center of the received bit on RxD, $\overline{\text{RxA}}$ and $\overline{\text{RxB}}$
26	$\overline{\text{F0i}}$	I	Frame Pulse.	Frame synchronization signal; defines the startof the 32-channel PCM-BUS frame
27	IC		Internal Connection	Tied to V_{SS} for normal operation
28	V_{DD}		Positive Power	+ 5V ± 5%

Absolute Maximum Ratings*

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

• Supply voltage	V_{DD}	-0.3V to 7V
• Voltage on any I/O pin	$V_{I/O}$	V_{SS}-0.3V to V_{DD} +0.3V
• Current on any I/O pin	$I_{I/O}$	±40 mA
• Package power dissipation	P_D	800 mW
• Storage temperature	T_{ST}	-55° C(min)to 125° C(max)

Operating Characteristics (Voltages are with respect to ground (Vss) unless otherwise stated)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Operating Conditions						
Supply voltage	V_{DD}	4.75	5	5.25	V	
Input high voltage	V_{IH}	2.4		V_{DD}	V	for 400 mV noise margin
Input low voltage	V_{IL}	V_{SS}		0.4	V	for 400 mV noise margin
Operating Temperature	T_{OP}	0		70	°C	
DC Electrical Characteristics Clocked operation over recommended temperature ranges and power supply voltages						
Supply current	I_{DD}		5	15	mA	outputs unloaded
Input high voltage	V_{IH}	2.0			V	digital inputs
Input low voltage	V_{IL}			0.8	V	digital inputs
Output high current	I_{OH}		20		mA	Source Current, V_{OH} = 2.4 V
Output low current	I_{OL}		10		mA	Sink Current, V_{OL} = 0.4 V
Input leakage current	I_{IL}		± 1	± 10	µA	digital inputs V_{IN} = 0 to V_{DD}
Schmitt Trigger Input (XSt)	V_{T+}	2.4		4.0	V	
	V_{T-}	1.6		3.0	V	
AC Electrical Characteristics[2] - Capacitance						
Input pin capacitance	C_I		10		pF	
Output pin capacitance	C_O		10		pF	

[1] Typical figures are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

[2] Timing is over recommended temperature and power supply voltages.

AC Electrical Characteristics[1] - Clock Timing (Figures 2 & 3)

Characteristics	Sym	Min	Typ[2]	Max	Units	Test Conditions
C2i clock period	t_{p20}	400	488	600	ns	
C2i clock width high or low	t_{w20}	200	244	300	ns	
Frame pulse set up time	t_{FPS}	50			ns	
Frame pulse hold time	t_{FPH}	50			ns	
Frame pulse width	t_{FPW}	50			ns	
$\overline{\text{RxSF}}$ output delay	t_{FPOD}		100		ns	50pF load
$\overline{\text{TxSF}}$ hold time	t_{TxSFH}		0.1	124.5	µs	
$\overline{\text{TxSF}}$ setup time	t_{TxSFS}		0.1	124.5	µs	

[1] Timing is over recommended temperature & power supply voltages

[2] Typical figures are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

Figure 2: Clock & Frame Alignment for PCM-BUS Streams

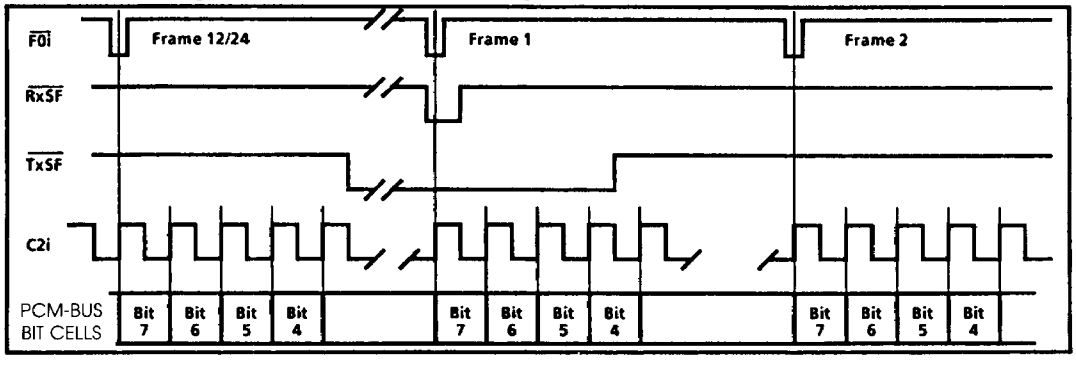
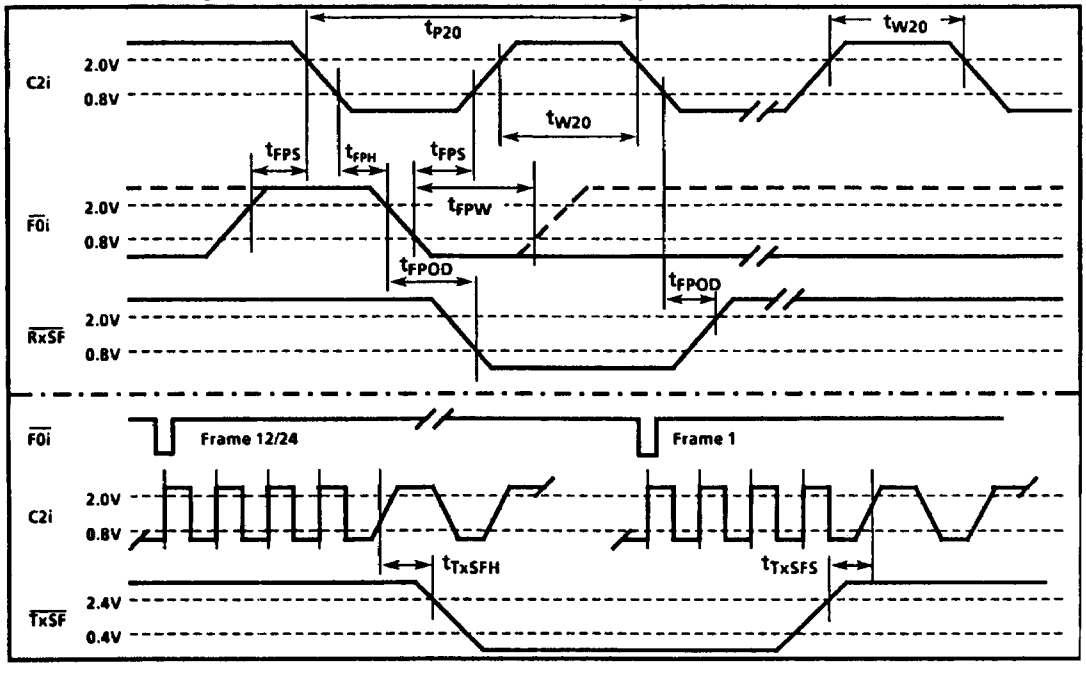


Figure 3: Clock & Frame Pulse Timing for PCM-BUS Streams



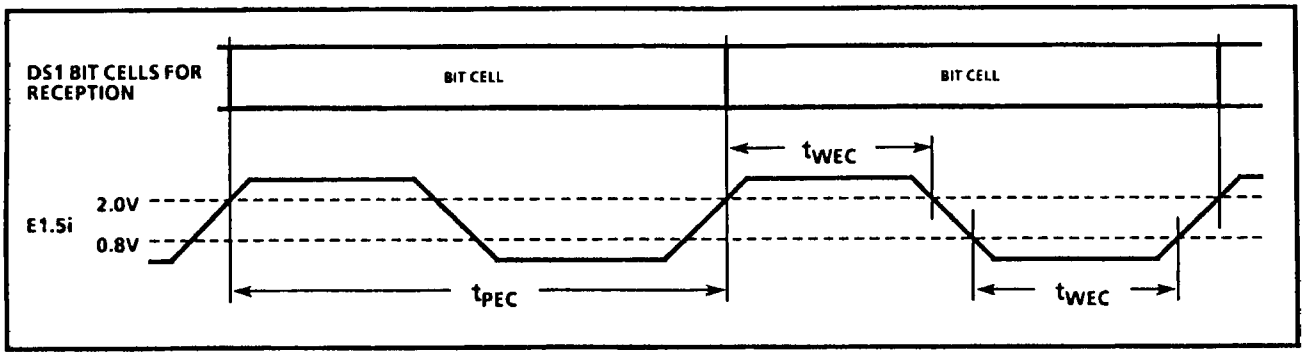
AC Electrical Characteristics[1] - Timing for DS1 Link Bit Cells (Figure 4)

Characteristics	Sym	Min	Typ[2]	Max	Units	Test Conditions
E1.5i clock period	t_{PEC}		648		ns	
E1.5i clock width high or low	t_{WEC}		324		ns	

[1] Timing is over recommended temperature & power supply voltages.

[2] Typical figures are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

Figure 4: DS1 Receive Clock Timing



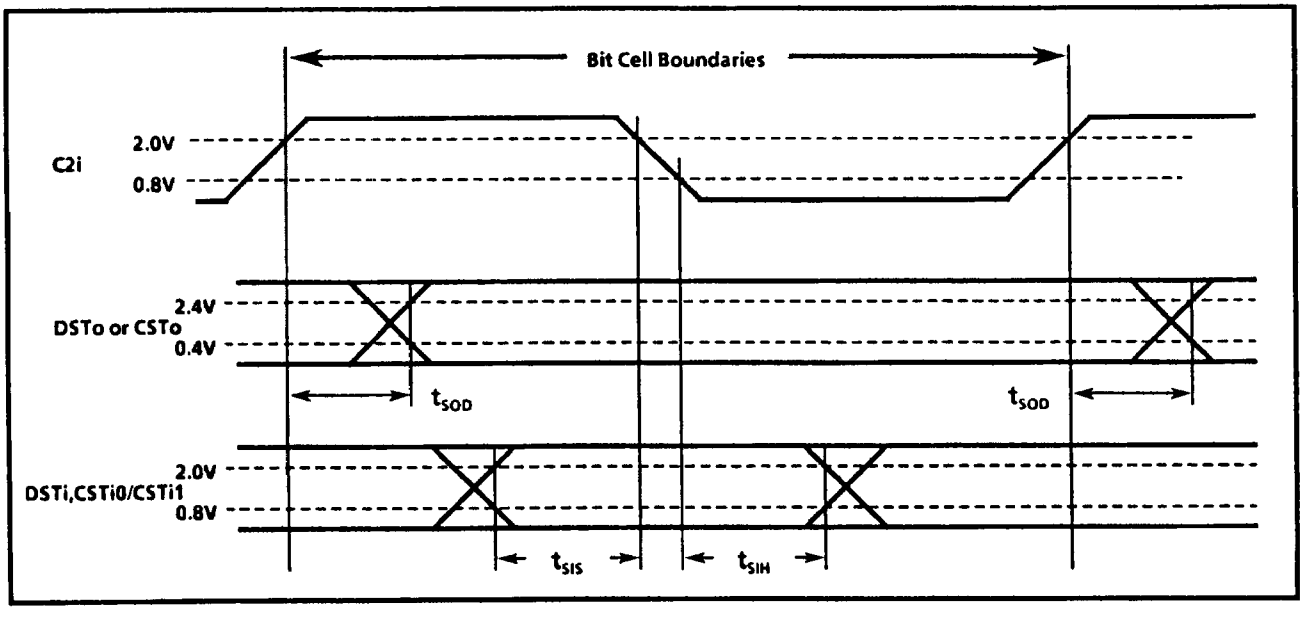
AC Electrical Characteristics[1] - Timing for PCM-BUS Bit Cells (Figure 5)

Characteristics	Sym	Min	Typ[2]	Max	Units	Test Conditions
Serial output delay	t_{SOD}			125	ns	150pF load
Serial input set-up time	t_{SIS}	30			ns	
Serial input hold time	t_{SIH}	90			ns	

[1] Timing is over recommended temperature & power supply voltages.

[2] Typical figures are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

Figure 5: PCM-BUS Stream Timing



AC Electrical Characteristics[1] - Timing for XCTL, XST, & E8Ko (Figures 6, 7 & 8)

Characteristics	Sym	Min	Typ[2]	Max	Units	Test Conditions
External control delay	t_{XCD}		100		ns	50 pF load
External status set-up time	t_{XSS}		100		ns	
External status hold time	t_{XSH}		400		ns	
8 kHz output delay	t_{8OD}		75		ns	50 pF load
8 kHz output low width	t_{8OL}		78		µs	50 pF load
8 kHz output high width	t_{8OH}		47		µs	50 pF load
8 kHz rise time	t_{8R}		10		ns	50 pF load
8 kHz fall time	t_{8F}		10		ns	50 pF load
8 kHz disable delay	t_{8DD}		100		ns	50 pF load

[1] Timing is over recommended temperature & power supply voltages.

[2] Typical figures are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

Figure 6: XCTL Timing

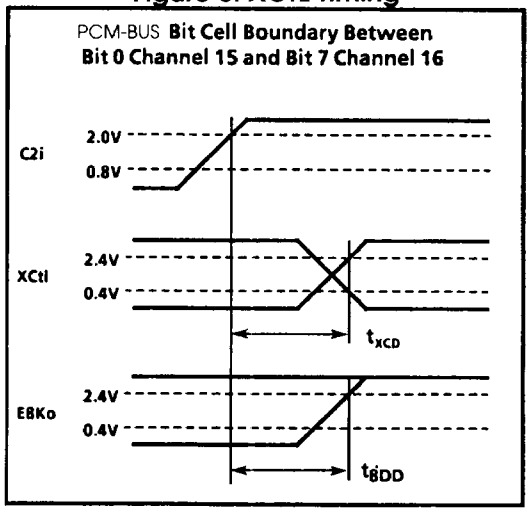


Figure 7: XST Timing

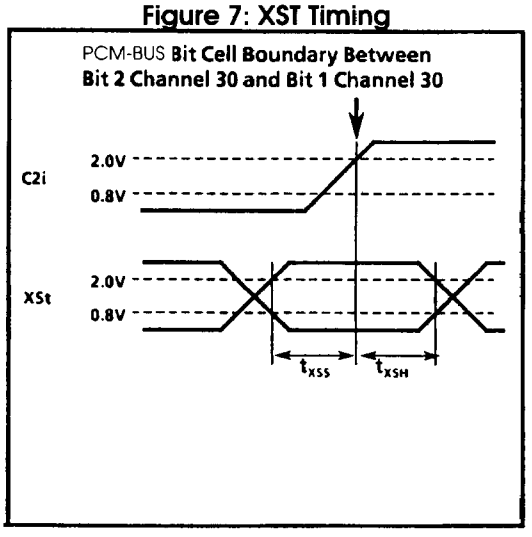
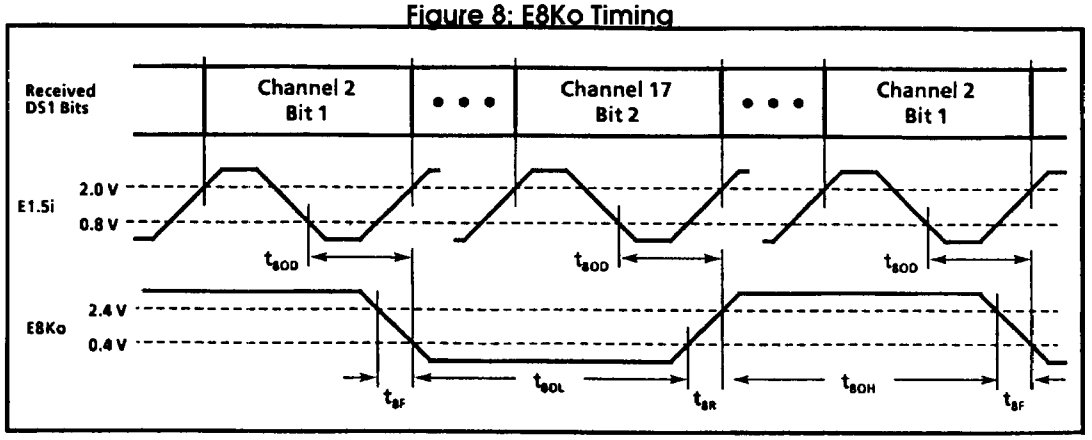


Figure 8: E8Ko Timing



AC Electrical Characteristics[1] - DS1 Link Timing (Figures 9 & 10)

Characteristics	Sym	Min	Typ[2]	Max	Units	Test Conditions
Transmit steering delay	t_{TSD}		90		ns	150 pF load
Transmit steering transition time	t_{TST}		30		ns	150 pF load
Received steering hold time	t_{RSH}		50		ns	
Received data set-up time	t_{RDS}		50		ns	See note 3
Received data hold time	t_{RDH}		75		ns	See note 3
Max. received data to clock delay	t_{RDCD}		20		ns	
C1.5i period	$t_{PC1.5}$		648		ns	
C1.5i pulse width high or low	$t_{WC1.5}$		324		ns	

[1] Timing is over recommended temperature & power supply voltages ranges.

[2] Typical figures are at 25° C and are for design aid only: not guaranteed and not subject to production testing.

[3] Parameters t_{RDS} and t_{RDH} relate to device functionality. Network constraints may require tighter tolerances than device specifications.

Figure 9: Transmit Timing for DS1 Link

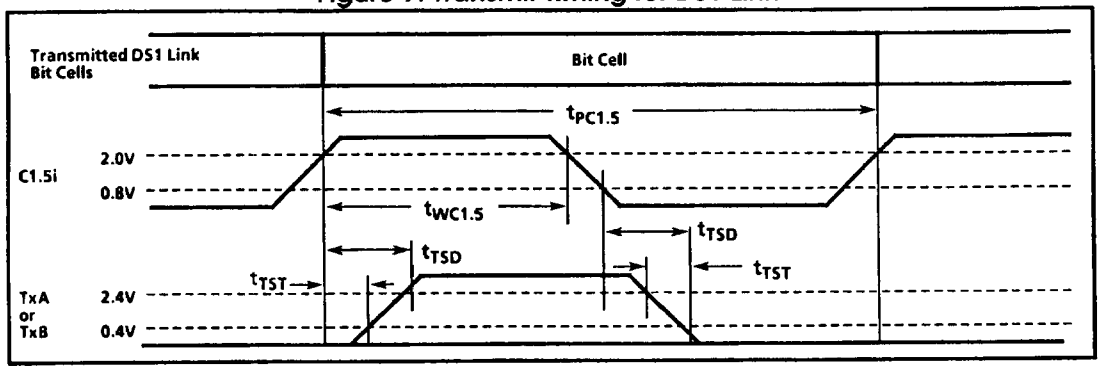
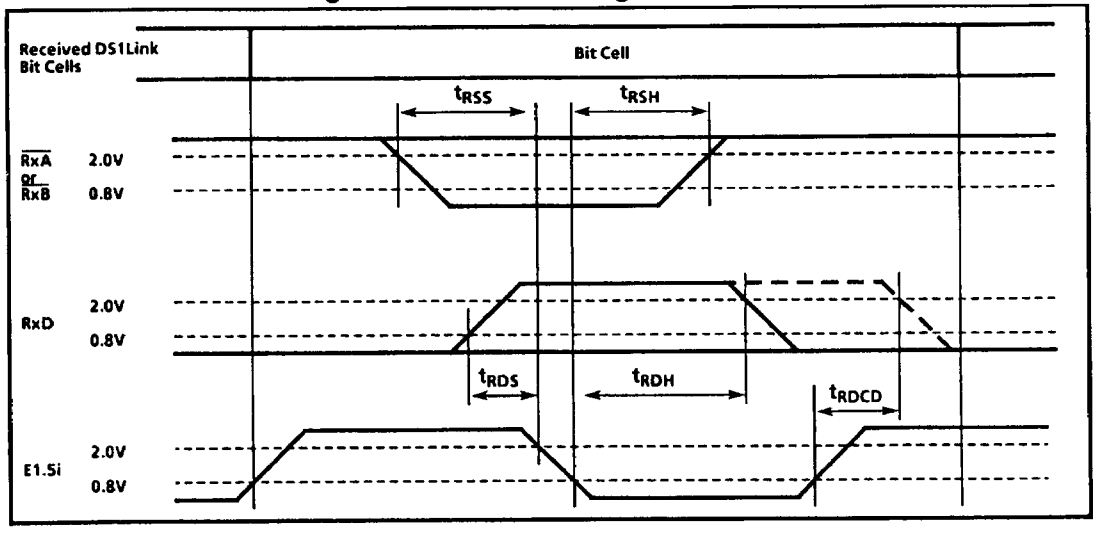


Figure 10: Receive Timing for DS1 Link[3]



AC Electrical Characteristics[1] - DS1 Link Timing (Figures 11& 12)

Characteristics	Sym	Min	Typ[2]	Max	Units	Test Conditions
Transmit FDL set-up time	t_{DLS}		50		ns	
Transmit FDL hold time	t_{DLH}		150		ns	
Receive FDL output delay	t_{DLOD}		100		ns	50 pF load
FDL clock period	t_{DLCP}		250		µs	
Facility data link clock delay	t_{FCD}		50		ns	50 pF load

[1] Timing is over recommended temperature & power supply voltages.

[2] Typical figures are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

Figure 11: Clock & Frame Alignment for PCM-BUS Streams

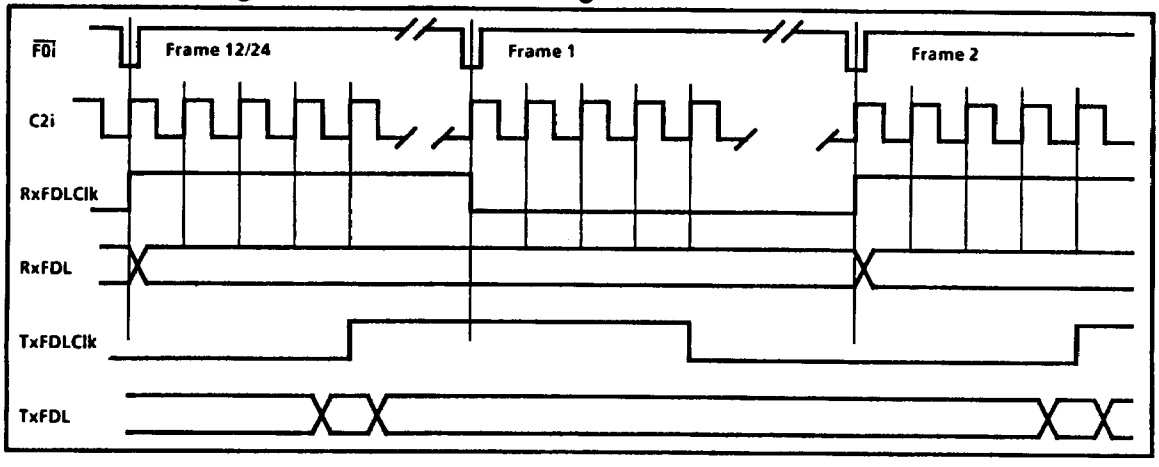


Figure 12: Facility Data Link Timing for ESF Mode

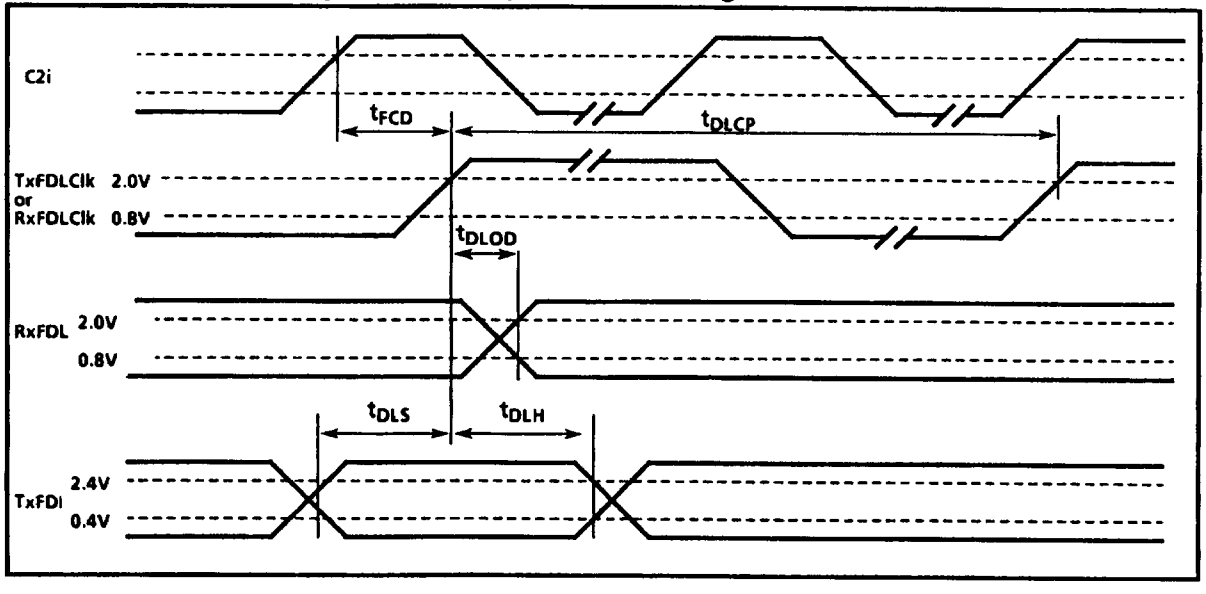


Figure 13: Format of 2048 kbps PCM-BUS Streams

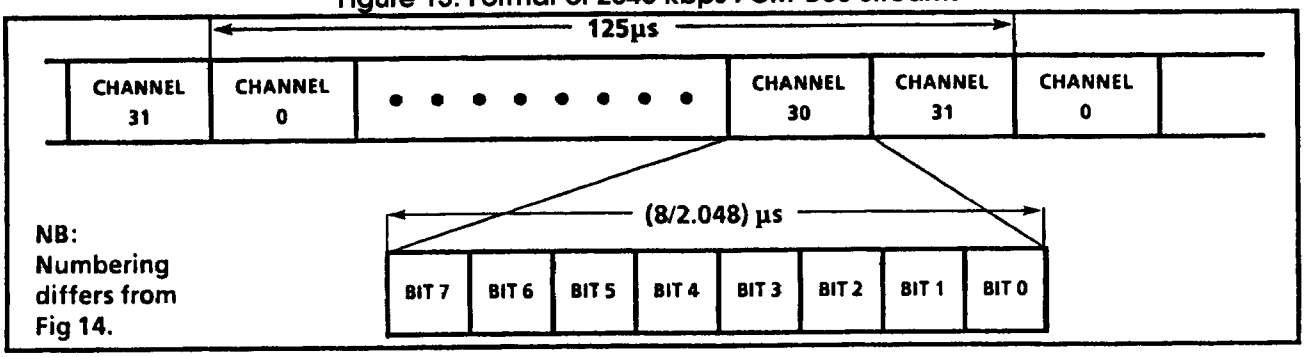
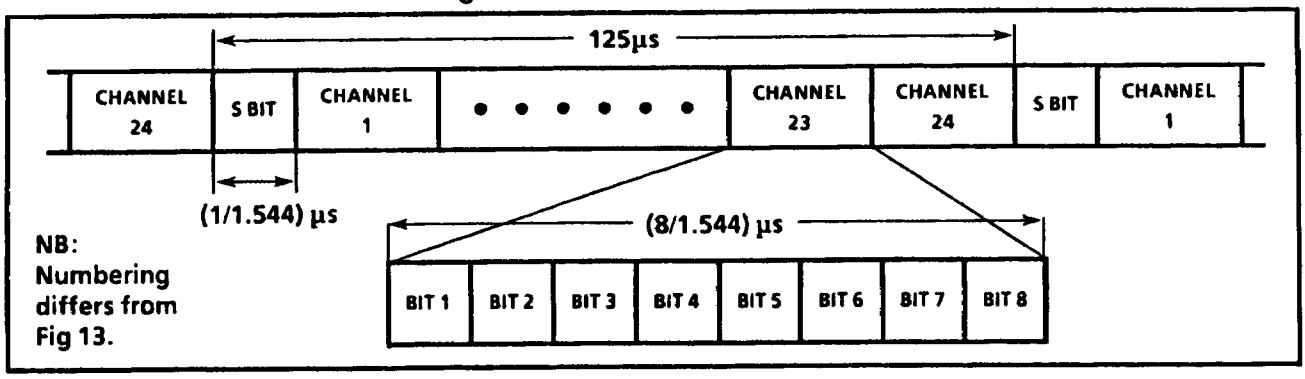


Figure 14: DS1 Link Frame Format



Functional Timing Diagrams

Figure 15: PCM-BUS Timing

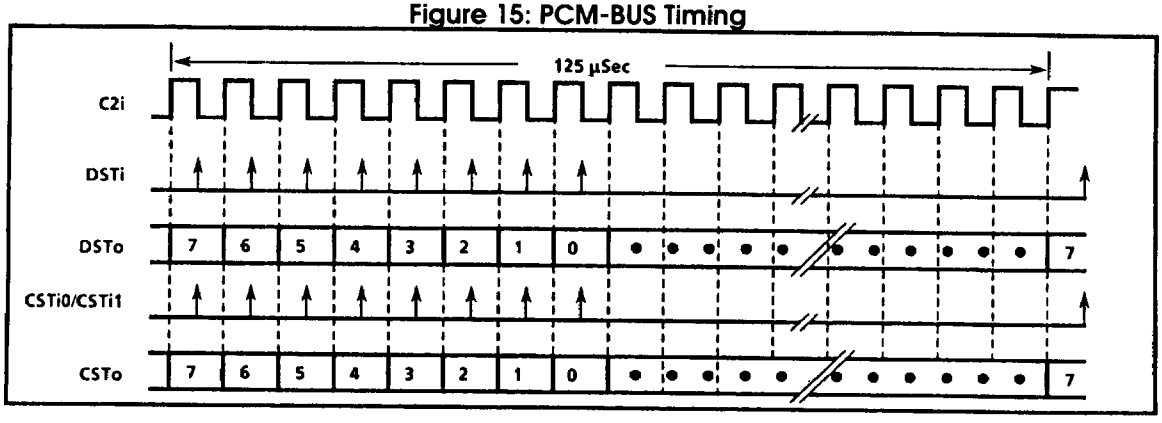


Figure 16: DS1 Receive Timing

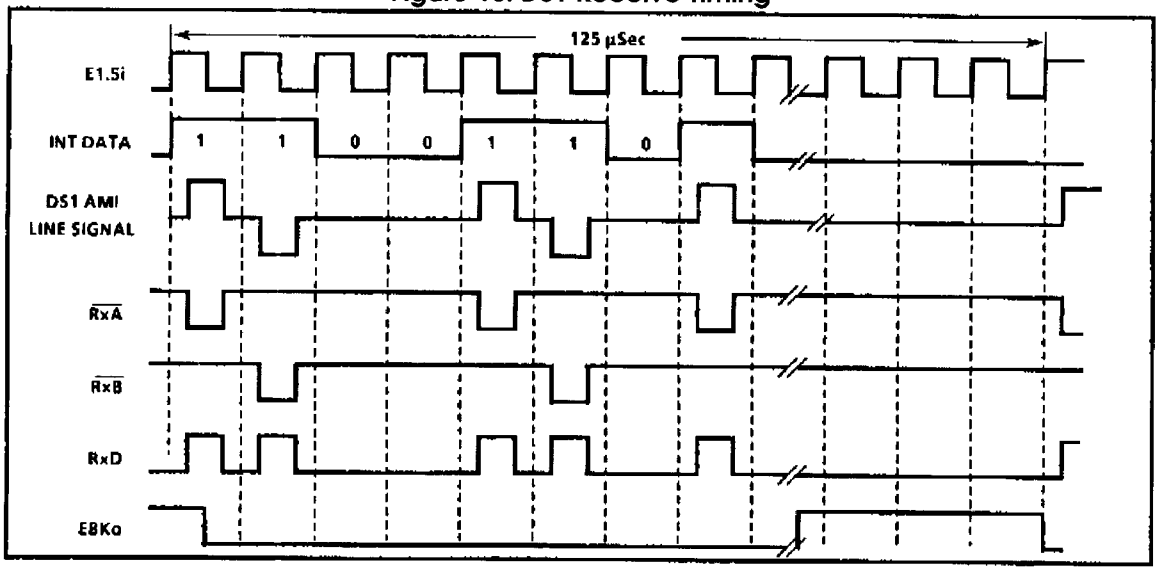
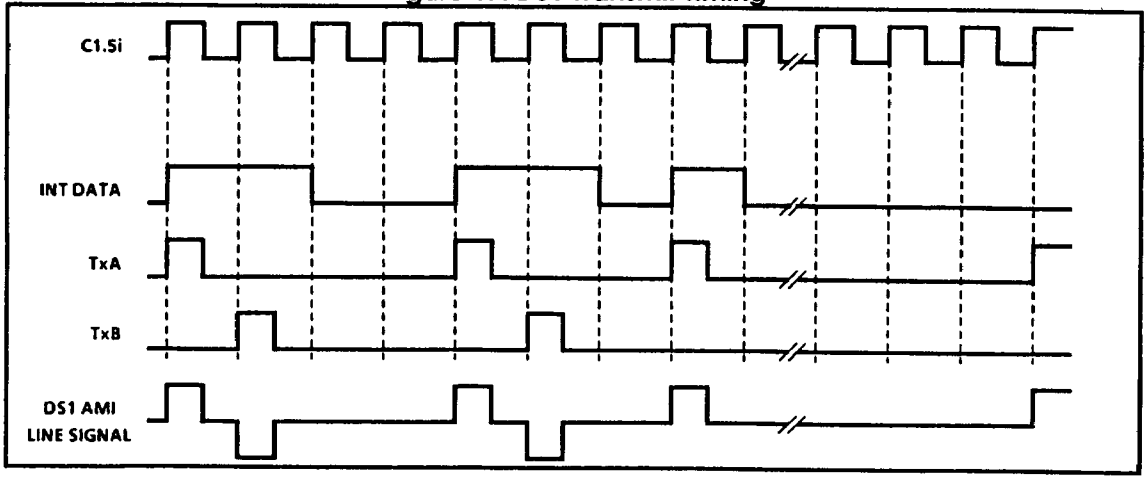


Figure 17: DS1 Transmit Timing



Functional Timing Diagrams

Figure 18: PCM-BUS Channel Allocations

DSTi	0 X	1	2	3	4 X	5	6	7	8 X	9	10	11	12 X	13	14	15	16 X	17	18	19	20 X	21	22	23	24 X	25	26	27	28 X	29	30	31
DS1		1	2	3		4	5	6		7	8	9		10	11	12		13	14	15		16	17	18		19	20	21		22	23	24

X = Unused channel

PCM-BUS Channel Versus DS1 Channel Transmitted

DSTo	0 X	1	2	3	4 X	5	6	7	8 X	9	10	11	12 X	13	14	15	16 X	17	18	19	20 X	21	22	23	24 X	25	26	27	28 X	29	30	31
DS1		1	2	3		4	5	6		7	8	9		10	11	12		13	14	15		16	17	18		19	20	21		22	23	24

X = Unused channel

PCM-BUS Channel Versus DS1 Channel Received

CSTi0	0 PCCW 1	1 PCCW 1	2 PCCW 1	3 X	4 PCCW 1	5 PCCW 1	6 PCCW 1	7 X	8 PCCW 1	9 PCCW 1	10 PCCW 1	11 X	12 PCCW 1	13 PCCW 1	14 PCCW 1	15 MCW1	16 PCCW 1	17 PCCW 1	18 PCCW 1	19 X	20 PCCW 1	21 PCCW 1	22 PCCW 1	23 X	24 PCCW 1	25 PCCW 1	26 PCCW 1	27 X	28 PCCW 1	29 PCCW 1	30 PCCW 1	31 MCW2
DS1	1	2	3		4	5	6		7	8	9		10	11	12		13	14	15		16	17	18		19	20	21		22	23	24	

PCCW = Per channel control word
MCW1/2 = Master control word 1/2
X = Unused channel

PCM-BUS Channel Versus DS1 Channel Controlled

CSTi1	0 PCCW 2	1 PCCW 2	2 PCCW 2	3 X	4 PCCW 2	5 PCCW 2	6 PCCW 2	7 X	8 PCCW 2	9 PCCW 2	10 PCCW 2	11 X	12 PCCW 2	13 PCCW 2	14 PCCW 2	15 X	16 PCCW 2	17 PCCW 2	18 PCCW 2	19 X	20 PCCW 2	21 PCCW 2	22 PCCW 2	23 X	24 PCCW 2	25 PCCW 2	26 PCCW 2	27 X	28 PCCW 2	29 PCCW 2	30 PCCW 2	31 X
DS1	1	2	3		4	5	6		7	8	9		10	11	12		13	14	15		16	17	18		19	20	21		22	23	24	

PCCW = Per channel control word
X = Unused channel

PCM-BUS Channel Versus DS1 Channel Controlled

CSTo	0 PCSW	1 PCSW	2 PCSW	3 PSW	4 PCSW	5 PCSW	6 PCSW	7 X	8 PCSW	9 PCSW	10 PCSW	11 X	12 PCSW	13 PCSW	14 PCSW	15 MSW1	16 PCSW	17 PCSW	18 PCSW	19 X	20 PCSW	21 PCSW	22 PCSW	23 X	24 PCSW	25 PCSW	26 PCSW	27 X	28 PCSW	29 PCSW	30 PCSW	31 MSW2
DS1	1	2	3		4	5	6		7	8	9		10	11	12		13	14	15		16	17	18		19	20	21		22	23	24	

PCSW = Per channel status word
PSW = Phase status word
MSW = Master status word
X = Unused channel

PCM-BUS Versus DS1 Channel Status

Functional Description

The LXP302 provides a simple interface to a bidirectional DS1 link. The device does all formatting and signalling insertion and detection. Programmable options in the device include: ESF, D3/D4, or SLC-96 mode, common-channel or robbed-bit signalling, zero code suppression, alarms, and local and remote loopback. All data and control information is communicated to the LXP302 via 2048 kbps serial streams conforming to the PCM-BUS format.

The PCM-BUS is a TDM serial bus that operates at 2048 kbps. The serial streams are divided into 125 µsec frames made up of 32 eight-bit channels. A serial stream made up of these 32 eight-bit channels is a PCM-BUS stream, and one of these 64-kbps channels is a PCM-BUS channel.

The system side of the LXP302 is made up of PCM-BUS inputs and outputs, i.e. control inputs and outputs (CSTi/o) and data inputs and outputs (DSTi/o). These signals are shown in Figure 15. The line side of the device is made up of the split-phase inputs and outputs that can be interfaced to an external bipolar receiver and transmitter. Figures 16 and 17 show functional receive and transmit timing.

Data for transmission on the DS1 line is clocked serially into the device at the DSTi pin. DSTi accepts a 32-channel time division multiplexed PCM-BUS stream. Data is clocked in with the falling edge of the C2i clock. PCM-BUS frame boundaries are defined by the frame pulse applied at the F0i pin. Only 24 of the available 32 channels on the PCM-BUS serial stream are actually transmitted on the DS1 side. The device ignores the unused eight channels.

Data received from the DS1 line is clocked out of the device at the DSTo pin, on the rising edge of the C2i clock. Only 24 of the 32 channels output by the device contain the information from the DS1 line. The DSTo pin is, however, actively driven during the unused channel time slots. Figure 18 shows the correspondence between DS1 channels and the PCM-BUS channels.

All device control and monitoring is accomplished through two PCM-BUS serial control inputs and one serial control output. Control PCM-BUS input number 0 (CSTi0) accepts a PCM-BUS serial stream which contains the 24 per-DS1 channel control words and two master control words. The per-channel control words relate directly to the 24 information channels output on the DS1 side. The master control words affect operation of the whole device.

Control PCM-BUS input number 1 (CSTi1) accepts a PCM-BUS stream containing the A, B, C and D signalling bits. Figure 18 shows the relationship between the CSTi channels and the controlled DS0 channels. Status and signalling information is received from the device via the control PCM-BUS output (CSTo). This serial output stream contains two master status words, 24 per-channel status words and one Phase Status Word. Figure 18 shows the correspondence between the received DS1 channels and the status words. Detailed information on the operation of the control interface is presented below.

Programmable Features

The main features in the device are programmed through two master control words which occupy channels 15 and 31 in Control PCM-BUS input stream number 0 (CSTi0). These two eight-bit words are used to:

- select the different operating modes of the device ESF, D3/D4 or SLC-96
- activate the features needed in a certain application; common channel signalling, zero code suppression, signalling debounce, etc.
- turn on in-service alarms, diagnostic loop-arounds, and the external control function

Tables 1 and 2 explain the function of the bits in Master Control Words 1 and 2.

Major Operating Modes

The major operating modes of the device are enabled by bits 2 and 4 of Master Control Word 2. The Extended Superframe (ESF) mode is enabled when bit 4 is set high. Bit 2 has no effect in this mode. The ESF mode enables the transmission of the S bit pattern shown in Table 3. This includes the frame/superframe pattern, the CRC-6, and the Facility Data Link (FDL). The device generates the frame/multiframe pattern and calculates the CRC for each superframe. The data clocked into the device on the TxFDL pin is incorporated into the FDL. ESF mode will also insert A, B, C and D signalling bits into the 24 frame multiframe. The DS1 frame begins after approximately 25 periods of C1.5i clock from the $\overline{F0i}$ frame pulse.

During synchronization, the receiver locks to the incoming frame, calculates the CRC, and compares it to the CRC received in the next multiframe. The device will not declare itself to be in synchronization unless a valid framing pattern in the S bit is detected and a correct CRC is received. The CRC check in this case provides protection against false framing. The CRC check can be turned off by setting bit 1 in Master Control Word 2.

The device can be forced to resynchronize itself. If bit 3 in Master Control Word 2 is set for one frame and then subsequently reset, the device will search for a new frame position. The decision to reframe is made by the user's system processor on the basis of the status conditions

Table 1: Master Control Word 1 (Channel 15, CSTi0)

Bit #	Name	Description
7	Debounce	When set, the received A, B, C and D signalling bits are reported directly in the per-channel status words output at CSTo. When clear, the signalling bits are debounced for 6 to 9 ms before they are placed on CSTo.
6	TSPZCS	**Transparent Zero Code Suppression.** When the bit is set, no zero code suppression is implemented.
5	B8ZS	**Binary Eight Zero Suppression.** When this bit is set, B8ZS zero code suppression is enabled. When clear, bit 7 in data channels containing all zeros is forced high before being transmitted on the DS1 side. This bit is inactive if the TSPZCS bit is set.
4	8KHSel	**8 KHz Output Select.** When set, the E8Ko pin is held high. When clear, the E8Ko generates an 8 kHz output derived from the E1.5i clock.
3	XCtl	**External Control Pin.** When set, the XCtl pin is held high. When clear, XCtl is held low.
2	ESFYLW	**ESF Yellow Alarm.** Valid only in ESF mode. When set, a sequence of eight 1's followed by eight 0's is sent in the FDL bit positions. When clear, the FDL bit contains data input at TxFDL.
1	Robbed bit	When this bit is set, robbed bit signalling is disabled on all DS0 transmit channels. When clear, A, B, C and D signalling bit insertion in bit 8 for all DS0 transmit channels in every 6th frame is enabled.
0	YLALR	**Yellow Alarm.** When set, bit 2 of all DS1 channels is set low. When clear, bit 2 operates normally.

detected in the received master status words. This may include consideration of the number of errors in the received CRC in conjunction with an indication of the presence of a mimic. When the device becomes synchronized, the mimic bit in Master Status Word 1 is set if the device found another possible candidate when it was searching for the framing pattern.

Note that the device resynchronizes automatically if the errors in the terminal framing pattern (F_T or FPS) exceed the threshold set with bit 0 in Master Control Word 2.

Standard D3/D4 framing is enabled when bit 4 of Master Control Word 2 is reset (logic 0). In this mode, the device searches for and inserts the framing pattern shown in Table 4. This mode only supports AB bit signalling and does not contain a CRC check.

The CRC/MIMIC bit in Master Control Word 2, when set high, allows the device to synchronize in the presence of a mimic. If this bit is reset, the device will not synchronize in the presence of a mimic.

In the D3/D4 mode, the device can also be made compatible with SLC-96 by setting bit two of Master Control Word 2. This allows the user to insert and extract the signalling framing pattern on the DS1 bit stream using the FDL input and output pins. The user must format this 4 kbps of information externally to meet all requirements of the SLC-96 specification (see Table 5). The device multiplexes and demultiplexes this information into the proper position. This mode of operation can also be used for any other application that uses all or part of the signalling framing pattern. As long as the serial stream clocked into the TxFDL contains two proper sets of consecutive synchronization bits (as shown in Table 5 for frames 1 to 24), the device will be able to insert and extract the A, B signalling bits. The TxSF pin should be held high in this mode. Superframe boundaries cannot be defined by a pulse on this input. The RxSF output functions normally and indicates the superframe boundaries based on the synchronization pattern in the Fs received bit position.

Zero Code Suppression

The combination of bits 5 and 6 in Master Control Word 1 allows one of three zero code suppression schemes to be selected. The three choices are: none, binary 8 zero

Table 2: Master Control Word 2 (Channel 31, CSTi0)

Bit #	Name	Description
7	RMLOOP	**Remote Loopback**. When set, the data received at $\overline{RxA}$ and $\overline{RxB}$ is looped back to TxA and TxB respectively. The data is clocked into the device with E1.5i. The device still monitors the received data and outputs it at DSTo. The device operates normally when the bit is clear.
6	DGLOOP	**Digital Loopback**. When set, the data input on DSTi is looped around to DSTo. The normal received data on $\overline{RxA}$, $\overline{RxB}$ and RxD is ignored. However, the data input at DSTi is still transmitted on TxA and TxB. The device frames up on the looped data using the C1.5i clock.
5	ALL 1s	**All Ones Alarm**. When set, the chip transmits unframed all ones signal on TxA and TxB.
4	ESF/D4	**ESF/D4 Select.** When set, the device is in ESF mode. When clear, device is in D3/D4 mode.
3	ReFR	**Reframe**. If set for at least one frame and then cleared, the chip will begin to search for a new frame position. Only the change from high to low will cause a reframe, not a continuous low level.
2	SLC-96	**SLC-96 Mode Select.** The chip is in SLC-96 mode when this bit is set. This enables input and output of the F_S bit pattern using the same pins as the facility data link in ESF mode. The chip will use the same framing algorithm as D3/D4 mode. The user must insert the valid F_S bits in 2 out of 6 superframes to allow the receiver to find superframe sync, and the transmitter to insert ABCD bits in every 6th frame. The SLC-96 FDL completely replaces the F_S pattern in the outgoing S bit position. Inactive in ESF mode.
1	CRC/ MIMIC	In ESF mode, when set, the chip disregards the CRC calculation during synchronization. When clear, the device will check for a correct CRC before going into synchronization. In D3/D4 mode, when set, the device will synchronize on the first correct S bit pattern detected. When this bit is clear, the device will not synchronize if it has detected more than one candidate for the frame alignment pattern (i.e. a mimic).
0	Maint.	**Maintenance Mode**. When set, the device will declare itself "out of sync" if 4 out of 12 consecutive F_T bits are in error. When clear, the out-of-sync threshold is 2 errors in 4 F_T bits. In this mode, four consecutive bits following an errored F_T bit are examined.

suppression (B8ZS), or jammed bit (bit 7 forced high). No zero code suppression allows the device to interface with systems that have already applied some form of zero code suppression to the data input on DSTi. B8ZS zero code suppression replaces all strings of eight zeros with a known bit pattern and a specific pattern of bipolar violations (see Figure 19.) The receiver monitors the received bit pattern and the bipolar violation pattern and replaces all matching strings with eight zeros.

Loopback Modes

Remote and digital loopback modes are enabled by bits 6 and 7 in Master Control Word 2. These modes can be used for diagnostics to locate the source of a fault condition. Remote loop-around loops data received at $\overline{RxA}$ and $\overline{RxB}$ back out on TxA and TxB, effectively sending the received DS1 data back to the far end unaltered so the transmission line can be tested. The received signal is still monitored with the appropriate received channels on the DS1 side made available in the proper format at DSTo.

Digital loop-around mode diverts the data received at DSTi back out the DSTo pin. Data received on DSTi is, however, still transmitted out via TxA and TxB. This loopback mode can be used to test the near-end interface equipment when there is no transmission line or when there is a suspected failure of the line.

The all-ones transmit alarm (also known as the blue alarm or the keep-alive signal) can be activated in conjunction with the digital loop-around so that the transmission line sends an all ones signal while the normal data is looped back locally.

The LXP302 also has a per-channel loopback mode. See Table 6 and the following section for more information.

Table 3: ESF Frame Pattern

Frame #	FPS	FDL	CRC	Signalling[1]
1		X		
2			CB1	
3		X		
4	0			
5		X		
6			CB2	A
7		X		
8	0			
9		X		
10			CB3	
11		X		
12	1			B
13		X		
14			CB4	
15		X		
16	0			
17		X		
18			CB5	C
19		X		
20	1			
21		X		
22			CB6	
23		X		
24	1			D

[1] These signalling bits valid only if the robbed-bit signalling is active.

Table 4: D3/D4 Framer

Frame #	FT	FS	Signalling[1]
1	1		
2		0	
3	0		
4		0	
5	1		
6		1	A
7	0		
8		1	
9	1		
10		1	
11	0		
12		0	B

[1] These signalling bits valid only if the robbed-bit signalling is active.

Per-Channel Control Features

In addition to the two master control words in CSTi0, there are also 24 Per-Channel Control Words. These control words only affect individual DS0 channels. The correspondence between the channels on CSTi0 and the affected DS0 channel is shown in Figure 18. Each control word has three bits that enable robbed-bit signalling, DS0 channel loopback and DS0 channel inversion. A full description of each of the bits is provided in Table 6.

Transmit Signalling Bits

Control PCM-BUS input number 1 (CSTi1) contains 24 additional per-channel control words. These 24 PCM-BUS channels contain the A, B, C and D signalling bits that the device uses at transmit time. The position of these 24 per-channel control words in the PCM-BUS is shown in Figure 18 and the position of the ABCD signalling bits is shown in Table 7. Even though the device only inserts the signalling information in every sixth DS1 frame, this information must be input every PCM-BUS frame.

Robbed-bit signalling can be disabled for all channels on the DS1 link by bit 1 of Master Control Word 1. It can also be disabled on a per-channel basis by bit 0 in the Per-Channel Control Word 1.

Operating Status Information

Status information regarding the operation of the device is output serially via the Control PCM-BUS output (CSTo). The CSTo serial stream contains Master Status Words 1 and 2, 24 Per Channel Status Words, and a Phase Status Word. The Master Status Words contain all of the information needed to determine the state of the interface and how well it is operating. The information provided includes frame and superframe synchronization, slip, bipolar violation counter, alarms, CRC error count, F_T error count, synchronization pattern mimic and a phase status word. Tables 8 and 9 give a description of each of the bits in Master Status Words 1 and 2, and Table 10 gives a description of the Phase Status Word.

Alarm Detection

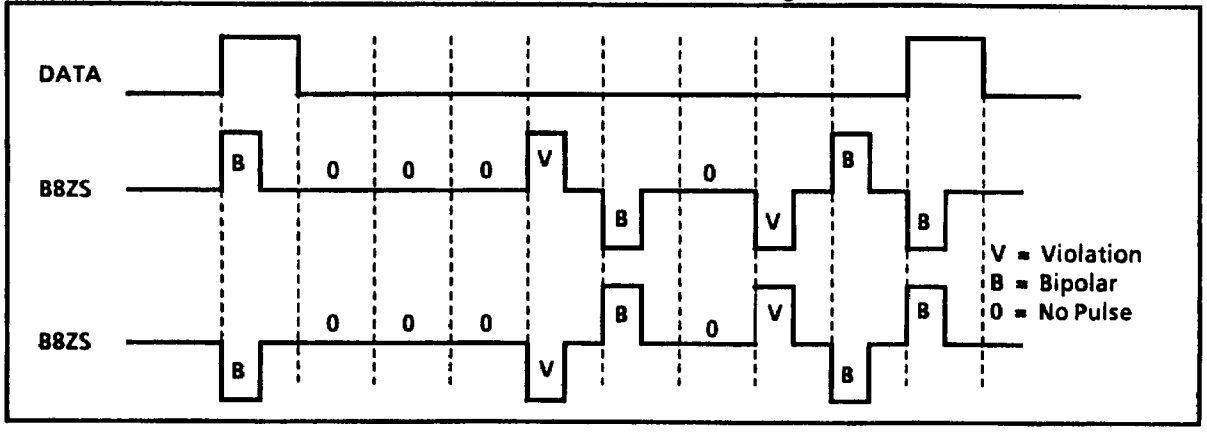
The device detects the yellow alarm for both D3/D4 frame format and ESF format. The D3/D4 yellow alarm will be activated if a '0' is received in bit position 2 of every DS0 channel for 600 msec. It will be released in 200 msec after the contents of the bit change. The alarm is detectable in the presence of errors on the line. The ESF yellow alarm will become active when the device has detected a string of eight 0's, followed by eight 1's in the facility data link. It is not detectable in the presence of errors on the line. This means that the ESF yellow alarm will drop out for relatively short periods of time, so the system will have to integrate the ESF yellow alarm. The blue alarm signal, in Master Status Word 2, will also drop out if there are errors on the line.

Table 5: SLC-96 Framing Pattern

Frame #	F_T	F_S†	Notes	Frame #	F_T	F_S†	Notes
1	1		Resynchronization Data Bits	37	1		X = Concentrator Field Bits
2		0		38		X	
3	0			39	0		
4		0		40		X	
5	1			41	1		
6		0		42		X	
7	0			43	0		
8		1		44		X	
9	1			45	1		
10		1		46		X	
11	0			47	0		S = Spoiler Bits
12		1		48		S	
13	1			49	1		
14		0		50		S	
15	0			51	0		
16		0		52		S	
17	1			53	1		
18		0		54		C	C = Maintenance Field Bits
19	0			55	0		
20		1		56		C	
21	1			57	1		
22		1		58		C	
23	0			59	0		A = Alarm Field Bits
24		1		60		A	
25	1		X = Concentrator Field Bits	61	1		
26		X		62		A	
27	0			63	0		L = Line Switch Field Bits
28		X		64		L	
29	1			65	1		
30		X		66		L	
31	0			67	0		
32		X		68		L	
33	1			69	1		
34		X		70		L	
35	0			71	0		S = Spoiler Bits
36		X		72		S	

†Note: The Fs pattern must be supplied by the user.

Figure 19: B8ZS Output Coding



Mimic Detection

The mimic bit in Master Status Word 1 will be set if, during synchronization, a frame alignment pattern (S-bit pattern) was observed in more than one position, i.e. if more than one candidate for the frame synchronization position was observed. It will be reset when the device resynchronizes. The mimic bit, the terminal framing error bit and the CRC error counter can be used separately or together to decide if the receiver should be forced to reframe.

Bipolar Violation Counter

The Bipolar Violation (BPV) bit in Master Status Word 1 will toggle after 256 violations have been detected in the received signal. It has a maximum refresh time of 96 ms. This means that the bit cannot change state faster than once every 96 ms. For example, if there are 256 violations in 80 ms the BPV bit will not change state until 96 ms. Any more errors in that extra 16 ms are not counted. If there are 256 errors in 200 ms, then the BPV bit will change state after 200 ms. The other two bits of BPV information in Master Status Word 2 are not refreshed in the same manner. They are the next most significant bits in the BPV counter and can change at almost any rate. It is only the terminal count that is updated every 96 ms. This puts an upper limit on the error rate that can be calculated from the BPV information, but this rate (1.7×10^{-3}) is well above any normal operating condition.

DS1/PCM-BUS Phase Difference

An indication of the phase difference between the PCM-BUS and the DS1 frame can be ascertained from the information provided by the eight bit Phase Status Word and the Frame Count bit. Channel three on CSTo contains the Phase Status Word. Bits 7-3 in this word indicate the number of PCM-BUS channels between the PCM-BUS frame pulse and the rising edge of the E8Ko signal. The remaining three bits provide one bit resolution within the channel count indicated by bits 7-3. The frame count bit in Master Status Word 2 is the ninth and most significant bit of the phase status word. It will toggle when the phase status word increments above channel 31, bit 7 or decrements below channel 0, bit 0. The E8Ko signal has a specific relationship with the received DS1 frame. The rising edge of E8Ko occurs during bit 2, channel 17 of the received DS1 frame. The Phase Status Word in conjunction with the frame count bit, can be used to monitor the phase relationship between the received DS1 frame and the local PCM-BUS frame.

Table 6: Per Channel Control Word 1 Input at CSTi0

Bit #	Name	Description
7-3	IC	**Internal Connections**. Must be kept at 0 for normal operation.
2	Polarity	When set, the applicable channel is not inverted on the transmit or the receive side of the device. When clear, all the bits within the applicable channel are inverted both on transmit and receive side.
1	Loop	**Per-Channel Loopback**. When set, the received DS0 channel is replaced with the transmitted DS0 channel. Only one DS0 channel may be looped back in this manner at a time. The transmitted DS0 channel remains unaffected. When clear, the transmit and receive DS0 sections operate normally.
0	Data	**Data Channel Enable**. When set, robbed-bit signalling for the applicable channel is disabled. When clear, every 6th DS1 frame is available for robbed bit signalling. This feature is enabled only if bit 1 in Master Control Word 1 is low.

Table 7: Per Channel Control Word 2 Input at CSTi1

Bit #	Name	Description
7-4	Unused	Keep at 0 for normal operation.
3 2 1-0	A B C,D	These are the 4 signalling bits inserted in the appropriate channels of the DS1 stream being output from the chip when in ESF mode. In D3/D4 modes where there are only two signalling bits, the values of C and D are ignored.

Table 8: Master Status Word 1 (Channel 15, CSTo)

Bit #	Name	Description
7	YLALR	**Yellow Alarm Indication**. This bit is set when the chip is receiving a 0 in bit position 2 of every DS1 channel.
6	MIMIC	This bit is set if the frame search algorithm found more than one possible frame candidate when it went into frame synchronization. Only active in ESF mode.
5	ERR	**Terminal Framing Bit Error**. The state of this bit changes every time the chip detects 4 errors in the F_T portion of the sync bit pattern.
4	ESFYLW	**ESF Yellow Alarm**. This bit is set when the device has observed a sequence of eight ones and eight 0's in the FDL bit positions.
3	$\overline{\text{MFSYNC}}$	**Multiframe Synchronization**. This bit is cleared when D3/D4 multiframe synchronization has been achieved. Applicable only in D3/D4 modes of operation.
2	BPV	**Bipoloar Violation Count.** The state of this bit changes state every time the device counts 256 bipolar violations.
1	SLIP	**Slip Indication**. This bit changes state every time the elastic buffer in the device performs a controlled slip.
0	$\overline{\text{SYN}}$	**Synchronization**. This bit is set when the device has not achieved synchronization. The bit is clear when the device has synchronized to the received DS1 data stream.

Table 9: Master Status Word 2 (Channel 31, CSTo)

Bit #	Name	Description
7	BlAlm	**Blue Alarm.** This bit is set if the receiver has detected two frames of 1's and an out of frame condition. It is reset by any 250 microsecond interval that contains a zero.
6	FrCnt	**Frame Count.** This is the ninth and most significant bit of the "Phase Status Word" (see Table 10). If the phase status word is incrementing, this bit will toggle when the phase reading exceeds channel 31, bit 7. If the phase word is decrementing, then this bit will toggle when the reading goes below channel 0, bit 0.
5	XSt	**External Status.** This bit reflects the state of the external status pin (XSt). The state of the XSt pin is sampled once per frame.
4-3	BPVCnt	**Bipolar Violation Count.** These two bits are from the 8 bit bipolar violation counter. They change state every 128 and every 64 bipolar violations.
2-0	CRCCNT	**CRC Error Count.** These three bits count received CRC errors. The counter will reset to zero when it reaches terminal count. Valid only in ESF mode.

Table 10: Phase Status Word (Channel 3, CSTo)

Bit #	Name	Description
7-3	ChannelCnt	**Channel Count.** These five bits indicate the PCM-BUS channel count between the PCM-BUS frame pulse and the rising edge of E8Ko.
2-0	BitCnt	**Bit Count**. These three bits provide one bit resolution within the channel count described above.

Table 11: Per Channel Status Word Output on CSTo

Bit #	Name	Description
7-4	Unused	Unused Bits. Will be output as 0's.
3 2 1 0	A B C D	These are the four signalling bits as extracted from the received DS1 bit stream. The bits are debounced for 6 to 9 ms if the debounce feature is enabled via bit 7 in Master Control Word 1.

The local 2.048 MHz PCM-BUS clock must be phase-locked to the 1.544 MHz clock extracted from the received data. When the two clocks are not phase-locked, the input data rate on the DS1 side will differ from the output data rate on the PCM-BUS side. If the average input data rate is higher than the average output data rate, the channel count and bit count in the phase status word will be seen to decrease over time, indicating that the E8Ko rising edge, and therefore the DS1 frame boundary, is moving with respect to the PCM-BUS frame pulse. Conversely, a lower average input data rate will result in an increase in the phase reading.

In an application where it is necessary to minimize jitter transfer from the received clock to the local system clock, a phase lock loop with a relatively large time constant can be implemented using information provided by the phase status word. In such a system, the local 2.048 MHz clock is derived from a precision VCO. Frequency corrections are made on the basis of the average trend observed in the phase status word. For example, if the channel count in the phase status word is seen to increase over time, the feedback applied to the VCO is used to decrease the system clock frequency until a reversal in the trend is observed.

The elastic buffer in the LXP302 permits the device to handle eight channels of jitter/wander (see description of elastic buffer in the next section). In order to prevent slips from occurring, the frequency corrections would have to be implemented such that the deviation in the phase status word is limited to eight channels peak to peak. It is possible to use a more sophisticated protocol which would center the elastic buffer and permit more jitter/wander to be handled. For most applications, however, the eight channels of jitter/wander tolerance is acceptable.

Received Signalling Bits

The A, B, C and D signalling bits are output from the device in the 24 Per-Channel Status Words. Their location in the serial stream output at CSTo is shown in Figure 18 and the bit positions are shown in Table 11. The internal debouncing of the signalling bits can be turned on or off by Master Control Word 1. In D3/D4 mode, only the A and B bits are valid. In ESF mode, A, B, C and D bits are valid. Even though the signalling bits are only received once every six frames, the device stores the information so that it is available on the PCM-BUS every frame. The PCM-BUS will always contain the most recent signalling bits. The state of the signalling bits is frozen if synchronization is lost.

Clock and Framing Signals

The LXP302 requires one 2.048 MHz clock (C2i) and an 8 kHz framing signal for the PCM-BUS side. Figure 2 shows the relationship between the two signals. The framing signal is used to delimit individual 32 channel PCM-BUS frames.

The DS1 side requires two clocks – a 1.544 MHz clock used for transmit (C1.5i), and a 1.544 MHz clock extracted from the DS1 line signal and applied at E1.5i pin to clock in the received data.

The C2i and C1.5i clocks must be phase-locked together. There must be 193 clock cycles of C1.5i for every 256 clock cycles of C2i. At the slave end of the link, the C2i and C1.5i must be phase-locked to the extracted E1.5i clock.

The clock applied at E1.5i is internally divided down by 193 and aligned with the DS1 frame. The resulting 8 kHz clock is output at the E8Ko pin. This signal can be used as a reference for phase locking the C2i and C1.5i clocks to the extracted 1.544 MHz clock.

DS1 Line Interface

Transmit Interface

The interface to the DS1 line is made up of two unipolar outputs, TxA and TxB, which can be used to drive a bipolar transmitter circuit. The output signal on TxA and TxB corresponds to the positive and negative bipolar pulses required for the Alternate Mark Inversion signal on the T1 line. The relationship between the signal output at TxA and TxB and the AMI signal is illustrated in Figure 17. For transmission over twisted pair wire, the AMI signal has to be equalized and transformer coupled to the line.

Receiver Interface

The receiver circuitry is made up of three pins – $\overline{RxA}$, $\overline{RxB}$ and RxD. The bipolar alternate mark inversion signal from the DS1 line should be converted into a unipolar split phase format. The resulting signals are clocked into the device at $\overline{RxA}$ and $\overline{RxB}$. The signals are also NANDed together and input at RxD. The signal input at RxD should have a RZ format for proper operation of the violation detection circuitry.

In special applications where the detection of bipolar violations is not required, it is possible to clock NRZ data directly into RxD. In this case, the $\overline{RxA}$ and $\overline{RxB}$ pins should be tied high.

Data is clocked into $\overline{RxA}$, $\overline{RxB}$, and RxD with the falling edge of the E1.5i clock. This clock signal is extracted from the received data. The relationship between the received signals and the extracted clock is shown in Figure 16.

Elastic Buffer

The LXP302 has a two-frame elastic buffer which absorbs jitter in the received DS1 signal. The buffer is also used in the rate conversion between the 1.544 Mbps DS1 rate and the 2.048 Mbps PCM-BUS data rate.

The received data is written into the elastic buffer with the extracted 1.544 MHz clock. The data is read out of the buffer on the PCM-BUS side with the system 2.048 MHz clock. The maximum delay through the buffer is 1.3 PCM-BUS frames (i.e. 42 PCM-BUS channels). The minimum delay required to avoid bus contention in the buffer memory is two PCM-BUS channels.

Under normal operating conditions, the system C2i clock is phase-locked to the extracted E1.5i clock using external circuitry. If the two clocks are not phase-locked, the rate at which the data is written into the device on the DS1 side may differ from the rate at which it is read out on the PCM-BUS side. The buffer circuit will perform a controlled slip if the throughput delay conditions described above are violated. For example, if the data on the DS1 side is being written in at a rate slower than it is being read out on the PCM-BUS side, the delay between the received DS1 write pointer and the PCM-BUS read pointer will begin to decrease over time. When this delay approaches the minimum two-channel threshold, the buffer performs a controlled slip which resets the internal PCM-BUS read pointers so that there is exactly 34 channels delay between the two pointers. This results in some PCM-BUS channels containing information output in the previous frame. Repetition of up to one DS1 frame of information is possible.

Conversely, if the data on the DS1 side is being written into the buffer at a rate faster than that at which it is being read out on the PCM-BUS side, the delay between the DS1 frame and the PCM-BUS frame will increase over time. A controlled slip will be performed when the throughput delay exceeds 42 PCM-BUS channels. This slip will reset the internal PCM-BUS counters so that there is a 10 channel delay between the DS1 write pointer and the PCM-BUS read pointer, resulting in a loss of up to one frame of received DS1 data.

When the device performs a controlled slip, the PCM-BUS address pointers are repositioned so that there is either a 10-channel or a 34-channel delay between the input DS1 frame and the output PCM-BUS frame. Since the buffer performs a controlled slip only if the delay exceeds 42 channels or is fewer than 2 channels, there is an 8-channel hysteresis built into the slip mechanism. The device can, therefore, absorb 8 channels or 32.5µs of jitter in the received channel.

There is no loss of frame sync, multiframe sync or any errors in the signalling bits when the device performs a slip. The information on the FDL pins in ESF or SLC-96 mode will, however, undergo slips at the same time.

Framing Algorithm

Figure 20 is a state diagram of the framing algorithm. The dotted lines show which feature can be switched in and out depending upon the operating mode of the device.

The main feature of the framer is that it performs its function "off line." That is, the framer repositions the receive circuit only when it has detected a valid frame position. When the framer exits maintenance mode, the receive counters remain where they are until the framer has found a new frame position. This means that if the user forces a reframe when the device was really in the right place, there will not be any disturbance in the circuit because the framer has no effect on the receiver until it has found synchronization. The out-of-synchronization criterion can be controlled by bit 0 in Master Control Word 2. This bit changes the out-of-frame conditions for the maintenance state. The out-of-sync threshold can be changed from 2 out of 4 errors in F_T to 4 out of 12 errors in F_T. The average reframe time is 24 ms for ESF mode, and 12 ms for D3/D4 modes.

Figure 21 is a bar graph which shows the probability of achieving frame synchronization at a specific time. The chart shows the results for ESF mode with CRC check and D3/D4 modes of operation. The average reframe time with random data is 24 ms for ESF, and 13 ms for D3/D4 modes. The probability of a reframe time of 35 ms or less is 88% for ESF mode, and 97% for D3/D4 modes. In ESF mode, it is recommended that the CRC check be enabled unless the line has a high error rate. With the CRC check disabled, the average reframe time is greater because the framer must also check for mimics.

Figure 20: Off-Line Framer State Diagram

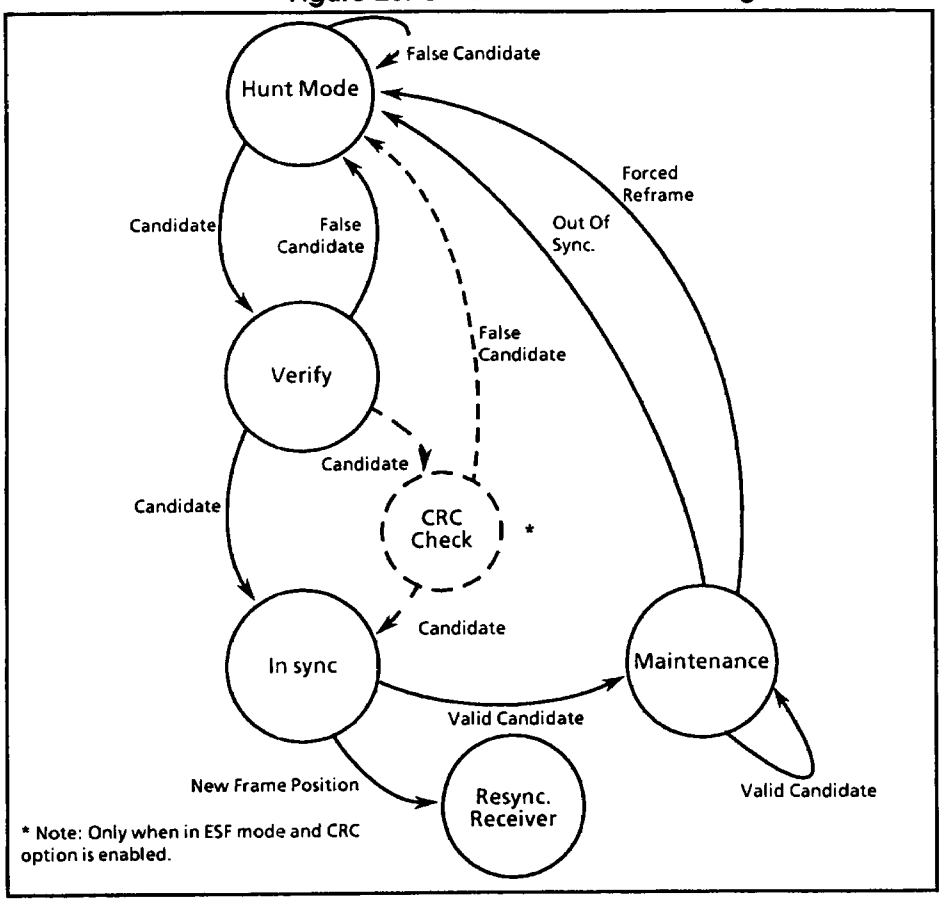
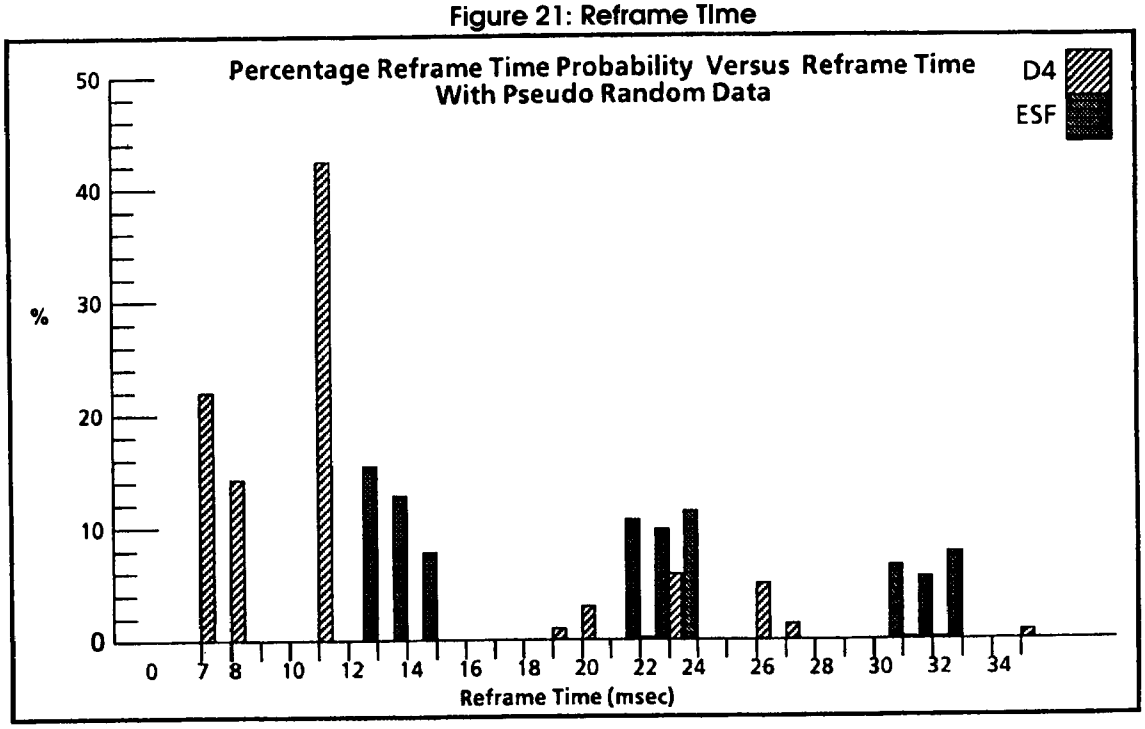


Figure 21: Reframe Time



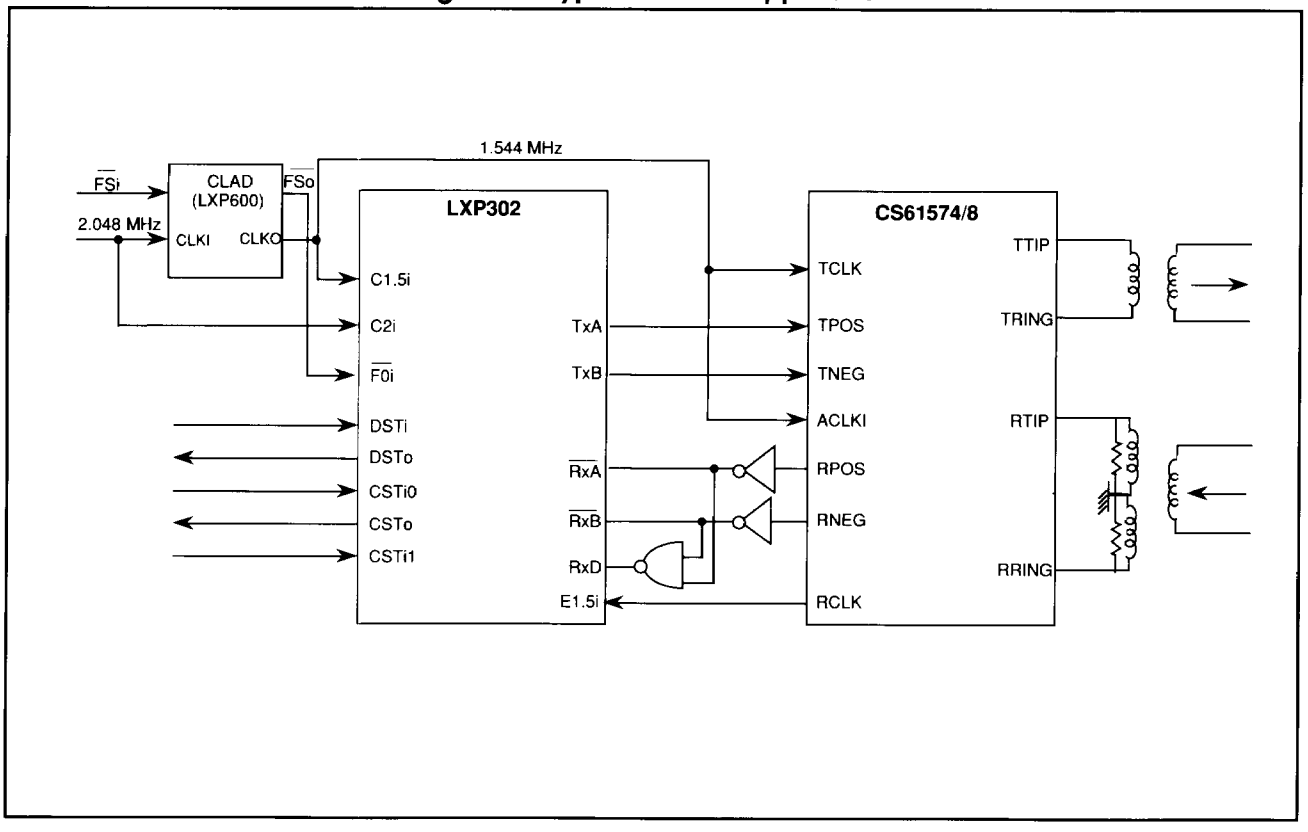
Applications

Figure 22 shows a typical application of the LXP302 framer with a 2.048 MHz system backplane.

The LXP600 (Clock Adapter Device) provides the 1.544 MHz transmit clock locked to the 2.048 MHz system master clock. This clock is also used as the master clock ACLKI for the CS61574/8 line interface device.

Two inverters and a NAND gate are required to interface the recovered data outputs from the CS61574/8 to the $\overline{RxA}$, $\overline{RxB}$ and RxD data inputs.

Figure 22: Typical LXP302 Application



Appendix: Control and Status Register Summary

Master Control Word 1 (Channel 15, CSTi0)

7	6	5	4	3	2	1	0
Debounce	**TSPZCS**	**B8ZS**	**8KHSel**	**XCtl**	**ESFYLW**	**Robbed Bit**	**YLALR**
1 Disabled	1 Disabled	1 B8ZS	1 Enabled	1 Set High	1 Enabled	1 Disabled	1 Enabled
Enabled	0 Enabled	0 Jammed Bit	0 Disabled	0 Cleared	0 Disabled	0 Enabled	0 Disabled

Master Control Word 2 (Channel 31, CSTi0)

RMLOOP	DGLOOP	ALL1's	ESF/D4	Reframe	SLC-96	CRC/MIMIC	Maint.
0 Enabled	0 Enabled	1 Enabled	1 ESF	Device Reframes on High to Low Transition	1 Enabled	See Note 1	1 4/12
1 Disabled	1 Disabled	0 Disabled	0 D3/D4		0 Disabled		0 2/4

Per Channel Control Words (All Channels on CSTi0 Except Channels 3, 7, 11, 15, 19, 23, 27 and 31)

	Polarity	Loop	Data
UNUSED - KEEP AT 0	1 No Inversion	1 Ch. looped back	1 Enabled
	0 Inversion	0 Normal	0 Disabled

Per Channel Control Words (All Channels on CSTi1 Except Channels 3, 7, 11, 15, 19, 23, 27 and 31)

	A	B	C	D.
UNUSED - KEEP AT 0	Txt. Sig. Bit	Txt. Sig. Bit	Txt. Sig. Bit	Txt. Sig. Bit

Master Status Word 1 (Channel 15, CSTo)

YLALR	MIMIC	ERR	ESFYLW	MFSYNC	BPV	SLIP	SYN
1 Detected	1 Detected	F_T Error Count	1 Detected	1 Not Detected	Bipolar Violation Count	Changes State when Slip Performed	1 Out of Sync.
0 Normal	0 Not Detected		0 Not Detected	0 Detected			0 In Sync.

Note 1: In ESF mode:
- 1: CRC calculation ignored during Sync.
- 0: CRC checked for Sync.

In D3/D4 mode:
- 1: Sync. to first correct S bit pattern.
- 0: Will not Sync if Mimic detected.

Appendix: Control and Status Register Summary continued

Master Status Word 2 (Channel 31, CSTo)

7	6	5	4	3	2	1	0
BIAlm 1 Detected 0 Not Detected	**FrCnt**	**XSt** 1 XSt High 0 XSt Low	BIPOLAR VIOLATION COUNT		CRC-ERROR COUNT		

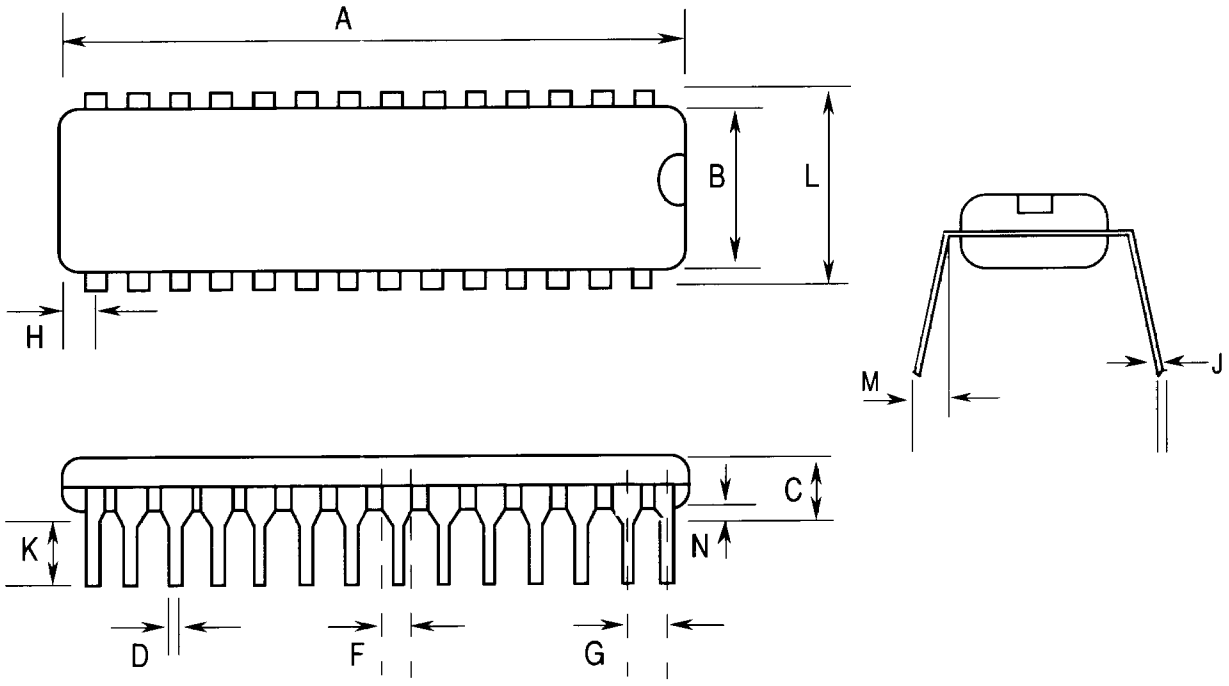
Phase Status Word (Channel 3, CSTo)

CHANNEL COUNT	BIT COUNT

Per Channel Status Word (All Channels on CSTo Except Channels 3, 7, 11, 15, 19, 23, 27, 31)

UNUSED	A Rec'd. Sig. Bit	B Rec'd. Sig. Bit	C Rec'd. Sig. Bit	D. Rec'd. Sig. Bit

Packaging Information



Dual In-Line Ceramic Case

- part number LXP302JC
- commercial temperature range

Dim.	Min	Max
A	—	1.520
B	.480	.593
C	.085	.225
D	.015	.021
F	.028	.070
G	.100 BSC	
H	.010	.080
J	.008	.015
K	.100	.200
L	.600 BSC	
M	0°	15°
N	.015	.040

Dimensions in inches

Dual In-Line Plastic Case

- part number LXP302NC
- commercial temperature range

Dim.	Min	Max
A	—	1.470
B	.535	.560
C	.100	.205
D	.015	.021
F	.028	.070
G	.100 BSC	
H	.010	.100
J	.008	.015
K	.100	.200
L	.600 BSC	
M	0°	15°
N	.015	.040

Dimensions in inches

Notes

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