HD81803

ADPCM Transcoder Conforming to G.721

Description

The HD81803 is a single-chip ADPCM (Adaptive Differential Pulse Code Modulation) Transcoder conforming to the ITU-T Recommendation G.721. It can compress and expand voice data by ADPCM transcoding, and is suitable for high-quality voice recording and playback systems. Applications include ISDN services, voice mail, and private broadcasting.

Converting data from PCM code to ADPCM code reduces the memory needed to store voice data by half the size. Also, since the HD81803 conforms to G.721, it can be used in ISDN line terminal equipment.

The HD81803 can be directly connected to a PCM CODEC, and can convert a 64-kbits/s μ-law or A-law PCM channel to and from a 32-kbits/s ADPCM channel.

Features

- Full conformity with ITU-T Recommendation G.721
- ADPCM transcoding ensures speech data accuracy
- 64-kbits/s channel can be compressed to 32 kbits/s (Half-Duplex)
- Serial or parallel input/output
- Parallel input/output allows digital sequence tests specified by the ITU-T
- Parallel input/output width can be selected as 4, 8, or 16 bits (suitable for a 125-, 250-, or 500-μs microprocessor I/O cycle)
- Through functions are available to input/output specific waveforms without ADPCM transcoding
- A-law or μ-law PCM can be input/output
- Direct connection to a PCM CODEC is possible
- Built-in interface for 8- and 16-bit microprocessors
- Operating mode can be controlled by microprocessor
- +5 V power supply

Data Flow Format

	PCM Data	ADPCM Data
Encoder	Serial input	Serial or parallel output
Decoder	Serial or parallel output	Serial or parallel input

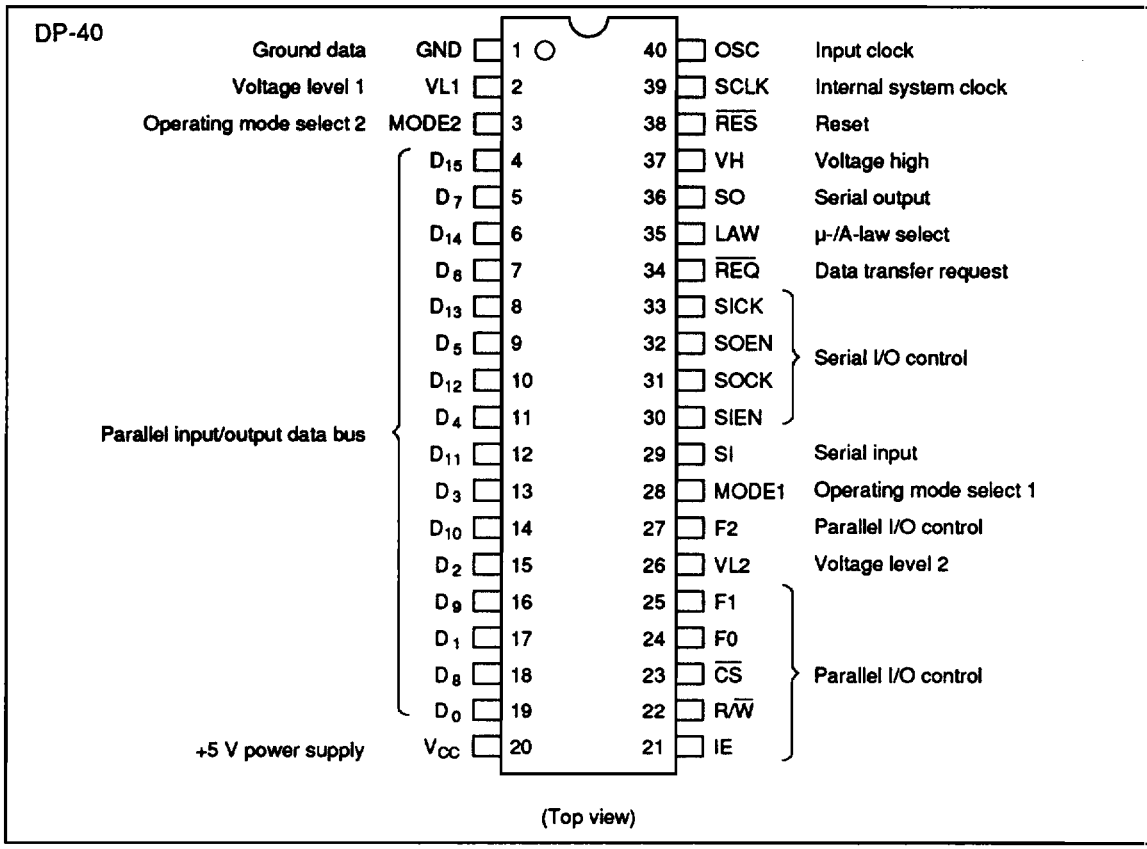
(Through and test functions are not included.)

Specifications

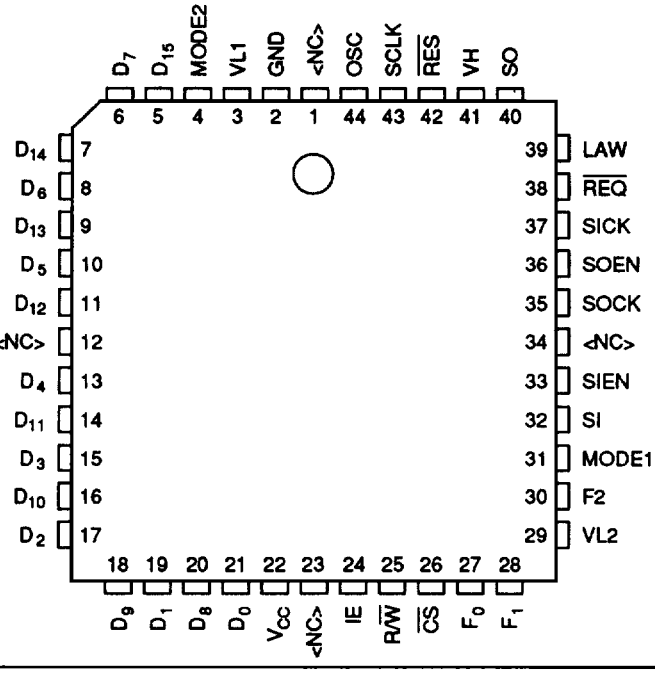
Item	Description
Coding process	ITU-T recommendation G.721 ADPCM
Sampling frequency	8 kHz
Code length	4 bits
Data rate	32 kbits/sec
Serial interface (PCM CODEC interface)	1. μ-law PCM CODEC (ex. HD44238P/HD44278P)
	2. A-law PCM CODEC (ex. HD44237P/HD44277P)
Parallel interface (microprocessor interface)	1. 8-bit microprocessor
	2. 16-bit microprocessor
Supplementary functions	1. Serial communication
	2. High-quality waveform input/output (through function)
	3. Digital sequence test (ITU-T Recommendation G.721)
Fabrication process	CMOS 1.3 μm
Power dissipation	150 mW (typ)
Power supply voltage	+5 V
Package	40-pin plastic DIP, 44-pin PLCC

Pin Arrangement

DP-40



CP-44



Absolute Maximum Ratings

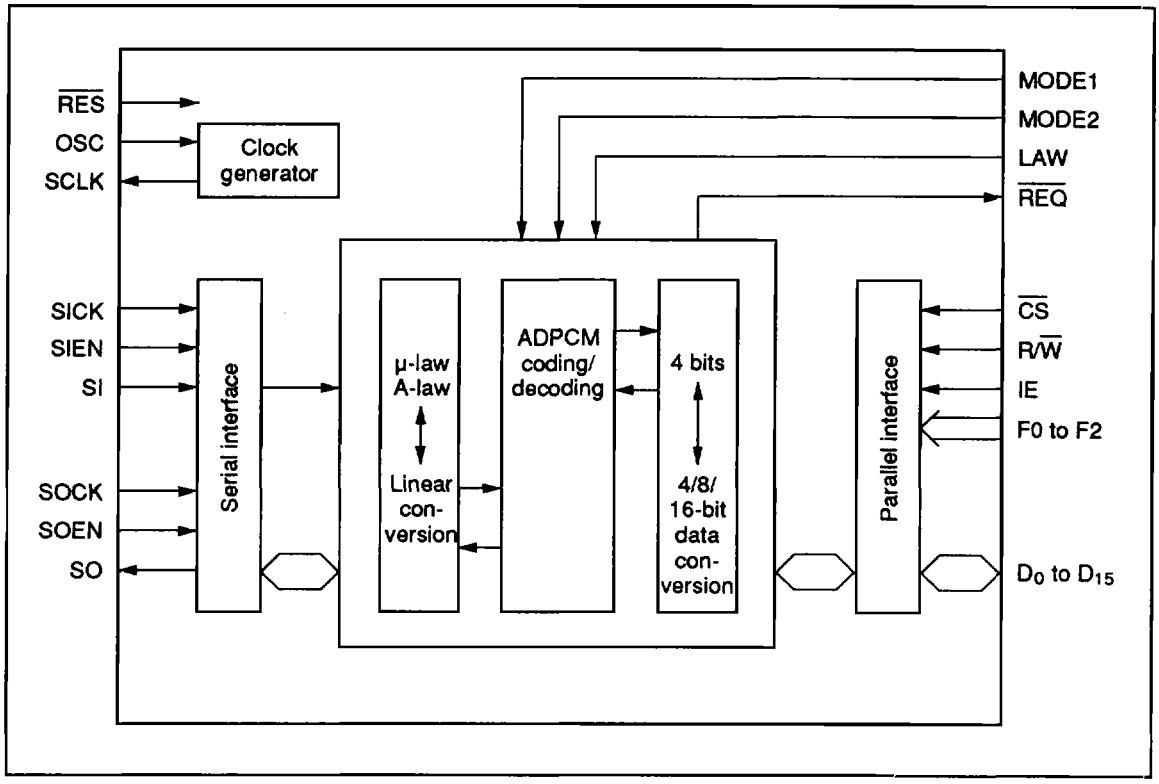
Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	–0.3 to +7.0	V
Input votlage	Vin	–0.3 to V_{CC} +0.3	V
Operating temperature	Topr	–20 to +75	°C
Storage temperature	Tstg	–55 to +125	°C

Electrical Characteristics

DC Characteristics (V_{CC} = 5.0 V ±5%, GND = 0 V, Ta = –20 to +75°C)

Item	Applied pin	Symbol	Min	Typ	Max	Unit	Test conditions
Input high level voltage	OSC	V_{IH}	2.4	—	V_{CC} + 0.3	V	
	IE, SICK, SOCK	V_{IH}	2.4	—	V_{CC} + 0.3		
	$\overline{RES}$	V_{IH}	V_{CC} × 0.7	—	V_{CC} + 0.3		
	Other inputs	V_{IH}	2.2	—	V_{CC} + 0.3		
Input low level voltage	OSC	V_{IL}	–0.3	—	0.4	V	
	IE, SICK, SOCK	V_{IL}	–0.3	—	0.4		
	$\overline{RES}$	V_{IL}	–0.3	—	0.4		
	Other inputs	V_{IL}	–0.3	—	0.4		
Input leakage current	IE, R/$\overline{W}$, $\overline{CS}$, F0 to F2 SI, SIEN, SOCK, SOEN, SICK, $\overline{RES}$, OSC	$\lvert I_{IL} \rvert$	—	—	10	µA	Vin = 0.4 to 2.4 V
Three-state current (off-state)	D0 to D15, SO	$\lvert I_{TS} \rvert$	—	—	10	µA	Vin = 0.4 to 2.4 V
Open-drain current (off state)	$\overline{REQ}$, MODE1, MODE2, LAW	$\lvert I_{LOH} \rvert$	—	—	10	µA	Vin = 0.4 to 2.4 V
Output high level voltage	D0 to D15, SO	V_{OH}	2.4	—	—	V	$-I_{OH}$ = 400 µA
Output low level voltage	Do to D15, SO, $\overline{REQ}$	V_{OL}	—	—	0.8	V	I_{OL} = 1.6 mA
Input capacitance	All inputs	Cin	—	—	12.5	pF	Vin = 0 V, f = 1 MHz, Ta = 25°C
Consumption current		I_{CC}	—	30	100	mA	Output no-load

Block Diagram



Sample of System Composition