THREE CHANNEL, DS3 ATM UNI/CLEAR-CHANNEL FRAMER IC

DECEMBER 2000 *REV. P1.0.1*

GENERAL DESCRIPTION

The XRT72L73 Three Channel DS3 ATM User Network Interface (UNI)/Clear Channel Framer is designed to function as either a DS3 ATM UNI or Clear channel framer. For ATM UNI applications, this device provides the ATM Physical Layer (Physical Medium Dependent and Transmission Convergence sublayers) interface for both the public and private networks at DS3 rates. For Clear-Channel framer applications, this device supports the transmission and reception of "user data" via the DS3 payload bits.

The XRT72L73 incorporates Receive, Transmit, Microprocessor Interface, Performance Monitor, Test and Diagnostic and Line Interface Unit Scan Drive sections.

APPLICATIONS

- Private User Network Interfaces
- ATM Switches
- ATM Concentrators
- DSLAM Equipment
- DS3 Frame Relay Equipment

FEATURES

- Compliant with UTOPIA Level 1 and 2 with 8 or 16 Bit Interface Specification and supports UTOPIA Bus speeds of up to 50 MHz
- Contains on-chip 16 cell FIFO in both the Transmit (TxFIFO) and Receive Directions (RxFIFO)
- Contains on-chip 54 byte Transmit OAM Cell buffer and a 108 byte Receive OAM cell buffer, for transmission, reception and processing of OAM cells.
- Supports PLCP or ATM Direct Mapping modes
- Supports M13 and C-Bit Parity Framing Formats
- Supports DS3 Clear Channel Framing Applications
- Includes PRBS Generator and Receiver
- Supports Local, Remote-Line, Cell, and PLCP Loop-backs
- Interfaces to 8 or 16 Bit wide Motorola and Intel µPs
- Low power 3.3V, 5V input tolerant, CMOS
- 352 pin PBGA Package
- 1 and 3 channel versions also available

FIGURE 1. XRT72L73 SIMPLIFIED BLOCK DIAGRAM WITH SYSTEM INTERFACES

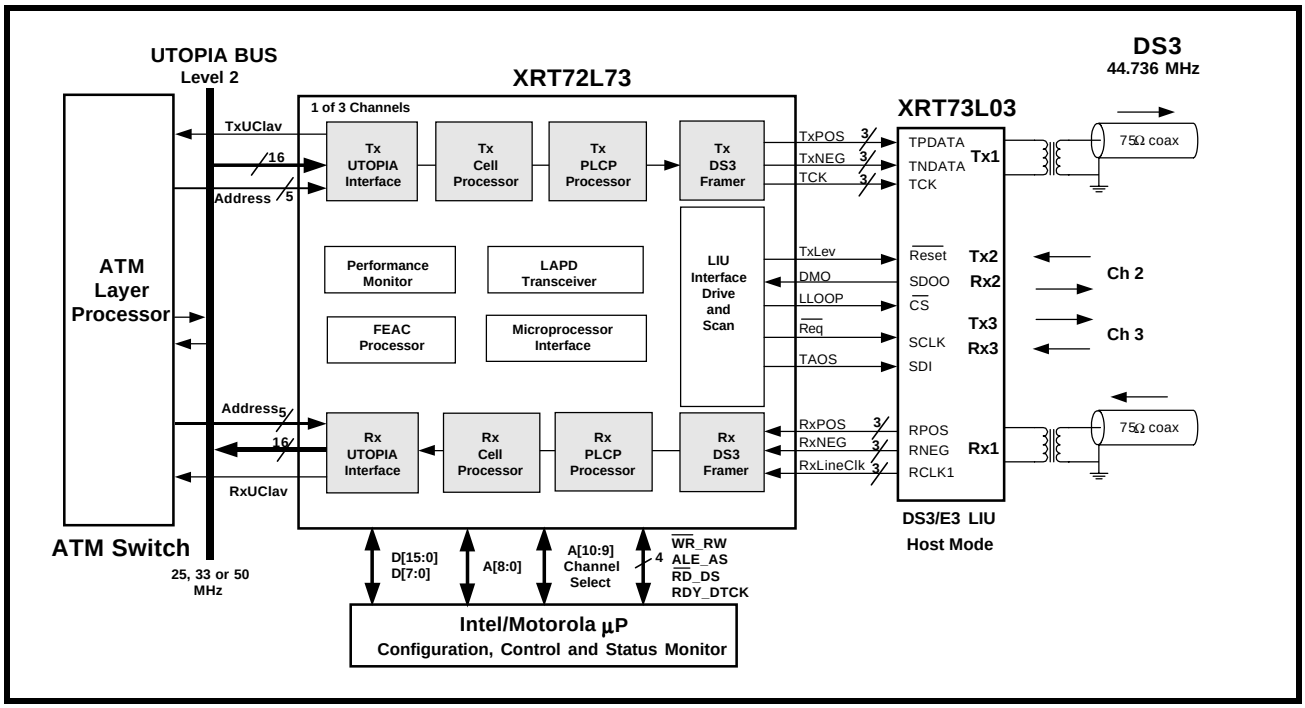
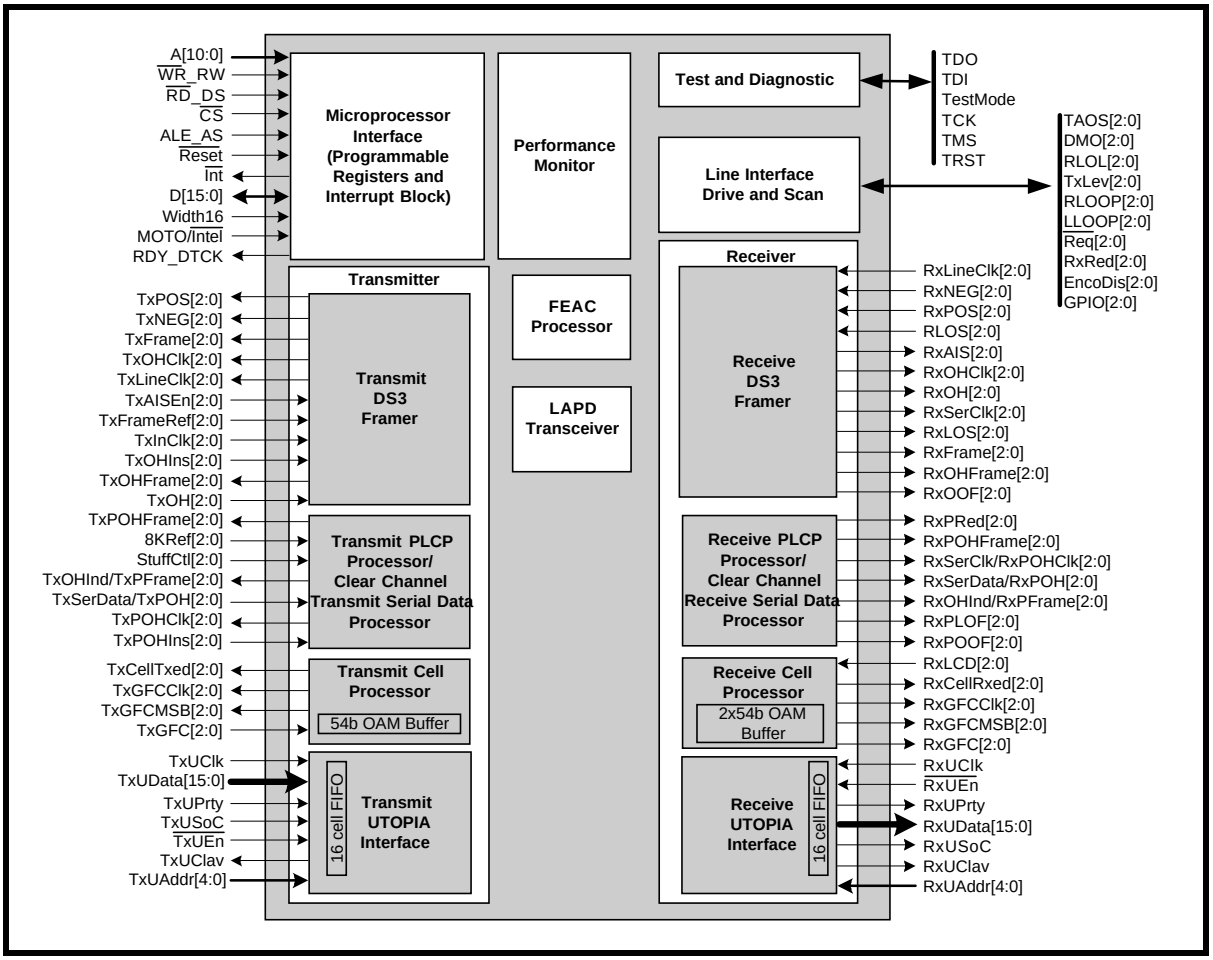


FIGURE 2. BLOCK DIAGRAM OF THE XRT72L73 DS3 UNI IC



SYSTEM/FUNCTIONAL DESCRIPTION

The XRT72L73 has 3 identical channels (0, 1, 2), the descriptions below apply to each channel.

FUNCTIONAL DESCRIPTION

The XRT72L73 DS3 ATM UNI/Framer IC can be configured to operate in either the "ATM UNI" or in the "Clear-Channel-Framer" Mode.

A brief listing of the features and description for each of these operating modes is presented below.

THE ATM UNI MODE OF OPERATION

When the XRT72L73 UNI/Framer has been configured to operate in the "ATM UNI" Mode, it can functionally be subdivided into 6 different sections, as shown in Figure 2 .

- Receive Section
- Transmit Section
- Microprocessor Interface Section
- Performance Monitor Section
- Test and Diagnostic Section
- Line Interface Unit Scan Drive Section

The features of each of these functional sections are briefly outlined below.

THE RECEIVE SECTION

The purpose of the Receive Section of the XRT72L73 DS3 ATM UNI is to allow a local ATM Layer (or ATM Adaptation Layer) processor to receive ATM cell data from a remote piece of equipment via a public or leased DS3 transport medium.

The Receive Section of the XRT72L73 DS3 UNI consists of the following functional blocks.

- Receive DS3 Framer Block
- Receive PLCP (Physical Layer Convergence Protocol) Processor Block
- Receive Cell Processor Block
- Receive UTOPIA Interface Block

Each of these functional blocks, within the Receive Section of the UNI Framer will do the following:

The Rx DS3 Framer Block

- Capable of receiving data, from the LIU IC, in either the "Single-Rail" or "Dual-Rail" mode.
- Capable of "sampling" the "inbound" DS3 data (at the "RxPOS" and "RxNEG" input pins) upon either the rising or falling edge of the "RxLineClk" signal.
- The Receive DS3 Framer will synchronize to the incoming DS3 data stream and remove or process the DS3 Framing/Overhead Bits. This procedure will result in either extracting PLCP frame data or "Direct-Mapped" ATM Cell data, from the payload portion of the incoming DS3 data stream.
- The Receive DS3 Framer can be used to receive FEAC (Far End Alarm & Control) messages via an on-chip FEAC Transceiver.
- The Receive DS3 Framer includes an on-chip LAPD Receiver along with 88 bytes of on-chip RAM that can receive incoming path maintenance data link messages from the Remote Terminal Equipment.
- Detects and generates interrupts upon "Detection of P and CP-bit Errors", "Change of State in LOS, AIS, OOF and FERF", "Receipt of New LAPD (PMDL) Message", "Validation and Removal of FEAC Message".

NOTE: *The Receive DS3 Framer supports both M13 and C-bit Parity Frame Formats.*

The Rx PLCP Processor Block

- The Receive PLCP Processor will identify the frame boundary of each incoming PLCP frame, extract and process the overhead bytes of these PLCP frames (applies only if the UNI is operating in the PLCP Mode). The Receive PLCP Processor will also perform some error checking on the incoming PLCP frames. The Receive PLCP Processor will inform the Remote Terminal Equipment of the results of this error-checking by internally routing these results to the "Near-End" Transmit PLCP Processor, for transmission back out to the RemoteTerminal Equipment.

The Rx Cell Processor Block

- The Receive Cell Processor will perform the following functions:
  - Cell Delineation
  - HEC Byte Verification of incoming cells (optional)
  - Cell-payload de-scrambling (optional)
  - Idle cell detection and removal (optional)
  - User and OAM Cell Filtering (optional)
  - OAM Cell Processing (optional)
- The UNI provides 108 bytes of on-chip RAM that allows for the reception and processing of selected OAM cells.

- The Receive Cell Processor block will also verify the CRC-10 value within all received OAM cells, per ITU-T I.610.
- Detects and generates interrupts upon “Detection of HEC Byte errors”, “Change in LCD (Loss of Cell Delineation) condition” and “Receipt of OAM Cell”.

The Receive UTOPIA Interface Block

- Provides a “UTOPIA Level -2” compliant interface to either the ATM or the ATM Adaptation Layer.
- Can be configured to operate in either the “Single-PHY” or “Multi-PHY” Modes.
- Supports either “Cell-Level” or “Octet-Level” Handshaking.
- Receive UTOPIA Data Bus can be configured to be either 8 or 16-bits wide.
- The RxFIFO, within the Receive UTOPIA Interface block will temporarily hold any ATM cells that pass through the Receive Cell Processor, where they can be read out by the ATM Layer processor, over the Receive UTOPIA Data Bus.
- The size of the “RxFIFO” is 16 cells.
- Supports read operations (from the ATM Layer device) at rates upto 50MHz.
- Detects and generates interrupts upon “Detection of RUNT cells” and “Overrun of RxFIFO”.

THE TRANSMIT SECTION

The purpose of the Transmit section of the XRT72L73 DS3 ATM UNI is to allow a local ATM Layer (or ATM Adaptation Layer) processor to transmit ATM Cell data to a remote piece of equipment via a public or leased DS3 transport medium.

The Transmit Section of the XRT72L73 DS3 UNI consists of the following functional blocks.

- Transmit UTOPIA Interface Block
- Transmit Cell Processor Block
- Transmit PLCP Processor Block
- Transmit DS3 Framer Block

Each of these functional blocks, within the Transmit Section (of the UNI/Framer) will do the following:

Transmit UTOPIA Interface Block

- Can be configured to operate in either the “Single-PHY” or Multi-PHY” Mode.
- Supports either the “Cell-Level” or “Octet-Level” Handshaking Mode.
- Transmit UTOPIA Data Bus can be configured to be either 8 or 16-bits wide.
- Allow the ATM Layer processor to write ATM cells into the Transmit FIFO (within the Transmit UTOPIA Interface block) via a standard UTOPIA Level 2 interface.
- The size of the “TxFIFO” is 16 cells. However, the operating depth can be configured to be 4, 8, 12 or 16 cells.
- Supports write operations (from the ATM Layer device) at rates upto 50MHz.
- Detects and generates interrupts upon “Detection of Parity Errors”, “Detection of RUNT cells” and “Overrun of TxFIFO”.

Transmit Cell Processor Block

- The Transmit Cell Processor will read in ATM cells from the Transmit FIFO (if available) for further processing.
- If no cell is available within the Transmit FIFO, then the Transmit Cell Processor will automatically generate an Idle cell. The UNI is equipped with on-chip registers to allow for the generation of customized Idle cells.
- The UNI provides 54 bytes of on-chip RAM that allows for the generation and transmission of “user-specified” OAM cells. The Transmit Cell Processor will generate and transmit these OAM cells upon software command.
- The Transmit Cell Processor block will also compute and insert a CRC-10 value into each “outbound” OAM cell, per ITU-T I.610.
- The Transmit Cell Processor will (optionally) scramble the Cell Payload bytes and (optionally) compute and insert the HEC (Header Error Check) byte. This HEC byte will be inserted into the fifth octet of each cell prior to being transferred to the Transmit PLCP Processor (or the Transmit DS3 Framer).

Transmit PLCP Processor Block

- The Transmit PLCP Processor will pack 12 ATM cells into each PLCP frame and automatically determine the nibble-stuffing option of the current PLCP frame. These PLCP frames will also include an overhead byte that reflect BIP-8 (Bit Interleaved Parity) calculation results, a byte that reflects the current stuffing option status of the current PLCP frame, Path Overhead and Identifier bytes, and diagnostic-related bytes reflecting any detected BIP-8 errors and alarm conditions detected in the Receive section of the UNI chip.

Transmit DS3 Framer Block

- These PLCP frames (or "Direct Mapped" ATM cells) will be inserted into the payload of an outgoing DS3 frame, for transmission to the "Remote" Terminal, by the Transmit DS3 Framer.
- The Transmit DS3 Framer will transmit FEAC (Far End Alarm & Control) messages to the Remote Terminal Equipment via an on-chip FEAC Transceiver.
- Additionally, the Transmit DS3 Framer can transmit path maintenance data link messages to the Remote Terminal Equipment via the on-chip LAPD Transmitter.
- Generates interrupts upon "Completion of Transmission of LAPD and FEAC" Messages.

Note: The Transmit DS3 Framer will support either M13 or C-bit Parity Framing Formats.

CLEAR-CHANNEL-FRAMING MODE OF OPERATION

When the XRT72L73 has been configured to operate in the "Clear-Channel Framer" mode, it can be functionally subdivided into 6 different sections.

- Receive Section
- Transmit Section
- Microprocessor Interface Section
- Performance Monitor Section
- Test and Diagnostic Section
- Line Interface Unit Scan/Drive Section.

The features of each of the "Receive" and "Transmit" Section (for Clear-Channel Framer applications) are listed below.

THE RECEIVE SECTION

The purpose of the Receive Section of the XRT72L73 Clear-Channel DS3 Framer is to allow a given Terminal to receive data from a remote terminal, which is being transported over a DS3 data stream.

The Receive Section of the XRT72L73 Clear-Channel DS3 Framer IC consists of the following functional blocks.

- Receive DS3 Framer block
- Receive Overhead Data Output Interface block
- Receive Payload Data Output Interface block

It should be noted that the "Receive DS3 Framer" block is also active, when the XRT72L73 has been configured to operate in the "ATM UNI" Mode.

Each of these functional blocks, within the Receive Section of the Framer will do the following.

- The Receive DS3 Framer block will synchronize to the incoming DS3 data stream. All "inbound" DS3 data will be routed to the "Receive Payload Data Output Interface" block. All overhead bits (which are extracted from each "inbound" DS3 frame) will be routed to the "Receive Overhead Data Output Interface" block.
- The Receive DS3 Framer block can also be used to receive FEAC (Far-End-Alarm & Control) messages and PMDL (Path Maintenance Data Link) messages via the "on-chip" Receive HDLC Controller block.
- The Receive Overhead Output Interface block outputs all overhead bits, which have been received via the "inbound" DS3 data stream. The purpose of the "Receive Overhead Output Interface" block is to permit external circuitry (within the local terminal equipment) to have access to these overhead bits, for additional processing.
- The Receive Payload Data Output Interface block outputs all data bits which have been received via the XRT72L73 device, to the local terminal equipment. Since the "Receive Payload Data Output Interface" block outputs both "payload" and "overhead" data bits, to the local terminal equipment; the "Receive Payload Data Output Interface" block also includes an "Overhead Indicator" output pin. This output pin pulses "High" whenever an overhead bit is being output via the "Receive Payload Data Output Interface" block.

THE TRANSMIT SECTION

The purpose of the Transmit Section of the XRT72L73 Clear-Channel DS3 Framer is to allow a local terminal to transmit data to a remote terminal equipment, via a DS3 transport medium.

The Transmit Section of the XRT72L73 Clear-Channel DS3 Framer consists of the following functional blocks.

- Transmit Payload Data Input Interface block
- Transmit Overhead Data Input Interface block
- Transmit DS3 Framer block

It should be noted that the "Transmit DS3 Framer" block is also active, whenever the XRT72L73 has been configured to operate in the "ATM UNI" Mode.

The Transmit Section of the Clear-Channel DS3 Framer will:

- Accept all "user" data, (which is required to be transported to the Remote Terminal Equipment via

a DS3 data stream) via the “Transmit Payload Data Input Interface block.

- Optionally accepts and insert overhead bits (into the “outbound” DS3 data-stream) via the “Transmit Overhead Input Interface block.
- The Transmit DS3 Framer block will accept payload data (from the Transmit Payload Data Input Interface block) and overhead data (from the Transmit Overhead Data Input Interface block) and will create a DS3 data stream. If no overhead data is inserted via the “Transmit Overhead Data Input interface” block, then the “Transmit DS3 Framer” block will insert its own values for the overhead bits.
- The Transmit DS3 Framer block will transmit FEAC (Far-End-Alarm & Control) messages to the remote terminal equipment via an “on-chip” FEAC Transmitter.
- The Transmit DS3 Framer block will also transmit PMDL (Path Maintenance Data Link) Messages to the remote terminal equipment via an “on-chip” LAPD Transmitter.

THE MICROPROCESSOR INTERFACE SECTION

The Microprocessor Interface Section allows a user (or a local “housekeeping” processor) to do the following:

- To configure the UNI/Framer IC into a wide variety of operating modes; by writing data into any one of a large number of “read/write” registers.
- To monitor many aspects of the UNI/Framer’s performance by reading data from any one of a large number of “read/write” and “read-only” registers.
- To run in a “polling” or “interrupt-driven” environment. The UNI/Framer IC contains an extensive interrupt structure consisting of a wide range of interrupt enable and interrupt status registers.
- To command the UNI/Framer IC to transmit OAM cells, FEAC messages and/or LAPD Messages frames, upon software command.
- To read in and process received OAM cells, FEAC messages and/or Path Maintenance Data Link Messages from the UNI/Framer IC.
- The Microprocessor Interface allows the user to interface the XRT72L73 DS3 UNI/Framer to either an Intel type or Motorola type processor. Additionally, the Microprocessor Interface can be configured to operate over an 8-bit or 16-bit data bus.
- The Microprocessor Interface section includes a “Loss of Clock Signal” protection feature that automatically completes (or terminates) a “Read/Write” operation, should a “Loss of Clock Signal” event occur.

PERFORMANCE MONITOR SECTION

The Performance Monitor Section of the XRT72L73 DS3 UNI/Framer consists of a large number of “Reset-upon-Read” and “Read-Only” registers that contains cumulative and “one-second” statistics that reflect the performance/health of the UNI/Framer chip/system. These cumulative and “one-second” statistics are kept on the following parameters.

- Number of Line Code Violation events detected by the Receive DS3 Framer
- Number of Framing Bit (F- and M-bit) errors detected by the Receive DS3 Framer
- Number of P-bit Errors detected by the Receive DS3 Framer
- Number of CP-bit Errors detected by the Receive DS3 Framer.
- Number of FEBE Events detected by the Receive DS3 Framer
- Cumulative number of BIP-8 errors, detected by the Receive PLCP Processor
- Number of PLCP framing errors, detected by the Receive PLCP Processor
- Cumulative sum of the FEBE value, in the incoming G1 bytes (within each PLCP frame), received by the Receive PLCP Processor
- Number of Single-bit HEC byte Errors detected
- Number of Multi-bit HEC byte Errors detected
- Number of Received Idle Cells
- Number of Received Valid (User and OAM) cells discarded
- Number of Discarded Cells
- Number of Transmitted Idle Cells
- Number of Transmitted Valid Cells

TEST AND DIAGNOSTIC SECTION

The Test and Diagnostic Section allows the user to perform a series of tests in order to verify proper functionality of the UNI/Framer chip and/or the user’s system. The “Test and Diagnostic” section provides the UNI IC with the following capabilities.

- Allows the UNI/Framer to operate in the Line, Cell, and PLCP Loop-back Modes.

FOR ATM UNI APPLICATIONS

- Contains an internal Test Cell Generator and an internal Test Cell Receiver. The Test Cell Generator will generate Test Cells with “user-defined” header byte patterns. The Test Cell Generator will also fill the payload portion of these test cells with bytes from an on-chip PRBS generator.

- The Test Cell Generator can generate test cells in "One Shot" Mode (e.g., a burst of 1024 test cells) or in "Continuous" Mode (e.g., a continuous stream of test cells).
- The Test Cell Receiver will identify and collect the Test Cells for further analyses, based upon the "user-defined" header byte patterns. Additionally, the Test Cell Receiver will report the occurrence of any errors by incrementing an on-chip register.

FOR CLEAR-CHANNEL FRAMING APPLICATIONS

- Contains an internal PRBS pattern generator and receiver. The PRBS pattern generator will generate and insert a PRBS pattern into the DS3 payload bits.
- The PRBS receiver will receive these DS3 frames, and will attempt to acquire "PRBS Lock" with this DS3 frame data. Additionally, the PRBS Receiver will report the occurrence of any errors by incrementing an on-chip register.

LINE INTERFACE DRIVE AND SCAN SECTION

The Line Interface Drive and Scan Section allows the user to monitor and control many aspects of the XRT73L04 E3/DS3/STS-1 Line Interface Unit, via on-chip registers, within the UNI IC. This feature eliminates the need for glue logic to interface the XRT72L73 DS3 UNI/Framer to the XRT73L04 DS3 Line Interface Unit IC.

- The On-Chip Line Interface Drive register allows the user to control the state of 6 output pins. The function of these output pins, when asserted, are tabulated below.

CLEAR CHANNEL MODE OPERATION

Signal Name	Function of Output Pin
$\overline{\text{Req}}$	**Receive Equalizer By-Pass:** "1" configures the XRT73L04 to shut off its internal Receive Equalizer. "0" configures the XRT73L04 to enable its internal Receive Equalizer.
TAOS	**Transmit "All Ones" Pattern.** "1" configures the XRT73L04 LIU IC to overwrite the DS3 data that is output via the TxPOS and TxNEG outputs, and transmit an "All Ones" pattern onto the line. "0" configures the XRT73L04 LIU IC to transmit data, as is applied to it via the TPDATA and TNDATA input pins.
EncoDis	**B3ZS Encoder Disable/Enable Select.** "1" disables the B3ZS Encoder, within the XRT73L04. "0" enables the B3ZS Decoder within the XRT73L04.
TxLev	**Transmit Output Signal Line Build Out Select.** Setting this bit-field to "1" disables the Transmit Line Build Out circuitry within the XRT73L04. In this case, the XRT73L04 will generate an "unshaped" square wave signal out onto the line (via the TTIP and TRING output pins). *Note: In order to configure the XRT73L04 to generate a line signal that complies with the Transmit Output Pulse Template Requirements (per Bellcore GR-499-CORE), this setting is advised if the cable length between the Transmit Output of the XRT73L04 and the DSX-3 Cross-Connect is greater than 225 feet.* Setting this bit-field to "0" enables the Transmit Line Build Out circuitry within the XRT73L04. In this case, the XRT73L04 will generate a "shaped" square wave out onto the line (via the TTIP and TRING output pins). *Note: In order to configure the XRT73L04 to generate a line signal that complies with the Transmit Output Pulse Template Requirements (per Bellcore GR-499-CORE), this setting is advised if the cable length between the Transmit Output of the XRT73L04 and the DSX-3 Cross-Connect is less than 225 feet.*

Signal Name	Function of Output Pin
RLOOP	**Remote Loop-Back Mode Select:** This bit-field, along with LLOOP can be used to configure the XRT73L04 into one of four different Loop-Back modes. Setting RLOOP to “1” (with LLOOP = 0) configures the XRT73L04 to operate in the Remote Loop-Back Mode. Setting RLOOP to “1” (with LLOOP = 1) configures the XRT73L04 to operate in the “Digital Local Loop-Back” Mode. Setting RLOOP to “0” (with LLOOP = 1) configures the XRT73L04 to operate in the “Analog Local Loop-Back” Mode. Setting RLOOP to “0” (with LLOOP = 0) configures the XRT73L04 to operate in the “Normal” (No-Loop-Back) Mode.
LLOOP	**Local Loop-Back Mode Select:** This bit-field along with RLOOP can be used to configure the XRT73L04 into one of four different Loop-Back modes. Setting LLOOP to “1” (with RLOOP = 0) configures the XRT73L04 to operate in the “Analog Local Loop-Back” Mode. Setting LLOOP to “1” (with RLOOP = 1) configures the XRT73L04 to operate in the “Digital Local Loop-Back” Mode. Setting LLOOP to “0” (with RLOOP = 0) configures the XRT73L04 to operate in the “Normal” (No-Loop-Back) Mode. Setting LLOOP to “0” (with RLOOP = 1) configures the XRT73L04 to operate in the “Remote Loop-Back” Mode.

- The On-Chip Line Interface Scan Register allows the user to monitor the state of 3 input pins. The function of these input pins, when asserted, are tabulated below.

Signal Name	Function of Input Pin if asserted
DMO	Indicates that the "Drive Monitor" circuitry within the XRT73L03 has not detected any bipolar signals within the last 128 ± 32 bit periods.
RLOL	Indicates that the "Clock Recovery" circuit, within the XRT73L03 has lost "lock" with the incoming DS3 line signal.
RLOS	Indicates that the XRT73L03 is declaring an LOS (Loss of Signal) Condition.

FEATURES

TRANSMIT AND RECEIVE SECTIONS

UTOPIA Interface Blocks

- Compliant with UTOPIA Level 2 Interface Specification (e.g., supports Single-PHY or Multi-PHY operation).
- 8-bit or 16-bit wide UTOPIA Data Bus operation in the Transmit and Receive Directions.
- The UTOPIA Data Bus runs at clock rates of 25 MHz, 33 MHz and 50 MHz
- Supports both Octet-Level and Cell-Level Handshaking between the UNI and the ATM Layer processor.
- The Transmit UTOPIA Interface block performs parity checking of ATM cell data that is written into it, by the ATM Layer processor. Will optionally discard errored cells.
- Contains on-chip 16 cell FIFO in the Transmit Direction (TxFIFO)
- The TxFIFO can be configured to operate with depths of 4, 8, 12 or 16 cells
- Contains on-chip 16 cell FIFO in the Receive Direction (RxFIFO)

TRANSMIT CELL PROCESSOR BLOCK

- Optionally computes and inserts HEC byte into all cells (user, OAM and Idle).
- Optionally scrambles the payload of each cell.
- Idle cells are automatically generated when no user cells are available in the TxFIFO.
- UNI contains on-chip registers that support the generation/transmission of default or custom Idle cells.
- UNI contains the on-chip "Transmit OAM Cell" buffer (54 bytes) that allows the user to write in and store the contents of OAM cells, in preparation for transmission.
- OAM cells are transmitted upon software command.
- Performs "Data Path Integrity" check on all incoming cell data, originating from the ATM Layer processor.
- Provides a serial input port to allow the user to insert the GFC (Generic Flow Control) field externally into the GFC nibble field of an outbound (e.g., Transmit direction) valid ATM Cell.

RECEIVE CELL PROCESSOR BLOCK

- Performs cell delineation on either "Direct Mapped" ATM cell data or PLCP frames.
- Verifies the HEC bytes of incoming cells and corrects most cells with single bit errors. Cells with multi-bit errors are detected and are optionally discarded.
- (Optionally) Performs filtering of Idle Cells.
- (Optionally) Performs filtering of User and OAM cells.
- UNI contains on-chip buffer space ("Receive OAM Cell" buffer) that allows for the reception and processing of selected OAM cells.
- Optionally de-scrambles the payload of each cell.
- Provides a serial output port that allows the user to read the GFC value of an incoming (e.g., Receive direction) ATM Cell.
- Inserts the "Data Path Integrity Check" patterns in all cells that are written to the RxFIFO.

TRANSMIT PLCP PROCESSOR BLOCK

- Can be disabled to support the "Direct Mapped" ATM mode.
- Packs 12 ATM cells into each PLCP frame along with various other overhead bytes.
- The Transmit PLCP Processor will automatically determine its own stuffing options.
- Overhead bytes include those that support BIP-8 calculations (B1), indicator of stuff-option status for current PLCP frame (C1), diagnostic byte that reflects alarms conditions that were detected in the Receive Section of the UNI (G1); and Path Overhead bytes.
- Provides a serial input port for user to insert PLCP Overhead Bytes externally.

RECEIVE PLCP PROCESSOR BLOCK

- Can be disabled to support the "Direct Mapped" ATM mode.
- Determines the frame boundaries of incoming PLCP frames (from the Receive DS3 Framer).
- Extracts and processes the PLCP frame overhead bytes.
- Provides a serial output port for user to read in the contents of the PLCP Overhead Bytes from the incoming data.

TRANSMIT/RECEIVE DS3 FRAMER BLOCK

- Supports the M13 and C-bit Parity Framing Formats.
- Transmit and Receive DS3 Framers can transmit/receive data in the Unipolar or the Bipolar (AMI or B3ZS line codes) format.
- The Transmit DS3 Framer provides a serial input port that allows the user to insert his/her own values for the overhead bits of the "outbound" DS3 frames.
- The Receive DS3 Framer provides a serial output port that allows the user access to the values of the overhead bits of the "incoming" DS3 frames.
- The Receive DS3 Framer can be configured to sample the incoming DS3 data (at the RxPOS and RxNEG input pins) via the rising edge or falling edge of the Receive Line Clock (RxLineClk) input.
- The Transmit DS3 Framer can be configured to update the "outbound" DS3 data (at the TxPOS and TxNEG output pins) at the rising edge or falling edge of the Transmit Line Clock (TxLineClk) output.
- UNI includes on-chip RAM space to support the transmission and reception of path maintenance data link messages via an on-chip LAPD Transceiver
- UNI includes on-chip registers to support the transmission and reception of FEAC (Far End Alarm & Control) messages via an on-chip FEAC Transceiver.
- Contains on-chip FEAC Transceiver.
- Contains on-chip LAPD Transceiver.

MICROPROCESSOR INTERFACE SECTION

- Can be interfaced to Motorola or Intel type of microprocessors/microcontrollers

- Microprocessor interface supports 8 bit wide or 16-bit wide read/write accesses.
- Supports polled or interrupt-driven environments.
- Supports burst mode “Read and Write” operations between the “local” microprocessor and the UNI on-chip registers and RAM locations.
- Includes a “Loss of Clock Signal” protection feature that terminates “Read/Write” cycles with the local µP, during a “Loss of Clock signal” event.

PERFORMANCE MONITOR SECTION

Contains numerous on-chip “Read-Only” registers that allows the user to monitor the overall “health” of the system.

TEST AND DIAGNOSTIC SECTION

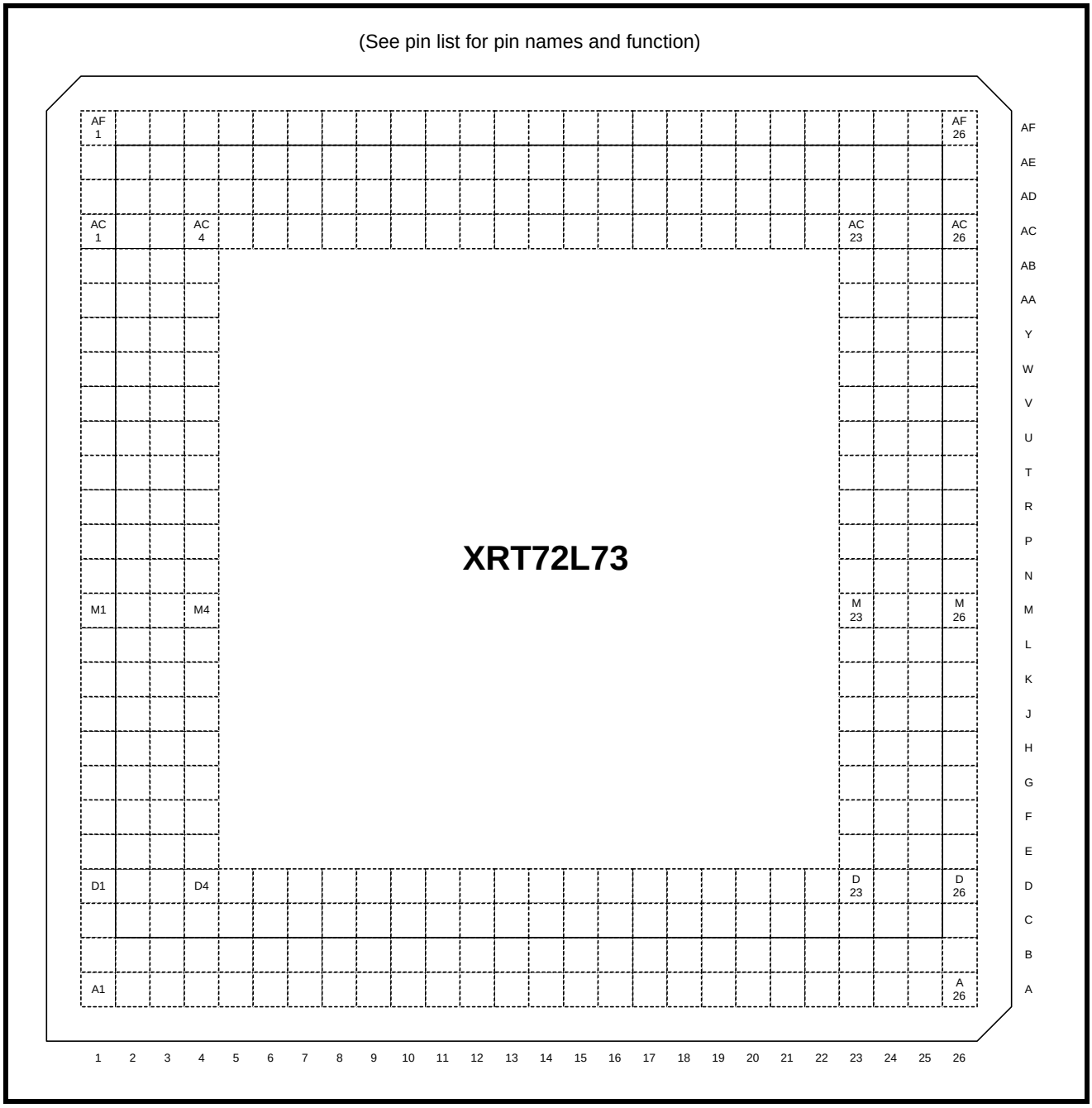
- Supports Line, PLCP, and Cell Loop-back Modes
- Supports Line-Side Testing
- Contains an on-chip Test Cell Generator and an on-chip Test Cell Receiver
- Test Cell Generator can generate a “continuous” stream of test cells, or a “one-shot” burst of 1024 test cells.
- The Test Cell Receiver identifies, collects and evaluates Test Cells for errors.
- The Test Cell Receiver also reports the occurrence of errors to the user.

LINE INTERFACE DRIVE AND SCAN SECTION

- Consists of an on-chip “Read/Write” register that allows the user to control the state of 6 output pins.

Consists of an on-chip “Read-Only” register that allows the user to monitor the state of 3 input pins.

FIGURE 3. PIN OUT OF THE XRT72L73 DS3 UNI FOR ATM (352 BALL PBGA)



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT72L73IB	35 x 35mm PBGA	-40°C to +85°C

LIST BY PIN NUMBER

PIN	PIN NAME
A1	TxOHIns_1
A2	RxLineClk_0
A3	TxOHIns_0
A4	No Connect
A5	LLOOP_0
A6	TxOHClk_1
A7	No Connect
A8	TxFrameRef_0
A9	EncoDis_1
A10	TxFrame_2
A11	TxFrame_0
A12	TxAISEn_0
A13	DMO_2
A14	RLOOP_2
A15	RLOOP_0
A16	TxLev_1
A17	No Connect
A18	RxFrame_1
A19	$\overline{\text{Req}}$_2
A20	No Connect
A21	No Connect
A22	TAOS_0
A23	RxOHClk_1
A24	No Connect
A25	RxOH_1
A26	No Connect
B1	TxPOS_0
B2	TxOHIns_2
B3	RxPOS_0
B4	RxNEG_0
B5	No Connect
B6	TxOHClk_0
B7	TxFrameRef_2
B8	No Connect
B9	EncoDis_0
B10	TxFrame_1
B11	No Connect
B12	No Connect
B13	DMO_1
B14	RLOOP_1
B15	No Connect
B16	TxLev_0
B17	RxFrame_2
B18	RxFrame_0
B19	$\overline{\text{Req}}$_1
B20	RxOHFrame_2
B21	TAOS_2
B22	No Connect
B23	RxOHClk_0
B24	No Connect
B25	RxOH_2
B26	RxOH_0
C1	No Connect
C2	TxInClk_0
C3	GND
C4	LLOOP_2
C5	TxOHClk_2
C6	TxPOS_1
C7	TxFrameRef_1
C8	TxNEG_1
C9	No Connect
C10	RxPOS_1
C11	TxAISEn_2
C12	RxNEG_1
C13	DMO_0
C14	TxNEG_2
C15	TxLev_2
C16	TxPOS_2
C17	RxNEG_2
C18	No Connect
C19	RxPOS_2
C20	RxOHFrame_1
C21	TAOS_1
C22	RxOHClk_2
C23	No Connect
C24	GND
C25	No Connect
C26	RxRed_2
D1	TxNEG_0
D2	TxOHFrame_1
D3	TxOHFrame_0
D4	GND
D5	LLOOP_1
D6	GND
D7	TxInClk_1
D8	VDD
D9	EncoDis_2
D10	GND
D11	RxLineClk_1
D12	TxAISEn_1
D13	GND
D14	No Connect
D15	VDD
D16	TxInClk_2
D17	GND
D18	RxLineClk_2
D19	VDD
D20	$\overline{\text{Req}}$_0
D21	RxOHFrame_0
D22	No Connect
D23	GND
D24	No Connect
D25	RxRed_1
D26	No Connect
E1	No Connect
E2	No Connect
E3	TxOHFrame_2
E4	TxLineClk_0
E23	RxRed_0
E24	RxAIS_1
E25	RxAIS_2
E26	No Connect
F1	TxOH_1
F2	TxLineClk_2
F3	TxOH_0
F4	VDD
F23	GND
F24	RLOS_2
F25	No Connect
F26	RxAIS_0
G1	8KRef_0
G2	No Connect
G3	TxOH_2
G4	TxLineClk_1
G23	RLOS_1
G24	RxOOF_2
G25	No Connect
G26	RLOS_0
H1	No Connect
H2	8KRef_2
H3	8KRef_1

PIN	PIN NAME
H4	VDD
H23	VDD
H24	No Connect
H25	RxOOF_0
H26	RxOOF_1
J1	TxOHInd/ TxPFrame_2
J2	TxOHInd/ TxPFrame_1
J3	TxOHInd/ TxPFrame_0
J4	No Connect
J23	RxLOS_2
J24	No Connect
J25	RxLOS_0
J26	RxLOS_1
K1	StuffCtl_2
K2	StuffCtl_1
K3	StuffCtl_0
K4	GND
K23	GND
K24	RxPRed_0
K25	RxPRed_1
K26	RxPRed_2
L1	TxPOHFrame_1
L2	TxPOHFrame_0
L3	No Connect
L4	TxPOHFrame_2
L23	No Connect
L24	RxPLOF_0
L25	RxPLOF_1
L26	RxPLOF_2
M1	TxSerData/ TxPOH_1

PIN	PIN NAME
M2	TxSerData/ TxPOH_0
M3	No Connect
M4	VDD
M23	No Connect
M24	RxSerClk/ RxPOHClk_0
M25	RxSerClk/ RxPOHClk_1
M26	RxSerClk/ RxPOHClk_2
N1	TxPOHClk_0
N2	No Connect
N3	TxSerData/ TxPOH_2
N4	TxPOHClk_1
N23	GND
N24	RLOL_1
N25	RLOL_2
N26	No Connect
P1	TxPOHIns_0
P2	No Connect
P3	TxPOHClk_2
P4	GND
P23	RLOL_0
P24	RxSerData/ RxPOH_1
P25	RxSerData/ RxPOH_2
P26	No Connect
R1	No Connect
R2	TxPOHIns_2
R3	TxPOHIns_1
R4	GPIO_0
R23	VDD
R24	RxPOHFrame_2

PIN	PIN NAME
R25	No Connect
R26	RxSerData/ RxPOH_0
T1	No Connect
T2	GPIO_2
T3	GPIO_1
T4	TMS
T23	RxPOHFrame_1
T24	RxOHInd/ RxPFrame_2
T25	No Connect
T26	RxPOHFrame_0
U1	TDI
U2	TCK
U3	TRST
U4	GND
U23	GND
U24	No Connect
U25	RxOHInd/ RxPFrame_0
U26	RxOHInd/ RxPFrame_1
V1	TestMode
V2	$\overline{\text{Reset}}$
V3	TDO
V4	A10
V23	RxPOOF_2
V24	No Connect
V25	RxPOOF_0
V26	RxPOOF_1
W1	A7
W2	A8
W3	A9
W4	VDD
W23	VDD

PIN	PIN NAME
W24	RxLCD_0
W25	RxLCD_1
W26	RxLCD_2
Y1	A4
Y2	A5
Y3	A6
Y4	D12
Y23	No Connect
Y24	RxGFCClk_0
Y25	RxGFCClk_1
Y26	RxGFCClk_2
AA1	A2
AA2	A3
AA3	D13
AA4	A1
AA23	VDD
AA24	RxUData3
AA25	RxGFCMSB_2
AA26	No Connect
AB1	$\overline{\text{CS}}$
AB2	D11
AB3	A0
AB4	D8
AB23	RxUData7
AB24	RxGFCMSB_0
AB25	RxUData2
AB26	RxGFCMSB_1
AC1	D14
AC2	$\overline{\text{WR}}$_RW
AC3	D9
AC4	GND
AC5	D4
AC6	No Connect

PIN	PIN NAME
AC7	D0
AC8	VDD
AC9	TxUSoC
AC10	GND
AC11	TxUAddr0
AC12	TxUData12
AC13	GND
AC14	TxUData6
AC15	VDD
AC16	TxCellTxed_0
AC17	GND
AC18	$\overline{\text{RxUEn}}$
AC19	VDD
AC20	RxUAddr3
AC21	GND
AC22	RxUData12
AC23	GND
AC24	RxUData6
AC25	No Connect
AC26	RxUData1
AD1	RDY_DTCK
AD2	D10
AD3	GND
AD4	D5
AD5	Width16
AD6	D1
AD7	TxGFC_0
AD8	TxUClav
AD9	$\overline{\text{TxUEn}}$
AD10	TxUClk
AD11	TxUAddr3
AD12	TxUData15
AD13	TxUData11

PIN	PIN NAME
AD14	TxUData8
AD15	TxUData5
AD16	TxUData2
AD17	RxUClk
AD18	RxUSoC
AD19	RxCellRxed_0
AD20	No Connect
AD21	RxUData15
AD22	RxUAddr0
AD23	RxUData9
AD24	GND
AD25	RxUData5
AD26	RxGFC_2
AE1	D15
AE2	ALE_AS
AE3	D6
AE4	$\overline{\text{Int}}$
AE5	D2
AE6	TxGFCClk_1
AE7	TxGFC_1
AE8	No Connect
AE9	TxGFCMSB_1
AE10	No Connect
AE11	TxUAddr2
AE12	TxUData14
AE13	TxUData10
AE14	TxUPrty
AE15	TxUData4
AE16	TxUData1
AE17	TxCellTxed_1
AE18	RxUClav
AE19	RxCellRxed_1
AE20	RxUData14

PIN	PIN NAME
AE21	RxUAddr2
AE22	RxUData11
AE23	RxUPrty
AE24	RxUData8
AE25	GND
AE26	RxUData4
AF1	$\overline{\text{RD}}$_DS
AF2	D7
AF3	MOTO/$\overline{\text{Intel}}$
AF4	D3
AF5	TxGFCClk_0
AF6	TxGFCClk_2
AF7	TxGFC_2
AF8	TxGFCMSB_0
AF9	TxGFCMSB_2
AF10	TxUAddr4
AF11	TxUAddr1
AF12	TxUData13
AF13	TxUData9
AF14	TxUData7
AF15	TxUData3
AF16	TxUData0
AF17	TxCellTxed_2
AF18	No Connect
AF19	RxCellRxed_2
AF20	RxUAddr4
AF21	RxUAddr1
AF22	RxUData13
AF23	RxGFC_0
AF24	RxUData10
AF25	RxGFC_1
AF26	RxUData0

PIN DESCRIPTIONS

PIN#	NAME	TYPE	DESCRIPTION
Microprocessor Interface			
AB3 AA4 AA1 AA2 Y1 Y2 Y3 W1 W2	A0 A1 A2 A3 A4 A5 A6 A7 A8	I	**Address Bus Input (Microprocessor Interface):** These pins are used to select the on-chip UNI register and RAM space for READ/ WRITE operations with the “local” microprocessor.
W3 V4	A9 A10	I	**Channel Selection:** A9 / A10 / Channel 0 / 0 / 0 1 / 0 / 1 0 / 1 / 2 1 / 1 / Reserved
AC7 AD6 AE5 AF4 AC5 AD4 AE3 AF2 AB4 AC3 AD2 AB2 Y4 AA3 AC1 AE1	D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15	I/O	**Bi-Directional Data Bus (Microprocessor Interface Section):** These pins function as the Microprocessor Interface bi-directional data bus and is intended to be interfaced to the “local” microprocessor. This pin is inactive if the Microprocessor Interface block is configured to operate over an 8 bit data bus.
AE2	ALE_AS	I	**Address Latch Enable/Address Strobe:** This input is used to latch the address (present at the Microprocessor Interface Address Bus, A[8:0]) into the UNI Microprocessor Interface circuitry and to indicate the start of a READ/WRITE cycle. This input is active-"High" in the Intel Mode (MOTO = “Low”) and active-”Low” in the Motorola Mode (MOTO = “High”).
AB1	$\overline{CS}$	I	**Chip Select Input:** This active-”Low” input signal selects the Microprocessor Interface Section of the UNI/Framer and enables Read/Write operations between the “local” microprocessor and the UNI/Framer on-chip registers and RAM locations.
AE4	$\overline{Int}$	O	**Interrupt Request Output:** This open-drain, active-”Low” output signal will be asserted when the UNI/Framer is requesting interrupt service from the local microprocessor. This output pin should typically be connected to the “Interrupt Request” input of the local microprocessor.

PIN DESCRIPTIONS

PIN#	NAME	TYPE	DESCRIPTION
AF3	MOTO/$\overline{\text{Intel}}$	I	**Motorola/Intel Processor Interface Select Mode:** This input pin allows the user to configure the Microprocessor Interface to interface with either a “Motorola-type” or “Intel-type” microprocessor/microcontroller. Tying this input pin to VDD, configures the microprocessor interface to operate in the Motorola mode (e.g., the UNI/Framer can be readily interfaced to a “Motorola type” local microprocessor). Tying this input pin to GND configures the microprocessor interface to operate in the Intel Mode (e.g., the UNI/Framer can be readily interfaced to an “Intel type” local microprocessor).
AF1	$\overline{\text{RD}}$_DS	I	**Read Data Strobe (Intel Mode):** If the microprocessor interface is operating in the Intel Mode, then this input will function as the RD (READ STROBE) input signal from the local µP. Once this active-”Low” signal is asserted, then the UNI/Framer will place the contents of the addressed registers (within the UNI/Framer IC) on the Microprocessor Data Bus (D[15:0]). When this signal is negated, the Data Bus will be tri-stated. **Data Strobe (Motorola Mode):** If the microprocessor interface is operating in the Motorola mode, then this pin will function as the active-”Low” Data Strobe signal.
AD1	RDY_DTCK	O	**READY or DTACK:** This active-”Low” output pin will function as the READY output, when the microprocessor interface is running in the “Intel” Mode; and will function as the DTACK output, when the microprocessor interface is running in the “Motorola” Mode. **Intel Mode—READY Output.** When the UNI negates this output pin (e.g., toggles it “Low”), it indicates (to the µP) that the current READ or WRITE cycle is to be extended until this signal is asserted (e.g., toggled “High”). **Motorola Mode:—DTACK (Data Transfer Acknowledge) Output.** The UNI Framer will assert this pin in order to inform the local microprocessor that the present READ or WRITE cycle is nearly complete. If the UNI Framer requires that the current READ or WRITE cycle be extended, then the UNI will delay its assertion of this signal. The 68000 family of µPs requires this signal from its peripheral devices, in order to quickly and properly complete a READ or WRITE cycle.
V2	$\overline{\text{Reset}}$	I	**Reset Input:** When this active-”Low” signal is asserted, the UNI Framer will be asynchronously reset. Additionally, all outputs will be “tri-stated”, and all on-chip registers will be reset to their default values.
AD5	Width16	I	**Microprocessor Interface Block Data Bus Width Selector:** This input pin permits the user to configure the microprocessor interface of the UNI/Framer, to operate over either an 8 or 16 bit wide bi-directional data bus. Tying this pin to VDD configures the Microprocessor Interface Data Bus width to be 16 bits. Tying this pin to GND configures the Microprocessor Interface Data Bus width to be 8 bits.
AC2	$\overline{\text{WR}}$_RW	I	**Write Data Strobe (Intel Mode):** If the microprocessor interface is operating in the Intel Mode, then this active-”Low” input pin functions as the WR (Write Strobe) input signal from the µP. Once this active-”Low” signal is asserted, then the UNI will latch the contents of the µP Data Bus, into the addressed register (or RAM location) within the UNI/Framer IC. **R/W Input Pin (Motorola Mode):** When the Microprocessor Interface Section is operating in the “Motorola Mode”, then this pin is functionally equivalent to the “R/W*” pin. In the Motorola Mode, a “READ” operation occurs if this pin is at a logic “1”. Similarly, a WRITE operation occurs if this pin is at a logic “0”.

PIN DESCRIPTIONS

PIN#	NAME	TYPE	DESCRIPTION
Test and Diagnostic			
U2	TCK	I	**Test Clock:** Boundry Scan clock input. ***NOTE:*** *This input pin should be pulled "Low" for normal operation.*
U1	TDI	I	**Test Data In:** Boundry Scan Test data input. ***NOTE:*** *This input pin should be pulled "Low" for normal operation.*
V3	TDO	O	**Test Data Out:** Boundry Scan test data output.
V1	TestMode	***	**Factory Test Mode Pin:** *The user should tie this pin to ground.*
T4	TMS	I	**Test Mode Select:** Boundary Scan Mode Select input pin. *This input pin should be pulled "Low" for normal operation.*
U3	TRST	I	**Test Mode Reset:** Boundary Scan Mode Reset input pin. ***NOTE:*** *This input pin should be pulled "low" for normal operation.*
Line Interface Drive and Scan			
C13 B13 A13	DMO_0 DMO_1 DMO_2	I	**"Drive Monitor Output" Input (from the XRT73L03 LIU IC):** This input pin is intended to be tied to the DMO output pin of the XRT73L03 E3/DS3/STS-1 LIU IC. The user can determine the state of this input pin by reading Bit 2 (DMO) within the Line Interface Scan Register (Address = 0x73). If this input signal is "High", then it means that the drive monitor circuitry (within the XRT73L03 LIU IC) has not detected any bipolar signals at the MTIP and MRING inputs within the last 128 ± 32 bit-periods. If this input signal is "Low", then it means that bipolar signals are being detected at the MTIP and MRING input pins of the XRT73L03 device. ***NOTE:*** *If the designer is not using the XRT73L03 E3/DS3/STS-1 LIU IC, then this input pin can be used for other purposes.*
R4 T3 T2	GPIO_0 GPIO_1 GPIO_2	I/O	**General Purpose Input/Output pins:** Each of these pin can be configured to function as either input or output pins. If a given pin is configured to function as an Input pin, then the state of this input pin can be monitored by reading Bit X within the "XXX" Register (Address Location = 0x###). If a given pin is configured to function as a Output pin, then the state of this output pin can be controlled by writing the appropriate value into Bit X within the "XXX" Register.
A5 D5 C4	LLOOP_0 LLOOP_1 LLOOP_2	O	**Local Loop-back Output Pin (to the XRT73L03 E3/DS3/STS-1 LIU IC):** This output pin is intended to be connected to the LLOOP input pin of the XRT73L03 LIU IC. This input pin, along with "RLOOP" permits the user to configure the XRT73L03 LIU IC to operate in either of the following three (3) loop-back modes. • Analog Local Loop-Back Mode • Digital Local Loop-Back Mode • Remote Loop-Back Mode. Writing a "1" to bit 1 of the "Line Interface Drive Register" (Address = 0x72) will cause this output pin to toggle "High". Writing a "0" to this bit-field will cause the RLOOP output to toggle "Low". ***NOTE:*** *If the user is not using the XRT73L03 DS3/E3/STS-1 LIU IC, then this output pin can be used for other purposes.*

PIN DESCRIPTIONS

PIN#	NAME	TYPE	DESCRIPTION
D20 B19 A19	$\overline{\text{Req}}$_0 $\overline{\text{Req}}$_1 $\overline{\text{Req}}$_2	O	**Receive Equalization Bypass Control Output Pin—(to be connected to the XRT73L03 E3/DS3/STS-1 LIU IC):** This output pin is intended to be connected to the $\overline{\text{Req}}$ input pin of the XRT73L03 E3/DS3/STS-1 LIU IC. The user can control the state of this output pin by writing a '0' or '1' to Bit 5 ($\overline{\text{Req}}$) of the Line Interface Driver Register (Address = 0x72). If the user commands this signal to toggle "High" then it will cause the incoming DS3 line signal to "by-pass" equalization circuitry, within the XRT73L03 Device. Conversely, if the user commands this output signal to toggle "Low", then the incoming DS3 line signal with be routed through the equalization circuitry. For information on the criteria that should be used when deciding whether to bypass the equalization circuitry or not, please consult the "XRT73L03 E3/DS3/STS-1 LIU IC" data sheet. Writing a "1" to Bit 5 of the Line Interface Drive Register (Address = 0x72) will cause this output pin to toggle "High". Writing a "0" to this bit-field will cause this output pin to toggle "Low". ***NOTE:*** *If the designer is not using the XRT73L03 E3/DS3/STS-1 LIU IC, then this output pin can be used for other purposes.*
P23 N24 N25	RLOL_0 RLOL_1 RLOL_2	I	**Receive Loss of Lock Indicator—from the XRT73L03 E3/DS3/STS-1 LIU IC:** This input pin is intended to be connected to the RLOL (Receive Loss of Lock) output pin of the XRT73L03 LIU IC. The user can monitor the state of this pin by reading the state of Bit 1 (RLOL) within the Line Interface Scan Register (Address = 0x73). If this input pin is "Low", then it means that the phase-locked-loop circuitry, within the XRT73L03 is properly locked onto the incoming DS3 data-stream; and is properly recovering clock and data from this DS3 data-stream. However, if this input pin is "High", then it means that the phase-locked-loop circuitry, within the XRT73L03 has lost lock with the incoming DS3 data-stream, and is not properly recovering clock and data. For more information on the operation of the XRT73L03 E3/DS3/STS-1 LIU IC, please consult the "XRT73L03 E3/DS3/STS-1 LIU IC" data sheet. ***NOTE:*** *If the designer is not using the XRT73L03 DS3/E3/STS-1 LIU IC, this input pin can be used for other purposes.*
A15 B14 A14	RLOOP_0 RLOOP_1 RLOOP_2	O	**Remote Loop-back Output Pin (to the XRT73L03 DS3/E3/STS-1 LIU IC):** This output pin is intended to be connected to the RLOOP input pin of the XRT73L03 LIU IC. This output pin, along with the LLOOP input pin permits the user to configure the XRT73L03 to operate in either of the following three (3) loop-back modes. • Analog Local Loop-Back Mode • Digital Local Loop-Back Mode • Remote Loop-Back Mode. Writing a "1" to bit 1 of the "Line Interface Drive Register (Address = 0x72) will cause this output pin to toggle "High". Writing a "0" to this bit-field will cause the RLOOP output to toggle "Low". ***NOTE:*** *If the customer is not using the XRT73L03 DS3/E3/STS-1 IC, then this output pin can be used for other purposes.*

PIN DESCRIPTIONS

PIN#	NAME	TYPE	DESCRIPTION
G26 G23 F24	RLOS_0 RLOS_1 RLOS_2	I	**Receive LOS (Loss of Signal) Indicator Input (from XRT73L03 E3/DS3/STS-1 Line Interface Unit).** This input pin is intended to be connected to the RLOS (Receive Loss of Signal) output pin of the XRT73L03 E3/DS3 /STS-1 Line Interface IC. The user can monitor the state of this pin by reading the state of Bit 0 (RLOS) within the Line Interface Scan Register (Address = 73h). If this input pin is “Low”, then it means that the XRT73L03 is detecting a sufficient amount of signal energy on the line, due to the incoming DS3 data-stream. However, if this input pin is “High”, then it means that the XRT73L03 is not detecting a sufficient amount of signal energy on the line, due to the incoming DS3 data-stream, and may be experiencing a “Loss of Signal” condition. For more information on the operation of the XRT73L03 E3/DS3/STS-1 Line Interface Unit IC, please consult the “XRT73L03 ” data sheet. ***NOTE:*** *Asserting the RLOS input pin will cause the XRT72L73 DS3 UNI to declare an “LOS” (Loss of Signal) condition. Therefore, this input pin should not be used as a general purpose input.*
E23 D25 C26	RxRed_0 RxRed_1 RxRed_2	O	**Receiver Red Alarm Indicator—Receive DS3 Framer:** The UNI asserts this output pin to denote that one of the following conditions is currently being declared by the Receive DS3 Framer block: • LOS—Loss of Signal Condition • OOF—Out of Frame Condition • AIS—Alarm Indication Signal Detection ***NOTE:*** *This output pin is effectively, the “Wired-OR” of the “RxLOS”, the “RxOOF” and the “RxAIS” output pins.*
A22 C21 B21	TAOS_0 TAOS_1 TAOS_2	O	**“Transmit All Ones Signal” (TAOS) Command (for the XRT73L03 LIU IC).** This output pin is intended to be connected to the TAOS input pin of the XRT73L03 LIU IC. The user can control the state of this output pin by writing a ‘0’ or ‘1’ to Bit 4 (TAOS) within the Line Interface Drive Register (Address = 0x72). If the user commands this signal to toggle "High" then it will force the XRT73L03 DS3 Line Transmitter IC to transmit an "All Ones" pattern onto the line. Conversely, if the user commands this output signal to toggle "Low" then the XRT73L03 DS3 Line Transmitter IC will proceed to transmit data based upon the pattern that it receives via the TxPOS and TxNEG output pins. Writing a "1" to Bit 4 of the Line Interface Drive Register (Address = 0x72) will cause this output pin to toggle "High". Writing a "0" to this bit-field will cause this output pin to toggle "Low". ***NOTE:*** *If the designer is not using the XRT73L03 DS3/E3/STS-1 LIU IC, then this output pin can be used for other purposes.*

PIN DESCRIPTIONS

PIN#	NAME	TYPE	DESCRIPTION
B16 A16 C15	TxLev_0 TxLev_1 TxLev_2	O	**Transmit Line Build Enable/Disable Select (to be connected to the TxLev input pin of the XRT73L03 E3/DS3/STS-1 LIU IC):** This output pin is intended to be connected to the TxLev input pin of the XRT73L03 E3/DS3/STS-1 LIU IC. The user can control the state of this output pin by writing a "0" or a "1" to Bit 2 (TxLev) within the Line Interface Driver Register (Address = 0x72). If the user commands this signal to toggle "High" then it will disable the "Transmit Line Build-Out" circuitry within the XRT73L03 device. In this case, the XRT73L03 will output unshaped (square-wave) pulses onto the "Transmit Line Signal". In order to insure that the XRT73L03 generates a line signal that is compliant with the Bellcore GR-499-CORE Pulse Template requirements (at the DSX-3 Cross-Connect), the user is advised to set this output pin "High", if the cable length (between the Transmit Output of the XRT73L03 and the DSX-3 Cross-Connect) is greater than 225 feet. Conversely, if the user commands this signal to toggle "High", then it will enable the "Transmit Line Build-Out" circuitry within the XRT73L03 device. In this case, the XRT73L03 will output shaped pulses onto the "Transmit Line Signal". In order to ensure that the XRT73L03 generates a line signal that is compliant with the Bellcore GR-499-CORE Pulse Template requirements (at the DSX-3 Cross-Connect), the user is advised to set this output pin "Low", if the cable length (between the Transmit Output of the XRT73L03 and the DSX-3 Cross Connect) is less than 225 ft. of cable. Writing a "1" to Bit 2 of the Line Interface Drive Register (Address = 0x72) will cause this output pin to toggle "High". Writing a "0" to this bit-field will cause this output pin to toggle "Low". ***NOTE:*** *If the customer is not using the XRT73L03 DS3/E3/STS-1 LIU IC, then this output pin can be used for other purposes.*
Tx DS3 Framer			
A12 D12 C11	TxAISEn_0 TxAISEn_1 TxAISEn_2	I	**Transmit AIS Pattern input:** When this input pin is pulled "High" then the Transmit DS3 Framer block will insert the AIS pattern into the DS3 output data stream.
A11 B10 A10	TxFrame_0 TxFrame_1 TxFrame_2	O	**Transmit End of DS3 Frame Indicator:** The function of this pin is same in both Clear Channel and ATM UNI modes of the XRT72L73. This pin marks the end of each DS3 frame. **ATM UNI Mode** This pin is pulsed for one DS3 clock period when the transmit input interface is processing the last bit of the given DS3 frame. This just serves as an indication to terminal equpiment in the ATM UNI mode. **Clear Channel Mode** When the XRT72L73 is configured to operate in the "Clear-Channel Framer" mode, then the Transmit DS3 Framer block will pulse this output pin "High" (for one bit period) when the "Transmit Payload Data Input Interface" block is processing the last bit of a given DS3 frame. The purpose of this output pin is to alert the Terminal Equipment that it needs to begin transmission of a new DS3 frame to the XRT72L73 (e.g., to permit the XRT72L73 to maintain Transmit DS3 framing alignment control over the Terminal Equipment).

PIN DESCRIPTIONS

PIN#	NAME	TYPE	DESCRIPTION
A8 C7 B7	TxFrameRef_0 TxFrameRef_1 TxFrameRef_2	I	**Transmit DS3 Framer—Frame Reference Input Pin:** The Transmit DS3 Framer can be configured to use this input signal as the “framing” reference for the Transmit DS3 Framer block. If this input pin is chosen to be the timing reference, then any rising edge at this input will cause the Transmit DS3 Framer to begin its creation a new DS3 M-frame. Consequently, the user must supply a clock signal that is equivalent to the DS3 Frame rate (or 9398.3 Hz). Further, the signal which is driving this input pin, must be synchronized witht he 44.736MHz clock signal, which is applied to the “TxInClk” input pin. ***NOTE:*** *This input pin should be tied to “GND” if it is not used as the Transmit DS3 Framer frame reference signal.*
C2 D7 D16	TxInClk_0 TxInClk_1 TxInClk_2	I	**Transmit DS3 Framer Block—Clock Signal:** The Transmit DS3 Framer can be configured to use this input signal as the timing reference. If this input pin is chosen to be the timing reference, then the user must supply a "High" quality 44.736 MHz signal to this input pin. In this configuration, frame generation, by the Transmit DS3 Framer, will be asynchronous (with any other timing signals within the UNI). However, frame timing will be based upon this clock signal. ***NOTE:*** *This input pin should be tied to “GND” if it is not used as the Transmit DS3 Framer timing reference.*
E4 G4 F2	TxLineClk_0 TxLineClk_1 TxLineClk_2	O	**Transmit Line Interface Clock:** This clock signal is output to the Line Interface Unit, along with the TxPOS and TxNEG signals. The purpose of this output clock signal is to provide the LIU with timing information that it can use to generate the AMI pulses and deliver them over the transmission medium to the Far-End Receiver. The user can configure the source of this clock to be either the RxLineClk (from the Receiver portion of the UNI) or the TxlineClk input. The nominal frequency of this clock signal is 44.736 MHz.
D1 C8 C14	TxNEG_0 TxNEG_1 TxNEG_2	O	**Transmit Negative Polarity Pulse:** The exact role of this output pin depends upon whether the UNI is operating in the Unipolar or Bipolar Mode. **Unipolar Mode:** This output signal pulses “High” for one bit period, at the end of each “outbound” DS3 frame. This output signal is at a logic “Low” for all of the remaining bit-periods of the “outbound” DS3 frames. **Bipolar Mode:** This output pin functions as one of the two dual-rail output signals that commands the sequence of pulses to be driven on the line. TxPOS is the other output pin. This input is typically connected to the TNDATA input of the external DS3 Line Interface Unit IC. When this output is asserted, it will command the LIU to generate a negative polarity pulse on the line.
F3 F1 G3	TxOH_0 TxOH_1 TxOH_2	I	**Transmit Overhead Input Pin** The Transmit Overhead Data Input Interface accepts the overhead data via this input pin, and inserts into the "overhead" bit position within the very next "outbound" DS3 frame. If the "TxOHIns" pin is pulled "High", the Transmit Overhead Data Input Interface will sample the data at this input pin (TxOH), on the falling edge of the "TxOHClk" output pin. Conversely, if the "TxOHIns" pin is pulled "Low", then the Transmit Overhead Data Input Interface will NOT sample the data at this input pin (TxOH). Consequently, this data will be ignored.
B6 A6 C5	TxOHClk_0 TxOHClk_1 TxOHClk_2	O	**Transmit Overhead Clock:** The function of this pin is the same in both Clear Channel and ATM UNI Modes of the XRT72L73. This pin serves as the clock signal for the external interface to insert the OH data on the TxOH pin. The user can insert OH data on the TxOH pin at the rising edge of this clock signal.

PIN DESCRIPTIONS

PIN#	NAME	TYPE	DESCRIPTION
D3 D2 E3	TxOHFrame_0 TxOHFrame_1 TxOHFrame_2	O	**Transmit Overhead Framing Pulse:** The function of this pin is same in both Clear Channel and ATM UNI modes of XRT72L73. When the external interface samples this pin "High" at the rising edge of TxOHClk, it should provide 'X' bit (first OH bit within DS3 frame) on the TxOH pin. This signal is "High" for one TxOHClk duration and repeats once for each DS3 frame.
A3 A1 B2	TxOHIns_0 TxOHIns_1 TxOHIns_2	I	**Transmit Overhead Data Insert Input:** The function of this pin is the same in both Clear Channel and ATM UNI Modes of the XRT72L73. This pin is used to indicate if the OH bit should be taken from the external interface. The OH data on TxOH will be considered by the only if this pin is "High" during OH positions.
B1 C6 C16	TxPOS_0 TxPOS_1 TxPOS_2	O	**Transmit Positive Polarity Pulse:** The exact role of this output pin depends upon whether the UNI is operating in the Unipolar or Bipolar Mode. **Unipolar Mode:** This output pin functions as the “Single-Rail” output signal for the “outbound” DS3 data stream. The signal, at this output pin, will be updated on the “user-selected” edge of the TxLineClk signal. **Bipolar Mode:** This output pin functions as one of the two dual rail output signals that commands the sequence of pulses to be driven on the line. TxNEG is the other output pin. This input is typically connected to the TPDATA input of the external DS3 Line Interface Unit IC. When this output is asserted, it will command the LIU to generate a positive polarity pulse on the line.
Rx DS3 Framer			
F26 E24 E25	RxAIS_0 RxAIS_1 RxAIS_2	O	**Receive “Alarm Indication Signal” Output pin:** The UNI/Framer IC will assert this pin to indicate that the Alarm Indication Signal (AIS) has been identified in the Receive DS3 data stream. An “AIS” is detected if the payload consists of the recurring pattern of 1010... and this pattern persists for 63 M-frames. An additional requirement for AIS indication is that the C-bits are set to 0, and the X-bits are set to 1. This pin will be negated when a sufficient number of frames, not exhibiting the “1010...” pattern in the payload has been detected.
B18 A18 B17	RxFrame_0 RxFrame_1 RxFrame_2	O	**Receive Boundary of DS3 Frame Output Indicator:** The exact functionality of this output pin depends upon whether the XRT72L73 UNI/Framer IC is operating in the Clear Channel or ATM UNI Mode. **Clear Channel Mode:** In clear channel mode this pin is pulsed “High” for one DS3 clock period whenever the 'X' bit (first OH bit in the DS3 frame) of the frame is being output on the RxSer pin. RxSer will contain 'X' bit (first OH bit of DS3 frame) if this pin is sampled “High”. **ATM UNI Mode:** In the ATM UNI mode, this signal indicates the start of the received DS3 frame and is "High" for one DS3 clock period.
A2 D11 D18	RxLineClk_0 RxLineClk_1 RxLineClk_2	I	**Receive LIU (Recovered) Clock Input:** This input signal serves three purposes: 1. The Receive DS3 Framer uses it to sample and “latch” the signals at the RxPOS and RxNEG input pins (into the Receive DS3 Framer circuitry). 2. This input signal functions as the timing reference for the Receive Framer block. 3. The Transmit DS3 Framer block can be configured to use this input signal as its timing reference. ***NOTE:*** *Note: This signal is the recovered clock from the external DS3 LIU (Line Interface Unit) IC, which is derived from the incoming DS3 data.*

PIN DESCRIPTIONS

PIN#	NAME	TYPE	DESCRIPTION
J25 J26 J23	RxLOS_0 RxLOS_1 RxLOS_2	O	**Receive DS3 Framer—Loss of Signal Output Indicator:** This pin is asserted when the Receive DS3 Framer encounters 180 consecutive 0's via the RxPOS and RxNEG pins. This pin will be negated once the Receive DS3 Framer has detected at least 60 "1s" out of 180 consecutive bits.
B4 C12 C17	RxNEG_0 RxNEG_1 RxNEG_2	I	**Receive Negative Data Input:** The exact role of this input pin depends upon whether the UNI is operating in the Unipolar or Bipolar Mode. **Unipolar Mode:** This input pin is inactive, and should be pulled ("Low" or "High") when the UNI is operating in the Unipolar Mode. **Bipolar Mode:** This input pin functions as one of the dual rail inputs for the incoming AMI/B3ZS encoded DS3 data that has been received from an external Line Interface Unit (LIU) IC. RxPOS functions as the other dual rail input for the UNI. When this input pin is asserted, it means that the LIU has received a "negative polarity" pulse from the line.
B26 A25 B25	RxOH_0 RxOH_1 RxOH_2	O	**Receive Overhead Output Port:** All overhead bits, which are received via the "Receive Section" of the Framer IC; will be output via this output pin, upon the rising edge of RxOHClk.
B23 A23 C22	RxOHClk_0 RxOHClk_1 RxOHClk_2	O	**Receive Overhead Output Clock Signal:** This pin serves as the clock signal for external device to sample the Overhead data on the RxOH pin. The external interface should use the rising edge of this clock to sample the OH data on RxOH pin.
D21 C20 B20	RxOHFrame_0 RxOHFrame_1 RxOHFrame_2	O	**Receive Overhead Frame Boundary Indicator:** This pin is pulsed "High" for one RxOHClk period whenever the first 'X' bit is output on RxOH pin. If external device samples this pin "High" on the rising edge of RxOHClk, the data on RxOH is 'X' bit (first OH bit in the received DS3 frame).
H25 H26 G24	RxOOF_0 RxOOF_1 RxOOF_2	O	**Receiver DS3 Framer—"Out of Frame" Indicator:** The Receive DS3 Framerblock will assert this output signal (e.g., pull it "High") whenever it has declared an "Out of Frame" (OOF) condition with the incoming DS3 frames. This signal is negated when the framer correctly locates the F- and M-bits and regains synchronization with the DS3 frame.
R26 P24 P25	RxSerData/ RxPOH_0 RxSerData/ RxPOH_1 RxSerData/ RxPOH_2	O	**Receive Serial Output/Receive PLCP Frame Path Overhead (POH) Byte Serial Output Port—Output Pin:** The exact functionality of this output pin depends upon whether the XRT72L71 Framer IC is operating in the Clear Channel or ATM UNI Mode. **Clear Channel Mode:** In clear channel mode, all DS3 data which is received by XRT72L71 will be output as a serial data stream via this pin. The XRT72L71 will output data (via this pin) upon the falling edge of "RxSerClk". As a consequence, this data should be sampled with the rising edge of RxSerClk. **ATM UNI Mode:** This output pin, along with RxPOHClk, RxPOHFrame, and RxPOHIns pins comprise the "Receive PLCP Frame POH Byte" serial output port. For each PLCP frame that is received by the Receive PLCP Processor, this serial output port will output the contents of all 12 POH (Path Overhead) bytes. The data that is output via this pin, is updated on the rising edge of the RxPOHClk output clock signal. The RxPOHFrame pin will pulse "High" when the first bit of the Z6 byte is being output on this output pin.

PIN DESCRIPTIONS

PIN#	NAME	TYPE	DESCRIPTION
M24 M25 M26	RxSerClk/ RxPOHClk_0 RxSerClk/ RxPOHClk_1 RxSerClk/ RxPOHClk_2	O	**Clear Channel Mode Receive Clock Output Signal for Serial Data Interface/ Receive PLCP Frame Path Overhead (POH) Byte Serial Output Port—Output Clock Signal:** The exact functionality of this output pin depends upon whether the XRT72L71 Framer IC is operating in the Clear Channel or ATM UNI Mode. **Clear Channel Mode - RxSerClk:** In clear channel mode, this pin can be used by the external interface to sample the clear channel serial data stream on RxSer pin. The Receive Section of the XRT72L71 will output all “inbound” DS3 data, via the “RxSerData” output pin, upon the rising edge of this output pin. Hence, the user should be sampling the data (on the “RxSerData” output pin) upon the rising edge of this clock. **ATM UNI MODE - RxPOHClk:** In the ATM UNI mode of operation, this pin serves as RxPOHClk. This output clock pin, along with RxPOH, RxPOHframe pins comprise the 'Receive PLCP OH serial output' interface.
B3 C10 C19	RxPOS_0 RxPOS_1 RxPOS_2	I	**Receive Positive Data Input:** The exact role of this input pin depends upon whether the UNI is operating in the Unipolar or Bipolar Mode. **Unipolar Mode:** This input pin functions as the “Single-Rail” input for the “incoming” DS3 data stream. The signal at this input pin will be sampled and latched (into the Receive DS3 Framer) on the “user-selected” edge of the RxLineClk signal. **Bipolar Mode:** This input functions as one of the dual rail inputs for the incoming AMI/B3ZS encoded DS3 data that has been received from an external Line Interface Unit (LIU) IC. RxNEG functions as the other dual rail input for the UNI. When this input pin is asserted, it means that the LIU has received a “positive polarity” pulse from the line.
Tx PLCP Processor			
G1 H3 H2	8KRef_0 8KRef_1 8KRef_2	I	**8 kHz Reference Clock Input for the PLCP Processors:** The Transmit PLCP processor can be configured to synchronize its PLCP frame processing to this clock signal. The Transmit PLCP Processor will also use this signal to compute the trailer nibble stuff opportunities. ***NOTES:*** 1. *This input signal is active only if the user has configured the PLCP Processors to use this signal as their “master clock” signal. The user can configure the UNI to use this signal by setting TimRefSel[1,0] (within the UNI Operating Mode Register) to 01.* 2. *The user should tie this pin to “GND” whenever the XRT72L73 has been configured to operate in the “Clear-Channel-Framer” Mode.*

PIN DESCRIPTIONS

PIN#	NAME	TYPE	DESCRIPTION
B9 A9 D9	EncoDis_0 EncoDis_1 EncoDis_2	O	**Encoder (B3ZS) Disable Output pin (intended to be connected to the XRT73L03 E3/DS3/STS-1 LIU IC):** This output pin is intended to be connected to the EncoDis input pin of the XRT73L03 LIU IC. The user can control the state of this output pin by writing a "0" or "1" to Bit 3 (EncoDis) of the Line Interface Driver Register (Address = 0x72). If the user commands this signal to toggle "High" then it will disable the B3ZS encoder circuitry within the XRT73L03 IC. Conversely, if the user commands this output signal to toggle "Low", then the B3ZS Encoder circuitry, within the XRT73L03 IC will be enabled. Writing a "1" to Bit 3 of the Line Interface Driver Register (Address = 0x72) will cause this output pin to toggle "High". Writing a "0" to this bit-field will cause this output pin to toggle "Low". ***NOTES:*** 1. *The user is advised to disable the B3ZS encoder (within the XRT73L03 IC) if the Transmit and Receive DS3 Framers (within the UNI) are configured to operate in the B3ZS line code.* 2. *If the designer is not using the XRT73L03 DS3/E3/STS-1 Line Transmitter IC, then output pin can be used for other purposes.*
K3 K2 K1	StuffCtl_0 StuffCtl_1 StuffCtl_2	I	**External PLCP Frame Stuff Control:** This input allows the user to externally exercise or forego trailer nibble stuffing opportunities by the Transmit PLCP Processor. PLCP trailer nibble stuff opportunities occur in periods of three PLCP frames (375µs). The first PLCP frame (first within a "stuff opportunity" period) will have 13 trailer nibbles appended to it. The second PLCP frame (second within a "stuff opportunity" period) will have 14 trailer nibbles appended to it. The third PLCP frame (the location of the stuff opportunity) will contain 13 trailer nibbles if the StuffCtl input is "Low" and 14 trailer nibbles is the StuffCtl input is "High". ***NOTE:*** *The user should tie this input pin to "GND" whenever the XRT72L73 has been configured to operate in the "Clear-Channel-Framer" Mode.*
J3 J2 J1	TxOHInd/ TxPFrame_0 TxOHInd/ TxPFrame_1 TxOHInd/ TxPFrame_2	O	**Transmit Overhead Data Indicator/Transmit PLCP Frame Boundary Indicator—Output:** The exact functionality of this output pin depends upon whether the XRT72L71 Framer IC is operating in the Clear Channel or ATM Uni Mode. **Clear Channel Mode:** In the Clear Channel Mode, this pin serves as the transmit OH Indication for the external interface. This pin is pulsed for one bit period of DS3 clock to indicate to the external device that the transmit input interface is going to process OH data at the rising edge of next clock. When the external interface samples TxOHInd as "High" With the rising edge of DS3 Clk; it is expected NOT to provide useful payload data bit on TxSer pin. Instead it can provide corresponding OH data bit on TxSer input. However, in that case the user has to program a register bit to configure XRT72L71 to accept the OH data from the TxSer input. Otherwise, the OH data will be geaerated internally or be taken from the TxOH pin if TxOHIns is "High". This pin is pulsed "High" for one bit period prior to all DS3 OH bit positions. **ATM UNI Mode:** In ATM UNI mode of operation, this pin functions as Transmit PLCP Frame signal which pulses "High" once for each outbound PLCP frame, when the last nibble is being routed.

PIN DESCRIPTIONS

PIN#	NAME	TYPE	DESCRIPTION
M2 M1 N3	TxSerData/ TxPOH_0 TxSerData/ TxPOH_1 TxSerData/ TxPOH_2	I	**Transmit Serial Payload Data Input/Transmit PLCP Frame POH Byte Insertion Serial Input:** The exact functionality of this output pin depends upon whether the XRT72L71 Framer IC is operating in the Clear Channel or ATM Uni Mode. **Clear Channel Mode:** In clear channel mode, this pin can be used by the external interface to provide the serial input data (payload and OH) that has to be mapped in outgoing DS3 frame. If user want to insert OH data on TxSer pin then the user should configure the XRT72L71 accordingly. **ATM UNI Mode:** This input pin becomes active when the user asserts the TxPOHIns input pin. When this happens the user will be permitted to serially input their own value for PLCP POH bytes into the "outbound" PLCP frame. This data will be clocked into the UNI Framer via the TxPOHClk output signal. This UNI will also assert the TxPOHMSB output pin when it expects the MSB (Most significant bit) of the Z6 Byte (within the PLCP frame).
N1 N4 P3	TxPOHClk_0 TxPOHClk_1 TxPOHClk_2	O	**Transmit PLCP Frame POH Byte Insertion Clock:** This pin, along with the TxPOH and the TxPOHMSB input pins, function as the "Transmit PLCP Frame POH Byte" serial input port. This output pin functions as a clock output signal that is used to sample the user's POH data at the TxPOH input pin. This output pin is always active, independent of the state of the "TxPOHIns" pin. ***NOTE:*** *This output pin is only active if the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*
L2 L1 L4	TxPOHFrame_0 TxPOHFrame_1 TxPOHFrame_2	O	**Transmit PLCP Frame Path Overhead Byte Serial Input Port—Beginning of Frame indicator.** This output pin, along with the TxPOH, TxPOHClk, and TxPOHIns pins comprise the "Transmit PLCP Frame POH Byte Insertion" serial input port. This particular pin will pulse "High" when the "Transmit PLCP POH Byte Insertion" serial input port is expecting the first bit of the Z6 byte at the TxPOH input pin. ***NOTE:*** *This output pin is only active if the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*
P1 R3 R2	TxPOHIns_0 TxPOHIns_1 TxPOHIns_2	I	**Transmit PLCP Frame POH Data Insert Enable:** This input can be asserted to allow the user to input his/her own value for the PLCP POH bytes via the TxPOH input pin, in each PLCP frame, prior to transmission. If this input pin is not asserted, then the UNI will generate its own PLCP POH bytes. ***NOTE:*** *The user should tie this input pin to "GND" if the XRT72L73 is going to be configured to operate in either the "Clear-Channel-Framer" Mode or in the "Direct-Mapped ATM" Mode.*
Rx PLCP Processor			
U25 U26 T24	RxOHInd/ RxPFrame_0 RxOHInd/ RxPFrame_1 RxOHInd/ RxPFrame_2	O	**Receive Overhead Bit Indicator/PLCP Frame Boundary Indicator Output—Receive PLCP Processor.** The exact functionality of this output pin depends upon whether the XRT72L71 UNI/Framer IC is operating in the Clear Channel or ATM Uni Mode. **Clear Channel Mode - RxOHInd:** In clear channel mode, this pin is pulsed "High" for one bit period whenever an over-head bit is being output via the RxSerData output pin. In other words, the "RxSer-Data" output pin will contain an over-head if this pin is sampled "High". **ATM UNI Mode:** This output pin pulses "High" when the Receive PLCP Processor is receiving the last bit of a given PLCP frame.

PIN DESCRIPTIONS

PIN#	NAME	TYPE	DESCRIPTION
L24 L25 L26	RxPLOF_0 RxPLOF_1 RxPLOF_2	O	**Receive PLCP—"Loss of Frame" Output Indicator:** The Receive PLCP Processor will assert this pin, when it declares a "Loss of Frame" condition. This output will be negated when the Receive PLCP Processor reaches the "In Frame" Condition. ***NOTE:*** *This output pin is only active if the user has configured the XRT72L73 to operate in the "ATM UNI" Mode.*
T26 T23 R24	RxPOHFrame_0 RxPOHFrame_1 RxPOHFrame_2	O	**Receive PLCP Frame Path Overhead (POH) Byte Serial Output Port—Beginning of Frame Signal Pin:** This output pin, along with RxPOH, RxPOHClk, and RxPOHIns pins comprise the "Receive PLCP Frame POH Byte" serial output port. This output pin provides framing information to external circuitry receiving and processing this POH (Path Overhead) data, by pulsing "High" when the first bit of the Z6 byte is output via the RxPOH output pin. This pin is "Low" at all other times during this PLCP POH framing cycle. ***NOTE:*** *This output pin is only active if the XRT72L73 has been configued to operate in the "ATM UNI" Mode.*
V25 V26 V23	RxPOOF_0 RxPOOF_1 RxPOOF_2	O	**Receive PLCP "Out of Frame" Indicator:** The Receive PLCP Processor will assert this pin, when it declares an "Out of Frame" condition. This output will be negated when the Receive PLCP Processor reaches the "In Frame" Condition. ***NOTE:*** *This output pin is only active if the user has configured the XRT72L73 to operate in the "ATM UNI" Mode.*
K24 K25 K26	RxPRed_0 RxPRed_1 RxPRed_2	O	**Receiver Red Alarm Indicator—Receive PLCP Processor:** The UNI asserts this output pin to denote that one of the following events has been detected by the Receive PLCP Processor: • OOF—Out of Frame Condition • LOF—Loss of Frame Condition ***NOTE:*** *This output pin is only active whenever the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*
Tx Cell Processor			
AC16 AE17 AF17	TxCellTxed_0 TxCellTxed_1 TxCellTxed_2	O	**Transmit Cell Processor—Cell Transmitted Indicator:** This output pin pulses "High" each time the Transmit Cell Processor transmits a cell to the Transmit PLCP Processor (or Transmit DS3 Framer). *This output pin is only active if the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*
AD7 AE7 AF7	TxGFC_0 TxGFC_1 TxGFC_2	I	**Transmit GFC Nibble-Field Serial Input Port:** This signal, along with TxGFCClk and TxGFCMSB combine to function as the "Transmit GFC Nibble-field" serial input port. The user will specify the value of the GFC field, within a given ATM cell, by serial transmitting its four bit value into this input. Each of these four bits will be clocked into the UNI via rising edge of the TxGFCClk clock output signal. ***NOTE:*** *The user should tie this input pin to "GND" whenever the XRT72L73 has been configured to operate in the "Clear-Channel-Framer" Mode.*
AF5 AE6 AF6	TxGFCClk_0 TxGFCClk_1 TxGFCClk_2	O	**Transmit GFC Nibble Field Serial Input Port Clock:** This signal, along with TxGFC, and TxGFCMSB combine to function as the "Transmit GFC Nibble-field" serial input port. The "Transmit GFC Nibble-field" serial input port uses this output clock signal to sample the values applied to the TxGFC pin, on its rising edge. This pin will provide four rising edges for each cell being transmitted. ***NOTE:*** *This output pin is only active whenever the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*

PIN DESCRIPTIONS

PIN#	NAME	TYPE	DESCRIPTION
AF8 AE9 AF9	TxGFCMSB_0 TxGFCMSB_1 TxGFCMSB_2	O	**Transmit GFC Nibble-Field Serial Input Port—MSB Indicator:** This signal, along with TxGFC and TxGFCClk combine to function as the "Transmit GFC Nibble Field" serial input port. This output signal will pulse "High" when the MSB (most significant bit) of the GFC Nibble (for a given cell) is expected at the TxGFC input pin. ***NOTE:*** *This output pin is only active whenever the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*
Rx Cell Processor			
AD19 AE19 AF19	RxCellRxed_0 RxCellRxed_1 RxCellRxed_2	O	**Receive Cell Processor—Cell Received Indicator:** This output pin pulses "High" each time the Receive Cell Processor receives a new cell from the Receive PLCP Processor or the Receive DS3 Framer. ***NOTE:*** *This output pin is only active if the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*
AF23 AF25 AD26	RxGFC_0 RxGFC_1 RxGFC_2	O	**Receive GFC Nibble Field Serial Output pin:** This pin, along with the RxGFCClk and the RxGFCMSB pins form the "Receive GFC Nibble-Field" serial output port. This pin will serially output the contents of the GFC Nibble field of each cell that is processed through the Receive Cell Processor. This data is serially clocked out of this pin on the rising edge of the RxGFCClk signal. The Most Significant Bit (MSB) of each GFC value is designated by a pulse at the RxGFCMSB output pin. ***NOTE:*** *This output pin is only active if the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*
Y24 Y25 Y26	RxGFCClk_0 RxGFCClk_1 RxGFCClk_2	O	**Received GFC Nibble Serial Output Port Clock Signal:** This output pin functions as a part of the "Receive GFC Nibble-Field" Serial Output Port; also consisting of the RxGFC and RxGFCMSB pins. This pin provides a clock pulse which allows external circuitry to latch in the GFC Nibble-Data via the RxGFC output pin. ***NOTE:*** *This output pin is only active if the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*
AB24 AB26 AA25	RxGFCMSB_0 RxGFCMSB_1 RxGFCMSB_2	O	**Received GFC Nibble Field—MSB Indicator**: This output pin functions as a part of the "Receive GFC-Nibble Field" Serial Output port; which also consists of the RxGFC and RxGFCClk pins. This pin pulses "High" the instant that the MSB (Most Significant Bit) of a GFC Nibble is being output on the RxGFC pin. ***NOTE:*** *This output pin is only active if the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*
W24 W25 W26	RxLCD_0 RxLCD_1 RxLCD_2	O	**Loss of Cell Delineation Indicator:** This active-"High" output pin will be asserted whenever the Receive Cell Processor has experienced a "Loss of Cell Delineation". This pin will return "Low" once the Receive Cell Processor has regained Cell Delineation. ***NOTE:*** *This output pin is only active if the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*

PIN DESCRIPTIONS

PIN#	NAME	TYPE	DESCRIPTION
Tx UTOPIA Interface			
AC11 AF11 AE11 AD11	TxUAddr0 TxUAddr1 TxUAddr2 TxUAddr3 TxUAddr4	I	**Transmit UTOPIA Address Bus Input:** These pins comprise the Transmit UTOPIA Address Bus input pins. The Transmit UTOPIA Address Bus is only in use when the UNI is operating in the M-PHY mode. When the ATM Layer processor wishes to write data to a particular UNI device, it will provide the address of the "intended UNI" on the Transmit UTOPIA Address Bus. The contents of the Transmit UTOPIA Address Bus input pins are sampled on the rising edge of TxUClk. The DS3 UNI will compare the data on the Transmit UTOPIA Address Bus with the pre-programmed contents of the TxUT Address Register (Address = 70h). If these two values are identical and the $\overline{\text{TxUEN}}$ pin is asserted, then the TxUClav pin will be driven to the appropriate state (based upon the TxFIFO fill level) for the Cell Level handshake mode of operation. ***NOTE:*** *The user should tie this input pin to "GND" whenever the XRT72L73 has been configured to operate in either the "Clear-Channel-Framer" Mode or in the "Single-PHY" Mode.*
AD8	TxUClav	O	**Transmit UTOPIA Interface—Cell Available Output Pin:** This output pin supports data flow control between the ATM Layer processor and the Transmit UTOPIA Interface block. The exact functionality of this pin depends upon whether the UNI is operating in the "Octet Level" or "Cell Level" handshaking mode. **Octet Level Handshaking:** When the Transmit UTOPIA Interface block is operating in the octet-level handshaking mode, this signal is negated (toggles "Low") when the TxFIFO is not capable of handling four more write operations; by the ATM Layer processor to the Transmit UTOPIA Interface block. This signal will be asserted when the TxFIFO is capable of receiving four or more write operations of ATM cell data. **Cell Level Handshaking:** When the Transmit UTOPIA Interface block is operating the cell-level handshaking mode, this signal is asserted (toggles "High") when the TxFIFO is capable of receiving at least one more full cell of data from the ATM Layer processor. This signal is negated, if the TxFIFO is not capable of receiving one more full cell of data from the ATM Layer processor. **Multi-PHY Operation:** When the UNI chip is operating in the Multi-PHY mode, this signal will be tri-stated until the TxUClk cycle following the assertion of a valid address on the Transmit UTOPIA Address bus input pins (e.g., when the contents on the Transmit UTOPIA Address bus pins match that within the Transmit UTOPIA Address Register). Afterwards, this output pin will behave in accordance with the cell-level handshake mode. ***NOTE:*** *This output pin is only active if the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*
AD9	$\overline{\text{TxUEn}}$	I	**Transmit UTOPIA Interface Block—Write Enable:** This active-"Low" signal, from the ATM Layer processor enables the data on the Transmit UTOPIA Data Bus to be written into the TxFIFO on the rising edge of TxUClk. When this signal is asserted, then the contents of the byte or word that is present, on the Transmit UTOPIA Data Bus, will be latched into the Transmit UTOPIA Interface block, on the rising edge of TxUClk. When this signal is negated, then the Transmit UTOPIA Data bus inputs will be tri-stated. ***NOTE:*** *The user should tie this input pin to "GND" whenever the XRT72L73 has been configured to operate in the "Clear-Channel-Framer" Mode.*

PIN DESCRIPTIONS

PIN#	NAME	TYPE	DESCRIPTION
AD10	TxUClk	I	**Transmit UTOPIA Interface Clock:** The Transmit UTOPIA Interface clock is used to latch the data on the Transmit UTOPIA Data bus, into the Transmit UTOPIA Interface block. This clock signal is also used as the timing source for circuitry used to process the ATM cell data into and through the TxFIFO. During Multi-PHY operation, the data on the Transmit UTOPIA Address bus pins is sampled on the rising edge of TxUClk. ***NOTE:*** *The user should tie this input pin to "GND" whenever the XRT72L73 has been configured to operate in the "Clear-Channel-Framer" Mode.*
AF16 AE16 AD16 AF15 AE15 AD15 AC14 AF14 AD14 AF13 AE13 AD13 AC12 AF12 AE12 AD12	TxUData0 TxUData1 TxUData2 TxUData3 TxUData4 TxUData5 TxUData6 TxUData7 TxUData8 TxUData9 TxUData10 TxUData11 TxUData12 TxUData13 TxUData14 TxUData15	I	**Transmit UTOPIA Data Bus Input:** These pins comprise the Transmit UTOPIA Data Bus input pins. When the ATM Layer Processor wishes to transmit ATM cell data through the XRT72L73 DS3 UNI, it must place this data on these pins. The data, on the Transmit UTOPIA Data Bus is latched into the Transmit UTOPIA Interface block on the rising edge of TxUClk. ***NOTE:*** *The user should tie this input pin to "GND" whenever the XRT72L73 has been configured to operate in the "Clear-Channel-Framer" Mode.*
AE14	TxUPrty	I	**Transmit UTOPIA Data Bus—Parity Input:** The ATM Layer processor will apply the parity value of the byte or word which is being applied to the Transmit UTOPIA Data Bus (e.g., TxUData[7:0] or TxUData[15:0]) inputs of the UNI, respectively. Note: this parity value should be computed based upon the odd-parity of the data applied at the Transmit UTOPIA Data Bus. The Transmit UTOPIA Interface block (within the UNI) will independently compute an odd-parity value of each byte (or word) that it receives from the ATM Layer processor and will compare it with the logic level of this input pin. ***NOTE:*** *The user should tie this input pin to "GND" whenever the XRT72L73 has been configured to operate in the "Clear-Channel-Framer" Mode.*
AC9	TxUSoC	I	**Transmitter—Start of Cell (SoC) Indicator Input:** This input pin is driven by the ATM Layer processor and is used to indicate the start of an ATM cell that is being transmitted from the ATM layer processor. This input pin must be pulsed "High" when the first byte (or word) of a new cell is present on the Transmit UTOPIA Data Bus. This input pin must remain "Low" at all other times. ***NOTE:*** *The user should tie this input pin to "GND" whenever the XRT72L73 has been configured to operate in the "Clear-Channel-Framer" Mode.*

PIN DESCRIPTIONS

PIN#	NAME	TYPE	DESCRIPTION
Rx UTOPIA Interface			
AD22 AF21 AE21 AC20 AF20	RxUAddr0 RxUAddr1 RxUAddr2 RxUAddr3 RxUAddr4	I	**Receive UTOPIA Address Bus input:** These input pins function as the Receive UTOPIA Address bus inputs. These input pins are only active when the UNI is operating in the Multi-PHY Mode. The Receive UTOPIA Address Bus input is sampled on the rising edge of the RxUClk signal. The contents of this address bus are compared with the value stored in the "Rx UT Address Register (Address = 6Ch). If these two values match, then the UNI will inform the ATM Layer Processor on whether or not it has any new ATM cells to be read from the RxFIFO; by driving the RxUClav output to the appropriate level. If these two address values do not match, then the UNI will not respond to the ATM Layer Processor; and will keep its RxUClav output signal tri-stated. ***NOTE:*** *The user should tie this pin to "GND", whenever the XRT72L73 has been configured to operate in the "Clear-Channel-Framer" Mode.*
AE18	RxUClav	O	**Receive UTOPIA—Cell Available:** The Receive UTOPIA Interface block will assert this output pin in order to indicate that the Rx FIFO has some ATM cell data that needs to be read by the ATM Layer Processor. The exact functionality of this pin depends upon whether the UNI is operating in the "Octet Level" or "Cell Level" handshake mode. **Octet Level Handshaking Mode** When the Receive UTOPIA Interface block is operating in the "octet-level hand-shaking" mode; this signal is asserted (toggles "High") when at least one byte of cell data exists within the RxFIFO (within the Receive UTOPIA Interface block). This output pin will toggle "Low" if the RxFIFO is depleted of ATM cell data. **Cell Level Handshaking Mode** When the Receive UTOPIA Interface block is operating in the "cell-level handshak-ing" mode; this signal is asserted if the RxFIFO contains at least one full cell of data. This signal will toggle "Low" if the RxFIFO is depleted of data, or if it contains less than one full cell of data. **Multi-PHY Operation:** When the UNI chip is operating in the Multi-PHY mode, this signal will be tri-stated until the RxUClk cycle following the assertion of a valid address on the Receive UTOPIA Address bus input pins (e.g., if the contents on the Receive UTOPIA Address bus pins match that with the Receive UTOPIA Address Register). Afterwards, this output pin will behave in accordance with the cell-level handshake mode. ***NOTE:*** *This output pin is only active if the XRT72L73 has been configured to oper-ate in the "ATM UNI" Mode.*
AD17	RxUClk	I	**Receive UTOPIA Interface Clock Input:** The byte (or word) data, on the Receive UTOPIA Data bus is updated on the rising edge of this signal. The Receive UTOPIA Interface can be clocked at rates up to 50 MHz. ***NOTE:*** *The user should tie this input pin to "GND" whenever the XRT72L73 has been configured to operate in the "Clear-Channel-Framer'" Mode.*

PIN DESCRIPTIONS

PIN#	NAME	TYPE	DESCRIPTION
AF26 AC26 AB25 AA24 AE26 AD25 AC24 AB23 AE24 AD23 AF24 AE22 AC22 AF22 AE20 AD21	RxUData0 RxUData1 RxUData2 RxUData3 RxUData4 RxUData5 RxUData6 RxUData7 RxUData8 RxUData9 RxUData10 RxUData11 RxUData12 RxUData13 RxUData14 RxUData15	O	**Receive UTOPIA Data Bus Output:** These output pins function as the Receive UTOPIA Data Bus. ATM cell data that has been received from the "Remote Terminal Equipment" is output on the Receive UTOPIA Data Bus, where it can be read and processed by the ATM Layer Processor. ***NOTE:*** *This output pin is only active if the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*
AC18	$\overline{\text{RxUEn}}$	I	**Receive UTOPIA Interface—Output Enable:** This active-"Low" input signal is used to control the drivers of the Receive UTOPIA Data Bus. When this signal is "High" (negated) then the Receive UTOPIA Data Bus is tri-stated. When this signal is asserted, then the contents of the byte or word that is at the "front of the RxFIFO" will be "popped" and placed on the Receive UTOPIA Data bus on the very next rising edge of RxUClk. ***NOTE:*** *The user should tie this pin to "GND" whenever the XRT72L73 has been configured to operate in the "Clear-Channel-Framer" Mode.*
AE23	RxUPrty	O	**Receive UTOPIA Interface—Parity Output pin:** The Receive UTOPIA interface block will compute the odd-parity of each byte (or word) that will place in the Receive UTOPIA Data Bus. This odd-parity value will be output on this pin, while the corresponding byte (or word) is present on the Receive UTOPIA Data Bus. ***NOTE:*** *This output pin is only active if the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*
AD18	RxUSoC	O	**Receive UTOPIA Interface—Start of Cell Indicator:** This output pin allows the ATM Layer Processor to determine the boundaries or the ATM cells that are output via the Receive UTOPIA Data bus. The Receive UTOPIA Interface block will assert this signal when the first byte (or word) of a new cell is present on the Receive UTOPIA Data Bus; RxUData[15:0]. ***NOTE:*** *This output pin is only active if the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*

PIN DESCRIPTIONS

PIN#	NAME	TYPE	DESCRIPTION
Power and Ground			
AA23 AC15 AC19 AC8 D8 D15 D19 F4 H23 H4 M4 R23 W4 W23	VDD VDD VDD VDD VDD VDD VDD VDD VDD VDD VDD VDD VDD VDD	***	**Power Supply Pin**
AC10 AC13 AC17 AC21 AC23 AC4 AD3 AD24 AE25 C3 C24 D4 D6 D10 D13 D17 D23 F23 K4 K23 N23 P4 U4 U23	GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND	***	**Ground**

PIN DESCRIPTIONS

PIN#	NAME	TYPE	DESCRIPTION
A4 A7 A17 A20 A21 A24 A26 B5 B8 B11 B12 B15 B22 B24 C1 C9 C18 C23 C25 D14 D22 D24 D26 E1 E2 E26 F25 G2 G25 H1 H24 J4 J24 L3 L23 M3 M23 N2 N26 P2 P26 R1 R25 T1 T25 U24 V24 Y23 AA26 AC6 AC25 AD20 AE8 AF18	N/C	****	**No Connection**

ABSOLUTE MAXIMUM RATINGS	
Power Supply.....-0.5V to +3.6V	Power Dissipation TQFP Package 1.2W
Storage Temperature.....-65°C to 150°C	Input Voltage (Any PIn).....-0.5V to VDD + 5V
Voltage at Any Pin.....-0.5V to VDD + 5 V	Input Current (Any Pin).....± 100mA

DC ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25°C, VDD = 3.3V ± 5% unless otherwise specified

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
I_{CC}	Power Supply Current		120		mA	TxUClk and RxUClk are operating at 25MHz
I_{LL}	Data Bus Tri-State Bus Leakage Current				µA	
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0		VDD	V	
V_{OL}	Output Low Voltage	0.0		0.4	V	
V_{OH}	Output High Voltage	2.4		VDD	V	I_{OC} = 1.6mA
I_{OC}	Open Drain Output Leakage Current				µA	I_{OH} = 40µA
I_{IH}	Input High Voltage Current	-10		10	µA	V_{IH} = VDD
I_{IL}	Input Low Voltage Current	-10		10	µA	V_{IL} = GND

AC ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25°C, VDD = 3.3V ± 5% unless otherwise specified

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Transmit UTOPIA Interface Block (See Figure 4)						
t_1	TxUData[15:0] to rising edge of TxUClk Setup Time	4			ns	
t_2	TxUData[15:0] Hold Time from rising edge of TxUClk	1			ns	
t_3	TxUTOPIA Write Enable Setup Time to rising edge of TxUClk	4			ns	
t_4	TxUTOPIA Write Enable Hold Time from rising edge of TxUClk	1			ns	
t_5	TxUPrty Setup Time to rising edge of TxUClk	4			ns	
t_6	TxUPrty Hold Time from rising edge of TxUClk	1			ns	
t_7	TxUSoC Setup Time to rising edge of TxUClk	4			ns	

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

Test Conditions: T_A = 25°C, VDD = 3.3V ± 5% unless otherwise specified

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_8	TxUSoC Hold Time from rising edge of TxUClk	1			ns	
t_9	TxUAddr[4:0] Setup Time to rising edge of TxUClk	4			ns	
t_{10}	TxUAddr[4:0] Hold Time from rising edge of TxUClk	1			ns	
t_{11}	TxUClav signal valid (not Hi-Z) from first TxUClk rising edge of valid and correct TxUAddr[4:0]		6	16	ns	
t_{12}	TxUClav signal Hi-Z from first TxUClk rising edge of different TxUAddr[4:0]		9	19	ns	
Transmit Cell Processor (GFC Serial Input Port)—See Figure 5						
t_{13}	Clock Period of TxGFCClk		232		ns	There will be a periodic clock gap every six clocks.
fTxGFCClk	Frequency of TxGFCClk		5.592		MHz	
t_{14}	Delay from rising edge of TxGFCClk to rising edge of TxGFCMSB pin		1.43		ns	
t_{15}	Pulse width of TxGFCMSB signal		232		ns	
t_{16}	TxGFC Data Setup time to rising edge of TxGFCClk	7			ns	
t_{17}	TxGFC Data Hold time from rising edge of TxGFCClk	3			ns	
Transmit PLCP Processor (Serial Input Port)—See Figure 6						
t_{18}	Clock Period of TxPOHClk signal		232		ns	periodically gapped
t_{19}	Delay from rising edge of TxPOHFrame signal to rising edge of TxPOHClk signal	90		113	ns	>0.5 t_{18}
t_{20}	TxPOH setup time to rising edge of TxPOHClk signal	11			ns	
t_{21}	TxPOH signal hold time from rising edge of TxPOHClk signal	3			ns	
t_{22}	TxPOHIns signal setup time to rising edge of TxPOHClk	11			ns	
t_{23}	TxPOHIns signal hold time from rising edge of TxPOHClk	3			ns	
Transmit DS3 Framer (Serial Input Port)—See Figure 7						
fTxOHClk	Frequency of TxOHClk signal		526.3		kHz	
t_{24}	Period of TxOHClk clock signal		1900		ns	44.736MHz/85
t_{25}	Delay from rising edge of TxOHFrame signal to rising edge of TxOHClk signal	950		970	ns	>0.5 t_{24}

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

Test Conditions: T_A = 25°C, VDD = 3.3V ± 5% unless otherwise specified

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_{26}	TxOH Data Setup time to rising edge of TxOHClk signal	11			ns	
t_{27}	TxOH Data Hold time from rising edge of TxOHClk signal	0			ns	
t_{28}	TxOHIns signal setup time to rising edge of TxOHClk	11			ns	
t_{29}	TxOHIns signal hold time from rising edge of TxOHClk	0			ns	
Transmit DS3 Framer (LIU Interface Port)—See Figure 8 and Figure 9						
t_{30}	Delay time of data on TxPOS or TxNEG, following the rising edge of the TxLineClk	0.7		2.0	ns	Transmit DS3 Framer is configured to update TxPOS and TxNEG on the rising edge of TxLineClk.
t_{31}	Delay time of data on TxPOS or TxNEG following the falling edge of the TxLineClk	0.7		1.5	ns	Transmit DS3 Framer is configured to update TxPOS and TxNEG on the falling edge of TxLineClk.
fTxLineClk	Clock frequency of TxLineClk		44.736		MHz	
t_{32}	Period of TxLineClk clock signal	10			ns	
t_{33}	Bit Period of data on TxPOS or TxNEG pins	10			ns	
Receive DS3 Framer (Serial Output Port)—See Figure 10						
fRxOHClk	Frequency of RxOHClk signal		526.3		kHz	
t_{34}	Period of RxOHClk clock signal		1900		ns	
t_{35}	Delay Time from rising edge of RxOHClk to RxOHFrame signal	950		970	ns	>0.5 t_{34}
t_{36}	Delay Time from rising edge of RxOHClk to valid data at RxOH	950		970	ns	>0.5 t_{34}
t_{37}	Bit Period of data at RxOH		1900		ns	
Receive DS3 Framer (LIU Interface Port)—See Figure 11 and Figure 12						
t_{38}	RxPOS/RxNEG data Setup Time to rising edge of RxLineClk	6			ns	Receive DS3 Framer is configured to sample RxPOS and RxNEG on the rising edge of RxLineClk.
t_{39}	RxPOS/RxNEG data Hold Time from rising edge of RxLineClk	3			ns	Receive DS3 Framer is configured to sample RxPOS and RxNEG on the rising edge of RxLineClk.
t_{40}	RxPOS/RxNEG data Setup Time to falling edge of RxLineClk	6			ns	Receive DS3 Framer is configured to sample RxPOS and RxNEG on the falling edge of RxLineClk.
t_{41}	RxPOS/RxNEG data Hold Time from falling edge of RxLineClk	3			ns	Receive DS3 Framer is configured to sample RxPOS and RxNEG on the falling edge of RxLineClk.

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

Test Conditions: T_A = 25°C, VDD = 3.3V ± 5% unless otherwise specified

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
fRxLineClk	Clock frequency of RxLineClk		44.736		MHz	
t_{42}	Period of RxLineClk clock signal	10			ns	
Receive PLCP Processor (Serial Output Port)—See Figure 13						
t_{43}	Clock Period of RxPOHClk signal		232		ns	
t_{44}	Delay from rising edge of RxPOHClk signal to rising edge of RxPOHFrame signal.	6		1.4	ns	
t_{45}	Delay from rising edge of RxPOHClk to Data valid at RxPOH output	3		10	ns	
t_{46}	Bit period of data at RxPOH output signal		232		ns	1 RxPOHClk pulse width
Receive Cell Processor (GFC Serial Output Port)—See Figure 14						
t_{47}	Clock Period of RxGFCClk		232		ns	
t_{48}	Delay from rising edge of RxGFCClk to rising edge of RxGFCMSB pin.	0.06		1.4	ns	
t_{49}	Pulse width of RxGFCMSB signal		232		ns	
t_{50}	Delay from rising edge of RxGFCMSB signal to first valid bit at RxGFC.		0		ns	
t_{51}	Delay from rising edge of RxGFCClk to valid bit at RxGFC.	0.9		2.4	ns	
t_{52}	Pulse width of Bit at RxGFC output.		232		ns	
Receive UTOPIA Interface Block -- See Figure 15						
t_{53}	Delay time from rising edge of RxUClk to Data Valid at RxUData[15:0]	1	9.9	16	ns	
t_{54}	Rx UTOPIA Read Enable setup time to rising edge of RxUClk	4			ns	
t_{55}	Delay time from rising edge of RxUClk to valid RxUPrty bit	1	10	16	ns	
t_{56}	Delay time from rising edge of RxUClk to valid RxUSoC bit	1	9.9	16	ns	
t_{57}	Delay time from Read Enable false to Data Bus being tri-stated	1	11.5	16	ns	
t_{58}	Delay time from Read Enable false to RxUPrty bit being tri-stated	1	12	16	ns	
t_{59}	Delay time from Read Enable false to RxUSoC bit being tri-stated	1	11.5	16	ns	
t_{60}	RxUAddr[4:0] Setup Time to rising edge of RxUClk	4			ns	
t_{61}	RxUAddr[4:0] Hold Time from rising edge of RxUClk	1			ns	

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

Test Conditions: T_A = 25°C, VDD = 3.3V ± 5% unless otherwise specified

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_{62}	RxUClav signal valid (not Hi-Z) from first RxUClk rising edge of valid and correct TxUAddr[4:0]	1	7.8	16	ns	
t_{63}	RxUClav signal Hi-Z from first RxUClk rising edge of different RxUAddr[4:0].	1	9.2	16	ns	
Microprocessor Interface—Intel -- See Figure 16 and Figure 17						
t_{64}	A8—A0 Setup Time to ALE_AS Low	3			ns	
t_{65}	A8—A0 Hold Time from ALE_AS Low.	2			ns	
t_{66}	$\overline{RD}$_DS, $\overline{WR}$_RW Pulse Width	30			ns	
Intel Type Read Operations -- See Figure 16						
t_{67}	Data Valid from $\overline{RD}$_DS Low.	6		11	ns	
t_{68}	Data Bus Floating from $\overline{RD}$_DS High.			10	ns	
t_{69}	ALE to $\overline{RD}$ Time	4			ns	
t_{70}	$\overline{RD}$ Time to :"NOT READY" (e.g., RDY_DTCK toggling "Low")	15		23	ns	
Intel Type Write Operations -- See Figure 17						
t_{71}	Data Setup Time to $\overline{WR}$_RW High	4			ns	
t_{72}	Data Hold Time from $\overline{WR}$_RW High	2			ns	
t_{73}	High Time between Reads and/or Writes	20			ns	
t_{74}	ALE to $\overline{WR}$ Time	4			ns	
t_{770}	$\overline{CS}$ Assertion to falling edge of $\overline{WR}$_RW	20			ns	
Microprocessor Interface—Motorola Read Operations -- See Figure 18						
t_{78}	A8—A0 Setup Time to falling edge of ALE_AS	5			ns	
t_{79}	A8—A0 Rising edge of $\overline{RD}$_DS to rising edge of RDY_DTCK	0			ns	
t_{80}	Rising edge of RDY_DTCK to tri-state of D[7:0]	0			ns	
Microprocessor Interface—Write Operations -- See Figure 19						
t_{78}	A8—A0 Setup Time to falling edge of ALE_AS	5			ns	
t_{81}	D[7:0] Setup Time to falling edge of $\overline{RD}$_DS	10			ns	
t_{82}	Rising edge of $\overline{RD}$_DS to rising edge of RDY_DTCK delay	0			ns	

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

Test Conditions: T_A = 25°C, VDD = 3.3V ± 5% unless otherwise specified

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Reset Pulse Width—Both Motorola and Intel Operations -- See Figure 20						
t_{90}	$\overline{\text{Reset}}$ pulse width	30				

TIMING DIAGRAMS

FIGURE 4. XRT72L73 TRANSMIT UTOPIA INTERFACE BLOCK TIMING

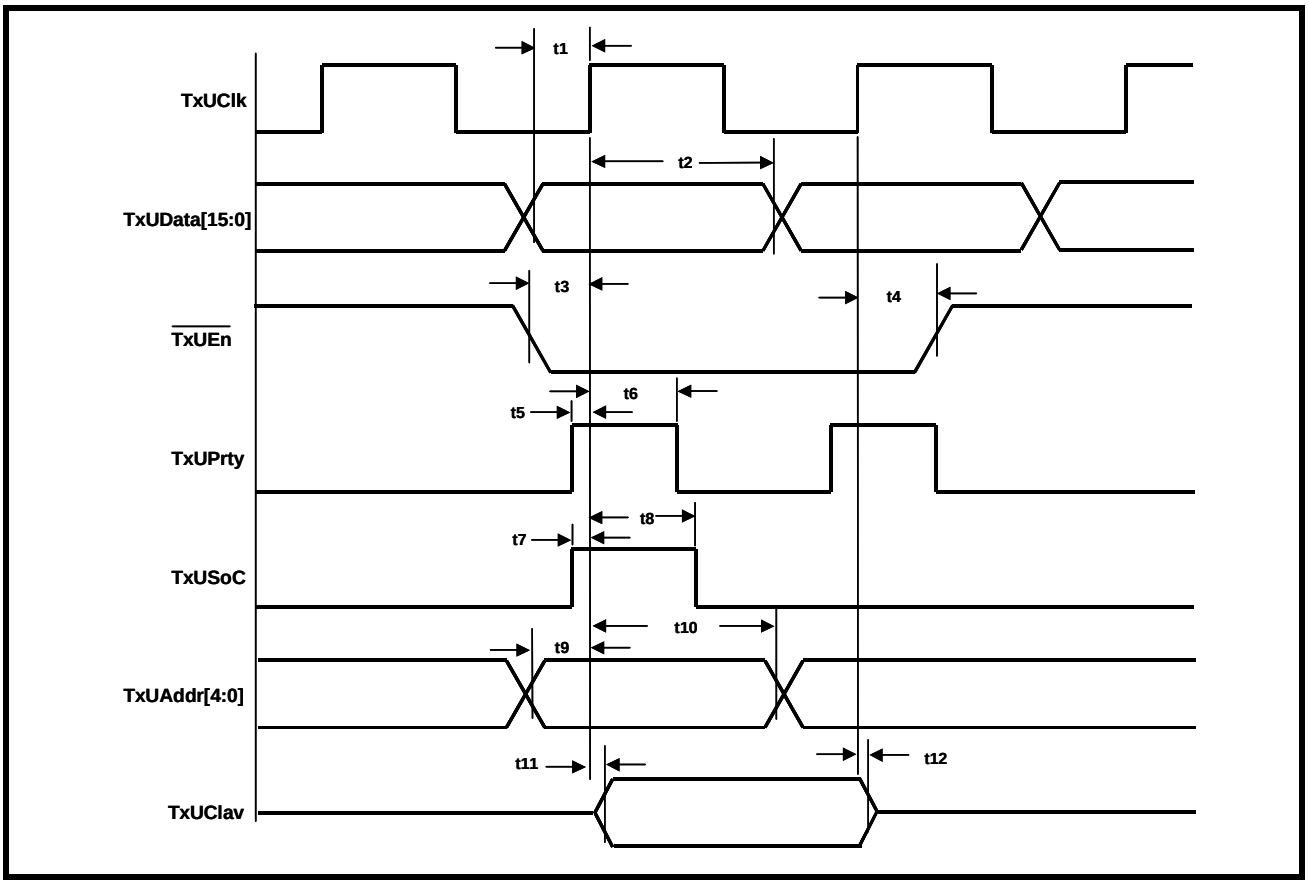


FIGURE 5. GFC NIBBLE-FIELD SERIAL INPUT INTERFACE (AT TRANSMIT CELL PROCESSOR) TIMING

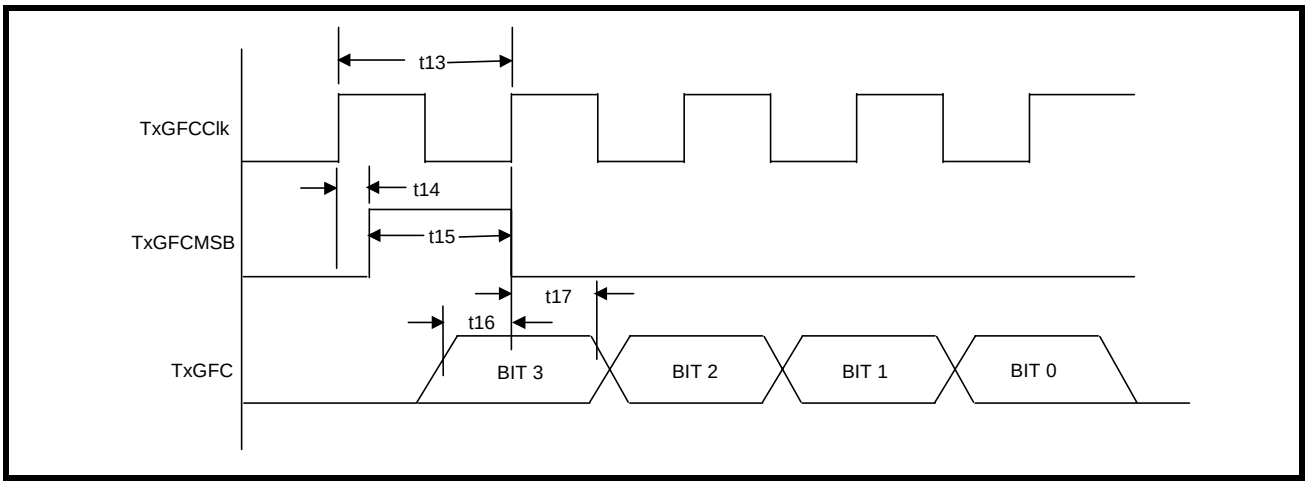


FIGURE 6. TRANSMIT PLCP PROCESSOR—POH BYTE SERIAL INPUT PORT INTERFACE TIMING

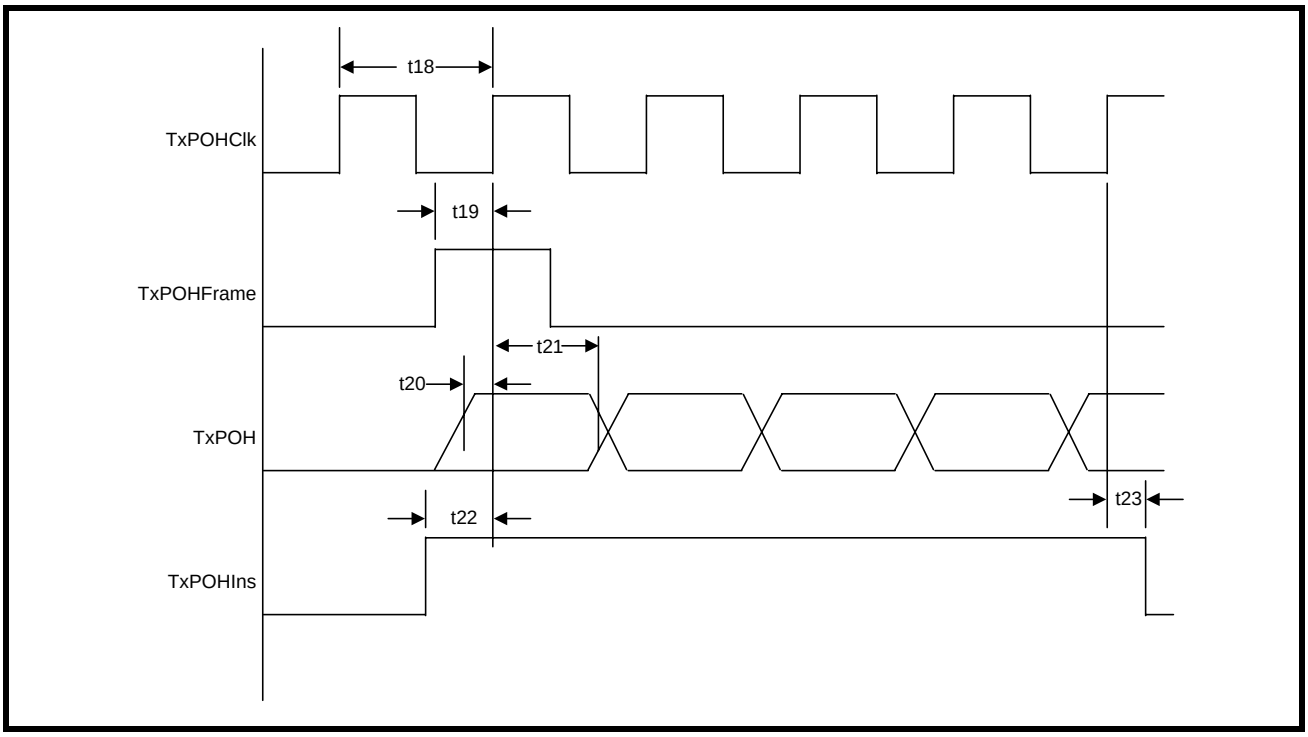


FIGURE 7. TRANSMIT DS3 FRAMER—OH BIT SERIAL INPUT PORT INTERFACE TIMING

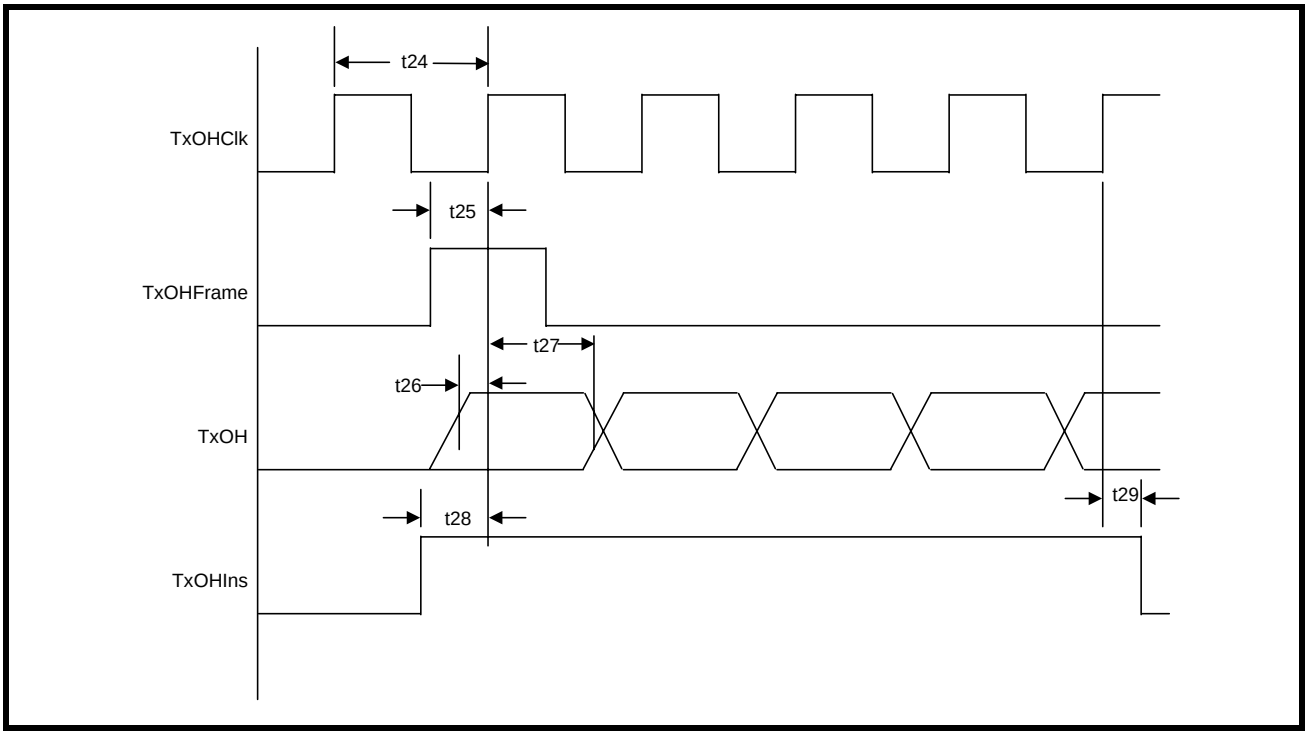


FIGURE 8. TRANSMIT DS3 FRAMER LINE INTERFACE OUTPUT TIMING (TXPOS AND TXNEG ARE UPDATED ON THE RISING EDGE OF TXLINECLK)

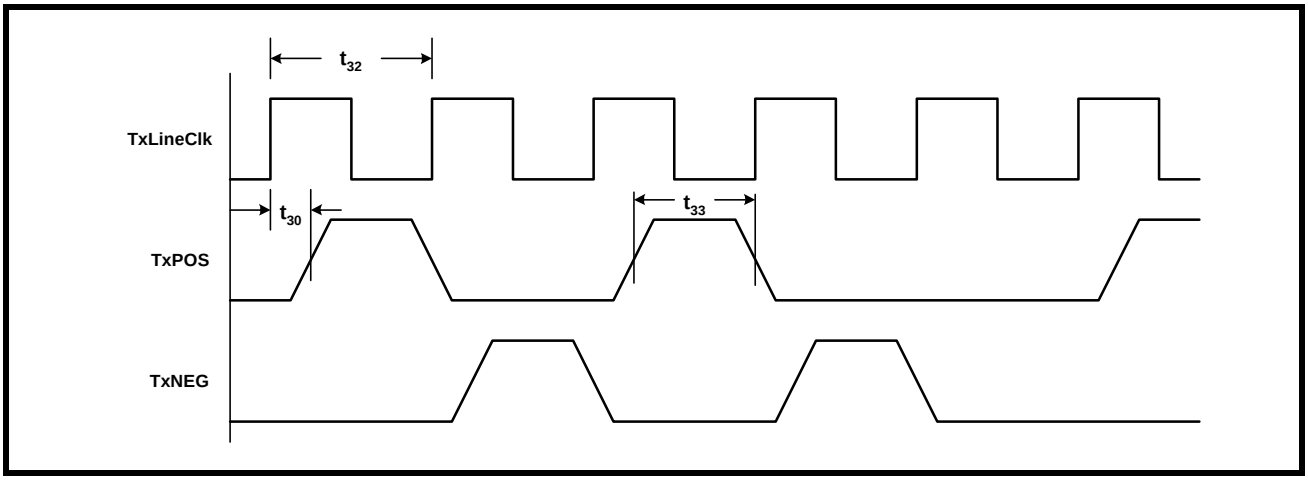


FIGURE 9. TRANSMIT DS3 FRAMER LINE INTERFACE OUTPUT TIMING (TXPOS AND TXNEG ARE UPDATED ON THE FALLING EDGE OF TXLINECLK)

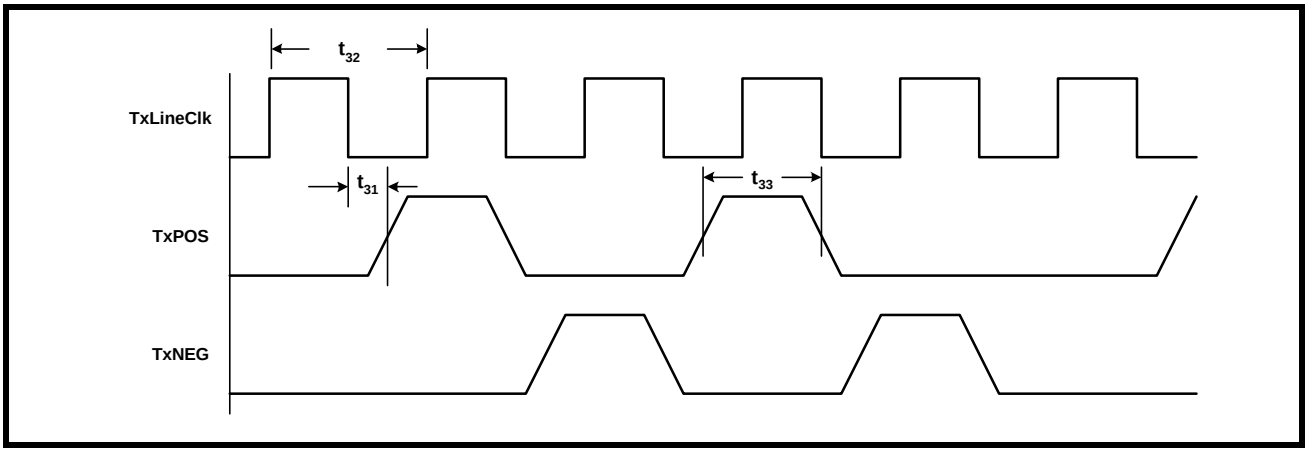


FIGURE 10. RECEIVE DS3 FRAMER—OH BIT SERIAL OUTPUT PORT INTERFACE TIMING

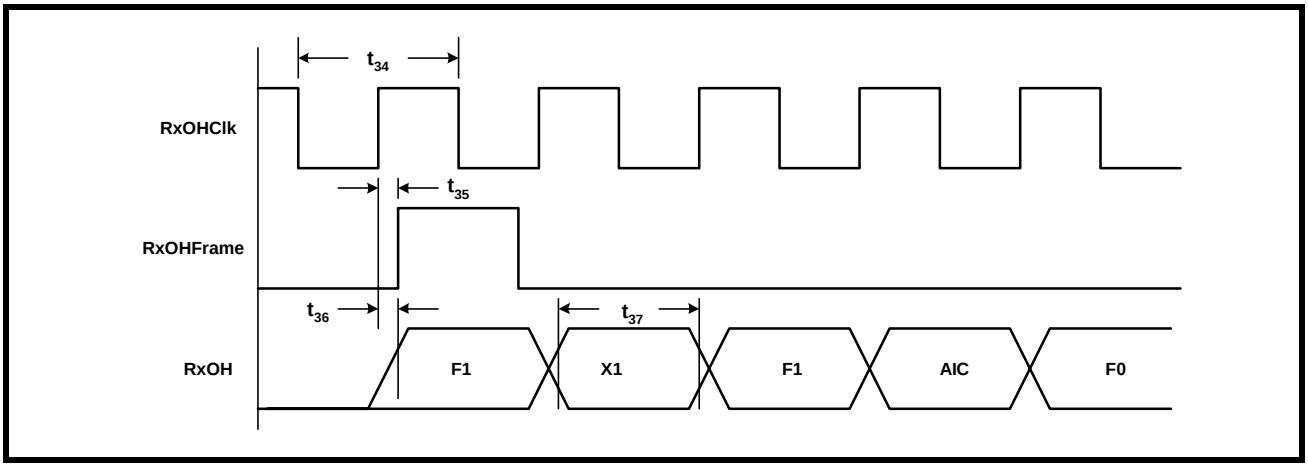


FIGURE 11. RECEIVE DS3 FRAMER LINE INTERFACE INPUT SIGNAL TIMING (RXPOS AND RXNEG ARE SAMPLED ON RISING EDGE OF RXLINECLK)

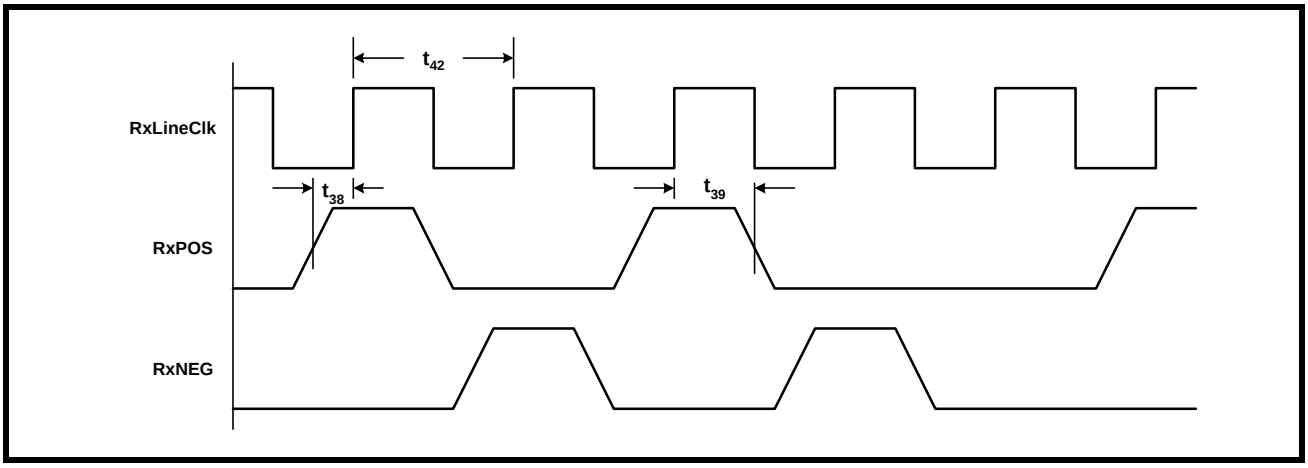


FIGURE 12. RECEIVE DS3 FRAMER LINE INTERFACE INPUT SIGNAL TIMING (RXPOS AND RXNEG ARE SAMPLED ON THE FALLING EDGE OF RXLINECLK)

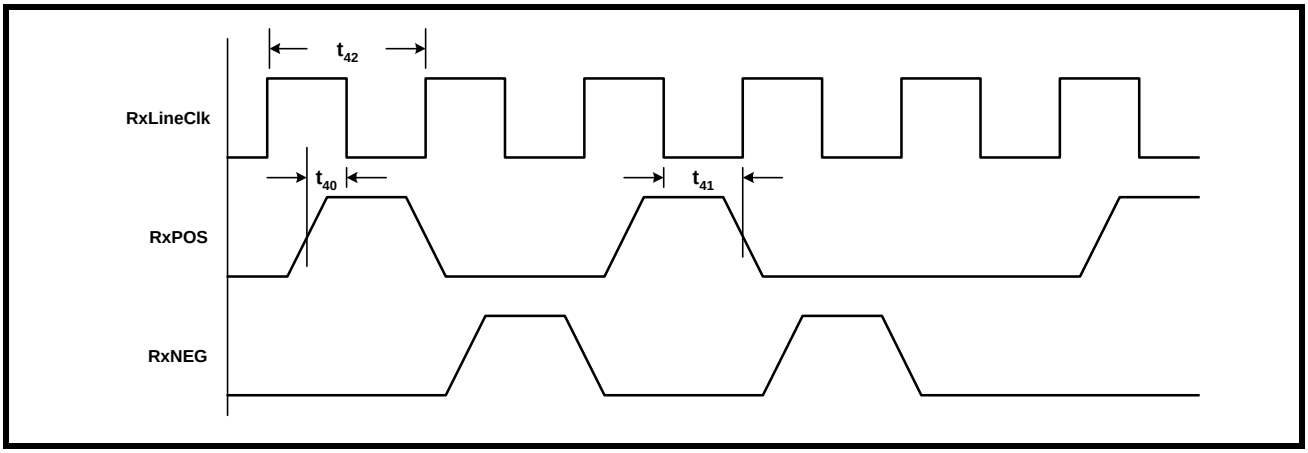


FIGURE 13. RECEIVE PLCP PROCESSOR—POH BYTE SERIAL OUTPUT PORT INTERFACE TIMING

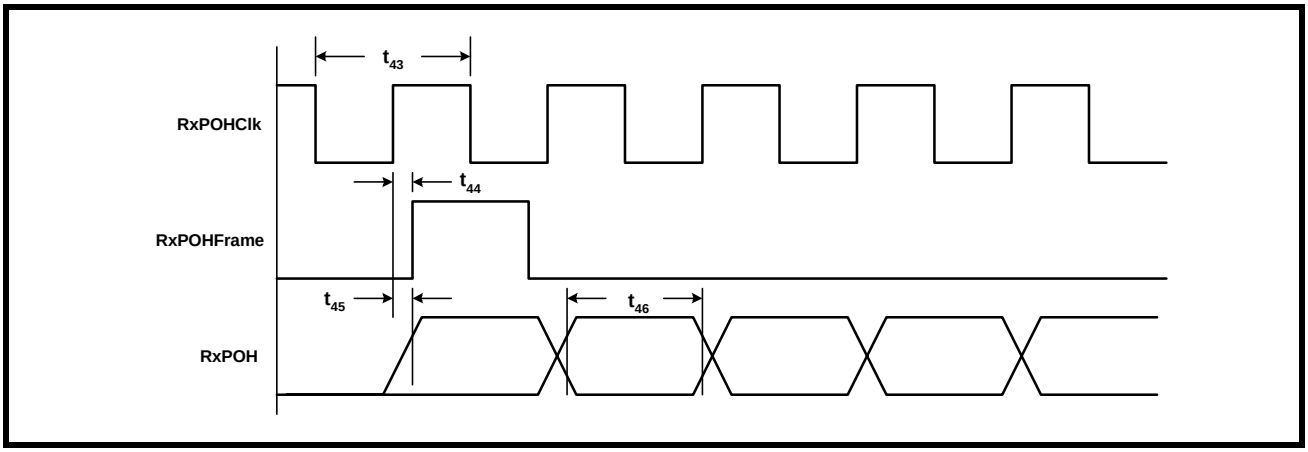


FIGURE 14. GFC NIBBLE-FIELD SERIAL OUTPUT PORT TIMING (RECEIVE CELL PROCESSOR)

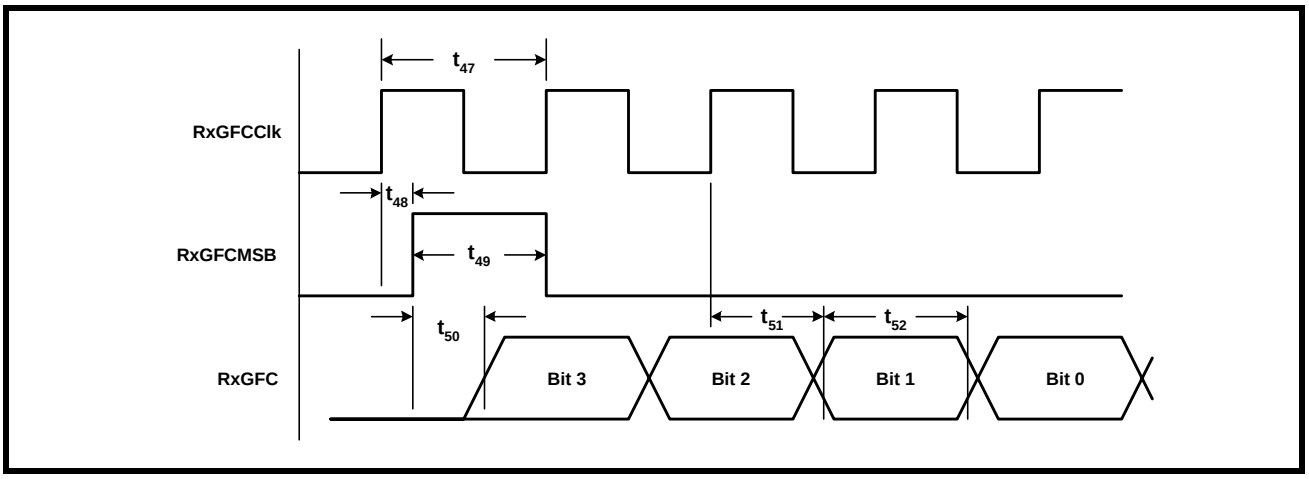


FIGURE 15. RECEIVE UTOPIA INTERFACE BLOCK TIMING

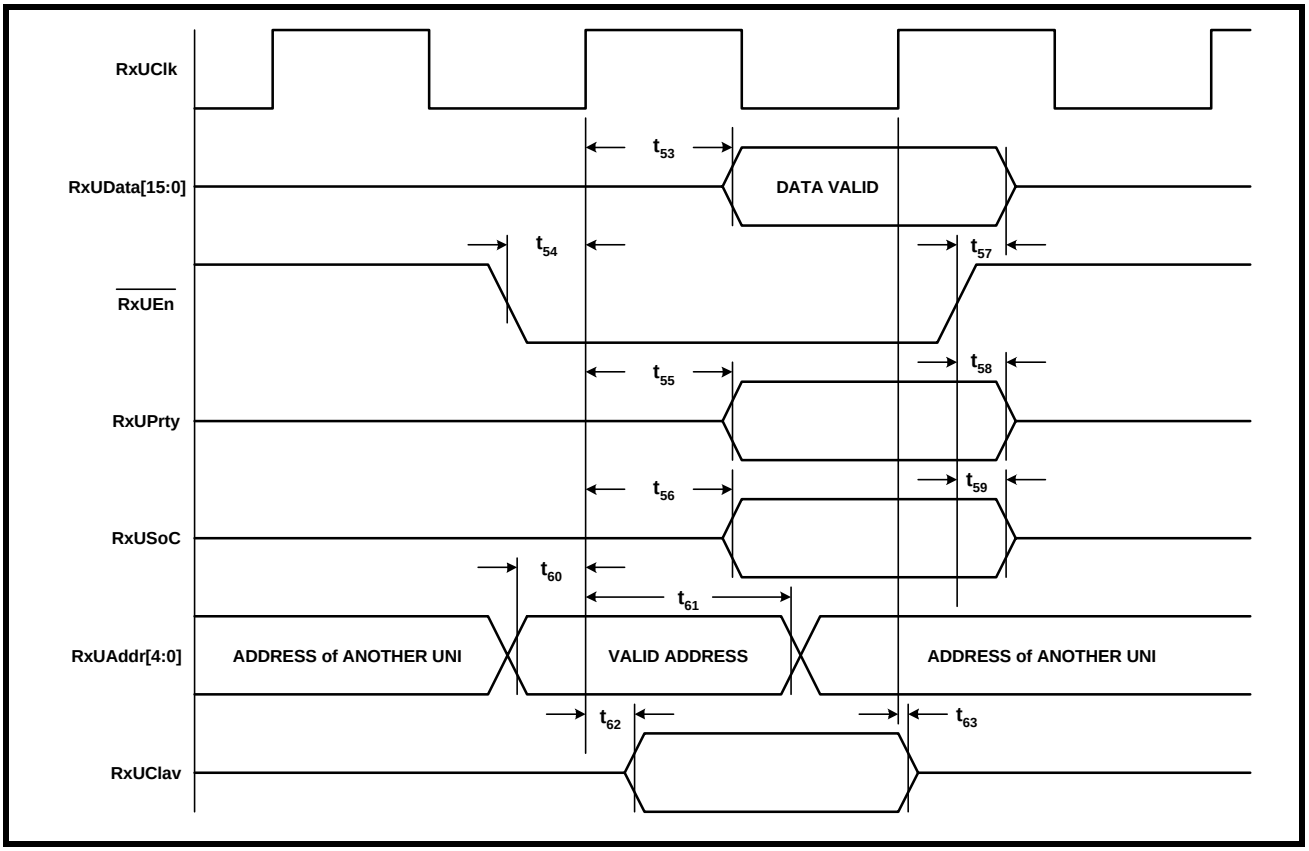


FIGURE 16. MICROPROCESSOR INTERFACE TIMING - INTEL TYPE PROGRAMMED I/O READ OPERATIONS

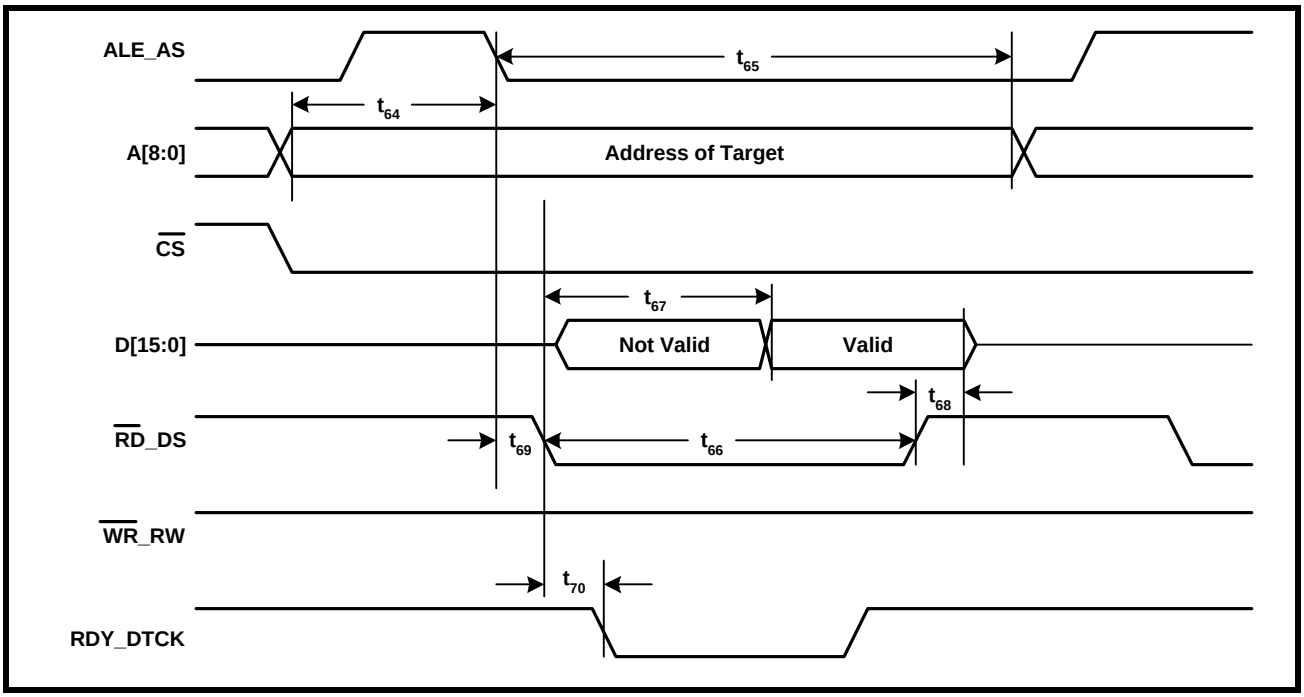


FIGURE 17. MICROPROCESSOR INTERFACE TIMING - INTEL TYPE PROGRAMMED I/O WRITE OPERATIONS

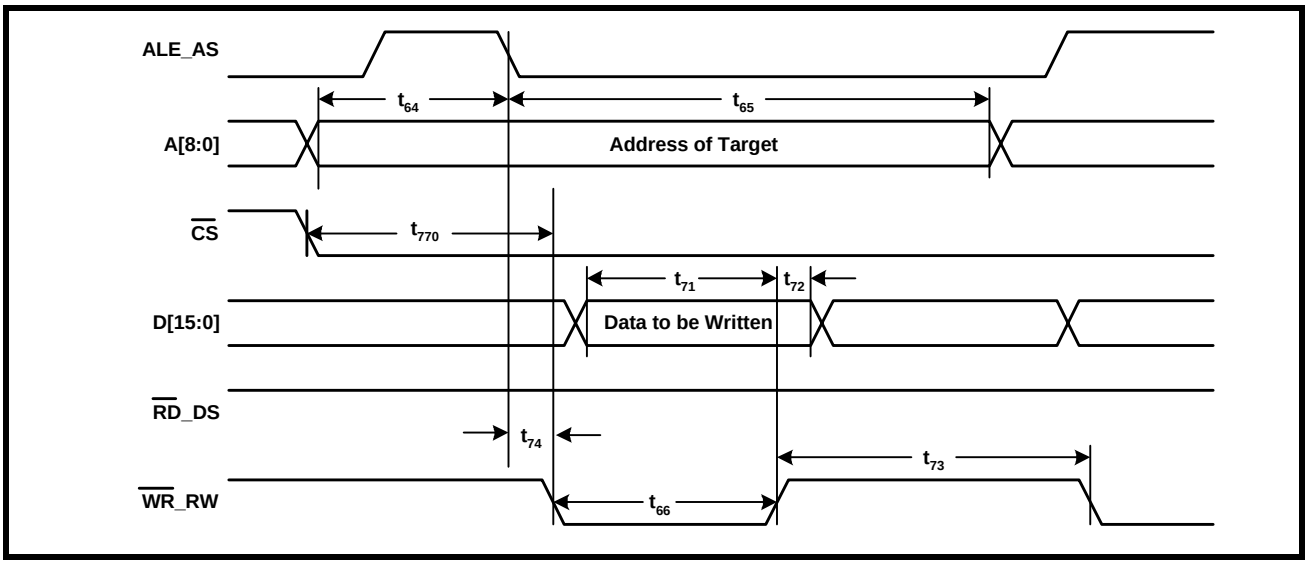


FIGURE 18. MICROPROCESSOR INTERFACE TIMING—MOTOROLA TYPE PROCESSORS (READ OPERATIONS) NON-BURST MODE

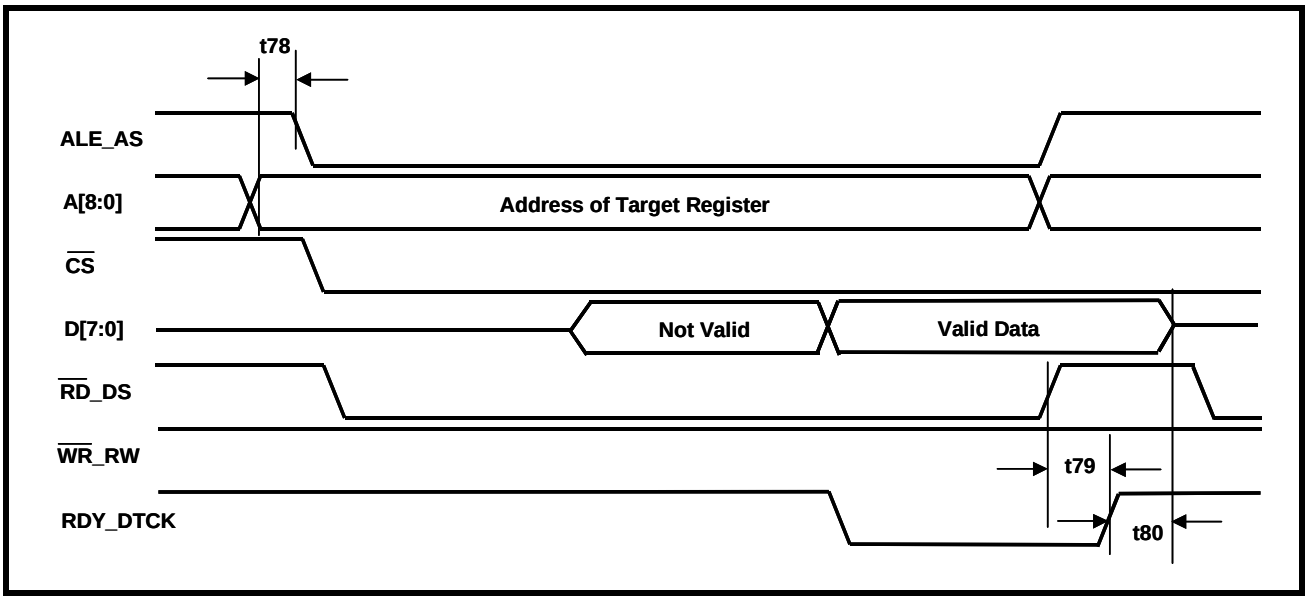


FIGURE 19. MICROPROCESSOR INTERFACE TIMING—MOTOROLA TYPE PROCESSOR (WRITE OPERATIONS) NON-BURST MODE

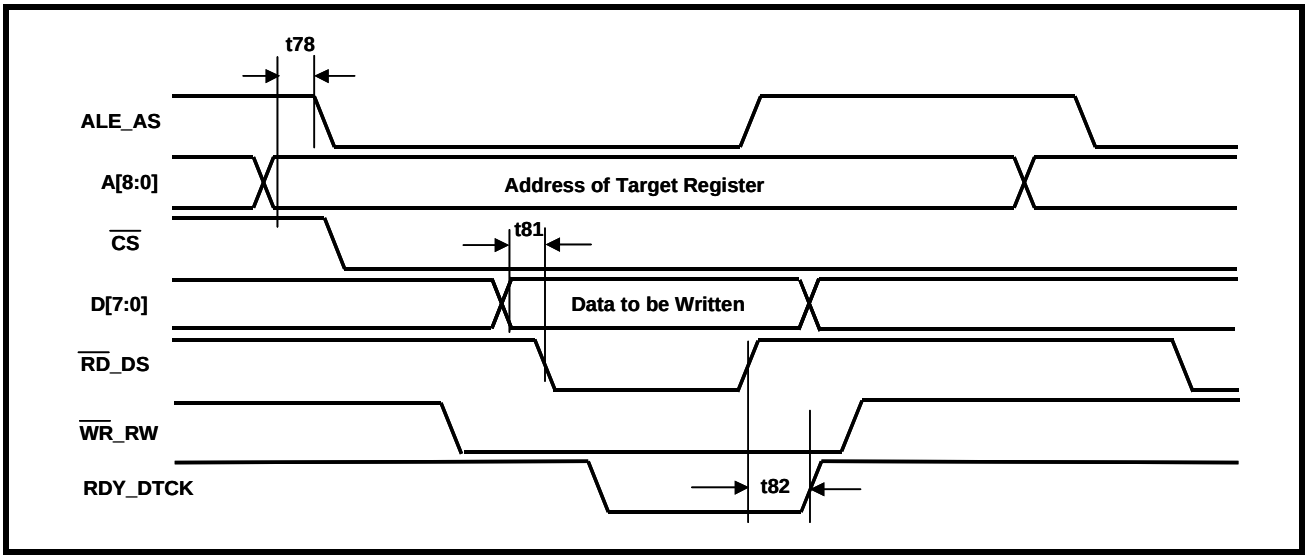
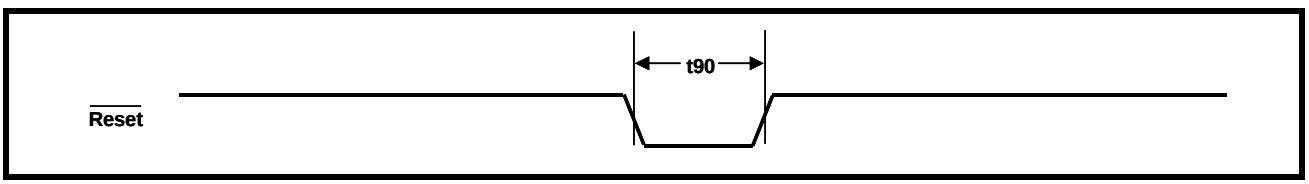


FIGURE 20. MICROPROCESSOR INTERFACE TIMING - RESET PULSE WIDTH



LIST OF REGISTERS

All even numbered registers get mapped onto the microprocessor data bus higher byte D15-D8

All Odd numbered registers get mapped onto the microprocessor data bus lower byte D7-D0

Even Numbered Register								Odd Numbered Register							
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

REGISTER SUMMARY LIST

REG. #	FUNCTION
0	UNI Operating Mode Register
1	UNI I/O Control Register
2	Part Number Register
3	Version Number Register
4	UNI Interrupt Enable Register
5	UNI Interrupt Status Register
6	Test Cell Control and Status Register
7	Test Cell Error Accumulator Holding Register
8	Test Cell Header Byte-1
9	Test Cell Header Byte-2
10	Test Cell Header Byte-3
11	Test Cell Header Byte-4
12	Test Cell Error Accumulator-MSB
13	Test Cell Error Accumulator-LSB
14	Rx DS3 Configuration and Status Register
15	Rx DS3 Status Register
16	Rx DS3 Interrupt Enable Register
17	Rx DS3 Interrupt Status Register
18	Rx DS3 FEAC Register
19	Rx DS3 FEAC Interrupt Enable/Status Register
20	Rx DS3 LAPD Control Register
21	Rx DS3 LAPD Status Register
22	Tx DS3 Configuration Register
23	Tx DS3 M-Bit Mask Register
24	Tx DS3 F-Bit Mask1 Register
25	Tx DS3 F-Bit Mask2 Register
26	Tx DS3 F-Bit Mask3 Register
27	Tx DS3 F-Bit Mask4 Register
28	Tx DS3 FEAC Configuration and Status Register

REG. #	FUNCTION
29	Tx DS3 FEAC Register
30	Tx DS3 LAPD Configuration Register
31	Tx DS3 LAPD Status/Interrupt Register
32	PMON LCV Event Count Register-MSB
33	PMON LCV Event Count Register-LSB
34	PMON Framing Bit Error Event Count Register-MSB
35	PMON Framing Bit Error Event Count Register-LSB
36	PMON P-Bit Error Count Register-MSB
37	PMON P-Bit Error Count Register-LSB
38	PMON FEBE Event Count Register-MSB
39	PMON FEBE Event Count Register-LSB
40	PMON PLCP BIP-8 Error Count Register-MSB
41	PMON PLCP BIP-8 Error Count Register-LSB
42	PMON PLCP Framing Byte Error Count Register-MSB
43	PMON PLCP Framing Byte Error Count Register-LSB
44	PMON PLCP FEBE Count Register-MSB
45	PMON PLCP FEBE Error Count Register-LSB
46	PMON Single-bit HEC Error Count-MSB
47	PMON Single-bit HEC Error Count -LSB
48	PMON Multiple-bit HEC Error Count-MSB
49	PMON Multiple-bit HEC Error Count-LSB
50	PMON Received Idle Cell Count/PRBS Error Count-MSB
51	PMON Received Idle Cell Count/PRBS Error Count-LSB
52	PMON Receive Valid Cell Count-MSB
53	PMON Receive Valid Cell Count-LSB
54	PMON Discarded Cell Count-MSB
55	PMON Discarded Cell Count-LSB
56	PMON Transmit Idle Cell Count-MSB

REG. #	FUNCTION
57	PMON Transmit Idle Cell Count-LSB
58	PMON Transmit Valid Cell Count-MSB
59	PMON Transmit Valid Cell Count-LSB
60	PMON Holding Register
61	One Second Error Status Register
62	LCV - One Second Accumulator Register-MSB
63	LCV - One Second Accumulator Register-LSB
64	P-Bit Errors-One Second Accumulator Register-MSB
65	P-Bit Errors-One Second Accumulator Register- LSB
66	HEC Byte Errors-One Sec Accumulator Register-MSB
67	HEC Byte Errors-One Sec Accumulator Register-LSB
68	Rx PLCP Configuration/Status Register
69	Rx PLCP Interrupt Enable Register
70	Rx PLCP Interrupt Status Register
71	Future Use
72	Tx PLCP FA1 Byte Error Mask Register
73	Tx PLCP FA2 Byte Error Mask Register
74	Tx PLCP BIP-8 Error Mask
75	Tx PLCP G1 Byte Register
76	Rx CP Configuration Register
77	Rx CP Additional Configuration Register
78	Rx CP Interrupt Enable Register
79	Rx CP Interrupt Status Register
80	Rx CP Idle Cell pattern Header Byte-1
81	Rx CP Idle Cell pattern Header Byte-2
82	Rx CP Idle Cell pattern Header Byte-3
83	Rx CP Idle Cell pattern Header Byte-4
84	Rx CP Idle Cell Mask Header Byte-1
85	Rx CP Idle Cell Mask Header Byte-2
86	Rx CP Idle Cell Mask Header Byte-3
87	Rx CP Idle Cell Mask Header Byte-4
88	Rx CP User Cell Filter Pattern Header Byte-1
89	Rx CP User Cell Filter Pattern Header Byte-2
90	Rx CP User Cell Filter Pattern Header Byte-3

REG. #	FUNCTION
91	Rx CP User Cell Filter Pattern Header Byte-4
92	Rx CP User Cell Filter Mask Header Byte-1
93	Rx CP User Cell Filter Mask Header Byte-2
94	Rx CP User Cell Filter Mask Header Byte-3
95	Rx CP User Cell Filter Mask Header Byte-4
96	Tx CP Control Register
97	Tx CP OAM Register
98	Tx CP HEC Error Mask Register
99	Future Use
100	Tx CP Idle Cell Pattern Header Byte-1
101	Tx CP Idle Cell Pattern Header Byte-2
102	Tx CP Idle Cell Pattern Header Byte-3
103	Tx CP Idle Cell Pattern Header Byte-4
104	Tx CP Idle Cell Pattern Header Byte-5
105	Tx CP Idle Cell Payload Register
106	Utopia Configuration Register
107	Rx UTOPIA Interrupt Enable/Status Register
108	Rx UTOPIA Address
109	Rx UTOPIA FIFO Status Register
110	Tx UTOPIA Interrupt/Status Register
111	Future Use
112	Tx UTOPIA Address
113	Tx UTOPIA Status Register
114	Line Interface Drive Register
115	Line Interface Scan Register
116	PMON CP-Bit Error Event Count Register - MSB
117	PMON CP-Bit Error Event Count Register - LSB
118	Frame CP-Bit Errors-One Second Accumulator Register - MSB
119	Frame CP-Bit Errors-One Second Accumulator Register - LSB
120-133	Unused

TABLE 1: UNI OPERATING MODE REGISTER

REGISTER 0 **UNI OPERATING MODE REGISTER** **HEX ADDRESS: 0X00**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Local Loop-back	R/W	0	0: Local Loop-back Mode operation is disabled 1: Local Loop-back Mode operation is enabled. The Transmit stream on TxPOS, TxNEG pins are looped back into the receive RxPOS, RxNEG pins
6	Cell Loop-back	R/W	0	0: Cell Loop-back Mode operation is disabled 1: Cell Loop-back Mode operation is enabled. Cells from the Receive Cell Processor block are written into the Tx FIFO. ***NOTE:*** *This bit-field is only active if the XRT72L73 is operating in the ATM UNI Mode.*
5	PLCP Loop-back	R/W	0	0: PLCP Loop-back Mode operation is disabled 1: PLCP Loop-back Mode operation is enabled. PLCP frames are looped from the Transmit PLCP Processor block into the Receive PLCP Processor Block. ***NOTE:*** *This bit-field is only active if the XRT72L73 is operating in the ATM UNI/ PLCP Mode.*
4	RESET	R/W	0	0: Normal Operation 1: A “0” to “1” transition causes a reset of the UNI/Framer device.
3	Direct-mapped ATM	R/W	1	0: PLCP Mode is enabled. Transmit and Receive PLCP Processor blocks are enabled. 1: Direct-Mapped ATM Mode. Transmit and Receive PLCP Processor blocks are disabled. ***NOTE:*** *This bit-field is only active if the XRT72L73 is operating in the ATM UNI Mode.*
2	C-BIT/M13	R/W	0	0: XRT72L73 will support the “DS3/C-Bit Parity” Framing Format. 1: XRT72L73 will support the “DS3/M13” Framing Format.
1	Timing Reference Select (1)	R/W	1	**PLCP block** 00: Transmitter timings taken from the Receive PLCP Processor (Loop-Timing). 01: 8 kHz reference signal on 8kRef pin used for stuffing and framing 10: StuffCtl is used for stuffing control, framing is asynchronous on power on 11: Fixed stuffing pattern is used. Framing is asynchronous on power on **Framer block** 00: Transmitter timings are taken from the Receive DS3 Framer (Loop-Timing) 01: Framing is asynchronous on power-on, and TxInClk is used as the transmit clock 10: Transmitter follows external pin (TxFrameRef) framing reference 11: Framin is asynchronous on power-on, and TxInClk is used as the transmit clock
0	Timing Reference Select (0)	R/W	1	

TABLE 2: UNI I/O CONTROL REGISTER

REGISTER 1 **UNI I/O CONTROL REGISTER** **HEX ADDRESS:0X01**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Disable LOC	R/W	1	0: Internal loss of clock detection circuit enabled 1: Internal loss of clock detection circuit disabled
6	LOC	RO	0	0: Indicates no Loss of Clock 1: Indicates TxLnCLk or RxLineLck is not present. Bit is valid only if Disable LOC is 0
5	INTERRUPT ENABLE RESET	R/Q	1	0: Interrupt enable register bits are not reset by the chip when active interrupts are read. 1: Reading of status of an active interrupt resets the corresponding interrupt enable bit.
4	B3ZS*/AMI	R/W	0	0: B3ZS Encoding and Decoding is enabled. 1: B3ZS Encoding and Decoding are disabled. ***NOTE:*** *Dual-Rail data must be selected (via bit 3 of this register) if B3ZS Encoding/Decoding are enabled.*
3	$\overline{\text{SINGLE-RAIL}}$/DUAL-RAIL	R/W	0	0: Dual-Rail data is transmitted and received between the XRT72L73 and the LIU IC. 1: Single-Rail data is transmitted and received between the XRT72L73 and the LIU IC.
2	Tx Clock Invert	R/W	0	0: Outputs on TxPOS, TxNEG are updated on rising edge of TxClk 1: Ouputs on TxPOS, TxNEG are updated on falling edge of TxClk
1	Rx Clock Invert	R/W	0	0: Inputs on RxPOS, RxNEG are sampled at rising edge of RxClk 1: Inputs on RxPOS, RxNEG are sampled at falling edge of RxClk
0	REFRAME	R/W	0	0 to 1 transition forces the Receive DS3 Framer block to start frame search

TABLE 3: PART NUMBER REGISTER

REGISTER 2 **PART NUMBER REGISTER** **HEX ADDRESS: 0X02**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Part Number	RO	0x04	Hex: 0x04 (0000 0100)

TABLE 4: VERSION NUMBER REGISTER

REGISTER 3 **VERSION NUMBER REGISTER** **HEX ADDRESS: 0X03**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
0-7	Version Number	RO	0x01	Hex 0x04: (0000 0001)

TABLE 5: UNI INTERRUPT ENABLE REGISTER

REGISTER 4 **UNI INTERRUPT ENABLE REGISTER** **HEX ADDRESS 0X04**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Rx DS3 INTERRUPT ENABLE	R/W	0	0: Receive DS3 Framer block interrupts are disabled 1: Receive DS3 Framer interrupts are enabled (at the Block Level)
6	Rx PLCP INTERRUPT ENABLE	R/W	0	0: Receive PLCP Processor block interrupts are disabled 1: Receive PLCP Processor block interrupts enabled (at the Block Level) ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI/PLCP" Modes.*
5	Rx CP INTERRUPT ENABLE	R/W	0	0: Receive Cell Processor block interrupts are disabled 1: Receive Cell Processor block interrupts are enabled (at the Block Level) ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*
4	Rx UTOPIA INTER-RUPT ENABLE	R/W	0	0: Receive UTOPIA Interface block interrupts are disabled 1: Receive UTOPIA Interface block interrupts are enabled (at the Block Level) ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*
3	Tx UTOPIA INTER-RUPT ENABLE	R/W	0	0: Transmit UTOPIA Interface block Interrupts are disabled 1: Transmit UTOPIA Interface block Interrupts are enabled (at the Block Level) ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI' Mode.*
2	Tx CP Interrupt Enable	R/W	0	0: Transmit Cell Processor interrupts are disabled 1: Transmit Cell Processor interrupts are enabled (at the Block Level). ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*
1	Tx DS3 Interrupt Enable	R/W	0	0: Transmit DS3 Framer block interrupts are disabled 1: Transmit DS3 Framer block interrupts are enabled (at the Block Level).
0	One Sec Interrupt Enable	R/W	0	0: One second interrupt disabled 1: One second interrupt enabled

TABLE 6: UNI INTERRUPT STATUS REGISTER

REGISTER 5 **UNI INTERRUPT STATUS REGISTER** **HEX ADDRESS: 0X05**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Rx DS3 Interrupt Status	RO	0	0: No pending interrupt from the Receive DS3 Framer block 1: Pending interrupt(s) from the Receive DS3 Framer block are awaiting service.
6	Rx PLCP Interupt Status	RO	0	0: No pending interrupt from the Receive PLCP Processor block 1: Pending interrupt(s) from the Receive PLCP Processor block are awaiting service. ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI/PLCP" Modes.*
5	Rx CP Interrupt Status	RO	0	0: No pending interrupt from the Receive Cell Processor block. 1: Pending interrupt(s) from the Receive Cell Processor block are awaiting service. ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*
4	Rx UTOPIA Interrupt Status	RO	0	0: No pending interrupt from the Receive UTOPIA Interface block. 1: Pending interrupt(s) from Receive UTOPIA Interface block are awaiting service. ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*
3	Tx UTOPIA Interrupt Status	RO	0	0: No pending interrupt from the Transmit UTOPIA Interface block. 1: Pending interrupt(s) from the Transmit UTOPIA Interface block are awaiting service. ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*
2	Tx CP Interrupt Status	RO	0	0: No pending interrupt from the Transmit Cell Processor block 1: Pending interrupt from the Transmit Cell Processor block is awaiting service. ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*
1	Tx DS3 Interrupt Status	RO	0	0: No pending interrupt from the Transmit DS3 Framer block 1: Pending interrupt(s) from the Transmit DS3 Framer block are awaiting service.
0	One Sec Interrupt Status	RUR	0	0: No pending interrupt requests from the One Second pulse generator 1: Pending One Second interrupt is awaiting service.

TABLE 7: TEST CELL CONTROL AND STATUS REGISTER

REGISTER 6 **TEST CELL CONTROL AND STATUS REGISTER** **HEX ADDRESS: 0X06**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	CLEAR CHANNEL ENABLE	R/W	0	0: Configures the XRT72L73 to operate in the “ATM UNI” Mode. 1: Configures the XRT72L73 to operate in the “Clear Channel Mode”
6	Tx Overheard Extracted Data Input	R/W	0	0: Transmit Payload Data Interface does not accept overhead bits via the “TxSerData” input pin 1: Transmit Payload Data Input Interface block accepts overhead bits via the “TxSerData” input pin. ***NOTE:*** *This register is only active if the XRT72L73 has been configured to operate in the “ATM UNI” Mode.*
5	Unused	RO	0	
4	TEST CELL ENABLE/ PRBS ENABLE	R/W	0	**If the XRT72L73 has been configured to operate in the ATM UNI Mode:** 0: Disables the Test Cell Generator and Receiver 1: Enables the Test Cell Generator and Receiver. The test cell Generator will begin generating an inserting “Test Cell” into the “outbound” DS3 data stream. The Test Cell Receiver will begin to “look for” Test Cells, and acquire a PRBS pattern with the “payload bytes” of these test cells. **If the XRT72L73 has beenconfigured to operate in the “Clear Channel Framer” Mode:** 0: Disables the PRBS Generator and Receiver 1: Enables the PRBS Generator and Receiver. The PRBS Generator will begin to insert a “PRBS” pattern into the “outbound” DS3 data strream. The PRBS Receiver will begin to “look” for this PRBS pattern and acquire “PRBS Lock”
3	Reserved	R/W	0	This bit-field is unused
2	ONE-SHOT TEST	R/W	0	O: Continous Mode - Test cells are generated as long as the “TEST CELL ENABLE” bit is high 1: Burst Mode - 0 to 1 transition in the “TEST CELL ENABLE” bit results in the generation of 1024 test cells. ***NOTE:*** *This register is only active if the XRT72L73 has been configured to operate in the “ATM UNI” Mode.*
1	ONE SHOT DONE	RO	0	0: Test Cell Generator is currently generating its burst of 1024 Test Cells. 1: Test Cell Generator has completed generating its “latest” burst of 1024 Test Cells. This bit-field is reset when a new cycle is begun by a 0 to 1 transition within the “TEST CELL ENABLE” bit-field. ***NOTE:*** *This bit-field is only active if both of the following conditions are true.* *1. The XRT72L73 has been configured to operate in the “ATM UNI Mode* *2. The Test Cell Generator/Receiver has been configured to operate in the “Burst” Mode.*
0	PRBS LOCK	RO	0	0: The Test Cell Receiver (for “ATM UNI” Applications” or the PRBS Receiver (for “Clear-Channel Framer” applications) has not yet acquired “Pattern Lock” with the “PRBS” data bening generated by the Test Cell Generator/PRBS Generator. 1: The Test Cell Receiver/PRBS Receiver has been able to acquire Pattern Lock with the PRBS data being generated by the Test Cell Generator. ***NOTE:*** *Once the Test Cell Receiver/PRBS Receiver has acquired PRBS Lock, then it will begin to record “Pattern Bit Error” events within the Test Cell Error Count (or PRBS Error Count) Registers.*

TABLE 8: TEST CELL ERROR ACCUMULATOR HOLDING REGISTER

REGISTER 7 **TEST CELL ERROR ACCUMULATOR HOLDING REGISTER** **HEX ADDRESS: 0X07**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	TEST CELL HOLDING REGISTER	RO	0x00	Holds the "Unread" byte of the 16-bit Test Cell Error Accumulator, when that register is read. The XRT72L73 will transfer the contents of the "Unread" byte to this "Holding" register, anytime the Bidirectional Data Bus (of the Microprocessor Interface) is configured to be 8-bits wide. ***NOTE:*** *This register is only active if the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*

TABLE 9: TEST CELL HEADER BYTE-1

REGISTER 8 **TEST CELL HEADER BYTE-1** **HEX ADDRESS: 0X08**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	TEST CELL HEADER BYTE 1	R/W	0x11	**Test Cell Header Byte - 1** Permits the user to define the value of "Header Byte # 1" within each Test Cell which is generated by the "Test Cell Generator". ***NOTE:*** *This register is only active if the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*

TABLE 10: TEST CELL HEADER BYTE-2

REGISTER 9 **TEST CELL HEADER BYTE-2** **HEX ADDRESS: 0X09**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	TEST CELL HEADER BYTE 2	R/W	0x22	**Test Cell Header Byte - 2** Permits the user to define the value of "Header Byte # 2" within each Test Cell which is generated by the "Test Cell Generator". ***NOTE:*** *This register is only active if the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*

TABLE 11: TEST CELL HEADER BYTE-3

REGISTER 10 **TEST CELL HEADER BYTE-3** **HEX ADDRESS: 0X0A**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	TEST CELL HEADER BYTE 3	R/W	0x33	**Test Cell Header Byte - 3** Permits the user to define the value of "Header Byte # 3" within each Test Cell which is generated by the "Test Cell Generator". ***NOTE:*** *This register is only active if the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*

TABLE 12: TEST CELL HEADER BYTE-4

REGISTER 11 **TEST CELL HEADER BYTE-4** **HEX ADDRESS: 0X0B**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	TEST CELL HEADER BYTE 4	R/W	0x44	**Test Cell Header Byte - 4** Permits the user to define the value of "Header Byte # 4" within each Test Cell which is generated by the "Test Cell Generator". ***NOTE:*** *This register is only active if the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*

TABLE 13: TEST CELL ERROR ACCUMULATOR - MSB

REGISTER 12 **TEST CELL ERROR ACCUMULATOR - MSB** **HEX ADDRESS: 0X0C**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	TEST CELL ERROR - MSB	RUR	0x00	**Test Cell Accumulator register - MSB** This register, along with "TEST CELL ERROR - LSB" contains the number of bit errors accumulated since the last read of these registers. This particular register contains the "Most Significant Byte" value of the total number of Test Cell Errors. ***NOTE:*** *This register is only active if the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*

TABLE 14: TEST CELL ERROR ACCUMULATOR - LSB

REGISTER 13 **TEST CELL ERROR ACCUMULATOR - LSB** **HEX ADDRESS: 0X0D**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	TEST CELL ERROR - LSB	RUR	0x00	**Test Cell Accumulator register - LSB** This register, along with "TEST CELL ERROR - MSB" contains the number of bit errors accumulated since the last read of these registers. This particular register contains the "Least Significant Byte" value of the total number of Test Cell Errors. ***NOTE:*** *This register is only active if the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*

TABLE 15: RX DS3 CONFIGURATION AND STATUS REGISTER

REGISTER 14 **RX DS3 CONFIGURATION AND STATUS REGISTER** **HEX ADDRESS: 0X0E**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Rx AIS	RO	0	**Receive AIS Alarm Indicator:** 0: Indicates that the Receive DS3 Framer block is NOT detecting the "AIS" (Alarm Indication Signal) pattern, within the inbound DS3 data stream. 1: Indicates that the Receive DS3 Framer block is currently detecting the "AIS" pattern within the "inbound" DS3 data stream.
6	Rx LOS	RO	0	**Receive LOS Alarm Indicator:** 0: Indicates that the Receive DS3 Framer block is NOT currently declaring an LOS (Loss of Signal) condition. 1: Indicates that the Receive DS3 Framer block is currently declaring an LOS (Loss of Signal) condition.
5	Rx Idle	RO	0	**Receive Idle Pattern Indicator:** 0: Indicates that the Receive DS3 Framer block is NOT currently detecting the "Idle" pattern, within the inbound DS3 data stream. 1: Indicates that the Receive DS3 Framer block is currently detecting the "Idle" pattern within the inbound DS3 data stream.
4	Rx OOF	RO	1	**Receive OOF (Out of Frame) Alarm Indicator:** 0: Indicates that the Receive DS3 Framer block is NOT currently declaring the "OOF (Out of Frame) condition. 1: Indicates that the Receive DS3 Framer block is currently declaring the "OOF" (Out of Frame) condition.
3	Internal LOS Disable	R/W	0	0: On chip LOS detector is disabled. The XRT72L73 will only declare LOS (Loss of Signal) is the "RLOS" input pin is pulled "high". 1: On chip LOS detected is enabled. The XRT72L73 will declare and clear LOS based upon the absence of a certain number of pulses in the incoming DS3 data stream.
2	Framing On Parity	R/W	0	**Framing On-Parity (In-Frame Declaration Criteria):** 0: Receive DS3 Framer block declares the "Inframe" condition after "F-bit" and "M-bit synchronization" have been achieved. P-bit checking is not a part of "Frame Acquisition" process. 1: Receive DS3 Framer block declares the "Inframe" condition after "F-bit" and "M-bit synchronization" process. Additionally, the Receive DS3 Framer block must also detect valid (e.g., un-erred) P-bits.
1	Fsync Algo	R/W	0	0: OOF (Receive Out of Frame) condition is declared when 6 out of 16 consecutive F bits are in error 1: OOF (Receive Out of Frame) condition is declared when 3 out of 16 consecutive F bits are in error
0	Msync Algo	R/W	0	0: M-bit errors do not result in declaration of OOF 1: OOF is declared when M-bits in 3 out of 4 frames are in error.

TABLE 16: RXDS3 STATUS REGISTER

REGISTER 15 **RXDS3 STATUS REGISTER** **HEX ADDRESS:0X0F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-5	Unused	RO	0	
4	Rx FERF	RO	0	**Receive FERF (Far-End Receive Failure) Alarm:** 0: The Receive DS3 Framer block is NOT currently declaring the “FERF” condition. 1: The Receive DS3 Framer block is currently declaring the “FERF” condition.
3	Rx AIC	RO	0	**Receive AIC (Application Identification Channe) State:** 0: Indicates that the AIC bit-field was set to “0” within two or more of the last 15 M-frames. This indicates that the inbound DS3 data stream is of the “M13 Framing” format. 1: Incoming frame is found to be in the C-bit format (AIC bit = 1) for at least 63 consecutive M-frames. This indicates that the inbound DS3 data stream is of the “C-bit Parity” Framing format.
2	Rx FEBE(2)	RO	0	**Received FEBE (Far-End-Block Error) Value:** RxFEBE[2:0] contains the value of the most recently received FEBE value. When RxFEBE[2:0] = 011, this indicates that the Remote Terminal has detected CP-bits or Framing Bit Errors in its DS3 data stream. When RxFEBE[2:0] = 111, this indicates that the Remote Terminal is not currently detecting any Framing Bit or CP-bit errors in its DS3 data stream. ***NOTE:*** *These bit-fields are only active if the XRT72L73 is configured to support the “C-bit Parity” Framing format.*
1	RxFEBE(1)	RO	0	
0	RxFEBE(0)	RO	0	

TABLE 17: RX DS3 INTERRUPT ENABLE REGISTER

REGISTER 16 **RX DS3 INTERRUPT ENABLE REGISTER** **HEX ADDRESS: 0X10**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	CP Bit Error Interupt Enable	R/W	0	0: Detection of CP-Bit Error Interrupt is disabled 1: Generates Interrupt upon Detection of CP (Path Parity) bit Error.
6	LOS Interrupt Enable	R/W	0	0: Change in LOS Condition Interrupt is disabled 1: Generates interrupt upon change of LOS (Loss of Signal) status
5	AIS Interrupt Enable	R/W	0	0: Change in AIS Condition Interrupt is disabled 1: Generates interrupt upon change of AIS (Alarm Indication Signal) status.
4	Idle Interrupt Enable	R/W	0	0: Change in Idle Condition Interrupt is disabled 1: Generates interrupt upon change of IDLE status
3	FERF Interrupt Enable	R/W	0	0: Change in FERF (Far-End Receive Failure) Condition Interrupt is disabled 1: Generates interrupt upon change in FERF Condition.
2	AIC Interrupt Enable	R/W	0	0: Change in AIC State Interrupt is disabled 1: Generates interrupt upon change of AIC values, in “inbound” DS3 data steam.
1	OOF Interrupt Enable	R/W	0	0: Change in OOF (Out of Frame) Condition Interrupt is disabled 1: Generates interrupt upon change of OOF condition.
0	P-Bit Error Interrupt Enable	R/W	0	0: Detection of P-Bit Error Interrupt disabled 1: Generates interrupt upon Detection of P-bit Error.

TABLE 18: RX DS3 INTERRUPT STATUS REGISTER

REGISTER 17	RX DS3 INTERRUPT STATUS REGISTER	HEX ADDRESS: 0X11

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	CP bit Error Interrupt Status	RUR	0	0: No CP-bit errors have been detected since the last read of this register. 1: Indicates that at least one CP-bit error was detected since the last time this register was read.
6	LOS Interrupt Status	RUR	0	0: LOS condition has NOT changed since the last read of this register. 1: LOS condition has changed since the last read of this register.
5	AIS Interrupt Status	RUR	0	0: AIS condition has NOT changed since the last read of this register. 1: AIS condition has changed since the last read of this register.
4	Idle Interrupt Status	RUR	0	0: Idle Condition has NOT changed since the last read of this register. 1: Idle Condition has changed since the last read of this register.
3	FERF Interrupt Status	RUR	0	0: FERF Condition has NOT changed since the last read of this register. 1: FERF Condition has changed since the last read of this register.
2	AIC Interrupt Status	RUR	0	0: AIC State has NOT changed since the last read of this register. 1: Validated AIC has changed since the last read of this register.
1	OOF Interrupt Status	RUR	0	0: OOF condition has NOT changed since the last read of this register. 1: OOF status has changed since the last read of this register.
0	P-Bit Error Interrupt Status	RUR	0	0: No P-bit Errors have been detected since the last read of this register. 1: Indicates that at least one P-bit error was detected since the last time this register was read.

TABLE 19: RX DS3 FEAC REGISTER

REGISTER 18	RX DS3 FEAC REGISTER	HEX ADDRESS: 0X12

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Unused	RO	0	
6	Rx FEAC(0)	RO	1	RxFEAC[5:0] contains the most recently validated receive FEAC code word. ***NOTE:*** *These bit-fields are only active if the XRT72L73 is configured to support the "C-bit Parity" Framing Forma*
5	RxFEAC(1)	RO	1	
4	RxFEAC(2)	RO	1	
3	RxFEAC(3)	RO	1	
2	RxFEAC(4)	RO	1	
1	RxFEAC(5)	RO	1	
0	Unused	RO	0	

TABLE 20: RX DS3 FEAC INTERRUPT ENABLE/STATUS REGISTER

REGISTER 19 **RX DS3 FEAC INTERRUPT ENABLE/STATUS REGISTER** **HEX ADDRESS: 0X13**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-5	Unused	RO	0	
4	FEAC Valid	RO	0	0: Received FEAC code (residing in "RxFEAC[5:0]") has been "removed". 1: Received FEAC code (residing in "RxFEAC[5:0]") has been "validated". ***NOTE:*** *This bit-field is only valid if the XRT72L73 is configured to support the "C-bit Parity" Framing Format.*
3	Rx FEAC Remove Interrupt Enable	R/W	0	0: RxFEAC Removal Interrupt is disabled. 1: Generates an interrupt upon removal of previously validated FEAC code is enabled ***NOTE:*** *This bit-field is only valid if the XRT72L73 is configured to support the "C-bit Parity" Framing Format.*
2	Rx FEAC Remove Interrupt Status	RUR	0	0: Indicates that no received FEAC Messages have been removed since the last read of this register. 1: Indicates that a received FEAC Message has been removed since the last read of this register. ***NOTE:*** *This bit-field is only valid if the XRT72L73is configured to support the "C-bit Parity" Framing Format.*
1	Rx FEAC Valid Interrupt Enable	R/W	0	0: RxFEAC Validation Interrupt is disabled. 1: Generates an interrupt upon validation of a newly received FEAC message. ***NOTE:*** *This bit-field is only valid if the XRT72L73 is configured to support the "C-bit Parity" Framing Format.*
0	Rx FEAC Valid Interrupt Status	RUR	0	0: Indicates that no received FEAC Messages have been validated since the last read of this register. 1: Indicates that a newly received FEAC Message has been validated since the last read of this register. ***NOTE:*** *This bit-field is only valid if the XRT72L73 is configured to support the C-bit Parity" Framing Format.*

TABLE 21: RX DS3 LAPD CONTROL REGISTER

REGISTER 20 **RX DS3 LAPD CONTROL REGISTER** **HEX ADDRESS: 0X13**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Enable 5 F(4)	R/W	1	0: Particular frame f-bit search block disabled 1: Particular frame f-bit search block enabled Each bit is an "Enable" to five f0bit framer parallel search blocks
6	Enable 5 F(3)	R/W	1	
5	Enable 5 F(2)	R/W	1	
4	Enable 5 F(1)	R/W	1	
3	Enable 5 F(0)	R/W	1	
2	Rx LAPD Enable	R/W	0	0: Disables the LAPD Receiver 1: Enables the LAPD Receiver ***NOTE:*** *This bit-field is only active if the XRT72L73 has been configured to support the "C-bit Parity" Framing Format.*
1	Rx LAPD Interrupt Enable	R/W	0	0: Receive LAPD Interrupt is disabled. 1: Generates interrupt anytime the LAPD Receiver receives a new LAPD (PMDL) Message. ***NOTE:*** *This bit-field is only active if the XRT72L73 has been configured to support the "C-bit Parity" Framing Format.*
0	Rx LAPD Interrupt Status	RUR/ WO	0	0: A new LAPD Message has NOT been received (by the LAPD Receiver) since the last read of this register. 1: A new LAPD Message has been received (by the LAPD Receiver) since the last read of this register. ***NOTE:*** *This bit-field is only active if the XRT72L73 has been configured to support the "C-bit Parity" Framing Format.*

TABLE 22: RX DS3 LAPD STATUS REGISTER

REGISTER 21 **RX DS3 LAPD STATUS REGISTER** **HEX ADDRESS: 0X15**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Unused	RO	0	
6	Rx ABORT	RO	0	0: Indicates that the LAPD Receiver is NOT currently receiving an ABORT Message. 1: Indicates that the LAPD Receiver is currently receiving an ABORT Message. ***NOTE:*** *This bit-field is only active if the XRT72L73 has been configured to support the "C-bit Parity" Framing format.*
5	Rx LAPD Type(0)	RO	0	00: LAPD Message is Test Signal Identification type. (RAM Depth is 76 bytes (38 words)) 01: LAPD Message is Idle Signal Identification type. (RAM Depth is 76 bytes (38 words)) 10: LAPD Message is CL Path Identification type. (RAM Depth is 76 bytes (38 words)) 11: LAPD Message is ITU-T Path Identification type. (RAM Depth is 82 bytes (41 words)) ***NOTE:*** *These two bit-fields are only active if the XRT72L73 has been configured to support the "C-bit Parity" Framing Format.*
4	Rx LAPD Type(1)	RO	0	
3	Rx CR Type	RO	0	0: Received LAPD message originated from customer installation 1: Received LAPD message originated from terminal in the network ***NOTE:*** *This bit-field is only active if the XRT72L73 has been configured to support the "C-bit Parity" Framing Format.*
2	Rx FCS Error	RO	0	0: CRC-16 Error was NOT detected within the most recently received LAPD Message. 1: CRC-16 Error was detected within the most recently received LAPD Message. ***NOTE:*** *This bit-field is only active if the XRT72L73 has been configured to support the "C-bit Parity" Framing Format.*
1	Rx End of Message	RO	0	0: Indicates that either the "Receive LAPD Message" Buffer is empty, or that the LAPD Receiver is currently receiving a LAPD Message. 1: Indicates that a full LAPD Message has been received by the LAPD Receiver and that this message is residing within the "Receive LAPD Message" Buffer. ***NOTE:*** *This bit-field is only active if the XRT72L73 has been configured to support the "C-bit Parity" Framing Format.*
0	Flag Present	RO	0	0: Indicates that the LAPD Receiver is NOT currently receiving the "Flag Sequence", within the LAPD Channel. 1: Indicates that the LAPD Receiver is currently receiving the "Flag Sequence" within the LAPD Channel. ***NOTE:*** *This bit-field is only active if the XRT72L73 has been configured to support the "C-bit Parity" Framing Format.*

TABLE 23: TX DS3 CONFIGURATION REGISTER

REGISTER 22 **TX DS3 CONFIGURATION REGISTER** **HEX ADDRESS: 0X16**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Tx Yellow Alarm	R/W	0	0: X-bits are transmitted as conditions (detected by the "Receive DS3 Framer" block) dictate. 1: All X-bits (within each "outbound" DS3 frame) are set to "0" (forced insertion of Yellow Alarm) ***NOTE:*** *This bit-field is ignored when the "TxIdle", the "TxAIS" or the "TxLOS" bits are set.*
6	Tx XBit	R/W	0	0: X-bits are transmitted as conditions (detected by the "Receive DS3 Framer" block) dictate. 1: All X-bits (within each "outbound" DS3 frame) are forced to "1". ***NOTE:*** *This bit-field is ignored when the "TxIdle", the "TxAIS" or the "TxLOS" bits are set.*
5	Tx Idle	R/W	0	0: The Idle pattern is NOT transmitted into the "outbound" DS3 data stream. 1: The Idle pattern is transmitted into the "outbound" DS3 data stream. ***NOTE:*** *This bit-field is ignored when the "TxAIS" or the "TxLOS" bits are set.*
4	Tx AIS	R/W	0	0: The "AIS" pattern is NOT transmitted into the "outbound" DS3 data stream. 1: The "AIS" pattern is transmitted into the "outbound" DS3 data stream. ***NOTE:*** *This bit-field is ignored when the "TxLOS" bit is set.*
3	Tx LOS	R/W	0	0: The "All Zeros" pattern is NOT transmitted into the "outbound" DS3 data stream. 1: The "LOS" (e.g., "All Zeros") pattern is transmitted into the "outbound" DS3 data stream.
2	FERF on LOS	R/W	1	0: FERF (Far-End Receive Failure) is NOT transmitted whenever the Receive DS3 Framer block declares an LOS (Loss of Signal) condition. 1: FERF is transmitted whenever the Receive DS3 Framer block declares an LOS condition.
1	FERF on OOF	R/W	1	0: FERF (Far-End Receive Failure) is NOT transmitted whenever the Receive DS3 Framer block declares an OOF (Out of Frame) condition. 1: FERF is transmitted whenever the Receive DS3 Framer block declares an OOF condition.
0	FERF on AIS	R/W	1	0: FERF is NOT transmitted whenever the Receive DS3 Framer block detects an AIS pattern in the "inbound" DS3 data stream. 1: FERF is transmitted whenever the Receive DS3 Framer block detects the AIS pattern in the "inbound" DS3 data stream.

TABLE 24: TX DS3 M-BIT MASK REGISTER

REGISTER 23 **TX DS3 M-BIT MASK REGISTER** **HEX ADDRESS: 0X17**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Tx FEBE Dat(2)	R/W	0	The Transmit DS3 Framer block will transmit the value "TxFEBEDat[2:0]" within the "FEBE" bit-fields, if the "FEBE Register Enable" bit-field is set to "1". ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to support the "C-bit Parity" Framing Format.*
6	Tx FEBE Dat(1)	R/W	0	
5	Tx FEBE Dat(0)	R/W	0	
4	FEBE Register Enable	R/W	0	0: FEBE bits, for transmission, are internally generated based on conditions, as detected by the Receive DS3 Framer block. 1: Transmit FEBE bits are taken from the TxFEBEDat [2:0] register bits ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to support the "C-bit Parity" Framing Format.*
3	Mbit Mask(2)	R/W	0	The Transmit DS3 Framer block performs an XOR operation of the MBitMask bits with the corresponding "M" bit, within each outbound DS3 frame. MBitMask(2) corresponds to first M-Bit (M0) in DS3 frame, MBitMask(1) corresponds to second M-Bit (M1) in DS3 frame, MBitMask(0) corresponds to last M-Bit (M0) in DS3 frame ***NOTES:*** 1. *Setting any of these bit-fields to "1", will cause an "erred" M-bit to be transmitted onto the line.* 2. *For normal operation, the user should set each of these bit-fields to "0".*
2	Mbit Mask(1)	R/W	0	
1	Mbit Mask(0)	R/W	0	
0	TxError PBit	R/W	0	0: P Bits are calculated from input payload and inserted into the P-bit fields. 1: Calculated P Bits are inverted before transmission (thereby creating a "P-Bit" Error). ***NOTE:*** *For normal operation, set this bit-field to "0".*

TABLE 25: TX DS3 F-BIT MASK1 REGISTER

REGISTER 24 **TX DS3 F-BIT MASK1 REGISTER** **HEX ADDRESS: 0X18**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-4	Unused	RO	0	
3	F-bit Mask (27)	R/W	0	The Transmit DS3 Framer block performs an XOR operation of the F-Bit Mask bits, with the corresponding "F" bits, within each outbound DS3 frame. FBitMask(0) corresponds to first F-Bit (F1) is the DS3 frame, FBitMask (1) corresponds to 2nd F-Bit (F0)in the DS3 frame,...FBitMask(27) corresponds to the last F-Bit of the M-Frame. ***NOTES:*** 1. *Setting any of these bit-fields to "1" will cause an "erred" F-bit to be transmitted onto the line.* 2. *For normal operation, the user should set each of these bit-fields to "0".*
2	F-bit Mask (26)	R/W	0	
1	F-bit Mask (25)	R/W	0	
0	F-bit Mask (24)	R/W	0	

TABLE 26: TX DS3 F-BIT MASK2 REGISTER

REGISTER 25 **TX DS3 F-BIT MASK2 REGISTER** **HEX ADDRESS: 0X19**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	F-bit Mask (23)	R/W	0	The Transmit DS3 Framer block performs an XOR operation of the F-Bit Mask bits, with the corresponding "F" bits, within each outbound DS3 frame. FBitMask(0) corresponds to first F-Bit (F1) is the DS3 frame, FBitMask (1) corresponds to 2nd F-Bit (F0)in the DS3 frame,...FBitMask(27) corresponds to the last F-Bit of the M-Frame. ***NOTES:*** 1. *Setting any of these bit-fields to "1" will cause an "erred" F-bit to be transmitted onto the line.* 2. *For normal operation, set each of these bit-fields to "0".*
6	F-bit Mask (22)	R/W	0	
5	F-bit Mask (21)	R/W	0	
4	F-bit Mask (20)	R/W	0	
3	F-bit Mask (19)	R/W	0	
2	F-bit Mask (18)	R/W	0	
1	F-bit Mask (17)	R/W	0	
0	F-bit Mask (16)	R/W	0	

TABLE 27: TX DS3 F-BIT MASK3 REGISTER

REGISTER 26 **TX DS3 F-BIT MASK3 REGISTER** **HEX ADDRESS: 0X1A**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	F-bit Mask (15)	R/W	0	The Transmit DS3 Framer block performs an XOR operation of the FBitMask bits, with the corresponding "F" bits, within each outbound DS3 frame. FBitMask(0) corresponds to first F-Bit (F1) is the DS3 frame, FBitMask (1) corresponds to 2nd F-Bit (F0)in the DS3 frame,...FBitMask(27) corresponds to the last F-Bit of the M-Frame. ***NOTES:*** 1. *Setting any of these bit-fields to "1" will cause an "erred" F-bit to be transmitted onto the line.* 2. *For normal operation,set each of these bit-fields to "0".*
6	F-bit Mask (14)	R/W	0	
5	F-bit Mask (13)	R/W	0	
4	F-bit Mask (12)	R/W	0	
3	F-bit Mask (11)	R/W	0	
2	F-bit Mask (10)	R/W	0	
1	F-bit Mask (9)	R/W	0	
0	F-bit Mask (8)	R/W	0	

TABLE 28: TX DS3 F-BIT MASK4 REGISTER

REGISTER 27 **TX DS3 F-BIT MASK4 REGISTER** **HEX ADDRESS: 0X1B**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	F-bit Mask (7)	R/W	0	The Transmit DS3 Framer block performs an XOR operation of the FBitMask bits, with the corresponding "F" bits, within each outbound DS3 frame. FBitMask(0) corresponds to first F-Bit (F1) is the DS3 frame, FBitMask (1) corresponds to 2nd F-Bit (F0)in the DS3 frame,...FBitMask(27) corresponds to the last F-Bit of the M-Frame. ***NOTES:*** 1. *Setting any of these bit-fields to "1" will cause an "erred" F-bit to be transmitted onto the line.* 2. *For normal operation, set each of these bit-fields to "0".*
6	F-bit Mask (6)	R/W	0	
5	F-bit Mask (5)	R/W	0	
4	F-bit Mask (4)	R/W	0	
3	F-bit Mask (3)	R/W	0	
2	F-bit Mask (2	R/W	0	
1	F-bit Mask (1)	R/W	0	
0	F-bit Mask (0)	R/W	0	

TABLE 29: TX DS3 FEAC CONFIGURATION AND STATUS REGISTER

REGISTER 28 **TX DS3 FEAC CONFIGURATION AND STATUS REGISTER** **HEX ADDRESS: 0X1C**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-5	Unused	RO	0	
4	Tx FEAC Interrupt Enable	R/W	0	0: Disables the "Transmit FEAC" Interrupt. 1: Enables the "Transmit FEAC" Interrupt. ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to support the "C-bit Parity" Framing format.*
3	Tx FEAC Interrupt Status	RUR	0	0: Indicates that the "Transmit FEAC" Interrupt has not occurred since the last read of this register. 1: Indicates that the "Transmit FEAC" Interrupt request has occurred since the last read of this register. ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to support the "C-bit Parity" Framing format.*
2	Tx FEAC Enable	R/W	0	0: The Transmit FEAC Processor is disabled, and cannot be commanded to transmit a FEAC Message to the remote terminal equipment. 1: The Transmit FEAC Processor is enabled, and is able to be commanded to transmit FEAC Messages to the remote terminal equipment. ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to support the "C-bit Parity" Framing format.*
1	Tx FEAC Go	R/W	0	0 to 1 transition within this bit-field commands the Transmit FEAC Processor to begin its transmission of the FEAC Message, which resides within the "TxFEAC" Register. ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to support the "C-bit Parity" Framing format.*
0	Tx FEAC Busy	RO	0	0: Indicates that the Transmit FEAC Processor is NOT currently transmitting a FEAC Message to the remote terminal equipment 1: Data from FEAC register is currently being transmitted to the remote terminal equipment. ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to support the "C-bit Parity" Framing format.*

TABLE 30: TX DS3 FEAC REGISTER

REGISTER 29 **TX DS3 FEAC REGISTER** **HEX ADDRESS 0X1D**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Unused	RO	0	
6	Tx FEAC (5)	R/W	1	Contains the value of the FEAC Code (or Message) that is to be transmitted to the remote terminal equipment. The LSB of this bit-field will be transmitted first. ***NOTE:*** *This register is only active if the XRT72L73 has been configured to operate in the "C-bit Parity" Framing Format*
5	Tx FEAC (4)	R/W	1	
4	Tx FEAC (3)	R/W	1	
3	Tx FEAC (2)	R/W	1	
2	Tx FEAC (1)	R/W	1	
1	Tx FEAC (0)	R/W	1	
0	Unused	RO	0	

TABLE 31: TX DS3 LAPD CONFIGURATION REGISTER

REGISTER 30 **TX DS3 LAPD CONFIGURATION REGISTER** **HEX ADDRESS: 0X1E**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-5	Unused	RO	0	
4	Reserved	R/W	0	Set bit to 0
3	Auto Retransmit	R/W	1	0: LAPD Transmitter will NOT automatically transmit a given PMDL (or LAPD Message) repeatedly at one second intervals. 1: LAPD Transmitter will transmit a given PMDL (or LAPD Message) repeatedly at one second intervals. ***NOTE:*** *This bit-field is only active if the XRT72L73 has been configured to support the "C-bit Parity" Framing format.*
2	Tx LAPD Type(1)	R/W	0	00: LAPD message RAM Depth is 76 bytes (38 words) 01: LAPD message RAM Depth is 76 bytes (38 words) 10: LAPD message RAM Depth is 76 bytes (38 words) 11: LAPD message RAM Dept his 82 bytes (41 words) ***NOTE:*** *These bit-fields are only active if the XRT72L73 has been configured to support the "C-bit Parity" Framing Format.*
1	Tx LAPD Type(0)	R/W	0	
0	Tx LAPD Enable	R/W	0	0: LAPD Transmitter is Disabled. The Transmit DS3 Framer block will set each "outbound" DL bit-field to "1". 1: LAPD Transmitter is Enabled. The LAPD Transmitter will begin to transmit the Flag Sequence octet (0x7E), until a "Transmit LAPD Message" command has been invoked. ***NOTE:*** *This bit-field is only active if the XRT72L73 has been configured to support the "C-bit Parity" Framing format.*

TABLE 32: TX DS3 LAPD STATUS/INTERRUPT REGISTER

REGISTER 31 **TX DS3 LAPD STATUS/INTERRUPT REGISTER** **HEX ADDRESS: 0X1F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-4	Unused	RO	0	
3	Tx DL Start	R/W	0	0 to 1 transition configures the LAPD Transmitter to begin its transmission of the PMDL (or LAPD Message) consisting of the data residing within the "Transmit LAPD Message" buffer. ***NOTE:*** *This bit-field is only active if the XRT72L73 has been configured to support the "C-bit Parity" Framing format.*
2	Tx DL Busy	RO	0	0: LAPD Transmitter is NOT currently transmitting a LAPD Message to the Remote Terminal Equipment; and is not available to transmit a new LAPD Message. 1: LAPD Transmitter is currently transmitting a LAPD Message to the Remote Terminal Equipment. ***NOTE:*** *This bit-field is only active if the XRT72L73 has been configured to support the "C-bit Parity" Framing format.*
1	Tx LAPD Interrupt Enable	R/W	0	0: "Completion of Transmission of LAPD Message" Interrupt is disabled. 1: "Completion of Transmission of LAPD Message" Interrupt is enabled. The XRT72L73 will generate an interrupt, anytime the LAPD Transmitter has completed its transmission of a given LAPD Message. ***NOTE:*** *This bit-field is only active if the XRT72L73 has been configured to support the "C-bit Parity" Framing format.*
0	Tx LAPD Interrupt Status	RUR	0	0: "Completion of Transmission of LAPD Message" interrupt has NOT occurred since the last read of this register. 1: "Completion of Transmission of LAPD Message" interrupt has occurred since the last read of this register. ***NOTE:*** *This bit-field is only active if the XRT72L73 has been configured to support the "C-bit Parity" Framing format.*

TABLE 33: PMON LCV EVENT COUNT REGISTER - MSB

REGISTER 32 **PMON LCV EVENT COUNT REGISTER - MSB** **HEX ADDRESS: 0X20**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	LCV Count High byte	RUR	0x00	This "Reset-upon-Read" register, along with "PMON LCV Event Count Register - LSB" contains the 16-bit value for the total number of Line Code Violations that have been detected since the last read of this register. This register contains the "High" Byte of this 16-bit expression. ***NOTE:*** *This register is only active if the "B3ZS Decoder" (within the XRT72L73) has been enabled.*

TABLE 34: PMON LCV EVENT COUNT REGISTER - LSB

REGISTER 33	PMON LCV EVENT COUNT REGISTER - LSB	HEX ADDRESS: 0X21

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	LCV Count Low byte	RUR	0x00	This "Reset-upon-Read" register, along with "PMON LCV Event Count Register - MSB" contains the 16 bit value for the total number of Line Code Violations that have been detected since the last read of this register. This register contains the "Low" Byte of this 16-bit expression. ***NOTE:*** *This register is only active if the "B3ZS Decoder" (within the XRT72L73) has been enabled.*

TABLE 35: PMON FRAMING BIT ERROR EVENT COUNT REGISTER - MSB

REGISTER 34	PMON FRAMING BIT ERROR EVENT COUNT REGISTER - MSB	HEX ADDRESS: 0X22

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	F Bit Error Count High-byte	RUR	0x00	This "Reset-upon-Read" register, along with "PMON Framing Bit Error Count Register - LSB" contains the 16 bit value for the total number of Framing Bit (e.g., both F and M-bit) errors that have been detected since the last read of this register. This register contains the "High" byte value of this 16-bit expression.

TABLE 36: PMON FRAMING BIT ERROR EVENT COUNT REGISTER - LSB

REGISTER 35	PMON FRAMING BIT ERROR EVENT COUNT REGISTER - LSB	HEX ADDRESS: 0X23

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	F Bit Error Count low-byte	RUR	0x00	This "Reset-upon-Read" register, along with "PMON Framing Bit Error Count Register - MSB" contains the 16 bit value for the total number of Framing Bit (e.g., both F and M-bit) errors that have been detected since the last read of this register. This register contains the "Low" byte value of this 16-bit expression.

TABLE 37: PMON P-BIT ERROR COUNT REGISTER - MSB

REGISTER 36	PMON P-BIT ERROR COUNT REGISTER - MSB	HEX ADDRESS: 0X24

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	P-Bit Error Count High-byte	RUR	0x00	This "Reset-upon-Read" register, along with "PMON P-Bit Error Count Register - LSB" contains the 16 bit value for the total number of P Bit errors that have been detected since the last read of this register. This register contains the "High" byte value of this 16-bit expression.

TABLE 38: PMON P-BIT ERROR COUNT REGISTER - LSB

REGISTER 37	PMON P-BIT ERROR COUNT REGISTER - LSB	HEX ADDRESS: 0X25

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	P-Bit Error Count Low-byte	RUR	0x00	This "Reset-upon-Read" register, along with "PMON P-Bit Error Count Register - MSB" contains the 16 bit value for the total number of P Bit errors that have been detected since the last read of this register. This register contains the "Low" byte value of this 16-bit expression.

TABLE 39: PMON FEBE EVENT COUNT REGISTER - MSB

REGISTER 38	PMON FEBE EVENT COUNT REGISTER - MSB	HEX ADDRESS: 0X26

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	FEBE Event Count High-byte	RUR	0x00	This "Reset-upon-Read" register, along with "PMON FEBE Event Count Register - LSB" contains the 16 bit value for the total number of FEBE events that have been detected since the last read of this register. This register contains the "High" byte value of this 16-bit expression. ***NOTE:*** *This register is only active if the XRT72L73 has been configured to support the "C-bit Parity" Framing format.*

TABLE 40: PMON FEBE EVENT COUNT REGISTER - LSB

REGISTER 39	PMON FEBE EVENT COUNT REGISTER - LSB	HEX ADDRESS: 0X27

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	FEBE Event Count Low-byte	RUR	0x00	This "Reset-upon-Read" register, along with "PMON FEBE Event Count Register - MSB" contains the 16 bit value for the total number of FEBE events that have been detected since the last read of this register. This register contains the "Low" byte value of this 16-bit expression. ***NOTE:*** *This register is only active if the XRT72L73 has been configured to support the "C-bit Parity" Framing format.*

TABLE 41: PMON PLCP BIP-8 ERROR COUNT REGISTER - MSB

REGISTER 40	PMON PLCP BIP-8 ERROR COUNT REGISTER - MSB	HEX ADDRESS: 0X28

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	PLCP BIP Error Count High-byte	RUR	0x00	This "Reset-upon-Read" register, along with "PMON PLCP BIP-8 Error Count Register - LSB" contains the 16 bit value for the total number of PLCP BIP-8 Errors that have been detected since the last read of this register. This register contains the "High" bye value of this 16-bit expression. ***NOTE:*** *This register is only active if the XRT72L73 has been configured to operate in both the "ATM UNI" and "PLCP" Modes.*

TABLE 42: PMON PLCP BIP-8 ERROR COUNT REGISTER - LSB

REGISTER 41 — PMON PLCP BIP-8 ERROR COUNT REGISTER - LSB — HEX ADDRESS: 0X29

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	PLCP BIP Error Count Low-byte	RUR	0x00	This "Reset-upon-Read" register, along with "PMON PLCP BIP-8 Error Count Register - MSB" contains the 16 bit value for the total number of PLCP BIP-8 Errors that have been detected since the last read of this register. This register contains the "Low" bye value of this 16-bit expression. ***NOTE:*** *This register is only active if the XRT72L73 has been configured to operate in both the "ATM UNI" and "PLCP" Modes.*

TABLE 43: PMON PLCP FRAMING BYTE ERROR COUNT REGISTER - MSB

REGISTER 42 — PMON PLCP FRAMING BYTE ERROR COUNT REGISTER - MSB — HEX ADDRESS: 0X2A

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	PLCP FA Error Count High-byte	RUR	0x00	This "Reset-upon-Read" register, along with "PMON PLCP FA Error Count Register - LSB" contains the 16 bit value for the total number of PLCP Framing (e.g, FA1 or FA2) byte errors that have been detected since the last read of this register. This register contains the "High" byte value of this 16-bit expression. ***NOTE:*** *This register is only active if the XRT72L73 has been configured to operate in both the "ATM UNI" and "PLCP" Modes.*

TABLE 44: PMON PLCP FRAMING BYTE ERROR COUNT REGISTER - LSB

REGISTER 43 — PMON PLCP FRAMING BYTE ERROR COUNT REGISTER - LSB — HEX ADDRESS: 0X2B

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	PLCP FA Error Count Low-byte	RUR	0x00	This "Reset-upon-Read" register, along with "PMON PLCP FA Error Count Register - MSB" contains the 16 bit value for the total number of PLCP Framing (e.g, FA1 or FA2) byte errors that have been detected since the last read of this register. This register contains the "Low" byte value of this 16-bit expression. ***NOTE:*** *This register is only active if the XRT72L73 has been configured to operate in both the "ATM UNI" and "PLCP" Modes.*

TABLE 45: PMON PLCP FEBE COUNT REGISTER - MSB

REGISTER 44 — PMON PLCP FEBE COUNT REGISTER - MSB — HEX ADDRESS: 0X2C

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	PLCP FEBE Count High-byte	RUR	0x00	This "Reset-upon-Read" register, along with "PMON PLCP FEBE Count Register - LSB" contains the 16 bit value for the total number of PLCP FEBE (Far-End Block Error) events that have been detected since the last read of this register. This register contains the "High" byte value of this 16-bit expression. ***NOTE:*** *This register is only active if the XRT72L73 has been configured to operate in both the "ATM UNI" and "PLCP" Modes.*

TABLE 46: PMON PLCP FEBE COUNT REGISTER -LSB

REGISTER 45 **PMON PLCP FEBE COUNT REGISTER -LSB** **HEX ADDRESS: 0X2D**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	PLCP FEBE Count Low-byte	RUR	0x00	This "Reset-upon-Read" register, along with "PMON PLCP FEBE Count Register - MSB" contains the 16 bit value for the total number of PLCP FEBE (Far-End Block Error) events that have been detected since the last read of this register. This register contains the "Low" byte value of this 16-bit expression. ***NOTE:*** *This register is only active if the XRT72L73 has been configured to operate in both the "ATM UNI" and "PLCP" Modes.*

TABLE 47: PMON SINGLE-BIT HEC ERROR COUNT - MSB

REGISTER 46 **PMON SINGLE-BIT HEC ERROR COUNT - MSB** **HEX ADDRESS: 0X2E**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	S-HEC Error Count High-byte	RUR	0x00	This "Reset-upon-Read" register, along with "PMON Single-Bit HEC Error Count Register - LSB" contains the 16 bit value for the total number of Single-bit HEC byte errors that have been detected since the last read of this register. This register contains the "High" byte value of this 16-bit expression. ***NOTE:*** *This register is only active if the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*

TABLE 48: PMON SINGLE-BIT HEC ERROR COUNT - LSB

REGISTER 47 **PMON SINGLE-BIT HEC ERROR COUNT - LSB** **HEX ADDRESS: 0X2F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	S-HEC Error Count Low-byte	RUR	0x00	This "Reset-upon-Read" register, along with "PMON Single-Bit HEC Error Count Register - MSB" contains the 16 bit value for the total number of Single-bit HEC byte errors that have been detected since the last read of this register. This register contains the "Low" byte value of this 16-bit expression. ***NOTE:*** *This register is only active if the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*

TABLE 49: PMON MULTIPLE-BIT HEC ERROR COUNT - MSB

REGISTER 48 **PMON MULTIPLE-BIT HEC ERROR COUNT - MSB** **HEX ADDRESS: 0X30**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	M-HEC Error Count High-byte	RUR	0x00	This "Reset-upon-Read" register, along with "PMON Multiple-Bit HEC Error Count Register - LSB" contains the 16 bit value for the total number of Multi-bit HEC byte errors that have been detected since the last read of this register. This register contains the "High" byte value of this 16-bit expression. ***NOTE:*** *This register is only active if the XRT72L73has been configured to operate in the "ATM UNI" Mode.*

TABLE 50: PMON MULTIPLE-BIT HEC ERROR COUNT - LSB

REGISTER 49 **PMON MULTIPLE-BIT HEC ERROR COUNT - LSB** **HEX ADDRESS: 0X31**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	M-HEC Error Count Low-byte	RUR	0x00	This "Reset-upon-Read" register, along with "PMON Multiple-Bit HEC Error Count Register - MSB" contains the 16 bit value for the total number of Multi-bit HEC byte errors that have been detected since the last read of this register. This register contains the "Low" byte value of this 16-bit expression. ***NOTE:*** *This register is only active if the device has been configured to operate in the "ATM UNI" Mode.*

TABLE 51: PMON RECEIVED IDLE CELL COUNT/PRBS ERROR COUNT - MSB

REGISTER 50 **PMON RECEIVED IDLE CELL COUNT/PRBS ERROR COUNT - MSB** **HEX ADDRESS: 0X32**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Rx Idle Cell Count High-byte/ PRBS Error Count High-byte	RUR	0x00	**ATM Mode**: This register, along with "PMON Received Idle Cell Count - LSB" contains the 16 bit value for the total number of idle cells that have been received by the Receive Cell Processor, since the last read of this register. This register contains the "High" byte value of this 16-bit expression. **Clear Channel Framer Mode**: This register, along with "PMON PRBS Error Count - LSB" regster contains the 16 bit value for the total number of PRBS bit errors that have been received (by the PRBS Receiver) since the last read of this register. This register contains the "High" byte value of this 16-bit expression.

TABLE 52: PMON RECEIVED IDLE CELL COUNT/PRBS ERROR COUNT - LSB

REGISTER 51 **PMON RECEIVED IDLE CELL COUNT/PRBS ERROR COUNT - LSB** **HEX ADDRESS: 0X33**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Rx Idle Cell Count Low-byte/ PRBS Error Count Low-byte	RUR	0x00	**ATM Mode**: This register, along with "PMON Received Idle Cell Count - MSB" contains the 16 bit value for the total number of idle cells that have been received by the Receive Cell Processor, since the last read of this register. This register contains the "Low" byte value of this 16-bit expression. **Clear Channel Framer Mode:** This register, along with "PMON PRBS Error Count - MSB" regster contains the 16 bit value for the total number of PRBS bit errors that have been received (by the PRBS Receiver) since the last read of this register. This register contains the "Low" byte value of this 16-bit expression.

TABLE 53: PMON RECEIVE VALID CELL COUNT - MSB

REGISTER 52	PMON RECEIVE VALID CELL COUNT - MSB	HEX ADDRESS: 0X34

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Rx Valid Cell Count High-byte	RUR	0x00	This Reset-upon-Read register, along with PMON Receive Valid Cell Count - LSB" contains the 16 bit value for the total number of Valid Cells that have been received since the last read of this register. This register contains the "High" byte value of this 16-bit expression. ***NOTE:*** *This register is only active if the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*

TABLE 54: PMON RECEIVE VALID CELL COUNT - LSB

REGISTER 53	PMON RECEIVE VALID CELL COUNT - LSB	HEX ADDRESS: 0X35

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Rx Valid Cell Count Low-byte	RUR	0x00	This Reset-upon-Read register, along with PMON Receive Valid Cell Count - MSB" contains the 16 bit value for the total number of Valid Cells that have been received since the last read of this register. This register contains the "Low" byte value of this 16-bit expression. ***NOTE:*** *This register is only active if the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*

TABLE 55: PMON DISCARDED CELL COUNT - MSB

REGISTER 54	PMON DISCARDED CELL COUNT - MSB	HEX ADDRESS: 0X36

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Cell Drop Count High-byte	RUR	0x00	This Reset-upon-Read register, along with PMON Discarded Cell Count - LSB" contains the 16 bit value for the total number of cells that have been discarded since the last read of this register. This register contains the "High" byte value of this 16-bit expression. ***NOTE:*** *This register is only active if the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*

TABLE 56: PMON DISCARDED CELL COUNT - LSB

REGISTER 55	PMON DISCARDED CELL COUNT - LSB	HEX ADDRESS: 0X37

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Cell Drop Count Low-byte	RUR	0x00	This Reset-upon-Read register, along with PMON Discarded Cell Count - MSB" contains the 16 bit value for the total number of cells that have been discarded since the last read of this register. This register contains the "Low" byte value of this 16-bit expression. ***NOTE:*** *This register is only active if the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*

TABLE 57: PMON TRANSMIT IDLE CELL COUNT - MSB

REGISTER 56	PMON TRANSMIT IDLE CELL COUNT - MSB	HEX ADDRESS: 0X38

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Tx Idle Cell Count High-byte	RUR	0x00	This Reset-upon-Read register, along with PMON Transmit Idle Cell Count - LSB contains the 16 bit value for the total number of Idle cells that have been trnasmitted by the Transmit Cell Processor, since the last read of this register. This register contains the "High" byte value of this 16-bit expression. ***NOTE:*** *This register is only active if the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*

TABLE 58: PMON TRANSMIT IDLE CELL COUNT - LSB

REGISTER 57	PMON TRANSMIT IDLE CELL COUNT - LSB	HEX ADDRESS: 0X39

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Tx Idle Cell Count Low-byte	RUR	0x00	This Reset-upon-Read register, along with PMON Transmit Idle Cell Count - MSB contains the 16 bit value for the total number of Idle cells that have been trnasmitted by the Transmit Cell Processor, since the last read of this register. This register contains the "Low" byte value of this 16-bit expression. ***NOTE:*** *This register is only active if the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*

TABLE 59: PMON TRANSMIT VALID CELL COUNT - MSB

REGISTER 58	PMON TRANSMIT VALID CELL COUNT - MSB	HEX ADDRESS: 0X3A

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Tx Valid Cell Count High-byte	RUR	0x00	This Reset-upon-Read register, along with PMON Transmit Valid Cell Count - LSB contains the 16 bit value for the total number of Valid cells that have been trnasmitted by the Transmit Cell Processor, since the last read of this register. This register contains the "High" byte value of this 16-bit expression. ***NOTE:*** *This register is only active if the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*

TABLE 60: PMON TRANSMIT VALID CELL COUNT - LSB

REGISTER 59	PMON TRANSMIT VALID CELL COUNT - LSB	HEX ADDRESS: 0X3B

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Tx Valid Cell Count Low-byte	RUR	0x00	This Reset-upon-Read register, along with PMON Transmit Valid Cell Count - MSB contains the 16 bit value for the total number of Valid cells that have been trnasmitted by the Transmit Cell Processor, since the last read of this register. This register contains the "Low" byte value of this 16-bit expression. ***NOTE:*** *This register is only active if the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*

TABLE 61: PMON HOLDING REGISTER

REGISTER 60 **PMON HOLDING REGISTER** **HEX ADDRESS: 0X3C**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	PMON Hold Value	RO	0x00	If the Bi-directional data bus (of the Microprocessor Interface) is configured to be “8-bits” wide; then this register holds the companion byte of any 16-bit PMON Count registers, 1-sec Accumulator registers, or the Test Cell Error Accumulator register, when one of these registers are read, during the previous Bus cycle.

TABLE 62: ONE SECOND ERROR STATUS REGISTER

REGISTER 61 **ONE SECOND ERROR STATUS REGISTER** **HEX ADDRESS: 0X3D**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-2	Unused	RO	0	
1	Errored Second	RO	0	0: No errors were detected during last one second accumulation interval 1: At least one error was detected during last one second accumulation interval
0	Severe Errored Second	RO	0	0: Error rate did not exceed 1 in 10,000 in last one second interval 1: Error rate in lat one second interval was greater than 1 in 10,000

TABLE 63: LCV - ONE SECOND ACCUMULATOR REGISTER - MSB

REGISTER 62 **LCV - ONE SECOND ACCUMULATOR REGISTER - MSB** **HEX ADDRES: 0X3E**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	LCV 1Sec High-byte	RO	0x00	This “Read-Only” register, along with “LCV - One Second Accumulator Register - LSB” contains a 16 bit value of the total number of Line Code Violations that have been detected within the last “one-second” accumulation interval. This register contains the “High” byte value of this expression.

TABLE 64: LCV - ONE SECOND ACCUMULATOR REGISTER - LSB

REGISTER 63 **LCV - ONE SECOND ACCUMULATOR REGISTER - LSB** **HEX ADDRES: 0X3F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	LCV 1Sec Low-byte	RO	0x00	This “Read-Only” register, along with “LCV - One Second Accumulator Register - MSB” contains a 16 bit value of the total number of Line Code Violations that have been detected within the last “one-second” accumulation interval. This register contains the “Low” byte value of this expression.

TABLE 65: P-BIT ERRORS - ONE SECOND ACCUMULATOR REGISTER - MSB

REGISTER 64 P-BIT ERRORS - ONE SECOND ACCUMULATOR REGISTER - MSB HEX ADDRESS: 0X40

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	P-Bit Errors 1Sec High-byte	RO	0x00	This "Read-Only" register, along with "P-Bit Errors - One Second Accumulator Register - LSB" contains the 16-bit expression for the total number of P-bit errors that have been detected within the last one second accumulation period. This register contains the "High" byte value of this expression.

TABLE 66: P-BIT ERRORS - ONE SECOND ACCUMULATOR REGISTER - LSB

REGISTER 65 P-BIT ERRORS - ONE SECOND ACCUMULATOR REGISTER - LSB HEX ADDRESS: 0X41

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	P-Bit Errors 1Sec Low-byte	RO	0x00	This "Read-Only" register, along with "P-Bit Errors - One Second Accumulator Register - MSB" contains the 16-bit expression for the total number of P-bit errors that have been detected within the last one second accumulation period. This register contains the "Low" byte value of this expression.

TABLE 67: HEC BYTE ERRORS - ONE SECOND ACCUMULATOR REGISTER - MSB

REGISTER 66 HEC BYTE ERRORS - ONE SECOND ACCUMULATOR REGISTER - MSB HEX ADDRESS: 0X42

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	HEC Errors 1Sec High-byte	RO	0x00	This "Read-Only" register, along with "HEC Byte Errors - One Second Accumulator Register - LSB" contains the 16-bit expression for the total number of HEC byte errors that have been detected within the last one second accumulation period. This register contains the "High" byte value of this expression. ***NOTE:*** *This register is only active if the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*

TABLE 68: HEC BYTE ERRORS - ONE SECOND ACCUMULATOR REGISTER -LSB

REGISTER 67 HEC BYTE ERRORS - ONE SECOND ACCUMULATOR REGISTER -LSB HEX ADDRESS: 0X43

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	HEC Errors 1Sec High-byte	RO	0x00	This "Read-Only" register, along with "HEC Byte Errors - One Second Accumulator Register - MSB" contains the 16-bit expression for the total number of HEC byte errors that have been detected within the last one second accumulation period. This register contains the "Low" byte value of this expression. ***NOTE:*** *This register is only active if the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*

TABLE 69: RX PLCP CONFIGURATION/STATUS REGISTER

REGISTER 68 **RX PLCP CONFIGURATION/STATUS REGISTER** **HEX ADDRESS: 0X44**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-4	Unused	RO	0	
3	PLCP Reframe	R/W	0	0 to 1 transition commands the Receive PLCP Processor block to transition into the “FA1” and “FA2” octet search state, and to reacquire PLCP Frame synchronization. ***NOTE:*** *This bit-field is only active if the XRT72L73 is operating in both the “ATM UNI” and the “PLCP” Modes.*
2	POOF Status	RO	1	0: Indicates that the Receive PLCP Processor block is NOT currently declaring an “Out of Frame” condition 1: Indicates that the Receive PLCP Processor block is currently declaring an “Out of Frame” condition. ***NOTE:*** *This bit-field is only active if the XRT72L73 is operating in both the “ATM UNI” and the “PLCP” Modes.*
1	PLOF Status	RO	1	0: Indicates that the Receive PLCP Processor block is NOT currently declaring a “Loss of Frame” condition. 1: Indicates that the Receive PLCP Processor block is currently declaring a “Loss of Frame” condition. ***NOTE:*** *This bit-field is only active if the XRT72L73 is operating in both the “ATM UNI” and the “PLCP” Modes.*
0	PLCP Yellow Alarm	RO	0	0: Indicates that the Receive PLCP Processor is currently declaring a “Yellow Alarm” condition. 1: Indicates that the Receive PLCP Processor is NOT currently declaring a “Yellow Alarm” condition. ***NOTE:*** *This bit-field is only active if the XRT72L73 is operating in both the “ATM UNI” and the “PLCP” Modes.*

TABLE 70: RX PLCP INTERRUPT ENABLE REGISTER

REGISTER 69 **RX PLCP INTERRUPT ENABLE REGISTER** **HEX ADDRESS: 0X45**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-2	Unused	RO	0	
1	POOF Interrupt Enable	R/W	0	0: The “Change in PLCP OOF Condition” Interrupt is disabled. 1: The “Change in PLCP OOF Condition” Interrupt is enabled. ***NOTE:*** *This bit-field is only active if the XRT72L73 is operating in both the “ATM UNI” and the “PLCP” Modes.*
0	PLOF Interrupt Enable	R/W	0	0: The “Change in PLCP LOF Condition” Interrupt is disabled. 1: The “Change in PLCP LOF Condition” Interrupt is enabled. ***NOTE:*** *This bit-field is only active if the XRT72L73is operating in both the “ATM UNI” and the “PLCP” Mode.*

TABLE 71: RX PLCP INTERRUPT STATUS REGISTER

REGISTER 70 **RX PLCP INTERRUPT STATUS REGISTER** **HEX ADDRESS: 0X46**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-2	Unused	RO	0	
1	POOF Interrupt Status	RUR	0	0: Indicates that the "Change in POOF Condition" Interrupt has not occurred since the last read of this register. 1: Indicates that the "Change in POOF Condition" interrupt has occurred since the last read of this register. ***NOTE:*** *This bit-field is only active if the XRT72L73is operating in both the "ATM UNI" and the "PLCP" Modes.*
0	PLOF Interrupt Status	RUR	0	0: Indicates that the "Change in PLOF Condition" Interrupt has not occurred since the last read of this register. 1: Indicates that the "Change in PLOF Condition" interrupt has occurred since the last read of this register. ***NOTE:*** *This bit-field is only active if the XRT72L73 is operating in both the "ATM UNI" and the "PLCP" Modes.*

TABLE 72: FUTURE USE

REGISTER 71 **FUTURE USE** **HEX ADDRESS: 0X47**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION

TABLE 73: TX PLCP FA1 BYTE ERROR MASK REGISTER

REGISTER 72 **TX PLCP FA1 BYTE ERROR MASK REGISTER** **HEX ADDRESS: 0X48**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	FA1 Error Mask	R/W	0x00	The Transmit PLCP Processor block always XORs contents of this register with the contents of the FA1 byte (within a PLCP frame). This "XORed" value is then written back into the "FA1" byte field, within each "outbound" PLCP Frame; prior to transmission. Setting any of these bit-fields to "1" introduces error in that specific bit, within each "outbound" FA1 byte. Register must be set to 0x00 for normal operation, ***NOTE:*** *This bit-field is only active if the XRT72L73 is operating in both the "ATM UNI" and the "PLCP" Modes.*

TABLE 74: TX PLCP FA2 BYTE ERROR MASK REGISTER

REGISTER 73	TX PLCP FA2 BYTE ERROR MASK REGISTER	HEX ADDRESS: 0X49

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	FA2 Error Mask	R/W	0x00	The Transmit PLCP Processor block always XORs contents of this register with the contents of the FA2 byte (within a PLCP frame). This "XORed" value is then written back into the "FA1" byte field, within each "outbound" PLCP Frame; prior to transmission. Setting any of these bit-fields to "1" introduces error in that specific bit, within each "outbound" FA1 byte. Register must be set to 0x00 for normal operation, ***NOTE:*** *This bit-field is only active if the XRT72L73 is operating in both the "ATM UNI" and the "PLCP" Modes.*

TABLE 75: TX PLCP BIP-8 ERROR MASK

REGISTER 74	TX PLCP BIP-8 ERROR MASK	HEX ADDRESS: 0X4A

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	B1 Error Mask	R/W	0x00	The Transmit PLCP Processor block always XORs contents of this register with the contents of the B1 byte (within a PLCP frame). This "XORed" value is then written back into the "B1" byte field, within each "outbound" PLCP Frame; prior to transmission. Setting any of these bit-fields to "1" introduces error in that specific bit, within each "outbound" B1 byte. Register must be set to 0x00 for normal operation, ***NOTE:*** *This bit-field is only active if the XRT72L73 is operating in both the "ATM UNI" and the "PLCP" Modes.*

TABLE 76: TX PLCP G1 BYTE REGISTER

REGISTER 75	TX PLCP G1 BYTE REGISTER	HEX ADDRESS: 0X4B

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-5	Unused	RO	0	
4	Tx PLCP FEBE Mask	R/W	0	0: FEBE Count is transmitted, based upon B1 Byte Error conditions, as detected by the Receive PLCP Processor. 1: FEBE is transmitted as 0000 ***NOTE:*** *This bit-field is only active if the XRT72L73 is operating in both the "ATM UNI" and the "PLCP" Modes.*
3	Force PLCP Yellow Alarm	R/W	0	0: PLCP Yellow Alarm generated from Receive PLCP Processor. 1: PLCP Yellow Alarm is Forced. ***NOTE:*** *This bit-field is only active if the XRT72L73 is operating in both the "ATM UNI" and the "PLCP" Modes.*
2	LSS(2)	R/W	0	Link Status Signal may be programmed by user
1	LSS(1)	R/W	0	
0	LSS(0)	R/W0	0	

TABLE 77: RX CP CONFIGURATION REGISTER

REGISTER 76 **RX CP CONFIGURATION REGISTER** **HEX ADDRESS: 0X4C**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Rx LCD	RO	1	0: Indicates that the Receive Cell Processor currently has cell delineation within the incoming stream of ATM cells. 1: Indicates that the Receive Cell Processor is currently declaring a “Loss of Cell Delineation”. ***NOTE:*** *This bit-field is only active if the XRT72L73 is operating in the “ATM UNI” Mode.*
6	RDP Chk Pat	R/W	0	0: Receive Cell Processor will insert an alternating “Data Path Integrity Check” value of 0x55 and 0xAA into the 5th octet position of each cell, written into the RxFIFO 1: Receive Cell Processor will insert a fixed “Data Path Integrity Check” value of 0x55 into the 5th octet position of each cell, written into the RxFIFO. ***NOTE:*** *This bit-field is only active if the XRT72L73 is operating in the “ATM UNI” Mode.*
5	RDP Chk Pat En	R/W	0	0: “Data Path Integrity Check” value is not written into ATM cells. ATM cells (with their received HEC byte value) are passed on into RxFIFO without modification. 1:”Data Path Integrity Check” value of 0x55 and 0xAA into the 5th octet position of each cell, is written into each ATM cell, which is routed to the “RxFIFO. ***NOTE:*** *This bit-field is only active if the XRT72L73 is operating in the “ATM UNI” Mode.*
4	IC Discard	R/W	1	0: Idle cells are NOT discarded by the Receive Cell Processor block 1: Idle cells are automatically discarded by the Receive Cell Processor block. ***NOTE:*** *This bit-field is only active if the XRT72L73 is operating in the “ATM UNI” Mode.*
3	SegOAM Pass Through	R/W	1	0: Segment-Type OAM cells are not written into RxFIFO. 1: Segment-Type OAM cells are passed to receiver FIFO ***NOTE:*** *This bit-field is only active if the XRT72L73 is operating in the “ATM UNI” Mode.*
2	De-Scramble Enable	R/W	1	0: Disables cell payload de-scrambling 1: Enables cell payload de-scrambling ***NOTE:*** *This bit-field is only active if the XRT72L73 is operating in the “ATM UNI” Mode.*
1	Rx Coset Enable	R/W	1	0: Coset polynomial is not added to the HEC byte of each “incoming” ATM cell. 1: Coset polynomial is added to HEC byte of each “incoming” ATM Cell. The Receive Cell Processor needs to account for the Coset polynomial during HEC byte verification. ***NOTE:*** *This bit-field is only active if the XRT72L73 is operating in the “ATM UNI” Mode.*
0	HEC Error Ignore	R/W	0	0: Discards/drops cells with HEC byte errors. 1: Retains cells with HEC byte errors, for further processing. ***NOTE:*** *This bit-field is only active if the XRT72L73 is operating in the “ATM UNI” Mode.*

TABLE 78: RX CP ADDITIONAL CONFIGURATION REGISTER

REGISTER 77 **RX CP ADDITIONAL CONFIGURATION REGISTER** **HEX ADDRESS: 0X4D**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Rx OAM FIFO Enable	R/W	0	0: The Receive OAM Cell Buffer functions as one cell (54 byte) buffer 1: The Receive OAM Cell Buffer functions as two-54-byte buffers. ***NOTE:*** *This bit-field is only active if the XRT72L73 is operating in the "ATM UNI" Mode.*
6	Rx CRC10 Enable	R/W	0	0: CRC-10 Verification is NOT performed on received OAM cells. 1: CRC-10 Verification is performed on received OAM cells. ***NOTE:*** *This bit-field is only active if the XRT72L73 is operating in the "ATM UNI" Mode.*
5	User Cell Filter Discard	R/W	0	0: Incoming cells with header bytes matching the "User Cell Filtering" criteria are written to the RxFIFO (all remaining cells are discarded). 1: Incoming cells with header bytes NOT matching the "User Cell Filtering" criteria are discarded (all remaining cells are written to RxFIFO) ***NOTES:*** 1. *This bit-field is only active if the XRT72L73 is operating in the "ATM UNI" Mode.* 2. *This bit-field is only active of the "User Cell Filter" is enabled.*
4	User Cell Filter Enable	R/W	0	0: User cell filter is disabled. All user cells will be written to the RxFIFO. 1: User cell filter is enabled. ***NOTE:*** *This bit-field is only active if the XRT72L73 is operating in the "ATM UNI" Mode.*
3	Correction Thresh(1)	R/W	1	These two bits permit the user to specify the Correction Threshold that the Receive Cell Processor will use, during HEC Byte Verification. 00: Sets Correction Threshold to "0". 01: Sets Correction Threshold to "1". 10: Sets Correction Threshold to "3". 11: Sets Correction Threshold to "7". ***NOTE:*** *This bit-field is only active if the XRT72L73 is operating in the "ATM UNI" Mode.*
2	Correction Thresh(0)	R/W	1	
1	Correction Enable	R/W	1	0: Disables header error correction. 1: Enables header error correction algorithm. ***NOTE:*** *This bit-field is only active if the XRT72L73 is operating in the "ATM UNI" Mode.*
0	OAM Pass Through	R/W	0	0: OAM cells are subject to the Idle Cell and User Cell Filtering criteria. 1: OAM cells are NOT subject to the Idle Cell and User Cell Filtering criteria. ***NOTE:*** *This bit-field is only active if the XRT72L73 is operating in the "ATM UNI" Mode.*

TABLE 79: RX CP INTERRUPT ENABLE REGISTER

REGISTER 78 **RX CP INTERRUPT ENABLE REGISTER** **HEX ADDRESS: 0X4E**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-3	Unused	RO	0	
2	OAM Interrupt Enable	R/W	0	0: "Receipt of OAM Cell" Interrupt is disabled. 1: "Receipt of OAM Cell" Interrupt is enabled. ***NOTE:*** *This bit-field is only active if the XRT72L73 is operating in the "ATM UNI" Mode.*
1	LCD Interrupt Enable	R/W	0	0: "Change in LCD (Loss of Cell Delineation) Condition" Interrupt is disabled. 1: "Change in LCD Condition" Interrupt is enabled. ***NOTE:*** *This bit-field is only active if the XRT72L73 is operating in the "ATM UNI" Mode.*
0	HEC Error Interrupt Enable	R/W	0	0: "Detection of HEC Byte Error" Interrupt is disabled. 1: "Detection of HEC Byte Error" Interrupt is enabled. ***NOTE:*** *This bit-field is only active if the XRT72L73 is operating in the "ATM UNI" Mode.*

TABLE 80: RX CP INTERRUPT STATUS REGISTER

REGISTER 79 **RX CP INTERRUPT STATUS REGISTER** **HEX ADDRESS: 0X4F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	OAM Buffer/FIFO Overflow	RUR	0	0: Receive OAM Cell Buffer/FIFO has not experienced an "Overrun" event since the last read of this register. 1: Receive OAM Cell Buffer/FIFO has experienced an "Overrun" event since the last read of this register. ***NOTE:*** *This bit-field is only active if the XRT72L73 is operating in the "ATM UNI" Mode.*
6-3	Unused	RO	0	
2	OAM Interrupt Status/ OAM Cell Pending	RUR/RO	0	**OAM FIFO mode:** 0: Indicates that the "Receive OAM Cell FIFO" is empty and does not contain any new OAM cell data. 1: Indicates that there at least one unread OAM cell exists within the "Receive OAM Cell FIFO". ***NOTE:*** *If the "Receive OAM Cell" Buffer/FIFO is configured to operate in the "FIFO" Mode, then this bit-field is "Read-Only".* **OAM Buffer Mode**: 0: Indicates that the "Receipt of OAM Cell" Interrupt has NOT occurred since the last read of this register. 1: Indicates that the "Receipt of OAM Cell" Interrupt has occurred since the last read of this register.
1	LCD Interrupt Status	RUR	0	0: Indicates that the "Change in LCD Condition" interrupt has NOT occurred since the last read of this register. 1: Indicates that the "Change in LCD Condition" Interrupt has occurred since the last read of this register. ***NOTE:*** *This bit-field is only active if the XRT72L73 is operating in the "ATM UNI" Mode.*
0	HEC Byte Error Interrupt Status	RUR	0	0: Indicates that the "Detection of HEC Byte" Error has NOT occurred since the last read of this register. 1: Indicates that the "Detection of HEC Byte" Error has occurred since the last read of this register. ***NOTE:*** *This bit-field is only active if the XRT72L73 is operating in the "ATM UNI" Mode.*

TABLE 81: RX CP IDLE CELL PATTERN HEADER BYTE-1

REGISTER 80 **RX CP IDLE CELL PATTERN HEADER BYTE-1** **HEX ADDRESS: 0X50**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Rx Idle Cell Pattern 1	R/W	0x00	This register (along with the "Rx Idle Cell Mask 1" register) permits the user to specify the "Idle Cell Filtering" criteria for Header Byte 1. ***NOTES:*** 1. *This register should be set to "0x00" when the Receive Cell Processor is receiving "ATM Forum" standard Idle Cells.* 2. *This bit-field is only active if the XRT72L73 is operating in the "ATM UNI" Mode.*

TABLE 82: RX CP IDLE CELL PATTERN HEADER BYTE-2

REGISTER 81 **RX CP IDLE CELL PATTERN HEADER BYTE-2** **HEX ADDRESS: 0X51**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Rx Idle Cell Pattern 2	R/W	0x00	This register (along with the "Rx Idle Cell Mask 2" register) permits the user to specify the "Idle Cell Filtering" criteria for Header Byte 2. ***NOTES:*** 1. *This register should be set to "0x00" when the Receive Cell Processor is receiving "ATM Forum" standard Idle Cells.* 2. *This bit-field is only active if the XRT72L73 is operating in the "ATM UNI" Mode.*

TABLE 83: RX CP IDLE CELL PATTERN HEADER BYTE-3

REGISTER 82 **RX CP IDLE CELL PATTERN HEADER BYTE-3** **HEX ADDRESS: 0X52**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Rx Idle Cell Pattern 3	R/W	0x00	This register (along with the "Rx Idle Cell Mask 3" register) permits the user to specify the "Idle Cell Filtering" criteria for Header Byte 3. ***NOTES:*** 1. *This register should be set to "0x00" when the Receive Cell Processor is receiving "ATM Forum" standard Idle Cells.* 2. *This bit-field is only active if the XRT72L73 is operating in the "ATM UNI" Mode.*

TABLE 84: RX CP IDLE CELL PATTERN HEADER BYTE-4

REGISTER 83 **RX CP IDLE CELL PATTERN HEADER BYTE-4** **HEX ADDRESS: 0X53**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Rx Idle Cell Pattern 4	R/W	0x01	This register (along with the "Rx Idle Cell Mask 1" register) permits the user to specify the "Idle Cell Filtering" criteria for Header Byte 4. ***NOTES:*** 1. *This register should be set to "0x01" when the Receive Cell Processor is receiving "ATM Forum" standard Idle Cells.* 2. *This bit-field is only active if the XRT72L73 is operating in the "ATM UNI" Mode.*

TABLE 85: RX CP IDLE CELL MASK HEADER BYTE-1

REGISTER 84	RX CP IDLE CELL MASK HEADER BYTE-1	HEX ADDRESS: 0X54

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Rx Idle Cell Mask 1	R/W	0xFF	This register, along with the "Rx Idle Cell Pattern - 1" Register permits the user to define "Idle Cell Filtering" criteria for Header byte 1. Any "1" in this register, configures the Receive Cell Processor to make the comparison between the corresponding bit-field within Header byte 1 and the contents of the "Rx Idle Cell Pattern - 1" register. Any "0" in this register, configures the Receive Cell Processor to NOT perform this comparison: This register should be set to "0xFF" when the Receive Cell Processor is receiving the "ATM Forum" Standard Idle cells. ***NOTE:*** *This register is only active if the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*

TABLE 86: RX CP IDLE CELL MASK HEADER BYTE-2

REGISTER 85	RX CP IDLE CELL MASK HEADER BYTE-2	HEX ADDRESS: 0X55

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Rx Idle Cell Mask 2	R/W	0xFF	This register, along with the "Rx Idle Cell Pattern - 2" Register permits the user to define "Idle Cell Filtering" criteria for Header byte 2. Any "1" in this register, configures the Receive Cell Processor to make the comparison between the corresponding bit-field within Header byte 2 and the contents of the "Rx Idle Cell Pattern - 2" register. Any "0" in this register, configures the Receive Cell Processor to NOT perform this comparison: This register should be set to "0xFF" when the Receive Cell Processor is receiving the "ATM Forum" Standard Idle cells. ***NOTE:*** *This register is only active if the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*

TABLE 87: RX CP IDLE CELL MASK HEADER BYTE-3

REGISTER 86 **RX CP IDLE CELL MASK HEADER BYTE-3** **HEX ADDRESS: 0X56**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Rx Idle Cell Mask 3	R/W	0xFF	This register, along with the "Rx Idle Cell Pattern - 3" Register permits the user to define "Idle Cell Filtering" criteria for Header byte 3. Any "1" in this register, configures the Receive Cell Processor to make the comparison between the corresponding bit-field within Header byte 3 and the contents of the "Rx Idle Cell Pattern - 3" register. Any "0" in this register, configures the Receive Cell Processor to NOT perform this comparison: This register should be set to "0xFF" when the Receive Cell Processor is receiving the "ATM Forum" Standard Idle cells. ***NOTE:*** *This register is only active if the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*

TABLE 88: RX CP IDLE CELL MASK HEADER BYTE-4

REGISTER 87 **RX CP IDLE CELL MASK HEADER BYTE-4** **HEX ADDRESS: 0X57**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Rx Idle Cell Mask 4	R/W	0xFF	This register, along with the "Rx Idle Cell Pattern - 4" Register permits the user to define "Idle Cell Filtering" criteria for Header byte 4. Any "1" in this register, configures the Receive Cell Processor to make the comparison between the corresponding bit-field within Header byte 4 and the contents of the "Rx Idle Cell Pattern - 4" register. Any "0" in this register, configures the Receive Cell Processor to NOT perform this comparison: This register should be set to "0xFF" when the Receive Cell Processor is receiving the "ATM Forum" Standard Idle cells. ***NOTE:*** *This register is only active if the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*

TABLE 89: RX CP USER CELL FILTER PATTERN HEADER BYTE-1

REGISTER 88 **RX CP USER CELL FILTER PATTERN HEADER BYTE-1** **HEX ADDRESS: 0X58**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	RxUser Cell Filter Pattern 1	R/W	0x00	This register (along with the "Rx User Cell Mask 1" register) permits the user to specify the "User Cell Filtering" criteria for Header Byte 1. ***NOTE:*** *This bit-field is only active if the XRT72L73 is operating in the "ATM UNI" Mode.*

TABLE 90: RX CP USER CELL FILTER PATTERN HEADER BYTE-2

REGISTER 89 **RX CP USER CELL FILTER PATTERN HEADER BYTE-2** **HEX ADDRESS: 0X59**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	RxUser Cell Filter Pattern 2	R/W	0x00	This register (along with the "Rx User Cell Mask 2" register) permits the user to specify the "User Cell Filtering" criteria for Header Byte 2. ***NOTE:*** *This bit-field is only active if the XRT72L73 is operating in the "ATM UNI" Mode.*

TABLE 91: RX CP USER CELL FILTER PATTERN HEADER BYTE-3

REGISTER 90 **RX CP USER CELL FILTER PATTERN HEADER BYTE-3** **HEX ADDRESS: 0X5A**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	RxUser Cell Filter Pattern 3	R/W	0x00	This register (along with the "Rx User Cell Mask 3" register) permits the user to specify the "User Cell Filtering" criteria for Header Byte 3. ***NOTE:*** *This bit-field is only active if the XRT72L73 is operating in the "ATM UNI" Mode.*

TABLE 92: RX CP USER CELL FILTER PATTERN HEADER BYTE-4

REGISTER 91 **RX CP USER CELL FILTER PATTERN HEADER BYTE-4** **HEX ADDRESS: 0X5B**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	RxUser Cell Filter Pattern 4	R/W	0x00	This register (along with the "Rx User Cell Mask 4" register) permits the user to specify the "User Cell Filtering" criteria for Header Byte 4. ***NOTE:*** *This bit-field is only active if the XRT72L73 is operating in the "ATM UNI" Mode.*

TABLE 93: RX CP USER CELL FILTER MASK HEADER BYTE-1

REGISTER 92 **RX CP USER CELL FILTER MASK HEADER BYTE-1** **HEX ADDRESS: 0X5C**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Rx User Cell Filter Mask 1	R/W	0xFF	This register, along with the "Rx User Cell Pattern - 1" Register permits the user to define "User Cell Filtering" criteria for Header byte 1. Any "1" in this register, configures the Receive Cell Processor to make the comparison between the corresponding bit-field within Header byte 1 and the contents of the "Rx User Cell Pattern - 1" register. Any "0" in this register, configures the Receive Cell Processor to NOT perform this comparison: ***NOTE:*** *This register is only active if the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*

TABLE 94: RX CP USER FILTER CELL MASK HEADER BYTE-2

REGISTER 93	RX CP USER FILTER CELL MASK HEADER BYTE-2	HEX ADDRESS: 0X5D

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Rx User Cell Filter Mask 2	R/W	0xFF	This register, along with the "Rx User Cell Pattern - 2" Register permits the user to define "User Cell Filtering" criteria for Header byte 2. Any "1" in this register, configures the Receive Cell Processor to make the comparison between the corresponding bit-field within Header byte 2 and the contents of the "Rx User Cell Pattern - 2" register. Any "0" in this register, configures the Receive Cell Processor to NOT perform this comparison: ***NOTE:*** *This register is only active if the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*

TABLE 95: RX CP USER CELL FILTER MASK HEADER BYTE-3

REGISTER 94	RX CP USER CELL FILTER MASK HEADER BYTE-3	HEX ADDRESS: 0X5E

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Rx User Cell Filter Mask 3	R/W	0xFF	This register, along with the "Rx User Cell Pattern - 3" Register permits the user to define "User Cell Filtering" criteria for Header byte 3. Any "1" in this register, configures the Receive Cell Processor to make the comparison between the corresponding bit-field within Header byte 3 and the contents of the "Rx User Cell Pattern - 3" register. Any "0" in this register, configures the Receive Cell Processor to NOT perform this comparison: ***NOTE:*** *This register is only active if the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*

TABLE 96: RX CP USER CELL FILTER MASK HEADER BYTE-4

REGISTER 95	RX CP USER CELL FILTER MASK HEADER BYTE-4	HEX ADDRESS: 0X5F

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Rx User Cell Filter Mask 4	R/W	0xFF	This register, along with the "Rx User Cell Pattern - 1" Register permits the user to define "User Cell Filtering" criteria for Header byte 1. Any "1" in this register, configures the Receive Cell Processor to make the comparison between the corresponding bit-field within Header byte 1 and the contents of the "Rx User Cell Pattern - 1" register. Any "0" in this register, configures the Receive Cell Processor to NOT perform this comparison: ***NOTE:*** *This register is only active if the XRT72L73 has been configured to operate in the "ATM UNI" Mode.*

TABLE 97: TX CP CONTROL REGISTER

REGISTER 96 **TX CP CONTROL REGISTER** **HEX ADDRESS: 0X60**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Scrambler Enable	R/W	1	0: Disables scrambling of payload bits 1: Enables scrambling of payload bits
6	Coset Enable	R/W	1	0: Disables addition of Coset Polynomial to HEC byte 1: Enables addition of Coset Polynomial to HEC byte
5	Valid Cell HEC Insert Enable	R/W	1	0: HEC Byte Calculation and Insertion is disabled. Hence, no modification is performed on the 5th octet within each "outbound" valid ATM cell. 1: HEC Byte Calculation and Insertion are enabled. ***NOTES:*** *1. This register bit-field only applies to Valid (e.g., User and OAM) cells.* *2. This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" mode.*
4	TDP Check Pattern	R/W	1	0: An Alternating 0x55/0xAA pattern is expected (as the "Data Path Integrity Check byte) in the fifth octet position, within each Valid cell that is processed by the Transmit Cell Processor. 1: A constant 0x55 pattern is expected (as the "Data Path Integrity Check" byte) in the fifth octet position, within each Valid cell that is processed by the Transmit Cell Processor. ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*
3	GFC Insert Enable	R/W	0	0: The "GFC Input Port" is disabled. 1: The "GFC Input Port" is enabled. Data is read via TxGFC serial input pin and is inserted into GFC nibble-field within of each "outbound" ATM cell. ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*
2	TDP Error Interrupt Enable	R/w	0	0: Disables the "Data Path Integrity Check" interrupt. 1: Enables the "Data Path Integrity Check" interrupt.
1	Idle Cell HEC Insert Enable	R/w	1	0: HEC Byte Calculation and Insertion is disabled. Hence, no modification is performed on the 5th octet within each "outbound" Idle ATM cell. 1: HEC Byte Calculation and Insertion are enabled. ***NOTES:*** *1. This register bit-field only applies to Idle cells.* *2. This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" mode.*
0	TDP Error Interrupt Status	RUR	0	0: Indicates that the "Data Path Integrity Check" Interrupt has not occurred since the last read of this register. 1: Indicates that the "Data Path Integrity Check" Interrupt has occurred since the last read of this register. ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*

TABLE 98: TX CP OAM REGISTER

REGISTER 97 **TX CP OAM REGISTER** **HEX ADDRESS: 0X61**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Send OAM	Sem	0	A "0" to "1" transitions configures the Transmit Cell Processor to transmit an OAM cell. ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*
6	Tx CRC10 Enable	R/W	0	0: OAM Cell CRC-10 Calculation and Insertion are disabled. 1: OAM Cell CRC-10 Calculation and Insertion is enabled. The Transmit Cell Processor will compute and insert the CRC-10 value within each "outbound" OAM cell. ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*
5-0	Unused	RO	0x00	

TABLE 99: TX CP HEC ERROR MASK REGISTER

REGISTER 98 **TX CP HEC ERROR MASK REGISTER** **HEX ADDRESS: 0X62**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	HEC Error Mask	R/W	0x00	The Transmit Cell Processor block always XORs contents of this register with the contents of the HEC byte (within each "outbound" ATM cell). This "XORed" value is then written back into the "HEC" byte field, within each "outbound" ATM cell; prior to transmission. Setting any of these bit-fields to "1" introduces error in that specific bit, within each "outbound" HEC byte. Register must be set to 0x00 for normal operation, ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*

TABLE 100: FUTURE USE

REGISTER 99 **FUTURE USE** **HEX ADDRESS: 0X63**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION

TABLE 101: TX CP IDLE CELL PATTERN HEADER BYTE-1

REGISTER 100 **TX CP IDLE CELL PATTERN HEADER BYTE-1** **HEX ADDRESS: 0X64**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Tx Idle Cell Pattern 1	R/W	0x00	Contains pattern for the first header byte of each "outbound" idle cell. Register is set to 0x00 when transmitting standard idle cell pattern. ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*

TABLE 102: TX CP IDLE CELL PATTERN HEADER BYTE-2

REGISTER 101	TX CP IDLE CELL PATTERN HEADER BYTE-2	HEX ADDRESS: 0X65

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Tx Idle Cell Pattern 2	R/W	0x00	Contains pattern for the second header byte of each "outbound" idle cell. Register is set to 0x00 when transmitting standard idle cell pattern. ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*

TABLE 103: TX CP IDLE CELL PATTERN HEADER BYTE-3

REGISTER 102	TX CP IDLE CELL PATTERN HEADER BYTE-3	HEX ADDRESS: 0X66

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Tx Idle Cell Pattern 3	R/W	0x00	Contains pattern for the third header byte of each "outbound" idle cell. Register is set to 0x00 when transmitting standard idle cell pattern. ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*

TABLE 104: TX CP IDLE CELL PATTERN HEADER BYTE-4

REGISTER 103	TX CP IDLE CELL PATTERN HEADER BYTE-4	HEX ADDRESS: 0X67

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Tx Idle Cell Pattern 4	R/W	0x01	Contains pattern for the fourth header byte of each "outbound" idle cell. Register is set to 0x01 when transmitting standard idle cell pattern. ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*

TABLE 105: TX CP IDLE CELL PATTERN HEADER BYTE-5

REGISTER 104	TX CP IDLE CELL PATTERN HEADER BYTE-5	HEX ADDRESS: 0X68

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Tx Idle Cell Pattern 5	R/W	0x52	Contains pattern for the fifth header byte of each "outbound" idle cell. Register is set to 0x00 when transmitting standard idle cell pattern. ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*

TABLE 106: TX CP IDLE CELL PAYLOAD REGISTER

REGISTER 105	TX CP IDLE CELL PAYLOAD REGISTER	HEX ADDRESS: 0X69

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Tx Idle Cell Payload	R/W	0x5A	This register contains the value of the payload bytes within each "outbound" Idle Cell. The contents of this register will be repeated 48 times, when filling the payload of each "outbound" Idle Cell. pRegister is set to 0x5A when transmitting standard idle cell pattern. ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*

TABLE 107: UTOPIA CONFIGURATION REGISTER

REGISTER 106	UTOPIA CONFIGURATION REGISTER	HEX ADDRESS: 0X6A

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-6	Unused	RO	0	
5	Handshake Mode	R/W	0	0: Transmit and Receive UTOPIA Interface blocks operate in the Octet-Level handshake mode 1: Transmit and Receive UTOPIA Interfaces blocks operate in the Cell-Level handshake mode ***NOTE:*** *This bit-field is ignore if the XRT72L73 is configured to operate in the "Clear-Channel Framer" Mode, or if the chip is configured to operate in the "Multi-PHY" Mode.*
4	M PHY	R/W	1	0: Transmit and Receive UTOPIA Interface block operates in the "Single-PHY" mode 1: Transmit and Receive UTOPIA Interface block operates in the "Multi-PHY" mode ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*
3	Cell of 52Bytes	R/W	0	0: Transmit and Receive UTOPIA Interface blocks process 53 bytes/cell when the UTOPIA Data Bus width is set to 8 bits. The Transmit and Receive UTOPIA Interface blocks process 54 bytes when the UTOPIA Data Bus width is set to 16 bits. 1: Transmit and Receive UTOPIA Interface blocks process 52 bytes/cell, independent of the UTOPIA Data Bus width. ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*
2	Tx FIFO Depth('1)	R/W	0	00: Operating Depth of Transmit FIFO is 16 cells 01: Operating Depth of Transmit FIFO is 12 cells 10: Operating Depth of Transmit FIFO is 8 cells 11: Operating Depth of Transmit FIFO is 4 cells ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*
1	Tx FIFO Depth(0)	R/W	0	
0	UTOPIA Width16	R/W	0	0: Transmit and Receive UTOPIA Data Bus Width is configured to be 8 bits. 1: Transmit and Receive UTOPIA Data Bus Width is configured to be16 bits. ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*

TABLE 108: RX UTOPIA INTERRUPT ENABLE/STATUS REGISTER

REGISTER 107 **RX UTOPIA INTERRUPT ENABLE/STATUS REGISTER** **HEX ADDRESS: 0X6B**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Unused	RO	0	
6	R FIFO Reset	R/W	0	0: Normal operation A "0" to "1" transition resets the Read-Write pointers and FIFO memory ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*
5	Rx FIFO Overrun Interrupt Enable	R/W	0	0: Disables the "Rx FIFO Over-run" interrupt. 1: Enables the "Rx FIFO Over-run" interrupt. ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*
4	Rx FIFO Underrun Interrupt Enable	RO	0	0: Disables the "Rx FIFO Under-run" interrupt. 1: Enables the "Rx FIFO Under-run" interrupt. ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*
3	RCOCA Interrupt Enable	R/W	0	0: Disables the "Detection of RxRUNT Cell" Interrupt. 1: Enables the "Detection of RxRUNT Cell" Interrupt. ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*
2	R FIFO Ovr Interrupt Status	RUR	0	0: Indicates that the "RxFIFO Overrun" Interrupt has NOT occurred since the last read of this register. 1: Indicates that the "RxFIFO Overrun" Interrupt has occurred since the last read of this register. ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*
1	R FIFO Under Interrupt Status	RO	0	0: Indicates that the "RxFIFO Underrun" Interrupt has NOT occurred since the last read of this register. 1: Indicates that the "RxFIFO Underrun" Interrupt has occurred since the last read of this register. ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*
0	RCOCA Interrupt Stats	RUR	0	0: Indicates that the "Detection of RUNT Cell" Interrupt has NOT occurred since the last read of this register. 1: Indicates that the "Detection of RUNT Cell" Interrupt has occurred since the last read of this register. ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*

TABLE 109: RX UTOPIA ADDRESS

REGISTER 108 **RX UTOPIA ADDRESS** **HEX ADDRESS: 0X6C**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-5	Unused	RO	000	
4-0	Rx UTOPIA Address	R/W	00000	Programmable Rx UTOPIA address register to select device

TABLE 110: RX UTOPIA FIFO STATUS REGISTER

REGISTER 109 **RX UTOPIA FIFO STATUS REGISTER** **HEX ADDRESS: 0X6D**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Rx FIFO 16	R/W	0	0: Operating Depth of RxFIFO is 4 cells deep. 1: Operating Depth of RxFIFO is 16 cells deep. ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*
6	Reserved	R/W	0	Set to 0
4-2	Unused	RO	0	
1	Rx FIFO Full	RO	0	0: RxFIFO is not full 1: RxFIFO is full and if next event is not a read operation, it may cause over-run. ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*
0	Rx FIFO Empty	RO	1	0: RxFIFO is not empty 1: RxFIFO is empty and any subsequent read operation may cause and under-run to occur. ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*

TABLE 111: TX UTOPIA INTERRUPT/STATUS REGISTER

REGISTER 110	TX UTOPIA INTERRUPT/STATUS REGISTER	HEX ADDRESS: 0X6E

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Tx FIFO Reset	R/W	0	0 to 1 transition resets internal FIFO memory and its read-write pointers. ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*
6	Discard Upon PErr	R/W	0	0: "Transmit UTOPIA" Parity errors do not result in cell discard 1: Cells in which a "Transmit UTOPIA" parity error is detected are discarded. ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*
5	Tx Parity Error Interrupt Enable	R/W	0	0: Disables the "Transmit UTOPIA Detection of Parity Error" Interrupt. 1: Enables the "Transmit UTOPIA Detection of Parity Error" Interrupt. ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*
4	Tx FIFO Overrun Interrupt Enable	R/W	0	0: Disables the "TxFIFO Overrun" interrupt. 1: Enables the "TxFIFO Overrun" interrupt. ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*
3	TC Out of Cell Alignment Interrupt Enable	R/W	0	0: Disables the "Detection of TxRUNT Cell" interrupt. 1: Enables the "Detection of TxRUNT Cell" interrupt. ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*
2	TP Error Interrupt Status	RUR	0	0: Indicates that the "Detection of Transmit UTOPIA - Parity Error" Interrupt has NOT occurred since the last read of this register. 1: Indicates that the "Detection of Transmit UTOPIA - Parity Error" Interrupt has occurred since the last read of this register. ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*
1	Tx FIFO Interrupt Status	RUR	0	0: Indicates that the "TxFIFO Overrun" Interrupt has NOT occurred since the last read of this register. 1: Indicates that the "TxFIFO Overrun" Interrupt has occurred since the last read of this register. ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*
0	TC OCA Interrupt Status	RUR	0	0: Indicates that the "Detection of TxRUNT Cell" Interrupt has NOT occurred since the last read of this register. 1: Indicates that the "Detection of TxRUNT Cell" Interrupt has occurred since the last read of this register. ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*

TABLE 112: FUTURE USE

REGISTER 111	FUTURE USE	HEX ADDRESS: 0X6F

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION

TABLE 113: TX UTOPIA ADDRESS

REGISTER 112 **TX UTOPIA ADDRESS** **HEX ADDRESS: 0X70**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-5	Unused	RO	000	
4-0	Tx UTOPIA Address	R/W	00000	Programmable Tx UTOPIA address register for device selection

TABLE 114: TX UTOPIA STATUS REGISTER

REGISTER 113 **TX UTOPIA STATUS REGISTER** **HEX ADDRESS: 0X71**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-2	Unused	RO	0	
1	Tx FIFO Full	RO	0	0: Indicates that the Tx FIFO is not full. 1: Indicates that the Tx FIFO is full and that the next write operation may cause an overrun in the TxFIFO. ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*
0	Tx FIFO Empty	RO	1	0: Indicates that the TxFIFO is not empty 1: Indicates that the TxFIFO is Empty ***NOTE:*** *This bit-field is only active if the XRT72L73 is configured to operate in the "ATM UNI" Mode.*

TABLE 115: LINE INTERFACE DRIVE REGISTER

REGISTER 114 **LINE INTERFACE DRIVE REGISTER** **HEX ADDRESS: 0X72**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	R/W	0	
6	Reserved	R/W	0	
5	REQB	R/W	0	This "Read/Write" bit-field permits the user to control the state of the "REQB" Output pin. The "REQB" output pin can be connected to the "REQB" input pin of the XRT73L03 device. 0: Sets the "REQB" output pin to "0". If this output pin is connected to the "REQB" input pin of the LIU IC, then this setting will enable the "Receive Equalizer" within the LIU IC. 1: Sets the "REQB" output pin to "1". If this output pin is connected to the "REQB" input pin of the LIU IC, then this setting will disable the "Receive Equalizer" within the LIU IC. ***NOTE:*** *For guidelines on when to enable or disable the Receive Equalizer, within the LIU IC, please consult the XRT73L03 Data Sheet.*
4	TAOS	R/W	0	This "Read/Write" bit-field permits the user to control the state of the "TAOS" output pin. The "TAOS" output pin can be connected to the "TAOS" input pin of the XRT73L03 device. 0: Sets the "TAOS" output pin to "0". If this output pin is connected to the "TAOS" input of the LIU IC, then this setting will configure the Transmit Section of the LIU IC to transmit an "All Ones" pattern. 1: Sets the "TAOS" output pin to "1". If this output pin is connected to the "TAOS" input pin of the LIU IC, then this setting will NOT configure the Transmit Section of the LIU IC to transmit an "All Ones" pattern.
3	ENCODIS	R/W	1	This "Read/Write" bit-field permits the user to control the state of the "ENCODIS" output pin. The "ENCODIS" output pin can be connected to the "ENDECDIS" input pin of the XRT73L03 device. 0: Sets the "ENCODIS" output pin to "0". If this output pin is connected to the (ENCODIS and DECODIS) or ENDECDIS input pins of the LIU IC, then this settting will enable the HDB3/B3ZS Encoder/Decoder blocks within the LIU IC. 1: Sets the "ENCODIS" output pin to "1". If this output pin is connected to the "(ENCODIS and DECODIS) or "ENDECDIS input pins fo the LIU IC, then this setting will disable the "HDB3/B3ZS Encoder/Decoder blocks within the LIU IC.
2	Tx Lev	R/W	0	This "Read/Write" bit-field permits the user to control the state of the "TxLEV" output pin. The "TxLEV" output pin can be connected to the "TxLEV" input pin of the XRT73L03 device. 0: Sets the "TxLEV" output pin to "0". If this output pin is connected to the "TxLEV" input pin of the LIU IC, then this setting will enable the "Transmit Line Build-Out" circuit, within the Transmit Section of the LIU IC. 1: Sets the "TxLEV" output pin to "1". If this output pin is connected to the "TxLEV" input of the LIU IC, then this setting will disable the "Transmit Line Build-Out" circuit, within the Transmit Section of the LIU IC. ***NOTE:*** *For guidelines on when to enable or disable the "Transmit Line Build-Out" circuit, within the LIU IC, please consult the XRT73L03 Data Sheet.*

TABLE 115: LINE INTERFACE DRIVE REGISTER

REGISTER 114 **LINE INTERFACE DRIVE REGISTER** **HEX ADDRESS: 0X72**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	RLoop	R/W	0	This "Read/Write" bit-field permits the user to control the state of the "RLOOP" output pin. The "RLOOP" output pin can be connected to the "RLOOP" input pin of the XRT73L03 device. 0: Sets the "RLOOP" output pin to "0". If this output pin is connected to the "RLOOP" input of the LIU IC, then a variety of LIU Loop-back Modes can be configured via this register bit. 1: Sets the "RLOOP" output pin to "1". ***NOTE:*** *For information on the various loopback modes, which are available via the XRT73L03 device, please consult the XRT73L03 data sheet.*
0	LLoop	R/W	0	This "Read/Write" bit-field permits the user to control the state of the "LLOOP" output pin. The "RLOOP" output pin can be connected to the "LLOOP" input pin of the XRT73L03 device. 0: Sets the "LLOOP" output pin to "0". If this output pin is connected to the "LLOOP" input of the LIU IC, then a variety of LIU Loop-back Modes can be configured via this register bit. 1: Sets the "LLOOP" output pin to "1". ***NOTE:*** *For information on the various loopback modes, which are available via the XRT73L03 device, please consult the XRT73L03 data sheet.*

TABLE 116: LINE INTERFACE SCAN REGISTER

REGISTER 115 **LINE INTERFACE SCAN REGISTER** **HEX ADDRESS: 0X73**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-3	Unused	RO	0	
2	DMO	RO	0	This "Read-Only" bit-field permits the user to determine the current state of the "DMO" input pin. This input pin can be connected to the "DMO" output pin of the XRT73L03 device. 0: Indicates that the current state of the "DMO" input pin is "LOW". If this input pin is connected to the DMO output of the LIU IC, then this may indicate the occurrence of a fault condition in the "Transmit Output" line. 1: Indicates that the current state of the "DMO" input pin is "High". If this input pin is connected to the DMO output of the LIU IC, then this may indicate the occurrence of normal operation in the "Transmit Output" line. ***NOTE:*** *For more detailed information on the behavior of the DMO output pin (from the LIU), please consult the XRT73L03 data sheet.*
1	RLOL	RO	0	This "Read-Only" bit-field permits the user to determine the current state of the "RLOL" input pin. This input pin can be connected to the "RLOL" output pin of the XRT73L03 device. 0: Indicates that the current state of the "RLOL" input pin is "LOW". If this input pin is connected to the "RLOL" output of the LIU IC, then it indicates that the "Clock Recovery PLL" (within the LIU IC) is locked onto the "incoming" DS3 line signal. 1: Indicates that the current state of the "RLOL" input pin is "HIGH'. If this input pin is connected to the "RLOL" output of the LIU IC, then it indicates that the "Clock Recovery PLL" (within the LIU IC) is NOT locked onto the "incoming" DS3 line signal. ***NOTE:*** *For more detailed information on the behavior of the "RLOL" output pin (from the LIU), please consult the XRT73L03 data sheet.*
0	RLOS	RO	0	This "Read-Only" bit-field permits the user to determine the current state of the "RLOS" input pin. This input pin can (and should be) connected to the "RLOS" output pin of the XRT73L03 device. 0: Indicates that the current state of the "RLOS" input pin is "LOW". If this input pin is connected to the "RLOS" output pin of the LIU IC, then it indicates that the LIU is NOT currently declaring an LOS (Loss of Signal) condition. 1: Indicates that the current state of the "RLOS" input pin is "HIGH". If this input pin is connected to the "RLOS output pin of the LIU IC, then it indicates that the LIU is currently declaring an LOS condition. ***NOTES:*** 1. *If this input pin is pulled "High", then the XRT72L73 will automatically declare an LOS condition. As a consequence, the user should not treat the the "RLOS" input pin as a General Purpose Input pin.* 2. *For more detailed on the "LOS Declaration Criteria" for the XRT73L03 device, please consult the XRT73L03 data sheet.*

Line Interface Scan register provides DS3UNI framer chip capability to monitor status of line interface units. Configuration in this register is connected directly to the corresponding discrete I/O pins.

Note: These signals drive and scan the line interface chip XRT73L03.

TABLE 117: PMON CP-BIT ERROR EVENT COUNT REGISTER - MSB

REGISTER 116	PMON CP-BIT ERROR EVENT COUNT REGISTER - MSB	HEX ADDRESS: 0X74

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	CP-bit Error Count High-byte	RUR	0x00	This “Reset-upon-Read” register, along with “PMON CP-Bit Error Count Register - LSB” contains the 16 bit value for the total number of CP Bit errors that have been detected since the last read of this register. This register contains the “High” byte value of this 16-bit expression.

TABLE 118: PMON CP-BIT ERROR EVENT COUNT REGISTER - LSB

REGISTER 117	PMON CP-BIT ERROR EVENT COUNT REGISTER - LSB	HEX ADDRESS: 0X75

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	CP-bit Error Count Low-byte	RUR	0x00	This “Reset-upon-Read” register, along with “PMON CP-Bit Error Count Register - MSB” contains the 16 bit value for the total number of CP Bit errors that have been detected since the last read of this register. This register contains the “Low” byte value of this 16-bit expression.

TABLE 119: FRAME CP-BIT ERRORS - ONE SECOND ACCUMULATOR REGISTER - MSB

REGISTER 118	FRAME CP-BIT ERRORS - ONE SECOND ACCUMULATOR REGISTER - MSB	HEX ADDRESS: 0X76

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	CP- Bit Err 1 Sec H	RO	0x00	This “Read-Only” register, along with “CP-Bit Errors - One Second Accmulator Register - LSB” contains the 16-bit expression for the total number of CP-bit errors that have been detected within the last one second accumulation period. This register contains the “High” byte value of this expression.

TABLE 120: FRAME CP-BIT ERRORS - ONE SECOND ACCUMULATOR REGISTER - LSB

REGISTER 119	FRAME CP-BIT ERRORS - ONE SECOND ACCUMULATOR REGISTER - LSB	HEX ADDRESS: 0X77

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	CP- Bit Err 1 Sec L	RO	0x00	This “Read-Only” register, along with “CP-Bit Errors - One Second Accmulator Register - MSB” contains the 16-bit expression for the total number of CP-bit errors that have been detected within the last one second accumulation period. This register contains the “Low” byte value of this expression.

TABLE 121: UNUSED

REGISTER 120 TO 133	UNUSED	HEX ADDRESS: 0X78H TO 0X85

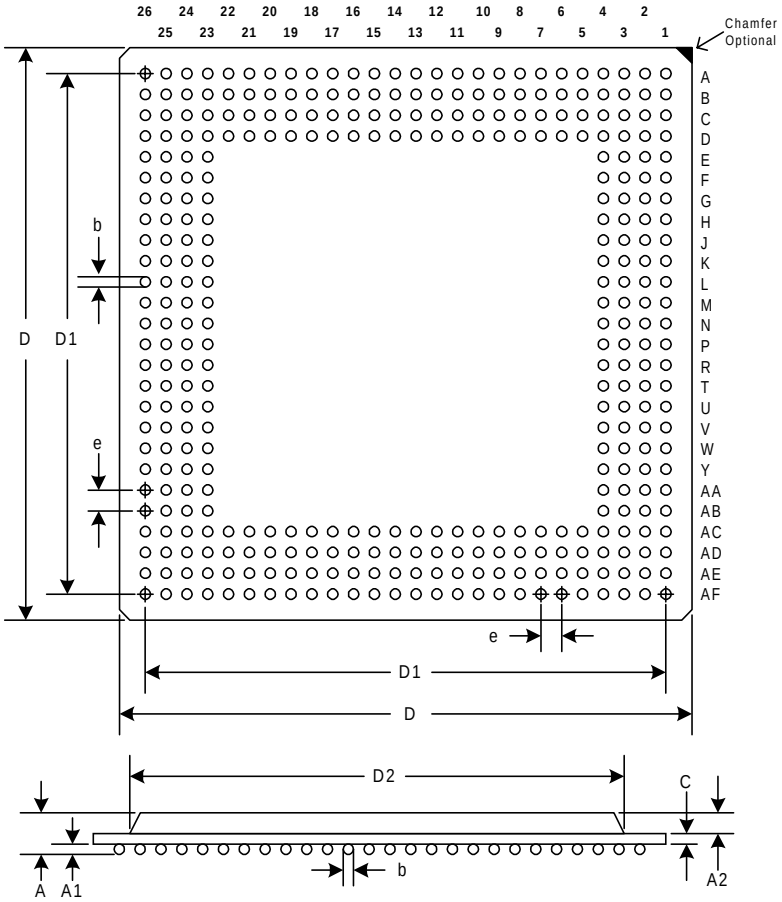
BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT72L73IB	35 X 35 MM, Plastic 352 Ball PBGA	-40°C to +85°C

PACKAGE DIMENSIONS

352 Ball Plastic Ball Grid Array
(35 x 35 mm PBGA)
Rev. 1.0



Symbol	Inches		Millimeters	
	MIN	MAX	MIN	MAX
A	0.075	0.106	1.90	2.70
A1	0.020	0.028	0.50	0.70
A2	0.039	0.051	1.00	1.30
b	0.024	0.035	0.60	0.90
C	0.016	0.028	0.40	0.70
D	1.370	1.386	34.80	35.20
D1	1.250BSC		31.75BSC	
D2	1.177	1.185	29.90	30.10
e	0.050BSC		1.27BSC	

Note: The control dimension is the millimeter column

REVISIONS

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