To all our customers

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Renesas Technology Home Page: http://www.renesas.com

Not recommend for new design

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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Keep safety first in your circuit designs!

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Not recommend for new design

2SJ576

Silicon P Channel MOS FET
High Speed Switching

ADE-208-741B (Z)
3rd.Edition.
June 1999

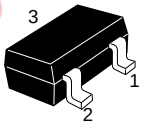
Not recommend for new design

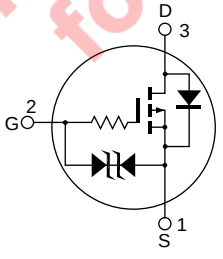
Features

- Low on-resistance
  R_{DS} =2.8 Ω typ. (V_{GS} = -10 V , I_D = -50 mA)
  R_{DS} =5.7 Ω typ. (V_{GS} = -4 V , I_D = -50 mA)
- 4 V gate drive device.
- Small package (CMPAK)

Outline

CMPAK





1. Source
2. Gate
3. Drain

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	-30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	-100	mA
Drain peak current	$I_{D(pulse)}$ Note1	-400	mA
Body-drain diode reverse drain current	I_{DR}	-100	mA
Channel dissipation	Pch Note 2	300	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Note: 1. PW ≤ 10 µs, duty cycle ≤ 1%
2. Value on the alumina ceramic board (12.5x20x0.7 mm)

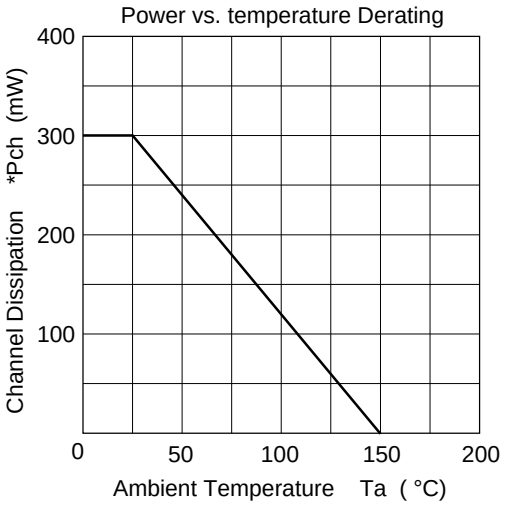
Not recommend for new design

Electrical Characteristics (Ta = 25°C)

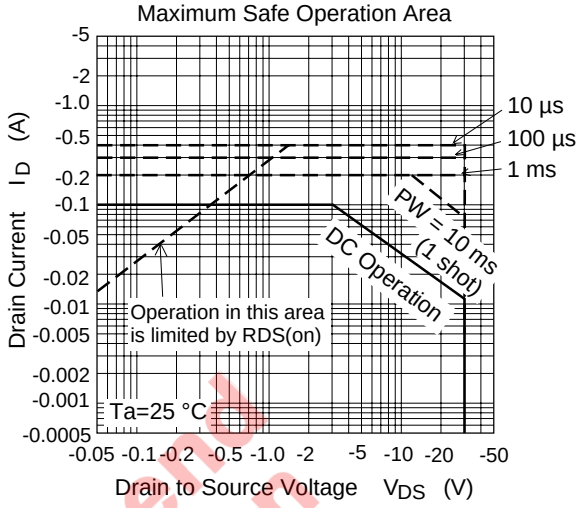
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-30	—	—	V	I_D = -100 µA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±5	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltege drain current	I_{DSS}	—	—	-1	µA	V_{DS} = -30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	-1.3	—	-2.3	V	I_D = -10µA, V_{DS} = -5 V
Static drain to source on state resistance	$R_{DS(on)}$	—	2.8	3.3	Ω	I_D = -50 mA,V_{GS} = -10 V Note 3
	$R_{DS(on)}$	—	5.7	7.9	Ω	I_D = -50 mA,V_{GS} = -4 V Note 3
Forward transfer admittance	$\|y_{fs}\|$	68	105	—	mS	I_D = -50 mA, V_{DS} = -10 V Note 3
Input capacitance	Ciss	—	25	—	pF	V_{DS} = -10 V
Output capacitance	Coss	—	20	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	8	—	pF	f = 1 MHz
Turn-on delay time	$t_{d(on)}$	—	10	—	ns	I_D = -50 mA, V_{GS} = -10 V
Rise time	t_r	—	15	—	ns	R_L = 200Ω
Turn-off delay time	$t_{d(off)}$	—	40	—	ns	
Fall time	t_f	—	45	—	ns	

Note: 3. Pulse test
4. Marking is AP
See characteristics curves of 2SJ575

Main Characteristics



*Value on the alumina ceramic board.(12.5x20x0.7mm)



Value on the alumina ceramic board.(12.5x20x0.7mm)

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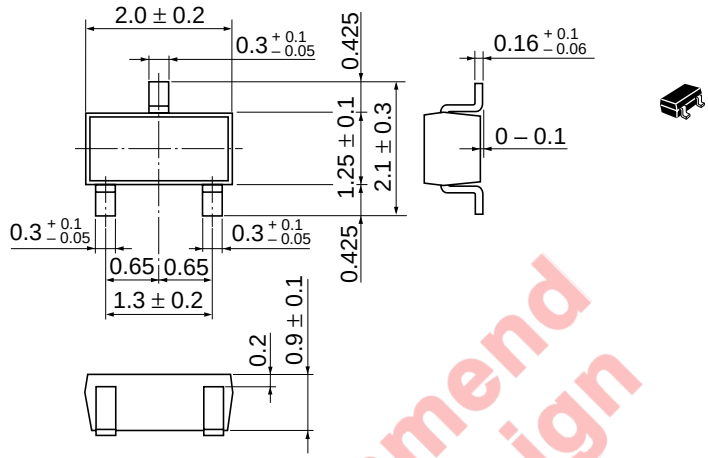
Package Dimensions

As of January, 2001

Unit: mm



Hitachi Code	CMPAK
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.006 g

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Cautions

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