PRELIMINARY

CY14C101Q
CY14B101Q, CY14E101Q

1-Mbit (128 K × 8) Serial (SPI) nvSRAM

Features

- 1-Mbit nonvolatile static random access memory (nvSRAM) internally organized as 128 K × 8
  - STORE to QuantumTrap nonvolatile elements initiated automatically on power-down (AutoStore) or by using SPI instruction (Software STORE) or $\overline{HSB}$ pin (Hardware STORE)
  - RECALL to SRAM initiated on power-up (Power-Up RECALL) or by SPI instruction (Software RECALL)
  - Support automatic STORE on power-down with a small capacitor (except for CY14X101Q1A)
- High reliability
  - Infinite read, write, and RECALL cycles
  - 1million STORE cycles to QuantumTrap
  - Data retention: 20 years at 85 °C
- 40 MHz, and 104 MHz High-speed serial peripheral interface (SPI)
  - 40-MHz clock rate SPI write and read with zero cycle delay
  - 104-MHz clock rate SPI write and SPI read (with special fast read instructions)
  - Supports SPI mode 0 (0,0) and mode 3 (1,1)
- SPI access to special functions
  - Nonvolatile STORE/RECALL
  - 8-byte serial number
  - Manufacturer ID and Product ID
  - Sleep mode
- Write protection
  - Hardware protection using Write Protect ($\overline{WP}$) pin
  - Software protection using Write Disable instruction
  - Software block protection for 1/4, 1/2, or entire array
- Low power consumption
  - Average active current of 3 mA at 40 MHz operation
  - Average standby mode current of 150 µA
  - Sleep mode current of 8 µA
- Industry standard configurations
  - Operating voltages:
    - CY14C101Q: V_{CC} = 2.4 V to 2.6 V
    - CY14B101Q: V_{CC} = 2.7 V to 3.6 V
    - CY14E101Q: V_{CC} = 4.5 V to 5.5 V
  - Industrial temperature
  - 8- and 16-pin small outline integrated circuit (SOIC) package
  - Restriction of hazardous substances (RoHS) compliant

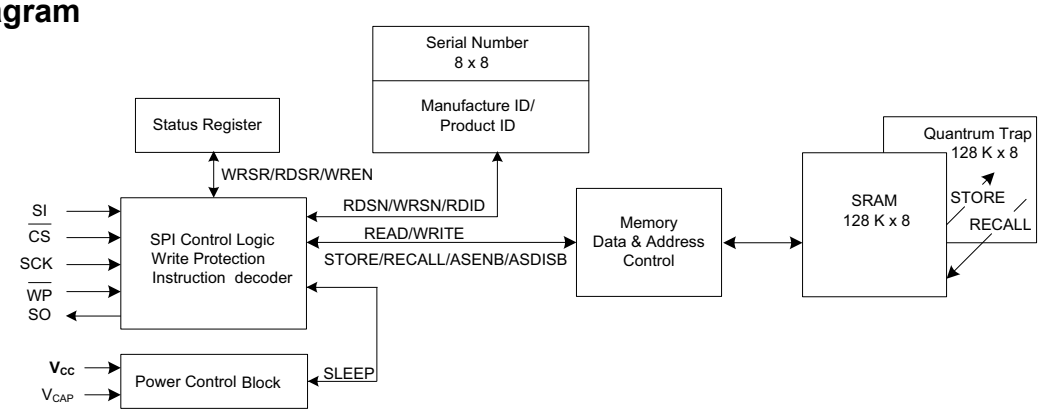
Functional Overview

The Cypress CY14X101Q combines a 1-Mbit nvSRAM with a nonvolatile element in each memory cell with serial SPI interface. The memory is organized as 128 K words of 8 bits each. The embedded nonvolatile elements incorporate the QuantumTrap technology, creating the world's most reliable nonvolatile memory. The SRAM provides infinite read and write cycles, while the QuantumTrap cells provide highly reliable nonvolatile storage of data. Data transfers from SRAM to the nonvolatile elements (STORE operation) takes place automatically at power-down (except for CY14X101Q1A). On power-up, data is restored to the SRAM from the nonvolatile memory (RECALL operation). You can also initiate the STORE and RECALL operations through SPI instruction.

Configuration

Feature	CY14X101Q1A	CY14X101Q2A	CY14X101Q3A
AutoStore	No	Yes	Yes
Software STORE	Yes	Yes	Yes
Hardware STORE	No	No	Yes

Logic Block Diagram



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Pinouts

Figure 1. Pin Diagram - 8-pin SOIC[1, 2, 3]

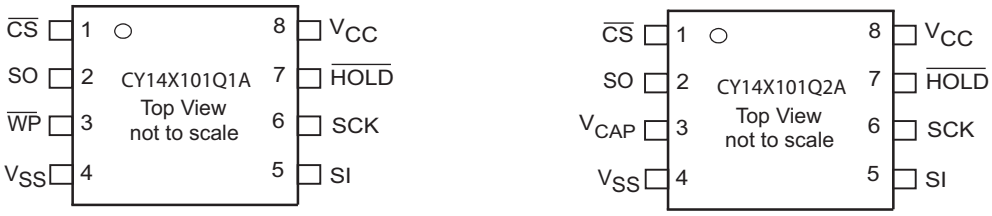
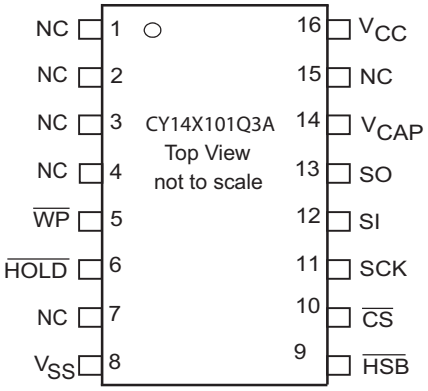


Figure 2. Pin Diagram - 16-pin SOIC



Pin Definitions

Pin Name[1, 2, 3]	I/O Type	Description
$\overline{CS}$	Input	Chip Select. Activates the device when pulled LOW. Driving this pin high puts the device in low power standby mode.
SCK	Input	Serial Clock. Runs at speeds up to a maximum of f_{SCK}. Serial input is latched at the rising edge of this clock. Serial output is driven at the falling edge of the clock.
SI	Input	Serial Input. Pin for input of all SPI instructions and data.
SO	Output	Serial Output. Pin for output of data through SPI.
$\overline{WP}$	Input	Write Protect. Implements hardware write protection in SPI.
$\overline{HOLD}$	Input	$\overline{HOLD}$ Pin. Suspends Serial Operation.
$\overline{HSB}$	Input/Output	Hardware STORE Busy: Output: Indicates busy status of nvSRAM when LOW. After each Hardware and Software STORE operation $\overline{HSB}$ is driven HIGH for a short time (t_{HHHD}) with standard output high current and then a weak internal pull up resistor keeps this pin HIGH (External pull up resistor connection optional). Input: Hardware STORE implemented by pulling this pin LOW externally.
V_{CAP}	Power supply	AutoStore Capacitor. Supplies power to the nvSRAM during power loss to STORE data from the SRAM to nonvolatile elements. If AutoStore is not needed, this pin must be left as No Connect. It must never be connected to ground.
NC	No connect	No Connect: This pin is not connected to the die.
V_{SS}	Power supply	Ground
V_{CC}	Power supply	Power supply

Notes
1. $\overline{HSB}$ pin is not available in 8-pin SOIC packages.
2. CY14X101Q1A part does not have V_{CAP} pin and does not support AutoStore.
3. CY14X101Q2A part does not have $\overline{WP}$ pin

Device Operation

CY14X101Q is a 1-Mbit serial (SPI) nvSRAM memory with a nonvolatile element in each memory cell. All the reads and writes to nvSRAM happen to the SRAM, which gives nvSRAM the unique capability to handle infinite writes to the memory. The data in SRAM is secured by a STORE sequence which transfers the data in parallel to the nonvolatile QuantumTrap cells. A small capacitor (V_{CAP}) is used to AutoStore the SRAM data in nonvolatile cells when power goes down providing power-down data security. The QuantumTrap nonvolatile elements built in the reliable SONOS technology make nvSRAM the ideal choice for secure data storage.

The 1-Mbit memory array is organized as 128 K words × 8 bits. The memory can be accessed through a standard SPI interface that enables very high clock speeds up to 40 MHz with zero cycle delay read and write cycles. This nvSRAM chip also supports 104 MHz SPI access speed with a special instruction for read operation. This device supports SPI modes 0 and 3 (CPOL, CPHA = 0, 0 and 1, 1) and operates as SPI slave. The device is enabled using the Chip Select ($\overline{CS}$) pin and accessed through Serial Input (SI), Serial Output (SO), and Serial Clock (SCK) pins.

This device provides the feature for hardware and software write protection through the $\overline{WP}$ pin and WRDI instruction respectively along with mechanisms for block write protection (1/4, 1/2, or full array) using BP0 and BP1 pins in the Status Register. Further, the $\overline{HOLD}$ pin is used to suspend any serial communication without resetting the serial sequence.

CY14X101Q uses the standard SPI opcodes for memory access. In addition to the general SPI instructions for read and write, it provides four special instructions that allow access to four nvSRAM specific functions: STORE, RECALL, AutoStore Disable (ASDISB), and AutoStore Enable (ASENB).

The major benefit of nvSRAM over serial EEPROMs is that all reads and writes to nvSRAM are performed at the speed of SPI bus with zero cycle delay. Therefore, no wait time is required after any of the memory accesses. The STORE and RECALL operations need finite time to complete and all memory accesses are inhibited during this time. While a STORE or RECALL operation is in progress, the busy status of the device is indicated by the Hardware STORE Busy ($\overline{HSB}$) pin and also reflected on the RDY bit of the Status Register.

The device is available in three different pin configurations that enable you to choose a part which fits in best in their application.

The feature summary is given in Table 1.

Table 1. Feature Summary

Feature	CY14X101Q1A	CY14X101Q2A	CY14X101Q3A
$\overline{WP}$	Yes	No	Yes
V_{CAP}	No	Yes	Yes
$\overline{HSB}$	No	No	Yes
AutoStore	No	Yes	Yes
Power-Up RECALL	Yes	Yes	Yes
Hardware STORE	No	No	Yes
Software STORE	Yes	Yes	Yes

SRAM Write

All writes to nvSRAM are carried out on the SRAM and do not use up any endurance cycles of the nonvolatile memory. This allows you to perform infinite write operations. A write cycle is performed through the WRITE instruction. The WRITE instruction is issued through the SI pin of the nvSRAM and consists of the WRITE opcode, three bytes of address, and one byte of data. Write to nvSRAM is done at SPI bus speed with zero cycle delay.

The device allows burst mode writes to be performed through SPI. This enables write operations on consecutive addresses without issuing a new WRITE instruction. When the last address in memory is reached in burst mode, the address rolls over to 0x00000 and the device continues to write.

The SPI write cycle sequence is defined explicitly in the Memory Access section of SPI Protocol Description.

SRAM Read

A read cycle is performed at the SPI bus speed. The data is read out with zero cycle delay after the READ instruction is executed. READ instruction can be used upto 40 MHz clock speed. The READ instruction is issued through the SI pin of the nvSRAM and consists of the READ opcode and three bytes of address. The data is read out on the SO pin.

A speed higher than 40 MHz (up to 104 MHz) requires FAST_READ instruction. The FAST_READ instruction is issued through the SI pin of the nvSRAM and consists of the FAST_READ opcode, three bytes of address, and one dummy byte. The data is read out on the SO pin.

This device allows burst mode reads to be performed through SPI. This enables reads on consecutive addresses without issuing a new READ instruction. When the last address in memory is reached in burst mode read, the address rolls over to 0x00000 and the device continues to read.

The SPI read cycle sequence is defined explicitly in the Memory Access section of SPI Protocol Description.

STORE Operation

STORE operation transfers the data from the SRAM to the nonvolatile QuantumTrap cells. The device STOREs data to the nonvolatile cells using one of the three STORE operations: AutoStore, activated on device power-down; Software STORE, activated by a STORE instruction; and Hardware STORE, activated by the HSB. During the STORE cycle, an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. After a STORE cycle is initiated, read/write to CY14X101Q is inhibited until the cycle is completed.

The HSB signal or the RDY bit in the Status Register can be monitored by the system to detect if a STORE or Software RECALL cycle is in progress. The busy status of nvSRAM is indicated by HSB being pulled LOW or RDY bit being set to '1'. To avoid unnecessary nonvolatile STOREs, AutoStore and Hardware STORE operations are ignored unless at least one write operation has taken place since the most recent STORE or RECALL cycle. However, software initiated STORE cycles are performed regardless of whether a write operation has taken place.

AutoStore Operation

The AutoStore operation is a unique feature of nvSRAM which automatically stores the SRAM data to QuantumTrap cells during power-down. This STORE makes use of an external capacitor (V_{CAP}) and enables the device to safely STORE the data in the nonvolatile memory when power goes down.

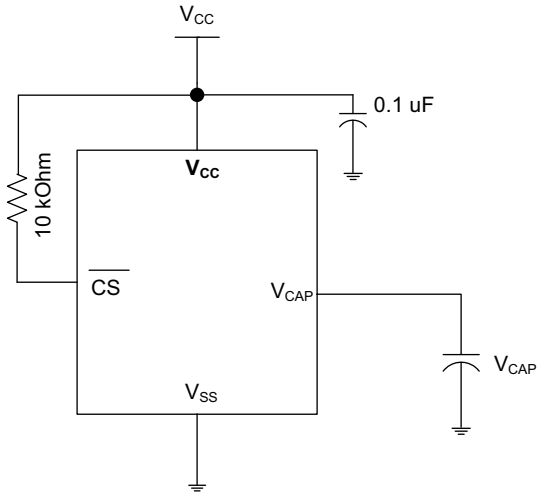
During normal operation, the device draws current from V_{CC} to charge the capacitor connected to the V_{CAP} pin. When the voltage on the V_{CC} pin drops below V_{SWITCH} during power-down, the device inhibits all memory accesses to nvSRAM and automatically performs a conditional STORE operation using the charge from the V_{CAP} capacitor. The AutoStore operation is not initiated if no write cycle has been performed since last RECALL.

Note If a capacitor is not connected to V_{CAP} pin, AutoStore must be disabled by issuing the AutoStore Disable instruction (AutoStore Disable (ASDISB) Instruction on page 15). If AutoStore is enabled without a capacitor on the V_{CAP} pin, the device attempts an AutoStore operation without sufficient charge to complete the STORE. This will corrupt the data stored in nvSRAM, Status Register as well as the serial number and it will unlock the SNL bit. To resume normal functionality, the WRSR instruction must be issued to update the nonvolatile bits BP0, BP1, and WPEN in the Status Register.

Figure 3 shows the proper connection of the storage capacitor (V_{CAP}) for AutoStore operation. Refer to DC Electrical Characteristics on page 21 for the size of the V_{CAP}.

Note CY14X101Q1A does not support AutoStore operation. You must perform Software STORE operation by using the SPI STORE instruction to secure the data.

Figure 3. AutoStore Mode



Software STORE Operation

Software STORE enables the user to trigger a STORE operation through a special SPI instruction. STORE operation is initiated by executing STORE instruction irrespective of whether a write has been performed since the last NV operation.

A STORE cycle takes t_{STORE} time to complete, during which all the memory accesses to nvSRAM are inhibited. The RDY bit of the Status Register or the HSB pin may be polled to find the Ready or Busy status of the nvSRAM. After the t_{STORE} cycle time is completed, the SRAM is activated again for read and write operations.

Hardware STORE and HSB pin Operation

The HSB pin in CY14X101Q3A is used to control and acknowledge STORE operations. If no STORE or RECALL is in progress, this pin can be used to request a Hardware STORE cycle. When the HSB pin is driven LOW, nvSRAM conditionally initiates a STORE operation after t_{DELAY} duration. A STORE cycle starts only if a write to the SRAM has been performed since the last STORE or RECALL cycle. Reads and Writes to the memory are inhibited for t_{STORE} duration or as long as HSB pin is LOW. The HSB pin also acts as an open drain driver (internal 100 kΩ weak pull up resistor) that is internally driven LOW to indicate a busy condition when the STORE (initiated by any means) is in progress.

Note After each Hardware and Software STORE operation HSB is driven HIGH for a short time (t_{HHHD}) with standard output high current and then remains HIGH by an internal 100 kΩ pull up resistor.

Note For successful last data byte STORE, a hardware STORE should be initiated at least one clock cycle after the last data bit D0 is received.

Upon completion of the STORE operation, the nvSRAM memory access is inhibited for t_{LZHSB} time after HSB pin returns HIGH. The HSB pin must be left unconnected if not used.

Note CY14X101Q1A/CY14X101Q2A do not have HSB pin. RDY bit of the SPI Status Register may be probed to determine the Ready or Busy status of nvSRAM.

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RECALL Operation

A RECALL operation transfers the data stored in the nonvolatile QuantumTrap elements to the SRAM. A RECALL may be initiated in two ways: Hardware RECALL, initiated on power-up and Software RECALL, initiated by a SPI RECALL instruction.

Internally, RECALL is a two step procedure. First, the SRAM data is cleared. Next, the nonvolatile information is transferred into the SRAM cells. All memory accesses are inhibited while a RECALL cycle is in progress. The RECALL operation does not alter the data in the nonvolatile elements.

Hardware RECALL (Power-Up)

During power-up, when V_{CC} crosses V_{SWITCH}, an automatic RECALL sequence is initiated, which transfers the content of nonvolatile memory on to the SRAM. The data would previously have been stored on the nonvolatile memory through a STORE sequence.

A Power-Up RECALL cycle takes t_{FA} time to complete and the memory access is disabled during this time. HSB pin is used to detect the ready status of the device.

Software RECALL

Software RECALL allows you to initiate a RECALL operation to restore the content of nonvolatile memory on to the SRAM. A Software RECALL is issued by using the SPI instruction for RECALL.

A Software RECALL takes t_{RECALL} time to complete during which all memory accesses to nvSRAM are inhibited. The controller must provide sufficient delay for the RECALL operation to complete before issuing any memory access instructions.

Disabling and Enabling AutoStore

If the application does not require the AutoStore feature, it can be disabled by using the ASDISB instruction. If this is done, the nvSRAM does not perform a STORE operation at power-down.

AutoStore can be re enabled by using the ASENB instruction. However, these operations are not nonvolatile and if you need this setting to survive the power cycle, a STORE operation must be performed following AutoStore Disable or Enable operation.

Note CY14X101Q2A/CY14X101Q3A has AutoStore enabled from the factory. In CY14X101Q1A, V_{CAP} pin is not present and AutoStore option is not available. The AutoStore Enable and Disable instructions to CY14X101Q1A are ignored.

Note If AutoStore is disabled and V_{CAP} is not required, then the V_{CAP} pin must be left open. The V_{CAP} pin must never be connected to ground. The Power-Up RECALL operation cannot be disabled in any case.

Serial Peripheral Interface

SPI Overview

The SPI is a four- pin interface with Chip Select ($\overline{CS}$), Serial Input (SI), Serial Output (SO), and Serial Clock (SCK) pins. CY14X101Q provides serial access to nvSRAM through SPI interface. The SPI bus on CY14X101Q can run at speeds up to 104 MHz except READ instruction.

The SPI is a synchronous serial interface which uses clock and data pins for memory access and supports multiple devices on the data bus. A device on SPI bus is activated using the $\overline{CS}$ pin.

The relationship between chip select, clock, and data is dictated by the SPI mode. This device supports SPI modes 0 and 3. In both these modes, data is clocked into the nvSRAM on the rising edge of SCK starting from the first rising edge after $\overline{CS}$ goes active.

The SPI protocol is controlled by opcodes. These opcodes specify the commands from the bus master to the slave device. After $\overline{CS}$ is activated the first byte transferred from the bus master is the opcode. Following the opcode, any addresses and data are then transferred. The $\overline{CS}$ must go inactive after an operation is complete and before a new opcode can be issued. The commonly used terms used in SPI protocol are given below:

SPI Master

The SPI master device controls the operations on a SPI bus. A SPI bus may have only one master with one or more slave devices. All the slaves share the same SPI bus lines and the master may select any of the slave devices using the $\overline{CS}$ pin. All the operations must be initiated by the master activating a slave device by pulling the $\overline{CS}$ pin of the slave LOW. The master also generates the SCK and all the data transmission on SI and SO lines are synchronized with this clock.

SPI Slave

The SPI slave device is activated by the master through the Chip Select line. A slave device gets the SCK as an input from the SPI master and all the communication is synchronized with this clock. SPI slave never initiates a communication on the SPI bus and acts on the instruction from the master.

CY14X101Q operates as a SPI slave and may share the SPI bus with other SPI slave devices.

Chip Select ($\overline{CS}$)

For selecting any slave device, the master needs to pull down the corresponding $\overline{CS}$ pin. Any instruction can be issued to a slave device only while the $\overline{CS}$ pin is LOW. When the device is not selected, data through the SI pin is ignored and the serial output pin (SO) remains in a high impedance state.

Note A new instruction must begin with the falling edge of $\overline{CS}$. Therefore, only one opcode can be issued for each active Chip Select cycle.

Serial Clock (SCK)

Serial clock is generated by the SPI master and the communication is synchronized with this clock after $\overline{CS}$ goes LOW.

CY14X101Q enables SPI modes 0 and 3 for data communication. In both these modes, the inputs are latched by the slave device on the rising edge of SCK and outputs are issued on the falling edge. Therefore, the first rising edge of SCK signifies the arrival of the first bit (MSB) of SPI instruction on the SI pin. Further, all data inputs and outputs are synchronized with SCK.

Data Transmission - SI/SO

SPI data bus consists of two lines, SI and SO, for serial data communication. The SI is also referred to as Master Out Slave

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In (MOSI) and SO is referred to as Master In Slave Out (MISO). The master issues instructions to the slave through the SI pin, while the slave responds through the SO pin. Multiple slave devices may share the SI and SO lines as described earlier.

CY14X101Q has two separate pins for SI and SO, which can be connected with the master as shown in Figure 4 on page 7.

Most Significant Bit (MSB)

The SPI protocol requires that the first bit to be transmitted is the Most Significant Bit (MSB). This is valid for both address and data transmission.

The 1-Mbit serial nvSRAM requires a 3-byte address for any read or write operation. However, since the address is only 17 bits, it implies that the first seven bits which are fed in are ignored by the device. Although these seven bits are 'don't care', Cypress recommends that these bits are treated as 0s to enable seamless transition to higher memory densities.

Serial Opcode

After the slave device is selected with $\overline{CS}$ going LOW, the first byte received is treated as the opcode for the intended operation. CY14X101Q uses the standard opcodes for memory accesses. In addition to the memory accesses, it provides additional opcodes for the nvSRAM specific functions: STORE, RECALL, AutoStore Enable, and AutoStore Disable. Refer to Table 2 on page 9 for details.

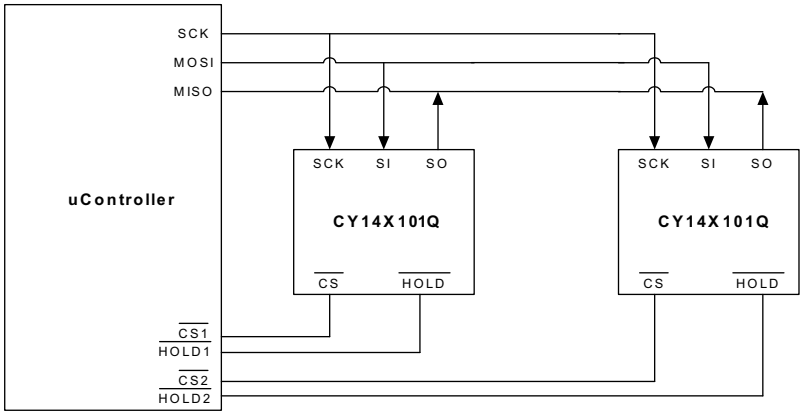
Invalid Opcode

If an invalid opcode is received, the opcode is ignored and the device ignores any additional serial data on the SI pin till the next falling edge of $\overline{CS}$ and the SO pin remains tri-stated.

Status Register

CY14X101Q has an 8-bit Status Register. The bits in the Status Register are used to configure the SPI bus. These bits are described in the Table 4 on page 10.

Figure 4. System Configuration Using SPI nvSRAM



SPI Modes

CY14X101Q may be driven by a microcontroller with its SPI peripheral running in either of the following two modes:

- SPI Mode 0 (CPOL=0, CPHA=0)
- SPI Mode 3 (CPOL=1, CPHA=1)

For both these modes, the input data is latched in on the rising edge of SCK starting from the first rising edge after $\overline{CS}$ goes active. If the clock starts from a HIGH state (in mode 3), the first rising edge after the clock toggles, is considered. The output data is available on the falling edge of SCK.

The two SPI modes are shown in Figure 5 and Figure 6. The status of clock when the bus master is in standby mode and not transferring data is:

- SCK remains at 0 for Mode 0
- SCK remains at 1 for Mode 3

CPOL and CPHA bits must be set in the SPI controller for either Mode 0 or Mode 3. The device detects the SPI mode from the status of SCK pin when the device is selected by bringing the $\overline{CS}$ pin LOW. If SCK pin is LOW when the device is selected, SPI Mode 0 is assumed and if SCK pin is HIGH, it works in SPI Mode 3.

Figure 5. SPI Mode 0

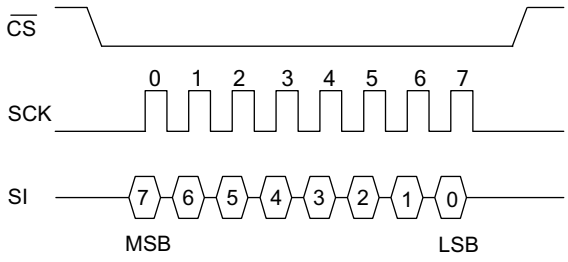


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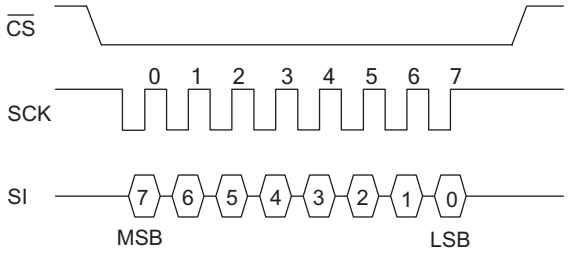
Figure 6. SPI Mode 3



SPI Operating Features

Power-Up

Power-up is defined as the condition when the power supply is turned on and V_{CC} crosses Vswitch voltage. During this time, the CS must be allowed to follow the V_{CC} voltage. Therefore, CS must be connected to V_{CC} through a suitable pull up resistor. As a built in safety feature, CS is both edge sensitive and level sensitive. After power-up, the device is not selected until a falling edge is detected on CS. This ensures that CS must have been HIGH, before going Low to start the first operation.

As described earlier, nvSRAM performs a Power-Up RECALL operation after power-up and therefore, all memory accesses are disabled for t_{FA} duration after power-up. The HSB pin can be probed to check the Ready/Busy status of nvSRAM after power-up.

Power On Reset

A Power On Reset (POR) circuit is included to prevent inadvertent writes. At power-up, the device does not respond to any instruction until the V_{CC} reaches the POR threshold voltage (V_{SWITCH}). After V_{CC} transitions the POR threshold, the device is internally reset and performs an power-Up RECALL operation. During power-Up RECALL all device accesses are inhibited. The device is in the following state after POR:

- Deselected (after power-up, a falling edge is required on CS before any instructions are started).
- Standby power mode
- Not in the HOLD condition
- Status Register state:
  - Write Enable (WEN) bit is reset to ‘0’.
  - WPEN, BP1, BP0 unchanged from previous STORE operation

The WPEN, BP1, and BP0 bits of the Status Register are nonvolatile bits and remain unchanged from the previous STORE operation.

Before selecting and issuing instructions to the memory, a valid and stable V_{CC} voltage must be applied. This voltage must remain valid until the end of the instruction transmission.

Power-Down

At power-down (continuous decay of V_{CC}), when V_{CC} drops from the normal operating voltage and below the V_{SWITCH} threshold voltage, the device stops responding to any instruction sent to it. If a write cycle is in progress and the last data bit D0 has been received when the power goes down, it is allowed t_{DELAY} time to complete the write. After this, all memory accesses are inhibited and a conditional AutoStore operation is performed (AutoStore is not performed if no writes have happened since the last RECALL cycle). This feature prevents inadvertent writes to nvSRAM from happening during power-down.

However, to completely avoid the possibility of inadvertent writes during power-down, ensure that the device is deselected and is in standby power mode, and the CS follows the voltage applied on V_{CC}.

Active Power and Standby Power Modes

When CS is LOW, the device is selected and is in the active power mode. The device consumes I_{CC} current, as specified in DC Electrical Characteristics on page 21. When CS is HIGH, the device is deselected and the device goes into the standby power mode after t_{SB} time if a STORE or RECALL cycle is not in progress. If a STORE/RECALL cycle is in progress, the device goes into the standby power mode after the STORE or RECALL cycle is completed. In the standby power mode, the current drawn by the device drops to I_{SB}.

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SPI Functional Description

The CY14X101Q uses an 8-bit instruction register. Instructions and their opcodes are listed in Table 2. All instructions, addresses, and data are transferred with the MSB first and start with a HIGH to LOW $\overline{CS}$ transition. There are, in all, 18 SPI instructions which provide access to most of the functions in nvSRAM. Further, the WP, HOLD and HSB pins provide additional functionality driven through hardware.

Table 2. Instruction Set

Instruction Category	Instruction Name	Opcode	Operation
Status Register Control Instructions			
Status Register access	RDSR	0000 0101	Read Status Register
	FAST_RDSR	0000 1001	Fast Status Register read - SPI clock >40 MHz
	WRSR	0000 0001	Write Status Register
Write protection and block protection	WREN	0000 0110	Set write enable latch
	WRDI	0000 0100	Reset write enable latch
SRAM Read/Write Instructions			
Memory access	READ	0000 0011	Read data from memory array
	FAST_READ	0000 1011	Fast read - SPI clock >40 MHz
	WRITE	0000 0010	Write data to memory array
Special NV Instructions			
nvSRAM special functions	STORE	0011 1100	Software STORE
	RECALL	0110 0000	Software RECALL
	ASENB	0101 1001	AutoStore Enable
	ASDISB	0001 1001	AutoStore Disable
Special Instructions			
Sleep	SLEEP	1011 1001	Sleep mode enable
Serial number	WRSN	1100 0010	Write serial number
	RDSN	1100 0011	Read serial number
	FAST_RDSN	1100 1001	Fast serial number read - SPI clock > 40 MHz
Device ID read	RDID	1001 1111	Read manufacturer JEDEC ID and product ID
	FAST_RDID	1001 1001	Fast manufacturer JEDEC ID and product ID Read - SPI clock > 40 MHz
Reserved	- Reserved -	0001 1110	

The SPI instructions are divided based on their functionality in the following types:

- Status Register control instructions:
  - Status Register access: RDSR, FAST_RDSR and WRSR instructions
  - Write protection and block protection: WREN and WRDI instructions along with WP pin and WEN, BP0, and BP1 bits
- SRAM read/write instructions
  - Memory access: READ, FAST_READ and WRITE instructions
- Special NV instructions
  - nvSRAM special instructions: STORE, RECALL, ASENB, and ASDISB
- Special instructions
  - SLEEP, WRSN, RDSN, FAST_RDSN, RDID, FAST_RDID

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Status Register

The Status Register bits are listed in Table 3. The Status Register consists of a Ready bit (RDY) and data protection bits BP1, BP0, WEN, and WPEN. The RDY bit can be polled to check the Ready or Busy status while a nvSRAM STORE or Software RECALL cycle is in progress. The Status Register can be modified by WRSR instruction and read by RDSR or FAST_RDSR instruction. However, only the WPEN, BP1, and BP0 bits of the Status Register can be modified by using the WRSR instruction. The WRSR instruction has no effect on WEN and RDY bits. The default value shipped from the factory for WEN, BP0, BP1, bits 4 -5, SNL and WPEN is '0'.

SNL (bit 6) of the Status Register is used to lock the serial number written using the WRSN instruction. The serial number can be written using the WRSN instruction multiple times while this bit is still '0'. When set to '1', this bit prevents any modification to the serial number. This bit is factory programmed to '0' and can only be written to once. After this bit is set to '1', it can never be cleared to '0'.

Table 3. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WPEN (0)	SNL (0)	X (0)	X (0)	BP1 (0)	BP0 (0)	WEN (0)	RDY

Table 4. Status Register Bit Definition

Bit	Definition	Description
Bit 0 (RDY)	Ready	Read only bit indicates the ready status of device to perform a memory access. This bit is set to '1' by the device while a STORE or Software RECALL cycle is in progress.
Bit 1 (WEN)	Write Enable	WEN indicates if the device is write enabled. This bit defaults to '0' (disabled) on power-up. WEN = '1' --> Write enabled WEN = '0' --> Write disabled
Bit 2 (BP0)	Block Protect bit '0'	Used for block protection. For details see Table 5 on page 12.
Bit 3 (BP1)	Block Protect bit '1'	Used for block protection. For details see Table 5 on page 12.
Bit 4-5	Don't care	These bits are non-writable and always return '0' upon read.
Bit 6 (SNL)	Serial Number Lock	Set to '1' for locking serial number
Bit 7 (WPEN)	Write Protect Enable bit	Used for enabling the function of Write Protect Pin (WP). For details see Table 6 on page 12.

Read Status Register (RDSR) Instruction

The Read Status Register instruction provides access to the Status Register at SPI frequency up to 40 MHz. This instruction is used to probe the Write Enable status of the device or the Ready status of the device. RDY bit is set by the device to 1 whenever a STORE or Software RECALL cycle is in progress. The block protection and WPEN bits indicate the extent of protection employed.

This instruction is issued after the falling edge of CS using the opcode for RDSR.

Fast Read Status Register (FAST_RDSR) Instruction

The FAST_RDSR instruction allows you to read the Status Register at a SPI frequency above 40 MHz and up to 104 MHz (max).This instruction is used to probe the Write Enable status of the device or the Ready status of the device. RDY bit is set by the device to 1 whenever a STORE or Software RECALL cycle is in progress. The block protection and WPEN bits indicate the extent of protection employed.

This instruction is issued after the falling edge of CS using the opcode for RDSR followed by a dummy byte.

Write Status Register (WRSR) Instruction

The WRSR instruction enables the user to write to the Status Register. However, this instruction cannot be used to modify bit 0 (RDY), bit 1 (WEN) and bits 4-5. The BP0 and BP1 bits can be used to select one of four levels of block protection. Further, WPEN bit must be set to '1' to enable the use of Write Protect (WP) pin.

WRSR instruction is a write instruction and needs writes to be enabled (WEN bit set to '1') using the WREN instruction before it is issued. The instruction is issued after the falling edge of CS using the opcode for WRSR followed by eight bits of data to be stored in the Status Register. WRSR instruction can be used to modify only bits 2, 3, 6 and 7 of the Status Register.

Note In CY14X101Q, the values written to Status Register are saved to nonvolatile memory only after a STORE operation. If AutoStore is disabled (or while using CY14X101Q1A), any modifications to the Status Register must be secured by performing a Software STORE operation.

Note CY14X101Q2A does not have WP pin. Any modification to bit 7 of the Status Register has no effect on the functionality of CY14X101Q2A.

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Figure 7. Read Status Register (RDSR) Instruction Timing

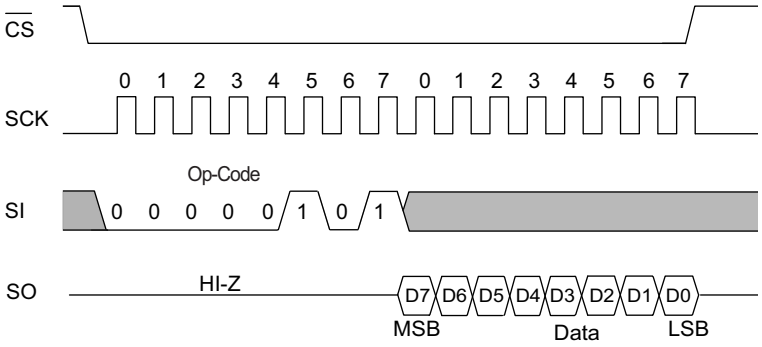


Figure 8. Fast Read Status Register (FAST_RDSR) Instruction Timing

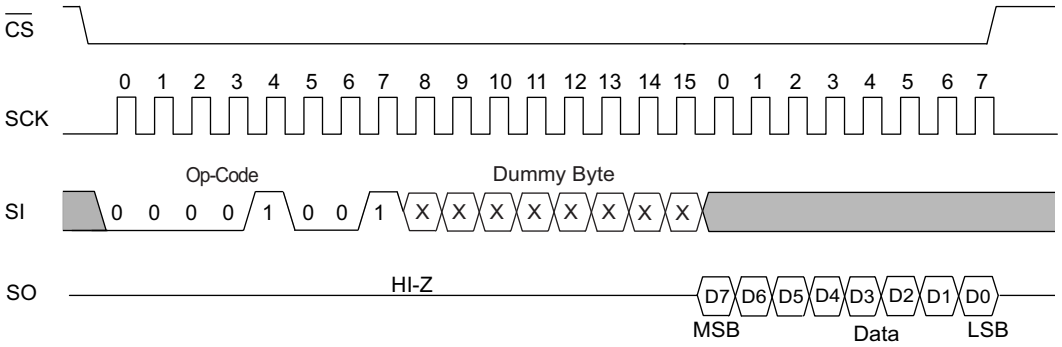
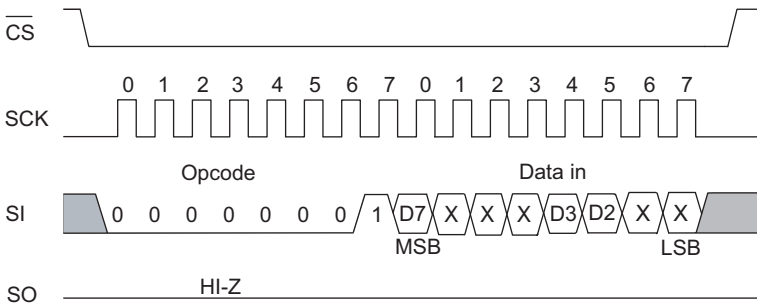


Figure 9. Write Status Register (WRSR) Instruction Timing



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Write Protection and Block Protection

CY14X101Q provides features for both software and hardware write protection using WRDI instruction and WP. Additionally, this device also provides block protection mechanism through BP0 and BP1 pins of the Status Register.

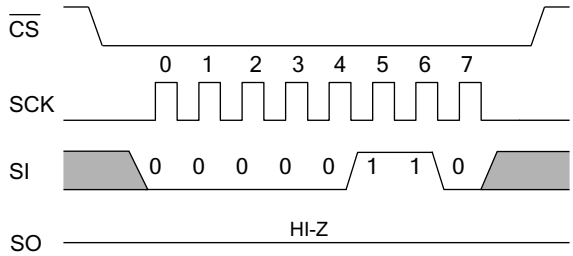
The write enable and disable status of the device is indicated by WEN bit of the Status Register. The write instructions (WRSR, WRITE and WRSN) and nvSRAM special instruction (STORE, RECALL, ASENB and ASDISB) need the write to be enabled (WEN bit = '1') before they can be issued.

Write Enable (WREN) Instruction

On power-up, the device is always in the write disable state. The following WRITE, WRSR, WRSN, or nvSRAM special instruction must therefore be preceded by a Write Enable instruction. If the device is not write enabled (WEN = '0'), it ignores the write instructions and returns to the standby state when CS is brought HIGH. A new CS falling edge is required to re-initiate serial communication. The instruction is issued following the falling edge of CS. When this instruction is used, the WEN bit of Status Register is set to '1'. WEN bit defaults to '0' on power-up.

Note After completion of a write instruction (WRSR, WRITE and WRSN) or nvSRAM special instruction (STORE, RECALL, ASENB, and ASDISB) instruction, WEN bit is cleared to '0'. This is done to provide protection from any inadvertent writes. Therefore, WREN instruction needs to be used before a new write instruction is issued.

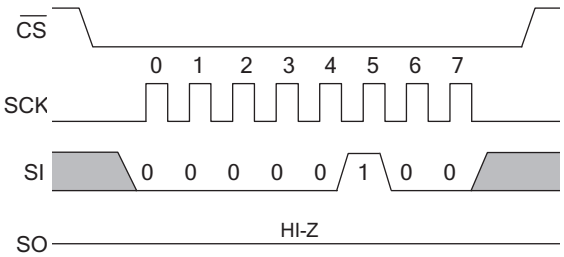
Figure 10. WREN Instruction



Write Disable (WRDI) Instruction

Write Disable instruction disables the write by clearing the WEN bit to '0' in order to protect the device against inadvertent writes. This instruction is issued following the falling edge of CS followed by opcode for WRDI instruction. The WEN bit is cleared on the rising edge of CS following a WRDI instruction.

Figure 11. WRDI Instruction



Block Protection

Block protection is provided using the BP0 and BP1 pins of the Status Register. These bits can be set using WRSR instruction and probed using the RDSR instruction. The nvSRAM is divided into four array segments. One-quarter, one-half, or all of the memory segments can be protected. Any data within the protected segment is read only. Table 5 shows the function of Block Protect bits.

Table 5. Block Write Protect Bits

Level	Status Register Bits		Array Addresses Protected
	BP1	BP0	
0	0	0	None
1 (1/4)	0	1	0x18000-0x1FFFF
2 (1/2)	1	0	0x10000-0x1FFFF
3 (All)	1	1	0x00000-0x1FFFF

Hardware Write Protection (WP)

The write protect pin (WP) is used to provide hardware write protection. WP pin enables all normal read and write operations when held HIGH. When the WP pin is brought LOW and WPEN bit is '1', all write operations to the Status Register are inhibited. The hardware write protection function is blocked when the WPEN bit is '0'. This allows you to install the device in a system with the WP pin tied to ground, and still write to the Status Register.

WP pin can be used along with WPEN and Block Protect bits (BP1 and BP0) of the Status Register to inhibit writes to memory. When WP pin is LOW and WPEN is set to '1', any modifications to the Status Register are disabled. Therefore, the memory is protected by setting the BP0 and BP1 bits and the WP pin inhibits any modification of the Status Register bits, providing hardware write protection.

Note WP going LOW when CS is still LOW has no effect on any of the ongoing write operations to the Status Register.

Note CY14X101Q2A does not have WP pin and therefore does not provide hardware write protection.

Table 6 summarizes all the protection features of this device

Table 6. Write Protection Operation

WPEN	WP	WEN	Protected Blocks	Unprotected Blocks	Status Register
X	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	LOW	1	Protected	Writable	Protected
1	HIGH	1	Protected	Writable	Writable

[+] Feedback

Memory Access

All memory accesses are done using the READ and WRITE instructions. These instructions cannot be used while a STORE or RECALL cycle is in progress. A STORE cycle in progress is indicated by the RDY bit of the Status Register and the HSB pin.

Read Sequence (READ) Instruction

The read operations on this device are performed by giving the instruction on the SI pin and reading the output on SO pin. The following sequence needs to be followed for a read operation: After the CS line is pulled LOW to select a device, the read opcode is transmitted through the SI line followed by three bytes of address. The most significant address byte contains A16 in bit 0 and other bits as 'don't cares'. Address bits A15 to A0 are sent in the following two address bytes. After the last address bit is transmitted on the SI pin, the data (D7-D0) at the specific address is shifted out on the SO line on the falling edge of SCK starting with D7. Any other data on SI line after the last address bit is ignored.

CY14X101Q allows reads to be performed in bursts through SPI which can be used to read consecutive addresses without issuing a new READ instruction. If only one byte is to be read, the CS line must be driven HIGH after one byte of data comes out. However, the read sequence may be continued by holding the CS line LOW and the address is automatically incremented and data continues to shift out on SO pin. When the last data memory address (0x1FFFF) is reached, the address rolls over to 0x00000 and the device continues to read.

Note The READ instruction operates up to a maximum of 40 MHz SPI frequency.

Fast Read Sequence (FAST_READ) Instruction

The FAST_READ instruction allows you to read memory at SPI frequency above 40 MHz and up to 104 MHz (Max). The host system must first select the device by driving CS low, the FAST_READ instruction is then written to SI, followed by 3 address byte containing the17 bit address (A16 -A0) and then a dummy byte.

From the subsequent falling edge of the SCK, the data of the specific address is shifted out serially on the SO line starting with MSB. The first byte specified can be at any location. The device automatically increments to the next higher address after each byte of data is output. The entire memory array can therefore be read with a single FAST_READ instruction. When the highest address in the memory array is reached, address counter rolls over to start address 0x00000 and thus allowing the read sequence to continue indefinitely. The FAST_READ instruction is terminated by driving CS High at any time during data output.

Note FAST_READ instruction operates up to maximum of 104 MHz SPI frequency.

Write Sequence (WRITE) Instruction

The write operations on this device are performed through the SI pin. To perform a write operation, if the device is write disabled, then the device must first be write enabled through the WREN instruction. When the writes are enabled (WEN = '1'), WRITE instruction is issued after the falling edge of CS. A WRITE instruction constitutes transmitting the WRITE opcode on SI line followed by three bytes of address and the data (D7-D0) which is to be written. The Most Significant address byte contains A16 in bit 0 with other bits being 'don't cares'. Address bits A15 to A0 are sent in the following two address bytes.

CY14X101Q enables writes to be performed in bursts through SPI which can be used to write consecutive addresses without issuing a new WRITE instruction. If only one byte is to be written, the CS line must be driven HIGH after the D0 (LSB of data) is transmitted. However, if more bytes are to be written, CS line must be held LOW and address is incremented automatically. The following bytes on the SI line are treated as data bytes and written in the successive addresses. When the last data memory address (0x1FFFF) is reached, the address rolls over to 0x00000 and the device continues to write. The WEN bit is reset to '0' on completion of a WRITE sequence.

Note When a burst write reaches a protected block address, it continues the address increment into the protected space but does not write any data to the protected memory. If the address roll over takes the burst write to unprotected space, it resumes writes. The same operation is true if a burst write is initiated within a write protected block.

Figure 12. Read Instruction Timing

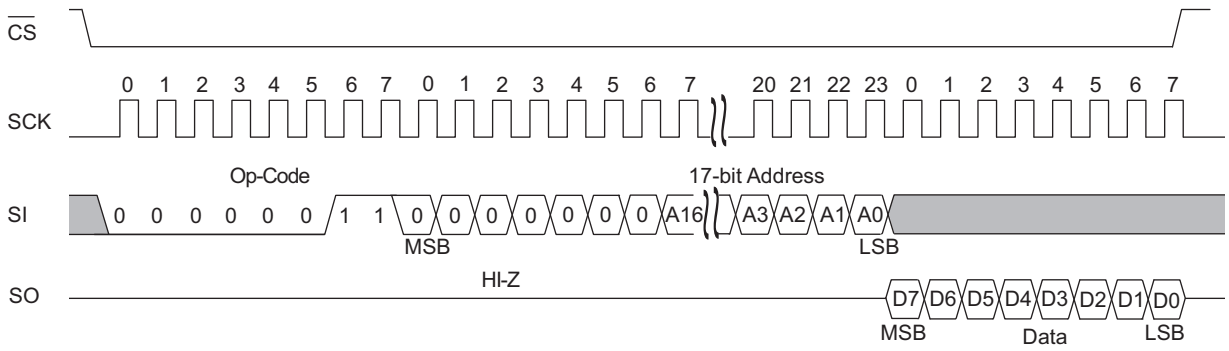


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Figure 13. Burst Mode Read Instruction Timing

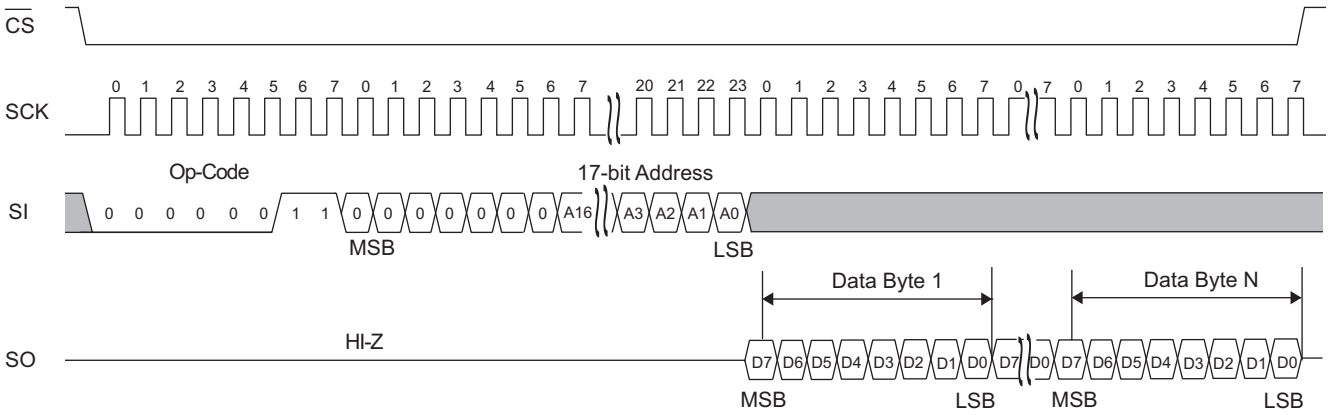


Figure 14. Fast Read Instruction Timing

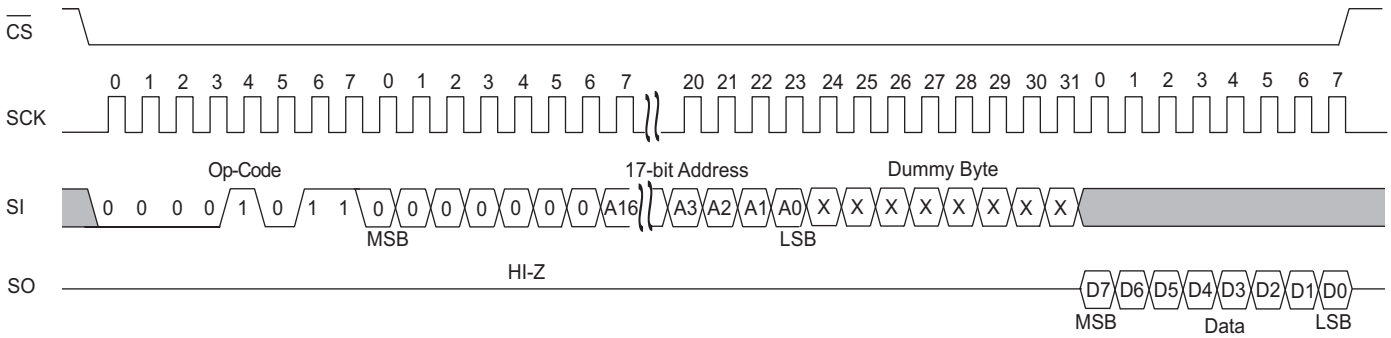


Figure 15. Write Instruction Timing

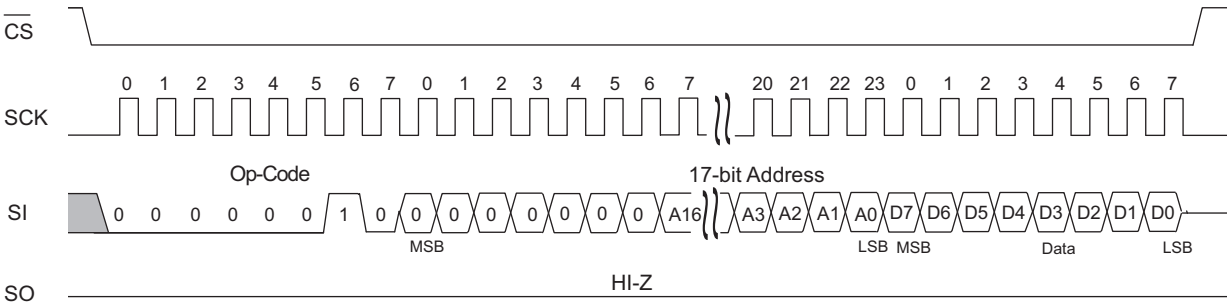
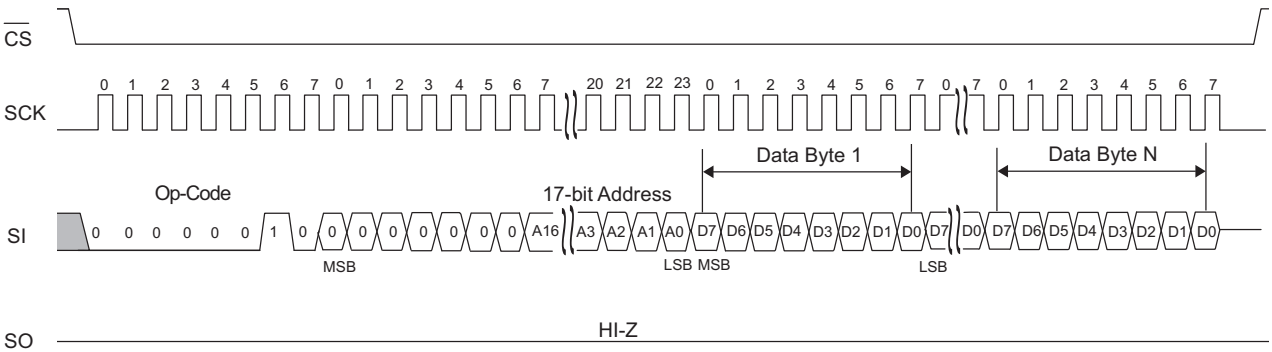


Figure 16. Burst Mode Write Instruction Timing



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nvSRAM Special Instructions

CY14X101Q provides four special instructions which enables access to the nvSRAM specific functions: STORE, RECALL, ASDISB, and ASENB. Table 7 lists these instructions.

Table 7. nvSRAM Special Instructions

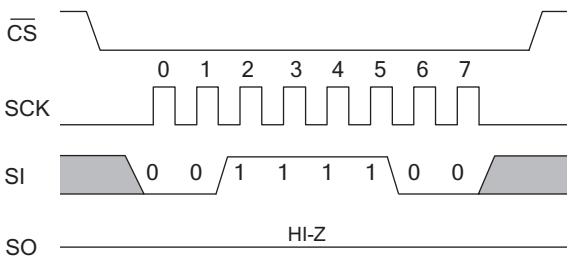
Function Name	Opcode	Operation
STORE	0011 1100	Software STORE
RECALL	0110 0000	Software RECALL
ASENB	0101 1001	AutoStore Enable
ASDISB	0001 1001	AutoStore Disable

Software STORE (STORE) Instruction

When a STORE instruction is executed, nvSRAM performs a Software STORE operation. The STORE operation is performed irrespective of whether a write has taken place since the last STORE or RECALL operation.

To issue this instruction, the device must be write enabled (WEN bit = '1'). The instruction is performed by transmitting the STORE opcode on the SI pin following the falling edge of CS. The WEN bit is cleared on the positive edge of CS following the STORE instruction.

Figure 17. Software STORE Operation

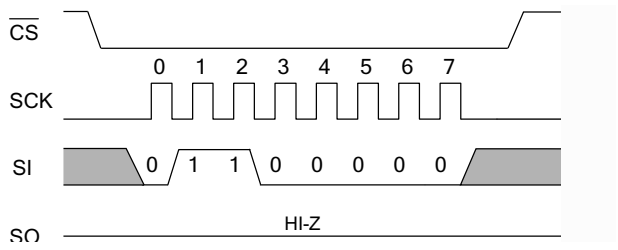


Software RECALL (RECALL) Instruction

When a RECALL instruction is executed, nvSRAM performs a Software RECALL operation. To issue this instruction, the device must be write enabled (WEN = '1').

The instruction is performed by transmitting the RECALL opcode on the SI pin following the falling edge of CS. The WEN bit is cleared on the positive edge of CS following the RECALL instruction.

Figure 18. Software RECALL Operation



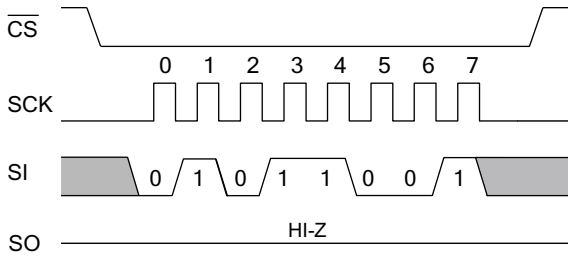
AutoStore Enable (ASENB) Instruction

The AutoStore Enable instruction enables the AutoStore on CY14X101Q2A/CY14X101Q3A. This setting is not nonvolatile and needs to be followed by a STORE sequence to survive the power cycle.

To issue this instruction, the device must be write enabled (WEN = '1'). The instruction is performed by transmitting the ASENB opcode on the SI pin following the falling edge of CS. The WEN bit is cleared on the positive edge of CS following the ASENB instruction.

Note If ASDISB and ASENB instructions are executed in CY14X101Q2A/CY14X101Q3A, the device is busy for the duration of software sequence processing time (t_{SS}). However, ASDISB and ASENB instructions have no effect on CY14X101Q1A as AutoStore is internally disabled.

Figure 19. AutoStore Enable Operation

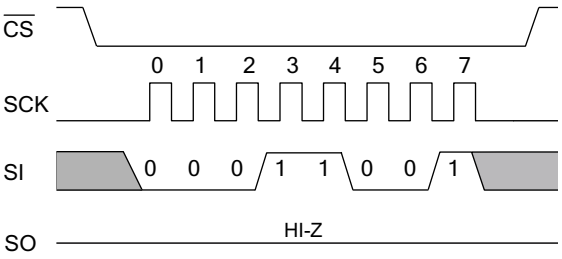


AutoStore Disable (ASDISB) Instruction

AutoStore is enabled by default in CY14X101Q2A/CY14X101Q3A. The ASDISB instruction disables the AutoStore. This setting is not nonvolatile and needs to be followed by a STORE sequence to survive the power cycle.

To issue this instruction, the device must be write enabled (WEN = '1'). The instruction is performed by transmitting the ASDISB opcode on the SI pin following the falling edge of CS. The WEN bit is cleared on the positive edge of CS following the ASDISB instruction.

Figure 20. AutoStore Disable Operation



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Special Instructions

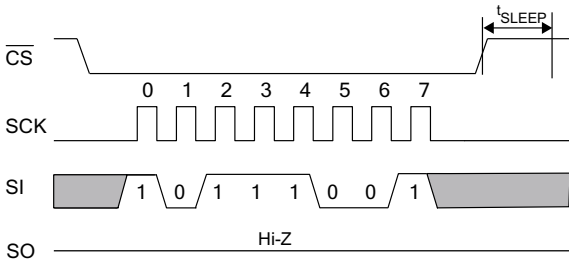
SLEEP Instruction

SLEEP instruction puts the nvSRAM in a sleep mode. When the SLEEP instruction is issued and $\overline{CS}$ is brought HIGH, the nvSRAM performs a STORE operation to secure the data to nonvolatile memory and then enters into sleep mode. The device starts consuming I_{ZZ} current after t_{SLEEP} time from the instance when SLEEP instruction is registered. The device is not accessible for normal operations after SLEEP instruction is issued. Once in sleep mode, the SCK and SI pins are ignored and SO is Hi-Z but device continues to monitor the $\overline{CS}$ pin.

To wake the nvSRAM from the sleep mode, the device must be selected by toggling the $\overline{CS}$ pin from HIGH to LOW. The device wakes up and is accessible for normal operations after t_{WAKE} duration after a falling edge of $\overline{CS}$ pin is detected.

Note Whenever nvSRAM enters into sleep mode, it initiates nonvolatile STORE cycle which results in an endurance cycle per sleep command execution. A STORE cycle starts only if a write to the SRAM has been performed since the last STORE or RECALL cycle.

Figure 21. Sleep Mode Entry



Serial Number

The serial number is an 8 byte programmable memory space provided to you uniquely identify this device. It typically consists of a two byte Customer ID, followed by five bytes of unique serial number and one byte of CRC check. However, nvSRAM does not calculate the CRC and it is up to the system designer to utilize the eight byte memory space in whatever manner desired. The default value for eight byte locations are set to ‘0x00’.

WRSN (Serial Number Write) Instruction

The serial number can be written using the WRSN instruction. To write serial number the write must be enabled using the WREN instruction. The WRSN instruction can be used in burst mode to write all the 8 bytes of serial number.

The serial number is locked using the SNL bit of the Status Register. Once this bit is set to '1', no modification to the serial number is possible. After the SNL bit is set to '1', using the WRSN instruction has no effect on the serial number.

A STORE operation (AutoStore or Software STORE) is required to store the serial number in nonvolatile memory. If AutoStore is disabled, you must perform a Software STORE operation to secure and lock the serial Number. If SNL bit is set to ‘1’ and is not stored (AutoStore disabled), the SNL bit and serial number defaults to ‘0’ at the next power cycle. If SNL bit is set to ‘1’ and is stored, the SNL bit can never be cleared to ‘0’. This instruction requires the WEN bit to be set before it can be executed. The WEN bit is reset to '0' after completion of this instruction.

Figure 22. WRSN Instruction

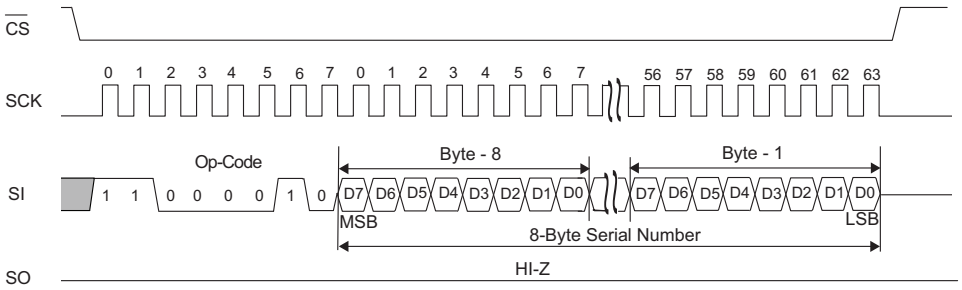
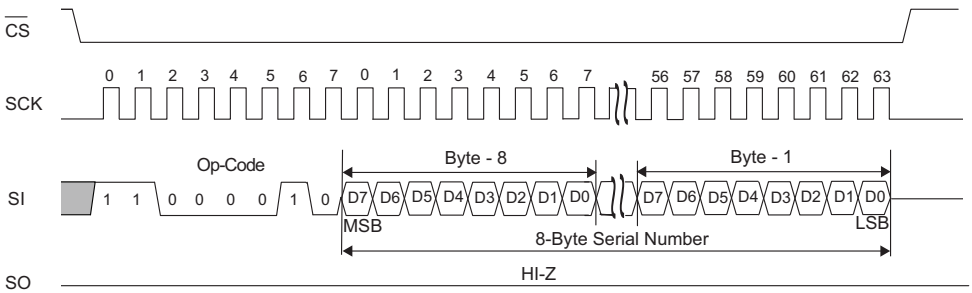


Figure 23. WRSN Instruction



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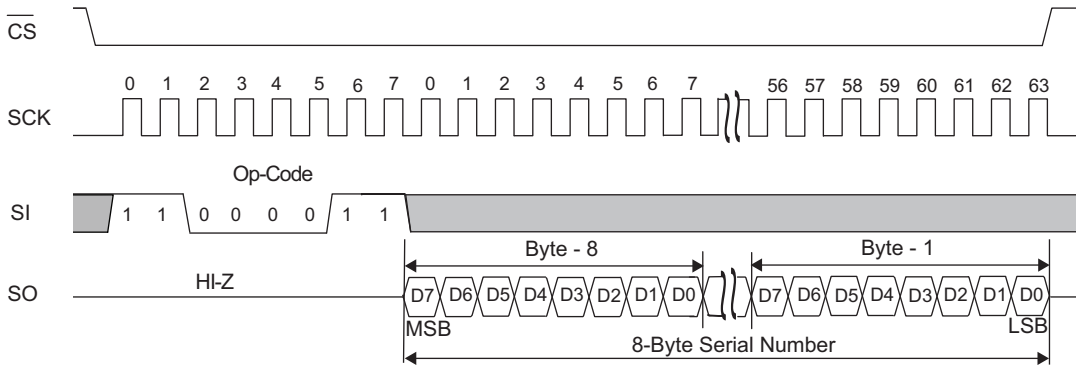
RDSN (Serial Number Read) Instruction

The serial number is read using RDSN instruction at SPI frequency upto 40 MHz. A serial number read may be performed in burst mode to read all the eight bytes at once. After the last byte of serial number is read, the device does not loop back. RDSN instruction can be issued by shifting the op-code for RDSN in through the SI pin of nvSRAM after CS goes LOW. This is followed by nvSRAM shifting out the eight bytes of serial number through the SO pin.

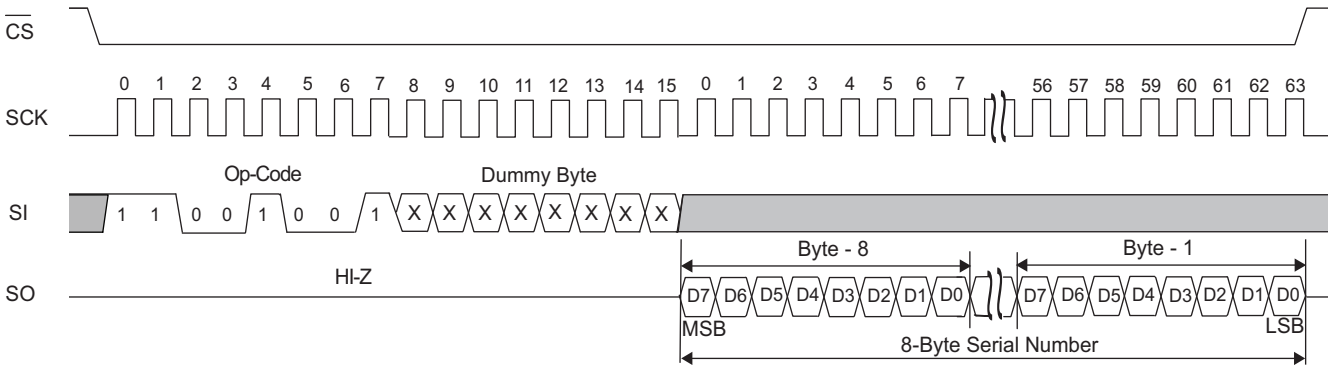
Figure 24. RDSN Instruction



FAST_RDSN (Fast Serial Number Read) Instruction

The FAST_RDSN instruction is used to read serial number at SPI frequency above 40 MHz and up to 104 MHz (max). A serial number read may be performed in burst mode to read all the eight bytes at once. After the last byte of serial number is read, the device does not loop back. FAST_RDSN instruction can be issued by shifting the op-code for FAST_RDSN in through the SI pin of nvSRAM followed by dummy byte after CS goes LOW. This is followed by nvSRAM shifting out the eight bytes of serial number through the SO pin.

Figure 25. FAST_RDSN Instruction



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Device ID

Device ID is 4-byte read only code identifying a type of product uniquely. This includes the product family code, configuration and density of the product.

Table 8. Device ID

Bits #of Bits	31 - 21 (11 bits)	20 - 7 (14 bits)	6- 3 (4 bits)	2 - 0 (3 bits)
Device	**Manufacture ID**	**Product ID**	**Density ID**	**Die Rev**
CY14C101Q1A	00000110100	00001000000001	0100	000
CY14C101Q2A	00000110100	00001100000000	0100	000
CY14C101Q3A	00000110100	00001100000001	0100	000
CY14B101Q1A	00000110100	00001000010001	0100	000
CY14B101Q2A	00000110100	00001100010000	0100	000
CY14B101Q3A	00000110100	00001100010001	0100	000
CY14E101Q1A	00000110100	00001000100001	0100	000
CY14E101Q2A	00000110100	00001100100000	0100	000
CY14E101Q3A	00000110100	00001100100001	0100	000

The device ID is divided into four parts as shown in Table 8:

1. Manufacturer ID (11 bits)

This is the JEDEC assigned manufacturer ID for Cypress. JEDEC assigns the manufacturer ID in different banks. The first three bits of the manufacturer ID represent the bank in which ID is assigned. The next eight bits represent the manufacturer ID.

Cypress's manufacturer ID is 0x34 in bank 0. Therefore the manufacturer ID for all Cypress nvSRAM products is:

Cypress ID - 000_0011_0100

2. Product ID (14 bits)

The product ID is defined as shown in the Table 8

3. Density ID (4 bits)

The 4 bit density ID is used as shown in Table 8 for indicating the 1Mb density of the product.

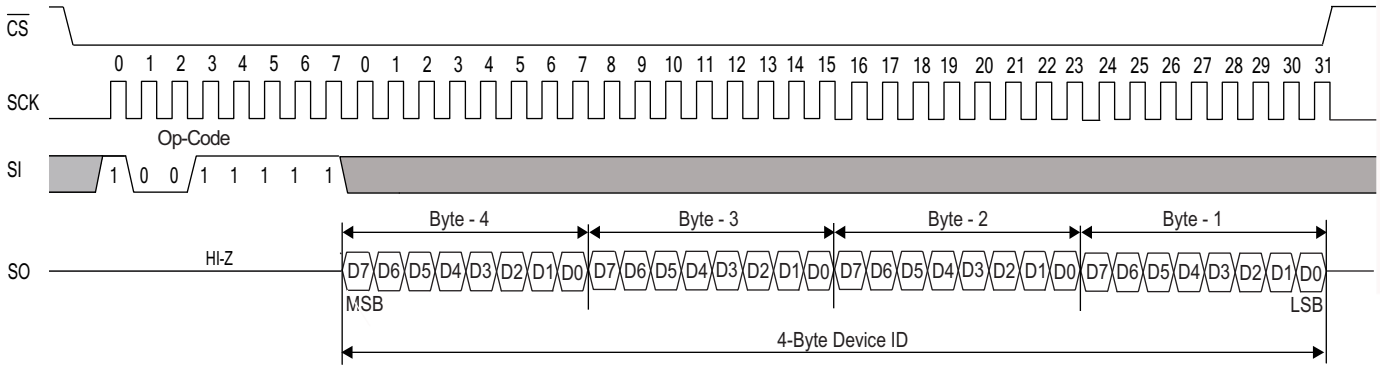
4. Die Rev (3 bits)

This is used to represent any major change in the design of the product. The initial setting of this is always 0x0.

RDID (Device ID Read) Instruction

This instruction is used to read the JEDEC assigned manufacturer ID and product ID of the device at SPI frequency upto 40 MHz. This instruction can be used to identify a device on the bus. RDID instruction can be issued by shifting the op-code for RDID in through the SI pin of nvSRAM after CS goes LOW. This is followed by nvSRAM shifting out the four bytes of device ID through the SO pin.

Figure 26. RDID instruction

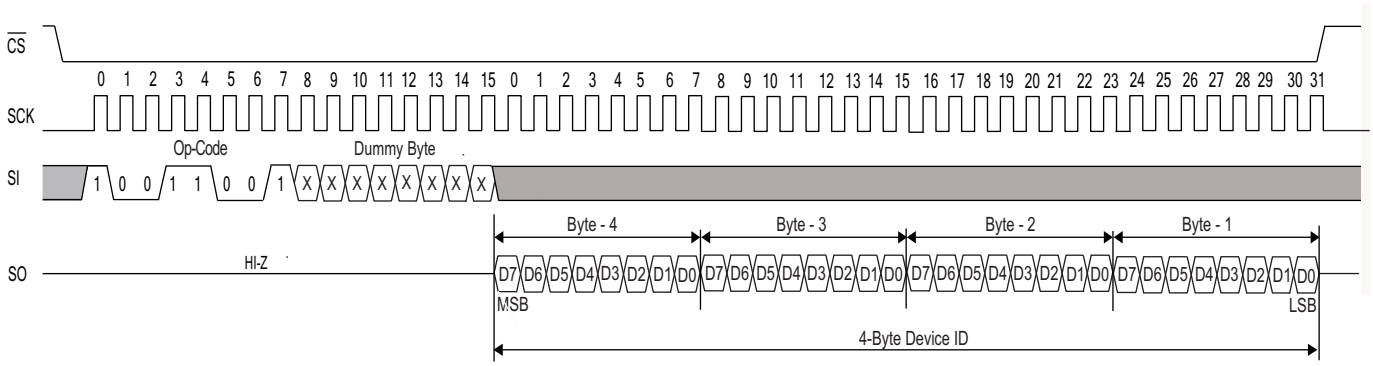


[+] Feedback

FAST_RDID (Fast Device ID Read) Instruction

The FAST_RDID instruction allows the user you to read the JEDEC assigned manufacturer ID and product ID at SPI frequency above 40 MHz and up to 104 MHz (max). FAST_RDID instruction can be issued by shifting the op-code for FAST_RDID in through the SI pin of nvSRAM followed by dummy byte after CS goes LOW. This is followed by nvSRAM shifting out the four bytes of device ID through the SO pin.

Figure 27. FAST_RDID instruction

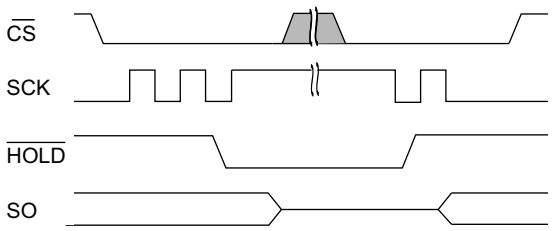


HOLD Pin Operation

The HOLD pin is used to pause the serial communication. When the device is selected and a serial sequence is underway, HOLD is used to pause the serial communication with the master device without resetting the ongoing serial sequence. To pause, the HOLD pin must be brought LOW when the SCK pin is LOW. To resume serial communication, the HOLD pin must be brought HIGH when the SCK pin is LOW (SCK may toggle during HOLD). While the device serial communication is paused, inputs to the SI pin are ignored and the SO pin is in the high impedance state.

This pin can be used by the master with the CS pin to pause the serial communication by bringing the pin HOLD LOW and deselecting an SPI slave to establish communication with another slave device, without the serial communication being reset. The communication may be resumed at a later point by selecting the device and setting the HOLD pin HIGH.

Figure 28. HOLD Operation



[+] Feedback

Best Practices

nvSRAM products have been used effectively for over 26 years. While ease-of-use is one of the product's main system values, experience gained working with hundreds of applications has resulted in the following suggestions as best practices:

- The nonvolatile cells in this nvSRAM product are delivered by Cypress with 0x00 written in all cells. Incoming inspection routines at customer or contract manufacturer's sites sometimes reprogram these values. Final NV patterns are typically repeating patterns of AA, 55, 00, FF, A5, or 5A. End product's firmware should not assume an NV array is in a set programmed state. Routines that check memory content values to determine first time system configuration, cold or warm boot status, and so on should always program a unique NV pattern (that is, complex 4-byte pattern of 46 E6 49 53 hex or more random bytes) as part of the final system manufacturing test to ensure these system routines work consistently.
- Power-up boot firmware routines should rewrite the nvSRAM into the desired state (for example, AutoStore enabled). While the nvSRAM is shipped in a preset state, best practice is to again rewrite the nvSRAM into the desired state as a safeguard against events that might flip the bit inadvertently such as program bugs and incoming inspection routines.
- The V_{CAP} value specified in this data sheet includes a minimum and a maximum value size. Best practice is to meet this requirement and not exceed the maximum V_{CAP} value because the nvSRAM internal algorithm calculates V_{CAP} charge and discharge time based on this max V_{CAP} value. Customers that want to use a larger V_{CAP} value to make sure there is extra store charge and store time should discuss their V_{CAP} size selection.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Maximum accumulated storage time

At 150 °C ambient temperature ..... 1000 h

At 85 °C ambient temperature ..... 20 Years

Ambient temperature with power applied ..... –55 °C to +150 °C

Supply voltage on V_{CC} relative to V_{SS}

CY14C101Q: V_{CC} = 2.4 V to 2.6 V ....–0.5 V to +3.1 V

CY14B101Q: V_{CC} = 2.7 V to 3.6 V ....–0.5 V to +4.1 V

CY14E101Q: V_{CC} = 4.5 V to 5.5 V ....–0.5 V to +7.0 V

DC voltage applied to outputs in High Z state ..... –0.5 V to V_{CC} + 0.5 V

Input voltage ..... –0.5 V to V_{CC} + 0.5 V

Transient voltage (< 20 ns) on any pin to ground potential ..... –2.0 V to V_{CC} + 2.0 V

Package power dissipation capability (T_A = 25 °C) ..... 1.0 W

Surface mount lead soldering temperature (3 seconds) ..... +260 °C

DC output current (1 output at a time, 1s duration) ..... 15 mA

Static discharge voltage ..... > 2001 V (per MIL-STD-883, Method 3015)

Latch up current ..... > 140 mA

Table 9. Operating Range

Device	Range	Ambient Temperature	V_{CC}
CY14C101Q	Industrial	–40 °C to +85 °C	2.4 V to 2.6 V
CY14B101Q			2.7 V to 3.6 V
CY14E101Q			4.5 V to 5.5 V

DC Electrical Characteristics

Parameter	Description	Test Conditions		Min	Typ[4]	Max	Unit
V_{CC}	Power supply		CY14C101Q	2.4	2.5	2.6	V
			CY14B101Q	2.7	3.0	3.6	V
			CY14E101Q	4.5	5.0	5.5	V
I_{CC1}	Average V_{CC} current	f_{SCK} = 40 MHz; Values obtained without output loads (I_{OUT} = 0 mA)	CY14C101Q	–	–	3	mA
			CY14B101Q				
			CY14E101Q	–	–	4	mA
		f_{SCK} = 104 MHz; Values obtained without output loads (I_{OUT} = 0 mA)		–	–	10	mA
I_{CC2}	Average V_{CC} current during STORE	All inputs don't care, V_{CC} = Max Average current for duration t_{STORE}		–	–	2	mA
I_{CC3}	Average V_{CC} current f_{SCK} = 1 MHz; V_{CC} = V_{CC} (Typ), 25 °C	All inputs cycling at CMOS levels. Values obtained without output loads (I_{OUT} = 0 mA)		–	–	1	mA
I_{CC4}	Average V_{CAP} current during AutoStore cycle	All inputs don't care. Average current for duration t_{STORE}		–	–	3	mA
I_{SB}	V_{CC} standby current	$\overline{CS} \geq (V_{CC} – 0.2\ V)$. $V_{IN} \leq 0.2$ V or $\geq (V_{CC} – 0.2\ V)$. Standby current level after nonvolatile cycle is complete. Inputs are static. f_{SCK} = 0 MHz.		–	–	150	µA
I_{ZZ}	Sleep mode current	t_{SLEEP} time after SLEEP Instruction is registered. All inputs are static and configured at CMOS logic level.		–	–	8	µA
I_{IX}[5]	Input leakage current (except $\overline{HSB}$)			–1	–	+1	µA
	Input leakage current (for $\overline{HSB}$)			–100	–	+1	µA

Notes

4. Typical values are at 25 °C, V_{CC} = V_{CC} (Typ). Not 100% tested.
5. The $\overline{HSB}$ pin has I_{OUT} = -2 µA for V_{OH} of 2.4 V when both active high and LOW drivers are disabled. When they are enabled standard V_{OH} and V_{OL} are valid. This parameter is characterized but not tested.

[+] Feedback

DC Electrical Characteristics (continued)

Parameter	Description	Test Conditions		Min	Typ[4]	Max	Unit
I_{OZ}	Off-state output leakage current			–1	–	+1	µA
V_{IH}	Input HIGH voltage		CY14C101Q	1.7	–	V_{CC} + 0.5	V
			CY14B101Q	2.0	–	V_{CC} + 0.5	V
			CY14E101Q				
V_{IL}	Input LOW voltage		CY14C101Q	V_{SS} – 0.5	–	0.7	V
			CY14B101Q	V_{SS} – 0.5	–	0.8	V
			CY14E101Q				
V_{OH}	Output HIGH voltage	I_{OUT} = –1 mA	CY14C101Q	2.0	–	–	V
		I_{OUT} = –2 mA	CY14B101Q	2.4	–	–	V
			CY14E101Q				
V_{OL}	Output LOW voltage	I_{OUT} = 2 mA	CY14C101Q	–	–	0.4	V
		I_{OUT} = 4 mA	CY14B101Q	–	–	0.4	V
			CY14E101Q				
V_{CAP}	Storage capacitor	Between V_{CAP} pin and V_{SS}	CY14C101Q	170	220	270	µF
			CY14B101Q	42	47	180	µF
			CY14E101Q				

Data Retention and Endurance

Parameter	Description	Min	Unit
$DATA_R$	Data retention	20	Years
NV_C	Nonvolatile STORE operations	1,000	K

Capacitance

Parameter[6]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = V_{CC} (Typ)	7	pF
C_{OUT}	Output pin capacitance		7	pF

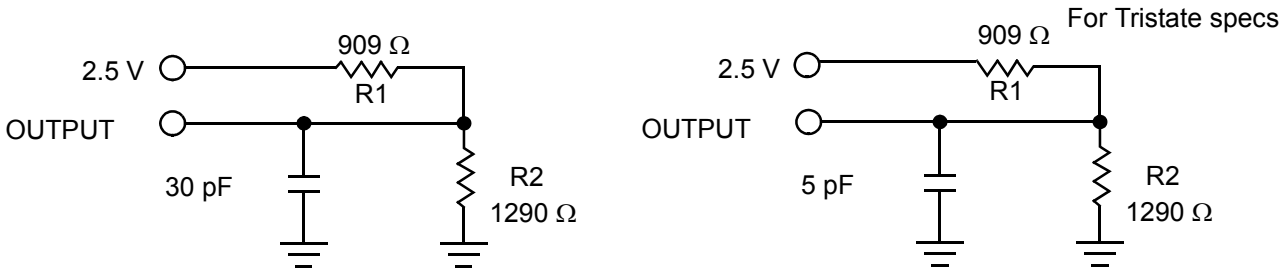
Thermal Resistance

Parameter [6]	Description	Test Conditions	8-pin SOIC	16-pin SOIC	Unit
Θ_{JA}	Thermal resistance (Junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	101.08	56.68	°C/W
Θ_{JC}	Thermal resistance (Junction to case)		37.86	32.11	°C/W

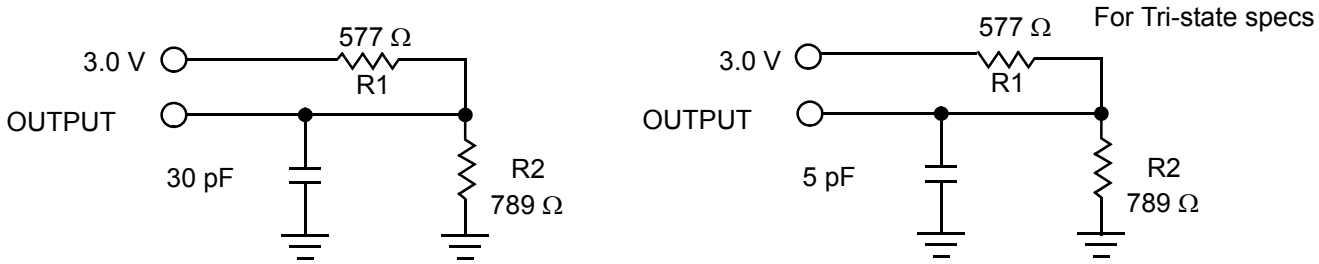
Note
6. These parameters are guaranteed by design and are not tested.

Figure 29. AC Test Loads and Waveforms

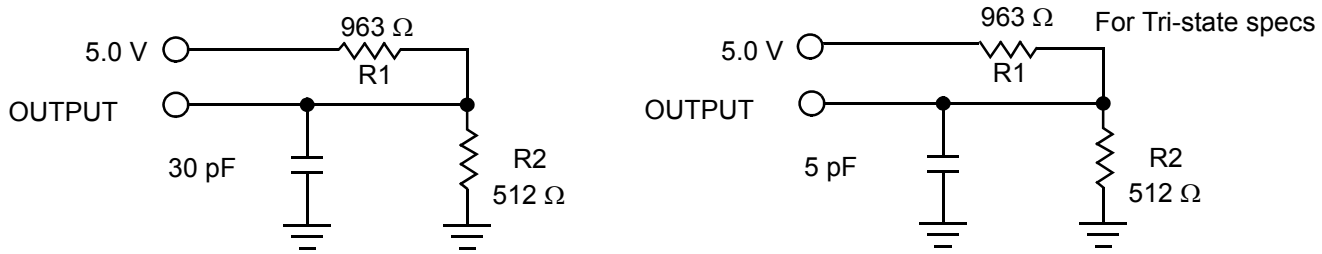
For 2.5 V (CY14C101Q):



For 3 V (CY14B101Q):



For 5 V (CY14E101Q):



AC Test Conditions

	CY14C101Q	CY14B101Q	CY14E101Q
Input pulse levels	0 V to 2.5 V	0 V to 3 V	0 V to 3 V
Input rise and fall times (10% - 90%)	≤ 3 ns	≤ 3 ns	≤ 3 ns
Input and output timing reference levels	1.25 V	1.5 V	1.5 V

AC Switching Characteristics

Cypress Parameter	Alt. Parameter	Description	40 MHz		104 MHz		Unit
			Min	Max	Min	Max	
f_{SCK}	f_{SCK}	Clock frequency, SCK	–	40	–	104	MHz
t_{CL}[7]	t_{WL}	Clock pulse width LOW	11	–	4.5	–	ns
t_{CH}[7]	t_{WH}	Clock pulse width HIGH	11	–	4.5	–	ns
t_{CS}	t_{CE}	CS HIGH time	20	–	20	–	ns
t_{CSS}	t_{CES}	CS setup time	10	–	5	–	ns
t_{CSH}	t_{CEH}	CS hold time	10	–	5	–	ns
t_{SD}	t_{SU}	Data in setup time	5	–	4	–	ns
t_{HD}	t_{H}	Data in hold time	5	–	3	–	ns
t_{HH}	t_{HD}	HOLD hold time	5	–	3	–	ns
t_{SH}	t_{CD}	HOLD setup time	5	–	3	–	ns
t_{CO}	t_{V}	Output Valid	–	9	–	8	ns
t_{HHZ}[7]	t_{HZ}	HOLD to output HIGH Z	–	15	–	8	ns
t_{HLZ}[7]	t_{LZ}	HOLD to output LOW Z	–	15	–	8	ns
t_{OH}	t_{HO}	Output hold time	0	–	0	–	ns
t_{HZCS}[7]	t_{DIS}	Output disable time	–	20	–	8	ns

Figure 30. Synchronous Data Timing (Mode 0)

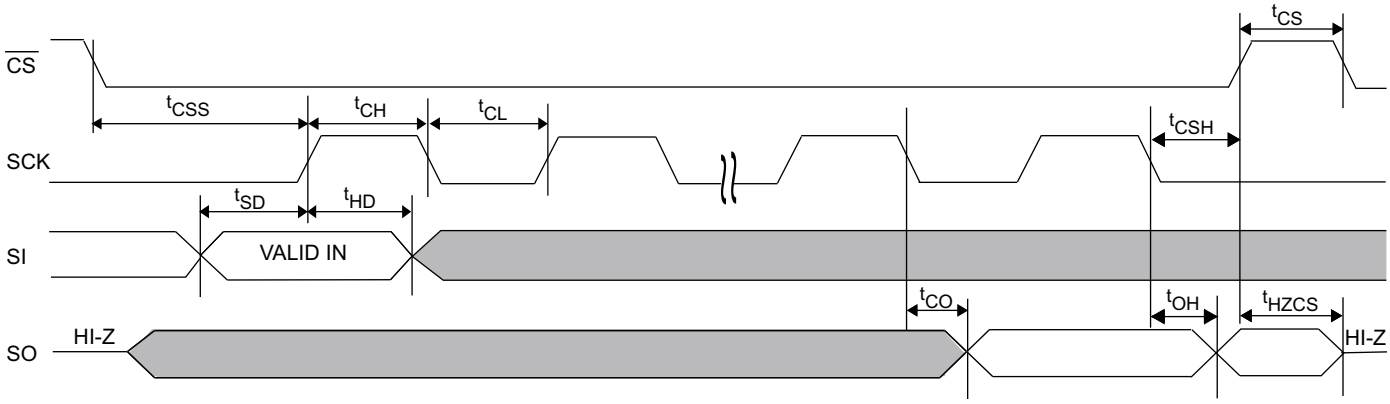
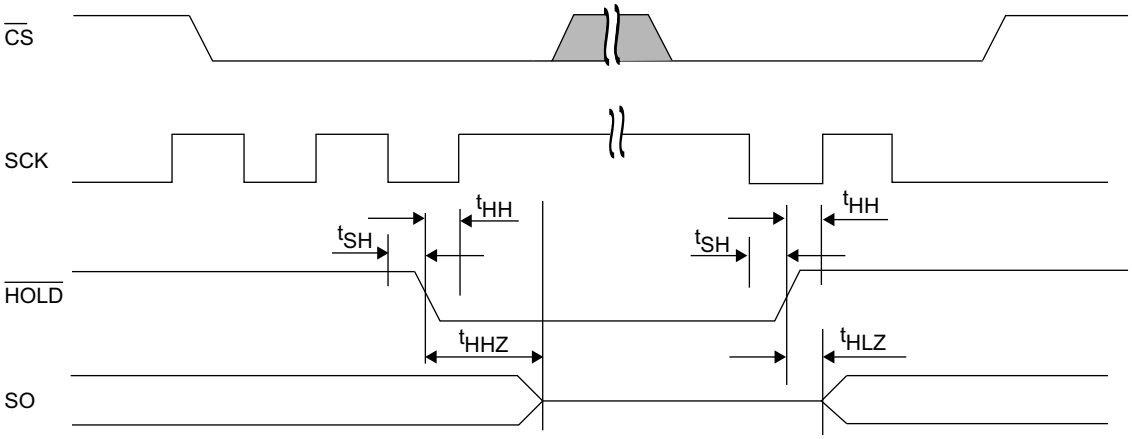


Figure 31. HOLD Timing



Note
7. These parameters are guaranteed by design and are not tested.

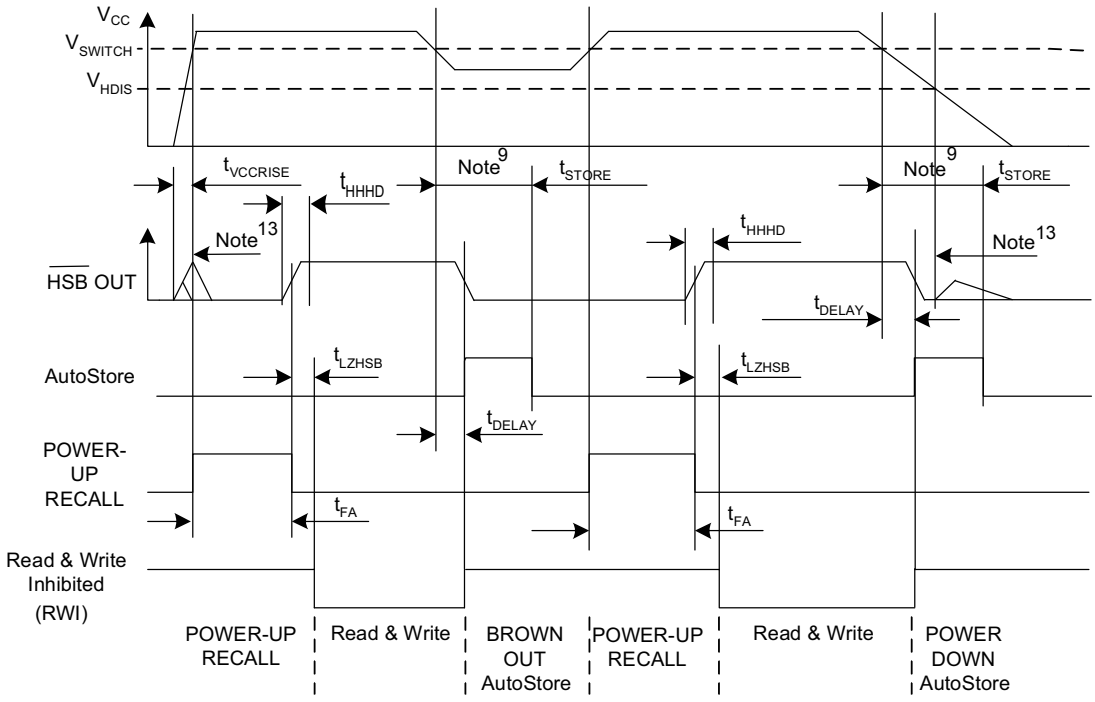
[+] Feedback

AutoStore or Power-Up RECALL

Parameter	Description		CY14X101Q Min	CY14X101Q Max	Unit
t_{FA} [8]	Power-Up RECALL duration	CY14C101Q	–	40	ms
		CY14B101Q	–	20	ms
		CY14E101Q	–	20	ms
t_{STORE} [9]	STORE cycle duration		–	8	ms
t_{DELAY} [10]	Time allowed to complete SRAM write cycle		–	25	ns
V_{SWITCH}	Low voltage trigger level	CY14C101Q	–	2.35	V
		CY14B101Q	–	2.65	V
		CY14E101Q	–	4.40	V
$t_{VCCRISE}$ [11]	V_{CC} rise time		150	–	µs
V_{HDIS} [11]	HSB output disable voltage		–	1.9	V
t_{LZHSB} [11]	HSB high to nvSRAM active time		–	5	µs
t_{HHHD} [11]	HSB high active time		–	500	ns
t_{WAKE}	Time for nvSRAM to wake up from SLEEP mode	CY14C101Q	–	40	ms
		CY14B101Q	–	20	ms
		CY14E101Q	–	20	ms
t_{SLEEP}	Time to enter SLEEP mode after issuing SLEEP instruction		–	8	ms
t_{SB}	Time to enter into standby mode after CS going HIGH		–	100	µs

Switching Waveforms

Figure 32. AutoStore or Power-Up RECALL[12]



Notes
8. t_{FA} starts from the time V_{CC} rises above V_{SWITCH}.
9. If an SRAM write has not taken place since the last nonvolatile cycle, AutoStore or Hardware STORE is not initiated.
10. On a Hardware STORE, Software STORE / RECALL, AutoStore Enable / Disable and AutoStore initiation, SRAM operation continues to be enabled for time t_{DELAY}.
11. These parameters are guaranteed by design and are not tested.
12. Read and Write cycles are ignored during STORE, RECALL, and while V_{CC} is below V_{SWITCH}.
13. During power-up and power-down, HSB glitches when HSB pin is pulled up through an external resistor.

[+] Feedback

Software Controlled STORE and RECALL Cycles

Parameter	Description	CY14X101Q		Unit
		Min	Max	
t_{RECALL}	RECALL duration	–	600	µs
t_{SS} [14, 15]	Soft sequence processing time	–	500	µs

Switching Waveforms

Figure 33. Software STORE Cycle[15]

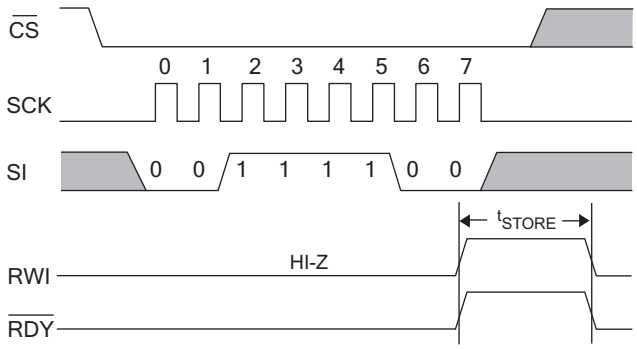


Figure 34. Software RECALL Cycle[15]

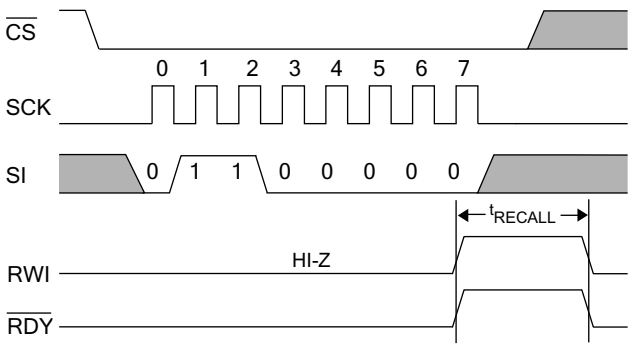


Figure 35. AutoStore Enable Cycle

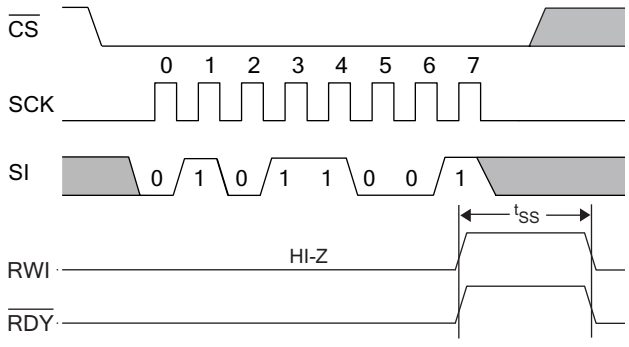
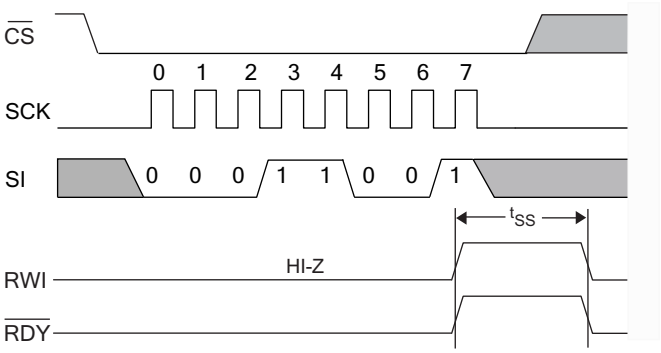


Figure 36. AutoStore Disable Cycle



Notes
14. This is the amount of time it takes to take action on a soft sequence command. Vcc power must remain HIGH to effectively register command.
15. Commands such as STORE and RECALL lock out I/O until operation is complete which further increases this time. See the specific command.

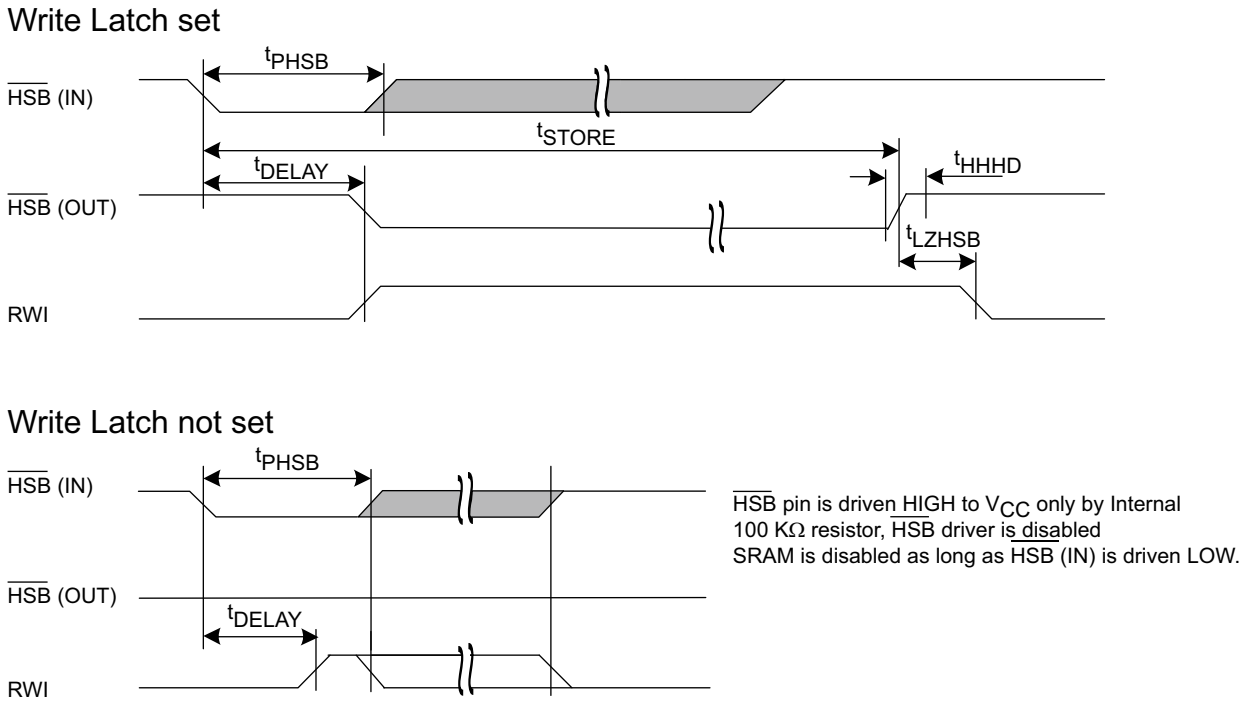
[+] Feedback

Hardware STORE Cycle

Parameter	Description	CY14C101Q3A/CY14B101Q3A/ CY14E101Q3A		Unit
		Min	Max	
t_{PHSB}	Hardware STORE pulse width	15	–	ns

Switching Waveforms

Figure 37. Hardware STORE Cycle[16]



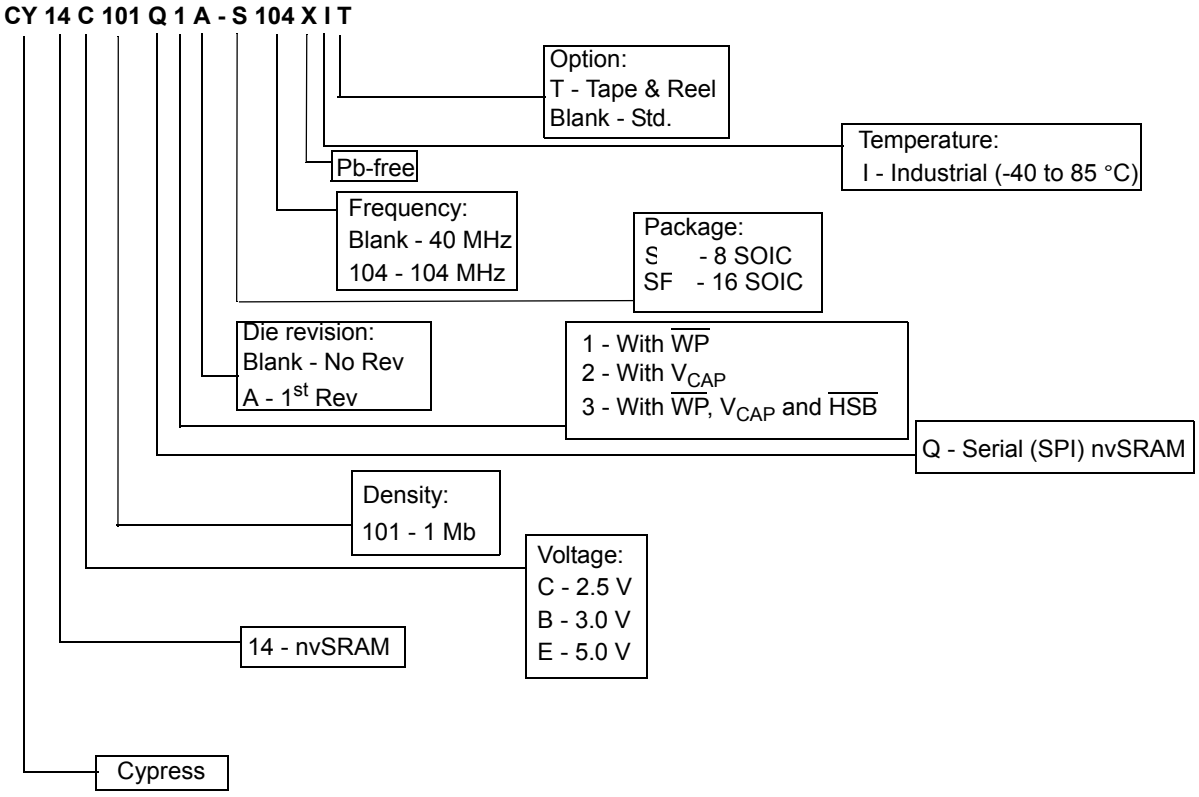
Note
16. If an SRAM write has not taken place since the last nonvolatile cycle, AutoStore or Hardware STORE is not initiated.

Ordering Information

Ordering Code	Package Diagram	Package Type	Operating Range
CY14C101Q1A-SXIT	51-85066	8-pin SOIC (with $\overline{WP}$), 40 MHz	Industrial
CY14C101Q1A-SXI	51-85066	8-pin SOIC (with $\overline{WP}$), 40 MHz	
CY14C101Q1A-S104XIT	51-85066	8-pin SOIC (with $\overline{WP}$), 104 MHz	
CY14C101Q1A-S104XI	51-85066	8-pin SOIC (with $\overline{WP}$), 104 MHz	
CY14B101Q1A-SXIT	51-85066	8-pin SOIC (with $\overline{WP}$), 40 MHz	
CY14B101Q1A-SXI	51-85066	8-pin SOIC (with $\overline{WP}$), 40 MHz	
CY14B101Q1A-S104XIT	51-85066	8-pin SOIC (with $\overline{WP}$), 104 MHz	
CY14B101Q1A-S104XI	51-85066	8-pin SOIC (with $\overline{WP}$), 104 MHz	
CY14E101Q1A-SXIT	51-85066	8-pin SOIC (with $\overline{WP}$), 40 MHz	
CY14E101Q1A-SXI	51-85066	8-pin SOIC (with $\overline{WP}$), 40 MHz	
CY14E101Q1A-S104XIT	51-85066	8-pin SOIC (with $\overline{WP}$), 104 MHz	
CY14E101Q1A-S104XI	51-85066	8-pin SOIC (with $\overline{WP}$), 104 MHz	
CY14C101Q2A-SXIT	51-85066	8-pin SOIC (with V_{CAP}), 40 MHz	
CY14C101Q2A-SXI	51-85066	8-pin SOIC (with V_{CAP}), 40 MHz	
CY14C101Q2A-S104XIT	51-85066	8-pin SOIC (with V_{CAP}), 104 MHz	
CY14C101Q2A-S104XI	51-85066	8-pin SOIC (with V_{CAP}), 104 MHz	
CY14B101Q2A-SXIT	51-85066	8-pin SOIC (with V_{CAP}), 40 MHz	
CY14B101Q2A-SXI	51-85066	8-pin SOIC (with V_{CAP}), 40 MHz	
CY14B101Q2A-S104XIT	51-85066	8-pin SOIC (with V_{CAP}), 104 MHz	
CY14B101Q2A-S104XI	51-85066	8-pin SOIC (with V_{CAP}), 104 MHz	
CY14E101Q2A-SXIT	51-85066	8-pin SOIC (with V_{CAP}), 40 MHz	
CY14E101Q2A-SXI	51-85066	8-pin SOIC (with V_{CAP}), 40 MHz	
CY14E101Q2A-S104XIT	51-85066	8-pin SOIC (with V_{CAP}), 104 MHz	
CY14E101Q2A-S104XI	51-85066	8-pin SOIC (with V_{CAP}), 104 MHz	
CY14C101Q3A-SFXIT	51-85022	16-pin SOIC (with $\overline{WP}$, V_{CAP} and $\overline{HSB}$), 40MHz	
CY14C101Q3A-SFXI	51-85022	16-pin SOIC (with $\overline{WP}$, V_{CAP} and $\overline{HSB}$), 40 MHz	
CY14C101Q3A-SF104XIT	51-85022	16-pin SOIC (with $\overline{WP}$, V_{CAP} and $\overline{HSB}$), 104 MHz	
CY14C101Q3A-SF104XI	51-85022	16-pin SOIC (with $\overline{WP}$, V_{CAP} and $\overline{HSB}$), 104 MHz	
CY14B101Q3A-SFXIT	51-85022	16-pin SOIC (with $\overline{WP}$, V_{CAP} and $\overline{HSB}$), 40 MHz	
CY14B101Q3A-SFXI	51-85022	16-pin SOIC (with $\overline{WP}$, V_{CAP} and $\overline{HSB}$), 40 MHz	
CY14B101Q3A-SF104XIT	51-85022	16-pin SOIC (with $\overline{WP}$, V_{CAP} and $\overline{HSB}$), 104 MHz	
CY14B101Q3A-SF104XI	51-85022	16-pin SOIC (with $\overline{WP}$, V_{CAP} and $\overline{HSB}$), 104 MHz	
CY14E101Q3A-SFXIT	51-85022	16-pin SOIC (with $\overline{WP}$, V_{CAP} and $\overline{HSB}$), 40 MHz	
CY14E101Q3A-SFXI	51-85022	16-pin SOIC (with $\overline{WP}$, V_{CAP} and $\overline{HSB}$), 40 MHz	
CY14E101Q3A-SF104XIT	51-85022	16-pin SOIC (with $\overline{WP}$, V_{CAP} and $\overline{HSB}$), 104 MHz	
CY14E101Q3A-SF104XI	51-85022	16-pin SOIC (with $\overline{WP}$, V_{CAP} and $\overline{HSB}$), 104 MHz	

All these parts are Pb-free. This table contains preliminary information. Contact your local Cypress sales representative for availability of these parts.

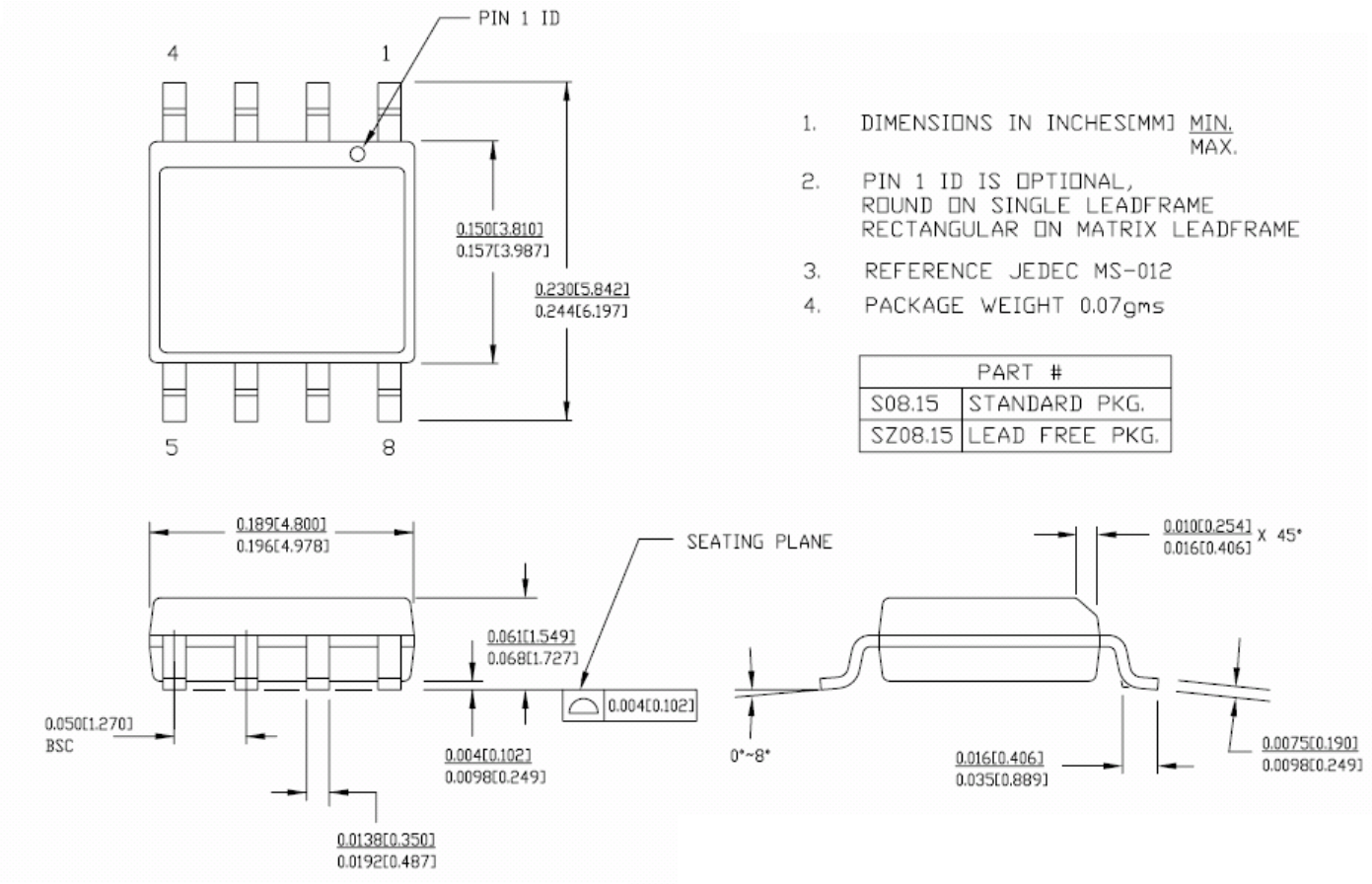
Ordering Code Definitions



[+] Feedback

Package Diagrams

Figure 38. 8-pin (150 mil) SOIC, 51-85066

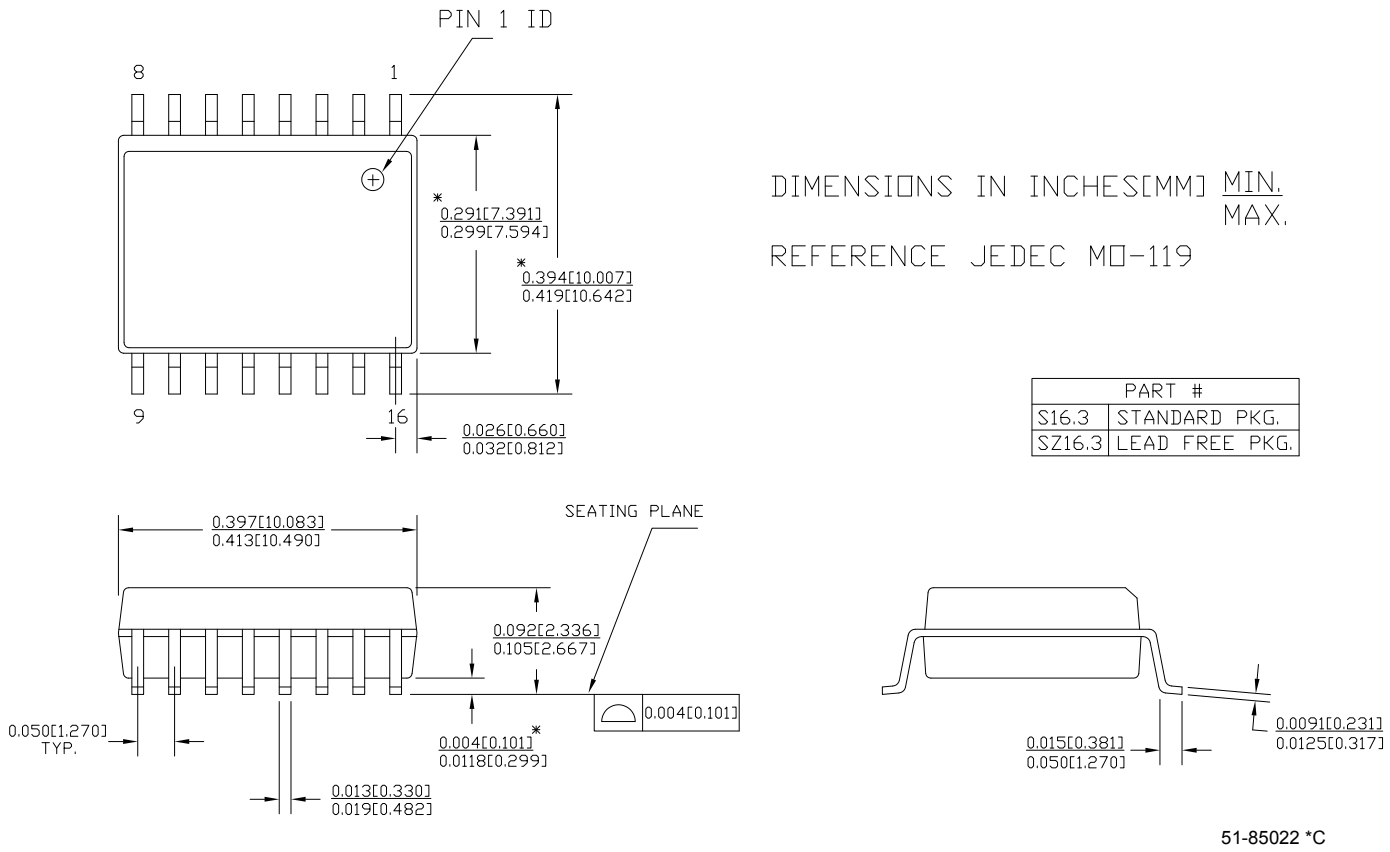


51-85066 *D

[+] Feedback

Package Diagrams (continued)

Figure 39. 16-pin (300 mil) SOIC, 51-85022



[+] Feedback

Acronyms

Acronym	Description
nvSRAM	Nonvolatile static random access memory
SPI	Serial peripheral interface
RoHS	Restriction of hazardous substances
I/O	Input/output
CMOS	Complementary metal oxide semiconductor
SOIC	Small outline integrated circuit
SONOS	Silicon-oxide-nitride-oxide-silicon
CPHA	Clock phase
CPOL	Clock polarity
EEPROM	Electrically erasable programmable read-only memory
JEDEC	Joint Electron Devices Engineering Council
CRC	Cyclic redundancy check
EIA	Electronic Industries Alliance
RWI	Read and write inhibited

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
Hz	Hertz
kbit	1024 bits
kHz	kilo Hertz
kΩ	kilo ohms
µA	micro Amperes
mA	milli Amperes
µF	micro Farad
MHz	Mega Hertz
µs	micro seconds
ms	milli seconds
ns	nano seconds
pF	pico Farad
V	Volts
Ω	ohms
W	Watts

Document History Page

Document Title: CY14C101Q, CY14B101Q, CY14E101Q 1-Mbit (128 K × 8) Serial (SPI) nvSRAM Document Number: 001-54393				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2754627	GVCH	08/21/09	New data sheet
*A	2864129	GVCH	01/22/2010	Changed Vcc range for CY14C101Q from 2.3 - 2.7 V to 2.4-2.6 V Removed 16-SOIC 150 mil package Added V_{OH}, V_{OL}, V_{IH}, V_{IL} and V_{CAP} specs for Vcc (Typ) = 2.5 V Updated V_{IH} min value from 1.4 V to 2.0 V for Vcc (Typ) = 3 V & 5 V
*B	2963131	06/28/2010	GVCH	Updated logic block diagram Updated Pinouts Updated Pin Definitions Complete content write Table 3: Added FAST_RDSR, FAST_RDSN and FAST_RDID opcodes Changed I_{CC4} value from 2 mA to 3 mA Added C_i parameter in DC Electrical Characteristics Changed V_{CAP} value from for V_{CC}=2.4 V-2.6 V in DC Electrical Characteristics Changed min value from 100 uF to 170 uF Changed typ value from 150 uF to 220 uF Changed max value from 330 uF to 270 uF Changed V_{CAP} value from for V_{CC}=2.7 V-3.6 V and V_{CC}=4.5-5.5 V in DC Electrical Characteristics Changed min value from 40 uF to 42 uF Added Data Retention and Endurance Table Added Capacitance Table Added Thermal Resistance Table Added AC Test Conditions Table Changed t_{CSS} parameter min value from 3 ns to 5 ns for 104 MHz Changed t_{CSH} parameter min value from 3 ns to 5 ns for 104 MHz Changed t_{SD} parameter min value from 3 ns to 4 ns for 104 MHz Changed t_{HD} parameter min value from 2 ns to 3 ns for 104 MHz Added Figures Added t_{FA} for V_{CC}=2.4 V-2.6 V Added t_{WAKE} for V_{CC}=2.4 V-2.6 V Added t_{SB} parameter Changed V_{SWITCH} from 4.45 V to 4.40 V for V_{CC} = 4.5 V to 5.5 V Added Software Controlled STORE and RECALL Cycles Table Updated t_{RECALL} value from 200 us to 300 us Changed t_{SS} value from 100 to 200 µs Added Hardware STORE Cycle Table Updated Ordering Information Updated package diagram
*C	3084950	11/12/2010	GVCH	Updated t_{SS} value from 200 us to 500 us Updated t_{RECALL} value from 300 us to 600 us Added Units of Measure table
*D	3148547	01/20/2011	GVCH	Hardware STORE and HSB pin Operation: Added more clarity on HSB pin operation Updated t_{LZHSB} parameter description Fixed typo in Figure 32.
*E	3202556	03/22/2011	GVCH	Updated AutoStore Operation (description). Updated Table 4 (definition of Bit 4-5). Updated DC Electrical Characteristics (Added I_{CC1} parameter for 104 MHz frequency). Updated in new template.

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