

- 65,536 X 8 Organization
- Single 5-V Supply (10% Tolerance)
- 30-Pin Single-in-Line Package (SIP)
- Utilizes Two 64K X 4 Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period . . . 4 ms (256 Cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance Ranges:

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)
TM4464LU8-12	120 ns	60 ns	230 ns
TM4464LU8-15	150 ns	75 ns	260 ns

- Low Power Dissipation:

	OPERATING (TYP)	STANDBY (TYP)
TM4464LU8-12	650 mW	25 mW
TM4464LU8-15	550 mW	25 mW

- Operating Free-Air Temperature . . . 0°C to 70°C

description

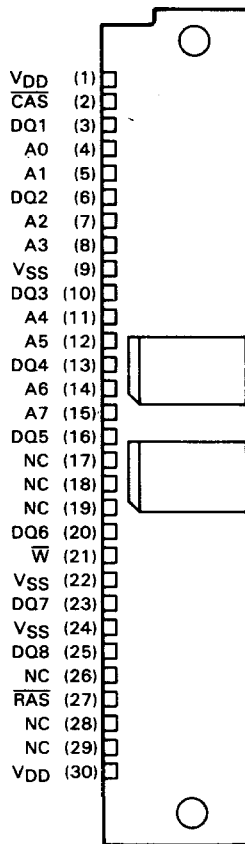
The TM4464LU8 is a 512K, dynamic random-access memory module organized as 65,536 × 8 bits in a 30-pin single-in-line package comprising two TMS4464FML, 65,536 × 4 bit dynamic RAM's in 22-lead plastic chip carriers mounted on top of a substrate together with two 0.2 μF decoupling capacitors mounted beneath the chip carriers. The onboard capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to reduced lead inductance.

operation

address (A0 through A7)

Fourteen address bits are required to decode 1 of 65,536 storage locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe (\overline{RAS}). Then the six column-address bits are set up on pins A1 through A6 and latched onto the chip by the column-address strobe (\overline{CAS}). All addresses must be stable on or before the falling edges of \overline{RAS} and \overline{CAS} . \overline{RAS} is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. \overline{CAS} is used as a chip select activating the column decoder and the input and output buffers.

**U SINGLE-IN-LINE PACKAGE
(TOP VIEW)**



PIN NOMENCLATURE	
A0-A7	Address Inputs
\overline{CAS}	Column-Address Strobe
DQ1-DQ8	Data In/Data Out
NC	No Connection
\overline{RAS}	Row-Address Strobe
VDD	5-V Supply
VSS	Ground
\overline{W}	Write Enable

TM4464LU8

65,536 BY 8-BIT DYNAMIC RAM MODULE

write enable (\overline{W})

The read or write mode is selected through the write-enable (\overline{W}) input. A logic high on the \overline{W} input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data inputs are disabled when the read mode is selected. The common I/O feature of the TM4464LU8 dictates the use of early write cycles to prevent contention on DQ. When \overline{W} goes low prior to \overline{CAS} , the data outputs will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (DQ1-DQ8)

Data is written during a write cycle. The falling edge of \overline{CAS} strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In the early write cycle, \overline{W} is brought low prior to \overline{CAS} and the data is strobed in by \overline{CAS} with setup and hold times referenced to this signal.

data out (DQ1-DQ8)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads for each output. Data out is the same polarity as data in. In a read cycle the outputs go active after the access time interval $t_{a(C)}$ that begins with the negative transition of \overline{CAS} as long as $t_{a(R)}$ is satisfied. The outputs become valid after the access time has elapsed and remains valid while \overline{CAS} is low; \overline{CAS} going high returns it to a high-impedance state. In the early write cycle, the outputs are always in the high-impedance state, a necessity due to the grounded output enable.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffers are in the high-impedance state unless \overline{CAS} is applied, the \overline{RAS} -only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with \overline{RAS} causes all bits in each row to be refreshed. \overline{CAS} can remain high (inactive) for this refresh sequence to conserve power.

page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 64 column locations on a single module, the row address and \overline{RAS} are applied to multiple modules. \overline{CAS} is then decoded to select the proper module.

power up

After power up, the power supply must remain at its steady-state value for 1 ms. In addition, the \overline{RAS} input must remain high for 100 μ s immediately prior to initialization. Initialization consists of performing eight \overline{RAS} cycles before proper device operation is achieved.

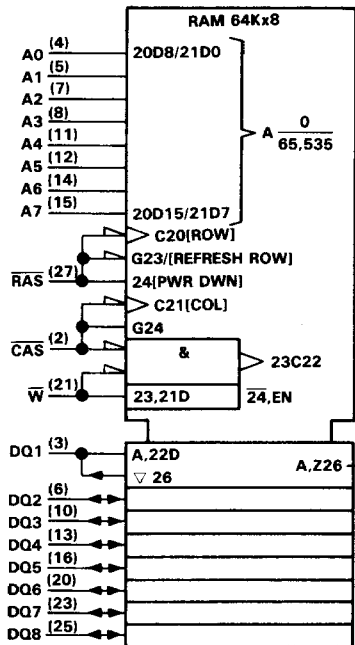
single-in-line package and components

PC substrate: 0,79 mm (0.031 inch) minimum thickness

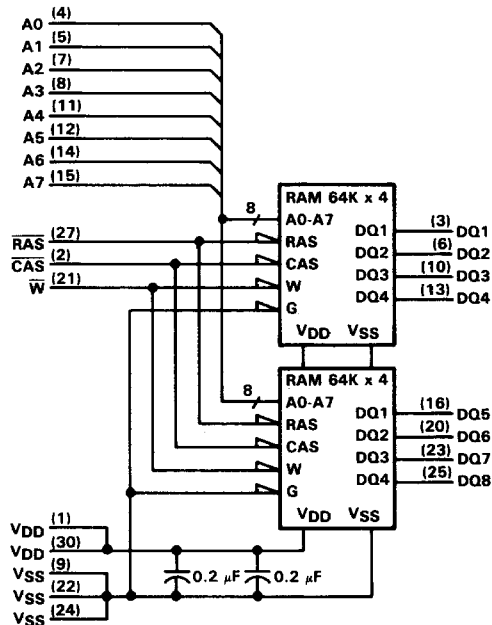
Bypass capacitors: Multilayer ceramic

Contact area for socketable devices: Nickel plate and solder plate on top of copper

logic symbol†



functional block diagram



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range for any pin except V _{DD} and data out (see Note 1)	-1.5 V to 10 V
Voltage range for V _{DD} supply and data out with respect to V _{SS}	-1 V to 6 V
Short circuit output current	50 mA
Power dissipation	2 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values in this data sheet are with respect to V_{SS}.
2. Additional information concerning the handling of ESD sensitive devices is available in a document entitled "Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies" in Section 12.

TM4464LU8

65,536 BY 8-BIT DYNAMIC RAM MODULE

recommended operating conditions

		MIN	NOM	MAX	UNIT	
V _{DD}	Supply voltage	4.5	5	5.5	V	
V _{SS}	Supply voltage		0		V	
V _{IH}	High-level input voltage	V _{DD} = 4.5 V		2.4	4.8	V
		V _{DD} = 5.5 V		2.4	5.8	
V _{IL}	Low-level input voltage (see Note 3)	-1	0	0.8	V	
T _A	Operating free-air temperature		0	70	°C	

NOTE 3: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TM4464LU8-12			TM4464LU8-15			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{OH}	High-level output voltage	I _{OH} = -2 mA			2.4			V
V _{OL}	Low-level output voltage	I _{OL} = 4.2 mA					0.4	V
I _I	Input current (leakage)	V _I = 0 V to 5.8 V, V _{DD} = 5 V, All other pins = 0 V					± 10	µA
I _O	Output current (leakage)	V _O = 0.4 V to 5.5 V, V _{DD} = 5 V, $\overline{\text{CAS}}$ high					± 10	µA
I _{DD1}	Average operating current during read or write cycle		130	160		110	140	mA
I _{DD2}	Standby current	After 1 memory cycle, $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ high, All outputs open				5	10	mA
I _{DD3}	Average refresh current	t _c = minimum cycle, $\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ high, All outputs open				100	120	mA
I _{DD4}	Average page-mode current	t _c (P) = minimum cycle, $\overline{\text{RAS}}$ low, $\overline{\text{CAS}}$ cycling, All outputs open				90	110	mA

†All typical values are at T_A = 25°C and nominal supply voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		MIN	MAX	UNIT
C _{i(A)}	Input capacitance, address inputs		14	pF
C _{i(RC)}	Input capacitance, strobe inputs		20	pF
C _{i(W)}	Input capacitance, write-enable input		20	pF
C _{i/o}	Input/output capacitance, data ports		10	pF
C _{0(VDD)}	Decoupling capacitance	0.4		µF

5

Dynamic RAM Modules

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER	TEST CONDITIONS	ALT. SYMBOL	TM4464LU8-12		TM4464LU8-15		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(C)}$ Access time from \overline{CAS}	$C_L = 100 \text{ pF}$, Load = 2 Series 74 TTL gates	t_{CAC}	70		80		ns
$t_{a(R)}$ Access time from \overline{RAS}	$t_{RLCL} = \text{MAX}$, $C_L = 100 \text{ pF}$, Load = 2 Series 74 TTL gates	t_{RAC}	120		150		ns

timing requirements over recommended supply voltage range and operating free-air temperature range

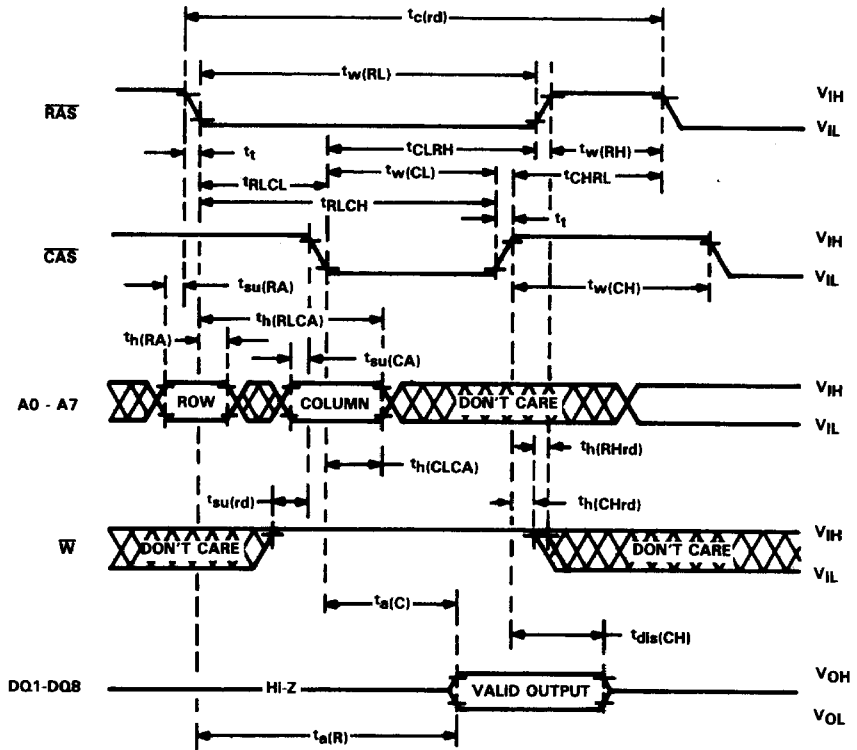
	ALT. SYMBOL	TM4464LU8-12		TM4464LU8-15		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(P)}$ Page-mode cycle time	t_{PC}	120		140		ns
$t_{c(rd)}$ Read cycle time [†]	t_{RC}	230		260		ns
$t_{c(W)}$ Write cycle time	t_{WC}	230		260		ns
$t_{c(rdW)}$ Read-write/read-modify-write cycle time	t_{RWC}	315		365		ns
$t_{w(CH)}$ Pulse duration, \overline{CAS} high (precharge time) [‡]	t_{CP}	40		50		ns
$t_{w(CL)}$ Pulse duration, \overline{CAS} low	t_{CAS}	70	10,000	80	10,000	ns
$t_{w(RH)}$ Pulse duration, \overline{RAS} high (precharge time)	t_{RP}	80		100		ns
$t_{w(RL)}$ Pulse duration, \overline{RAS} low	t_{RAS}	120	10,000	150	10,000	ns
$t_{w(W)}$ Write pulse duration	t_{WP}	30		40		ns
t_t Transition times (rise and fall) for \overline{RAS} and \overline{CAS}	t_T	3	50	3	50	ns
$t_{su(CA)}$ Column-address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$ Row-address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$ Data setup time	t_{DS}	5		5		ns
$t_{su(rd)}$ Read-command setup time	t_{RCS}	0		0		ns
$t_{su(WCH)}$ Write-command setup time before \overline{CAS} high	t_{CWL}	50		60		ns
$t_{su(WRH)}$ Write-command setup time before \overline{RAS} high	t_{RWL}	50		60		ns
$t_h(CLCA)$ Column-address hold time after \overline{CAS} low	t_{CAH}	35		40		ns
$t_h(RA)$ Row-address hold time	t_{RAH}	20		30		ns
$t_h(RLCA)$ Column-address hold time after \overline{RAS} low	t_{AR}	85		110		ns
$t_h(CLD)$ Data hold time after \overline{CAS} low	t_{DH}	40		60		ns
$t_h(RLD)$ Data hold time after \overline{RAS} low	t_{DHR}	90		130		ns
$t_h(RHrd)$ Read-command hold time after \overline{RAS} high	t_{RRH}	10		10		ns
$t_h(CHrd)$ Read-command hold time after \overline{CAS} high	t_{RCH}	0		0		ns
$t_h(CLW)$ Write-command hold time after \overline{CAS} low	t_{WCH}	40		60		ns
$t_h(RLW)$ Write-command hold time after \overline{RAS} low	t_{WCR}	90		130		ns
t_{RLCH} Delay time, \overline{RAS} low to \overline{CAS} high	t_{CSH}	120		150		ns
t_{CHRL} Delay time, \overline{CAS} high to \overline{RAS} low	t_{CRP}	0		0		ns
$t_{CLR H}$ Delay time, \overline{CAS} low to \overline{RAS} high	t_{RSH}	70		80		ns
t_{RLCL} Delay time, \overline{RAS} low to \overline{CAS} low (maximum value specified only to guarantee access time)	t_{RCD}	30	50	30	70	ns
t_{WLCL} Delay time, \overline{W} low to \overline{CAS} low (early write cycle)	t_{WCS}	-5		-5		ns
t_{rf} Refresh time interval	t_{REF}		4		4	ms

[†]All cycle times assume $t_t = 5 \text{ ns}$.

[‡]Page mode only.

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65,536 BY 8-BIT DYNAMIC RAM MODULE

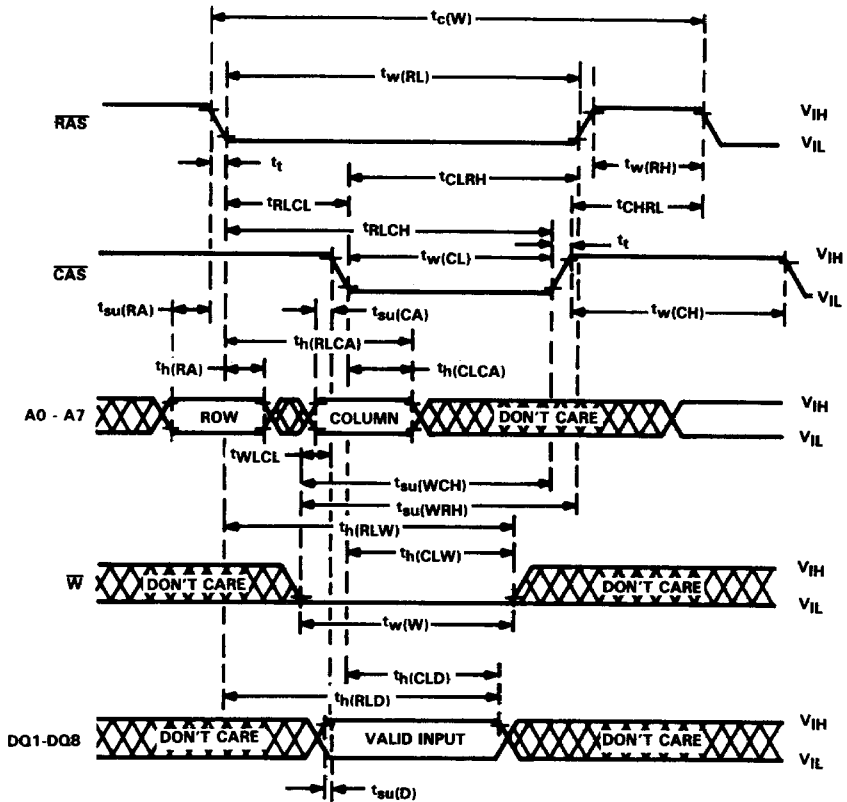
read cycle timing



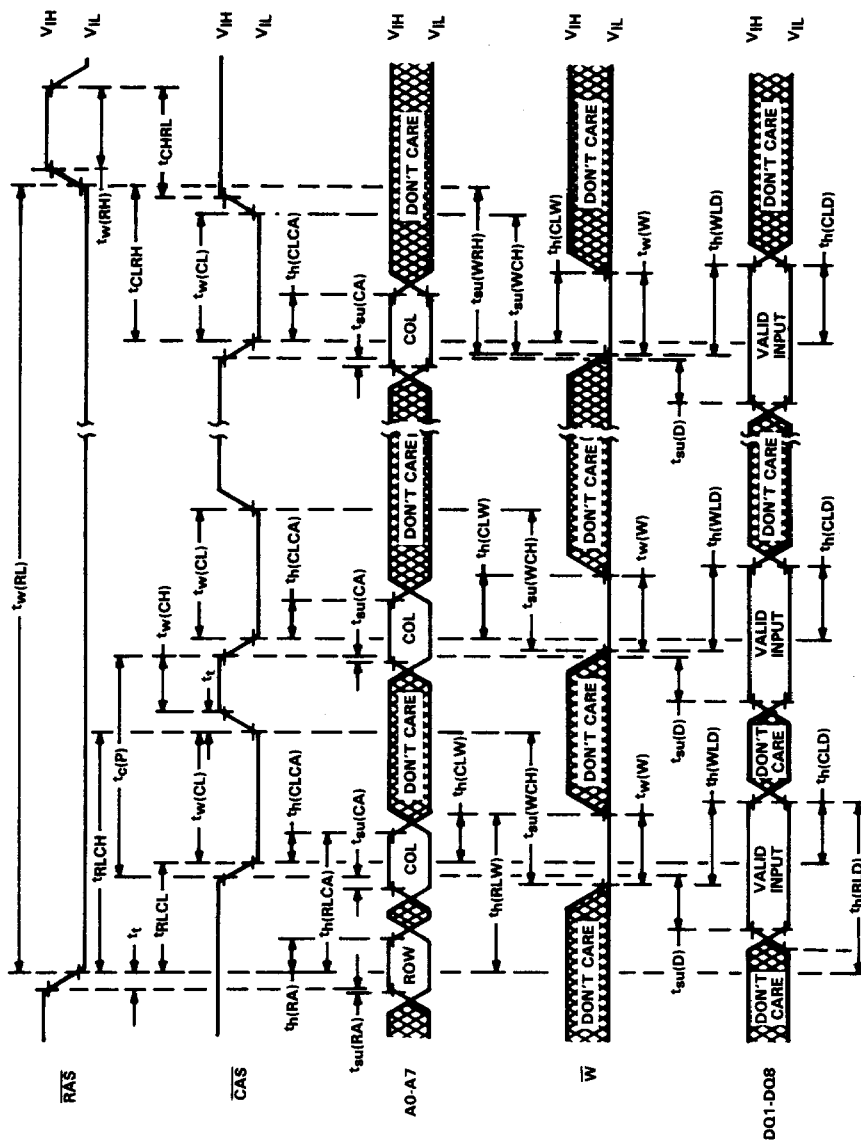
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Dynamic RAM Modules

early write cycle timing



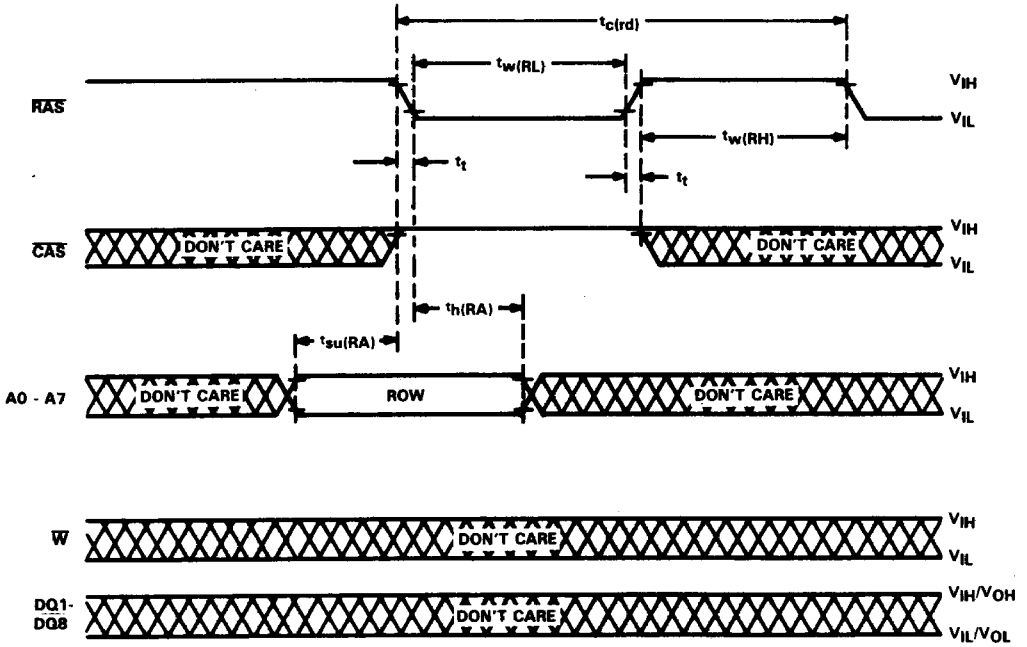
page-mode write cycle timing



NOTE 5: A read or a read-modify-write cycle can be intermixed with write cycles as long as read and read-modify-write timing specifications are not violated.

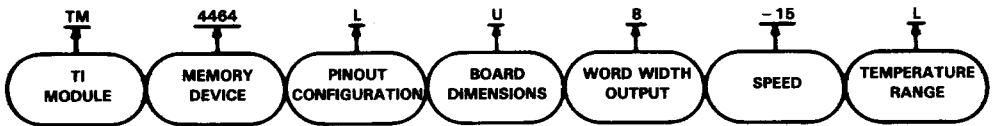
TM4464LU8
65,536 BY 8-BIT DYNAMIC RAM MODULE

RAS-only refresh timing



5 Dynamic RAM Modules

T1 single-in-line package nomenclature



(88.9 x 16.5 mm)
 (3.5 x 0.65 inches)

Max Access
 - 12 120 ns
 - 15 150 ns

L 0°C to 70°C