Z89C00

16-BIT DIGITAL SIGNAL PROCESSOR CORE

FEATURES

- 16-Bit Single Cycle Instructions
- Zero Overhead Hardware Looping
- 16-Bit Data
- Ready Control for Slow Peripherals
- Single Cycle Multiply/Accumulate
- Six-Level Stack
- 512 Words of On-Chip RAM
- Static Single-Cycle Operation
- 16-Bit I/O Port
- On-Chip Masked ROM
- Vectored Interrupts
- 64K Words of External Program Address Space
- Two Conditional Branch Inputs/Two User Outputs
- 24-Bit ALU, Accumulator and Shifter
- Development Tools

GENERAL DESCRIPTION

The Z89C00 is a second generation, 16-bit, fractional, two's complement CMOS Digital Signal Processor (DSP). All instructions, including multiply and accumulate, are executed in a single clock cycle. The processor contains 1 Kbyte of on-chip data RAM (two blocks of 256 16-bit words), program ROM and 64K words of program memory addressing capability. Also, the processor features a 24-bit ALU, a 16 x 16 multiplier, a 24-bit Accumulator and a shifter. Additionally, the processor contains a six-level stack, three vectored interrupts and two inputs for conditional program jumps. Each RAM block contains a set of three pointers which may be incremented or decremented automatically to affect hardware looping without software overhead. The data RAMs can be simultaneously addressed and loaded to the multiplier for a true single cycle multiply.

There is a 16-bit address and a 16-bit data bus for external program memory and data, and a 16-bit I/O bus for transferring data. Additionally, there are two general purpose user inputs and two user outputs. Operation with slow peripherals is accomplished with a ready input pin. The clock may be stopped to conserve power.

Development tools include a relocatable assembler, a linker loader, and an ANSI-C compiler. The development tools include a simulator/debugger, and a hardware emulator is available.

GENERAL DESCRIPTION (Continued)

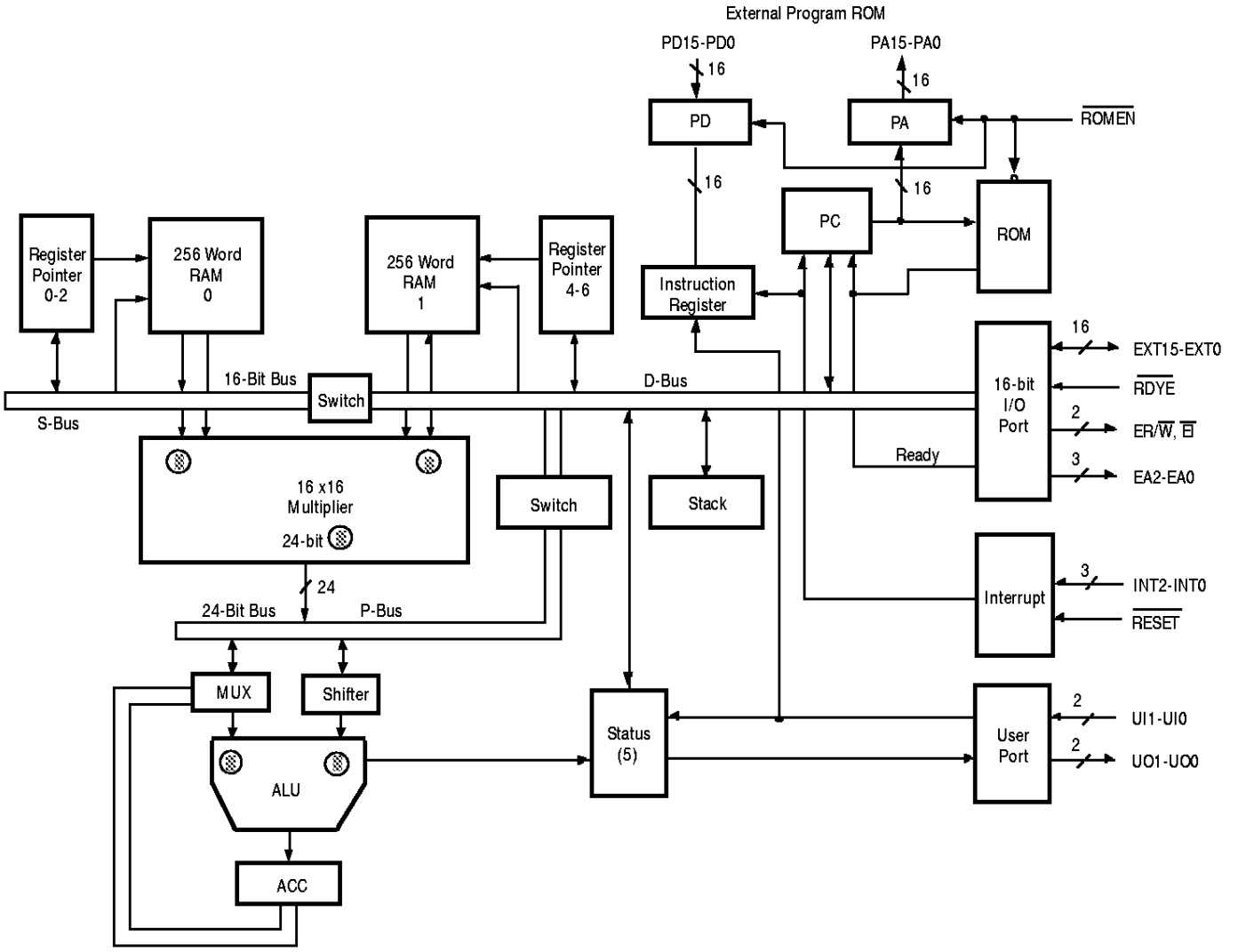

Figure 1. Z89C00 Core Functional Block Diagram

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