MOTOROLA

Quad Set-Reset Latch

ELECTRICALLY TESTED PER:
MIL-M-38510/31602

Military 54LS279

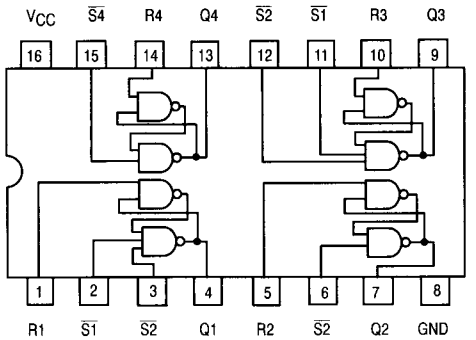
AVAILABLE AS:

1) JAN: JM38510/31602BXA
2) SMD: 7601801
3) 883: 54LS279/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

LOGIC DIAGRAM



TRUTH TABLE			
Inputs			Output
$\overline{S1}$	$\overline{S2}$	$\overline{R}$	(Q)
L	L	L	h
L	X	H	H
X	L	H	H
H	H	L	L
H	H	H	No Change

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
h = The output is HIGH as long as $\overline{S1}$ or $\overline{S2}$ is LOW. If all inputs go HIGH simultaneously, the output state is indeterminate; otherwise, it follows the Truth Table.

PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
R1	1	1	2	V_{CC}
$\overline{S1}$	2	2	3	GND
$\overline{S2}$	3	3	4	GND
Q1	4	4	5	V_{CC}
R2	5	5	7	V_{CC}
$\overline{S2}$	6	6	8	GND
Q2	7	7	9	V_{CC}
GND	8	8	10	GND
Q3	9	9	12	V_{CC}
R3	10	10	13	V_{CC}
$\overline{S1}$	11	11	14	GND
$\overline{S2}$	12	12	15	GND
Q4	13	13	17	V_{CC}
R4	14	14	18	V_{CC}
$\overline{S4}$	15	15	19	GND
V_{CC}	16	16	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

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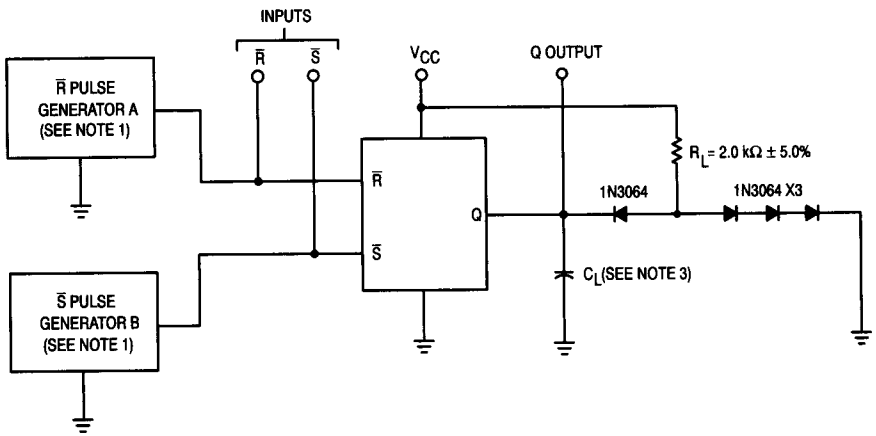
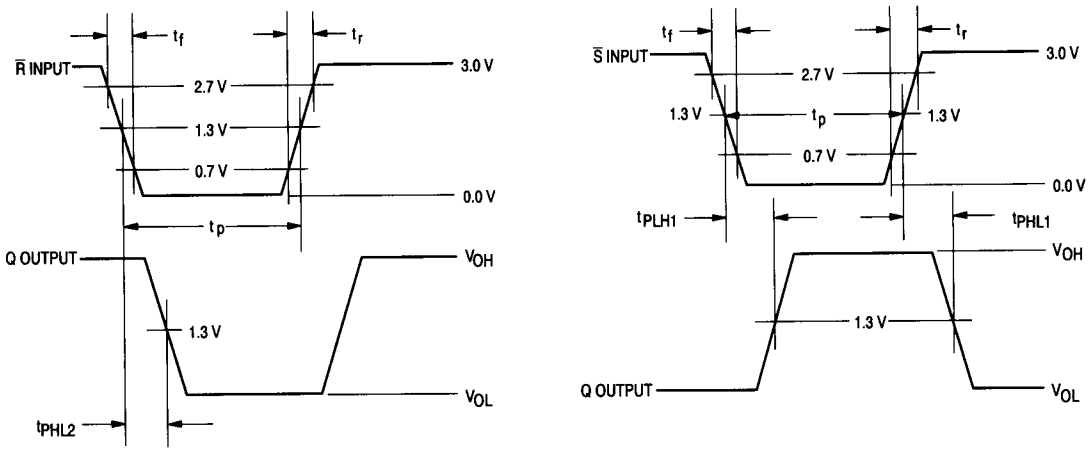
SWITCHING TEST CIRCUIT



WAVEFORMS



NOTES:

1. $\overline{R}$ and $\overline{S}$ pulse generators have the following characteristics: $t_f \leq 15$ ns, $t_r \leq 6.0$ ns, $t_p = 40$ ns ±10 ns, and PRR ≤ 1.0 MHz.
2. Inputs not under test are at 2.7 V.
3. $C_L = 50$ pF ± 10%, which includes scope probe and jig capacitance.
4. $R_L = 2.0$ kΩ ± 5.0%.
5. Voltage measurements are to be made with respect to network ground terminal.
6. All diodes are 1N3064 or equivalent.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		– 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = – 400 µA, V_{IH} = 2.0 V, other input = 2.0 V, or per truth table.
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 4.0 mA, V_{IH} = 2.0 V, other input = 2.0 V, or per truth table.
V_{IC}	Input Clamping Voltage		– 1.5					V	V_{CC} = 4.5 V, I_{IN} = – 18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open.
I_{IHH}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other inputs are open.
I_{IL}	Logical "0" Input Current	– 160	– 400	– 160	– 400	– 160	– 400	µA	V_{CC} = 5.5 V, V_{IN} = 0.4V, $\overline{S2}$ = GND, other inputs are open.
I_{OS}	Output Short Circuit Current	– 15	– 100	– 15	– 100	– 15	– 100	mA	V_{CC} = 5.5 V, V_{IN} = 5.0 V, other inputs = GND, V_{OUT} = GND.
I_{CC}	Power Supply Current		7.0		7.0		7.0	mA	V_{CC} = 5.5 V, V_{IN} ($\overline{S1}$, $\overline{S2}$) = 4.5 V, other inputs are GND.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.4 V, and V_{INH} = 2.5 V.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		– 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1} t_{PHL1}	Propagation Delay /Data-Output $\overline{S}$ to Output	3.0 —	20 21	3.0 —	26 26	3.0 —	26 26	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ.
t_{PLH1} t_{PLH1}	Propagation Delay /Data-Output $\overline{S}$ to Output	3.0 —	27 22	3.0 —	35 30	3.0 —	35 30	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ.
t_{PHL2} t_{PHL2}	Propagation Delay /Data-Output R to Output	3.0 —	32 27	3.0 —	42 37	3.0 —	42 37	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ.

NOTE:
1. The limits specified for C_L = 15 pF are guaranteed but not tested.