

74F382

4-Bit Arithmetic Logic Unit

General Description

The 'F382 performs three arithmetic and three logic operations on two 4-bit words, A and B. Two additional Select input codes force the Function outputs LOW or HIGH. An Overflow output is provided for convenience in twos complement arithmetic. A Carry output is provided for ripple expansion. For high-speed expansion using a Carry Look-ahead Generator, refer to the 'F381 data sheet.

Features

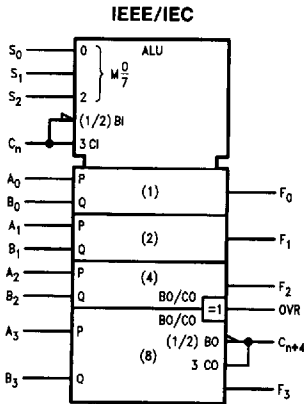
- Performs six arithmetic and logic functions
- Selectable LOW (clear) and HIGH (preset) functions
- LOW input loading minimizes drive requirements
- Carry output for ripple expansion
- Overflow output for twos complement arithmetic

Ordering Code: See Section 11

Commercial	Package Number	Package Description
74F382PC	N20A	20-Lead (0.300" Wide) Molded Dual-In-Line
74F382SC (Note 1)	M20B	20-Lead (0.300" Wide) Molded Small Outline, JEDEC
74F382SJ (Note 1)	M20D	20-Lead (0.300" Wide) Molded Small Outline, EIAJ

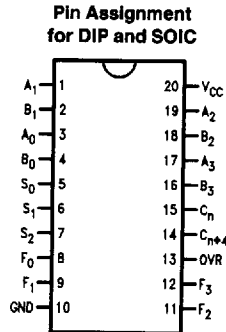
Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

Logic Symbols

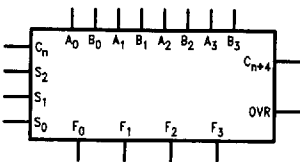


TL/F/9529-6

Connection Diagram



TL/F/9529-1



TL/F/9529-3

Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	74F	
		U.L. HIGH/LOW	Input I_H/I_L Output I_{OH}/I_{OL}
A_0-A_3	A Operand Inputs	1.0/4.0	20 μ A / -2.4 mA
B_0-B_3	B Operand Inputs	1.0/4.0	20 μ A / -2.4 mA
S_0-S_2	Function Select Inputs	1.0/1.0	20 μ A / -0.6 mA
C_n	Carry Input	1.0/5.0	20 μ A / -3.0 mA
C_{n+4}	Carry Output	50/33.3	-1 mA / 20 mA
OVR	Overflow Output	50/33.3	-1 mA / 20 mA
F_0-F_3	Function Outputs	50/33.3	-1 mA / 20 mA

Functional Description

Signals applied to the Select inputs S_0-S_2 determine the mode of operation, as indicated in the Function Select Table. An extensive listing of input and output levels is shown in the Truth Table. The circuit performs the arithmetic functions for either active HIGH or active LOW operands, with output levels in the same convention. In the Subtract operating modes, it is necessary to force a carry (HIGH for active HIGH operands, LOW for active LOW operands) into the C_n input of the least significant package. Ripple expansion is illustrated in Figure 1. The overflow output OVR is the Exclusive-OR of C_{n+3} and C_{n+4} ; a HIGH signal on OVR indicates overflow in twos complement operation. Typical delays for Figure 1 are given in Figure 2.

Function Select Table

Select			Operation
S_0	S_1	S_2	
L	L	L	Clear
H	L	L	B Minus A
L	H	L	A Minus B
H	H	L	A Plus B
L	L	H	$A \oplus B$
H	L	H	A + B
L	H	H	AB
H	H	H	Preset

H = HIGH Voltage Level
L = LOW Voltage Level

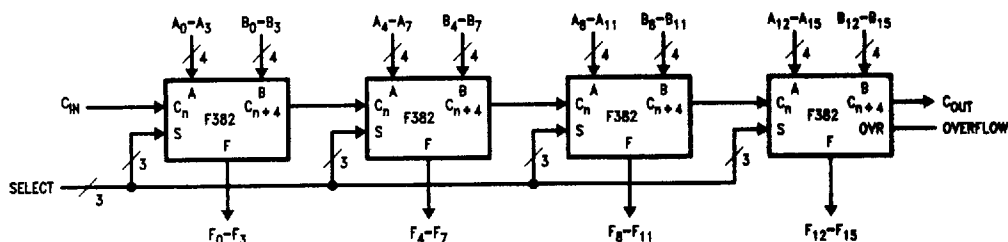


FIGURE 1. 16-Bit Ripply Carry ALU Expansion

TL/F/0629-5

Path Segment	Toward F	Output C_{n+4} , OVR
A_i or B_i to C_{n+4}	6.5 ns	6.5 ns
C_n to C_{n+4}	6.3 ns	6.3 ns
C_n to C_{n+4}	6.3 ns	6.3 ns
C_n to F	8.1 ns	—
C_n to C_{n+4} , OVR	—	8.0 ns
Total Delay	27.2 ns	27.1 ns

FIGURE 2. 16-Bit Delay Tabulation

Truth Table

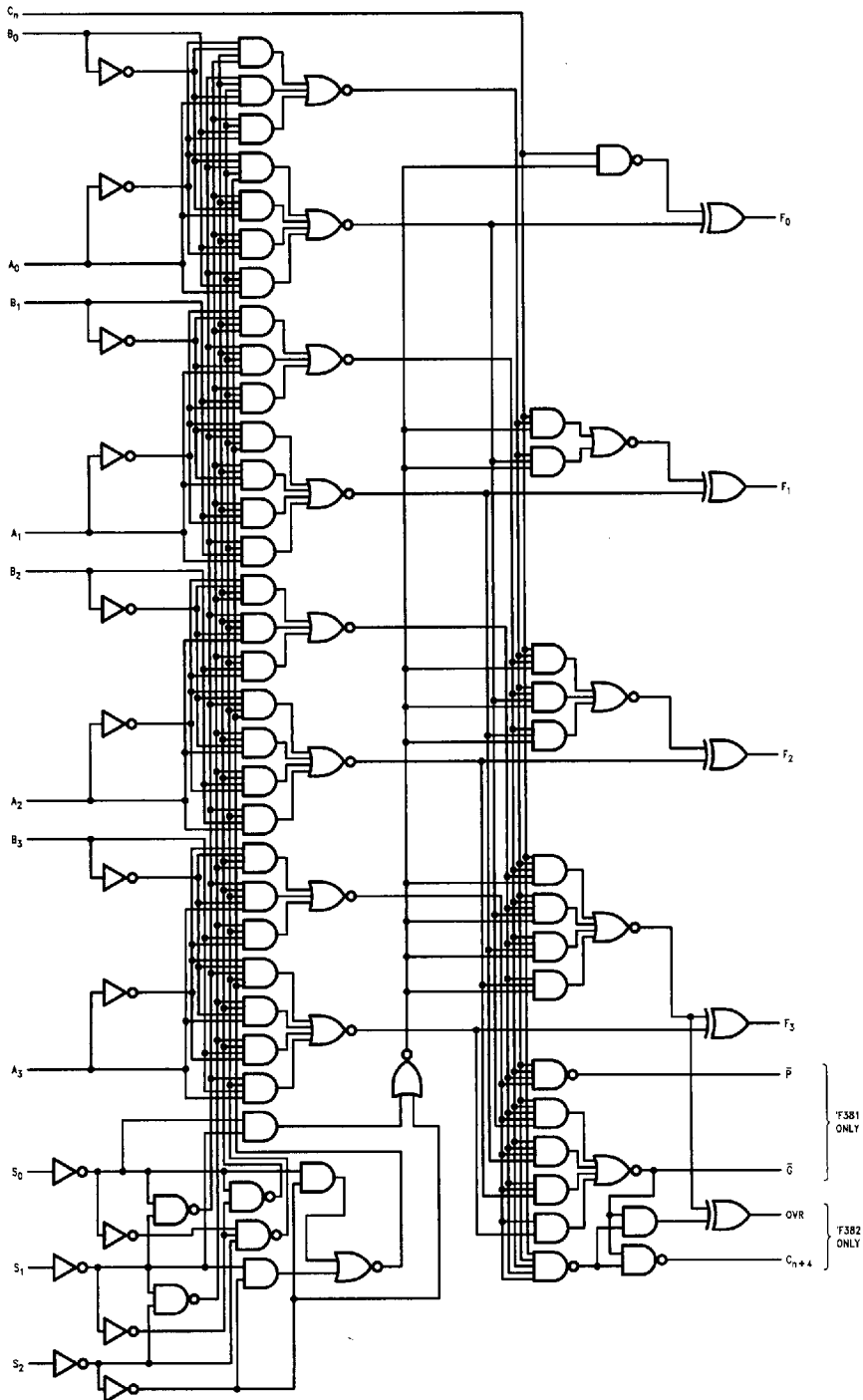
Function	Inputs						Outputs								
	S ₀	S ₁	S ₂	C _n	A _n	B _n	F ₀	F ₁	F ₂	F ₃	OVR	C _{n+4}			
CLEAR	L	L	L	L	X	X	L	L	L	L	H	H			
				H	X	X	L	L	L	L	H	H			
B MINUS A	H	L	L	L	L	L	H	H	H	H	L	L			
				L	L	H	L	H	H	L	L	L	H		
				L	H	L	L	L	L	L	L	L	L	L	
				L	H	H	L	H	H	L	L	L	L	L	
				H	L	L	L	L	L	L	L	L	L	L	
				H	L	H	L	H	H	L	L	L	L	L	H
				H	H	L	L	L	L	L	L	L	L	L	L
				H	H	H	L	H	H	L	L	L	L	L	L
A MINUS B	L	H	L	L	L	L	H	H	H	H	L	L			
				L	L	H	L	L	L	L	L	L	L		
				L	H	L	L	H	H	L	L	L	L	L	
				L	H	H	L	H	H	L	L	L	L	L	
				H	L	L	L	L	L	L	L	L	L	L	
				H	L	H	L	H	H	L	L	L	L	L	L
				H	H	L	L	L	L	L	L	L	L	L	L
				H	H	H	L	H	H	L	L	L	L	L	L
A PLUS B	H	H	L	L	L	L	L	L	L	L	L	L			
				L	L	H	H	H	H	L	L	L	L		
				L	H	L	H	H	H	L	L	L	L	L	
				L	H	H	L	H	H	L	L	L	L	L	
				H	L	L	L	L	L	L	L	L	L	L	
				H	L	H	L	L	L	L	L	L	L	L	L
				H	H	L	L	L	L	L	L	L	L	L	L
				H	H	H	L	H	H	L	L	L	L	L	L
A ⊕ B	L	L	H	X	L	L	L	L	L	L	L	L			
				X	L	H	H	H	H	L	L	L			
				L	H	L	H	H	H	L	L	L			
				X	H	H	L	L	L	L	L	L			
				H	H	L	L	L	L	L	L	L			
A + B	H	L	H	X	L	L	L	L	L	L	L	L			
				X	L	H	H	H	H	L	L	L			
				X	H	L	H	H	H	L	L	L			
				L	H	H	H	H	H	L	L	L			
				H	H	H	H	H	H	L	L	L			
AB	L	H	H	X	L	L	L	L	L	L	L	H			
				X	L	H	L	L	L	L	L	L	L		
				X	H	L	L	L	L	L	L	L	L		
				L	H	H	L	L	L	L	L	L	L	L	
				H	H	H	L	L	L	L	L	L	L	L	
PRESET	H	H	H	X	L	L	H	H	H	H	L	L			
				X	L	H	H	H	H	L	L	L			
				X	H	L	H	H	H	L	L	L			
				L	H	H	H	H	H	L	L	L			
				H	H	H	H	H	H	L	L	L			

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Logic Diagram



TL/F/9529-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
TRI-STATE® Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Commercial	
Supply Voltage	+4.5V to +5.5V
Commercial	

DC Electrical Characteristics over Operating Temperature Range unless otherwise specified

Symbol	Parameter	74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	74F 10% V _{CC} 74F 5% V _{CC}	2.5 2.7		V	Min	I _{OH} = -1 mA I _{OH} = -1 mA
V _{OL}	Output LOW Voltage	74F 10% V _{CC}		0.5	V	Min	I _{OL} = 20 mA
I _{IH}	Input HIGH Current	74F		5.0	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test	74F		7.0	μA	Max	V _{IN} = 7.0V
I _{CEX}	Output HIGH Leakage Current	74F		50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	74F	4.75		V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current	74F		3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			-0.6 -2.4 -3.0	mA	Max	V _{IN} = 0.5V (S ₀ -S ₂) V _{IN} = 0.5V (A ₀ -A ₃ , B ₀ -B ₃) V _{IN} = 0.5V (C _n)
I _{OS}	Output Short-Circuit Current		-60	-150	mA	Max	V _{OUT} = 0V
I _{CC}	Power Supply Current		54	81	mA	Max	

AC Electrical Characteristics: See Section 2 for U.L. definitions

Symbol	Parameter	74F			74F		Units	Fig. No.
		T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A , V _{CC} = Com C _L = 50 pF			
		Min	Typ	Max	Min	Max		
t _{PLH} t _{PHL}	Propagation Delay C _n to F _i	3.0 2.5	8.1 5.7	12.0 8.0	3.0 2.5	13.0 9.0	ns	2-4
t _{PLH} t _{PHL}	Propagation Delay Any A or B to Any F	4.0 3.0	10.4 8.2	15.0 11.0	3.5 2.5	17.0 12.0	ns	2-4
t _{PLH} t _{PHL}	Propagation Delay S _i to F _i	6.5 4.0	11.0 8.2	20.5 15.0	5.5 4.0	21.5 17.5	ns	2-4
t _{PLH} t _{PHL}	Propagation Delay A _i or B _j to C _n + 4	3.5 3.5	6.0 6.5	8.5 9.0	3.5 3.5	11.0 10.5	ns	2-4
t _{PLH} t _{PHL}	Propagation Delay S _i to OVR or C _n + 4	7.0 5.0	12.5 9.0	16.5 12.0	7.0 5.0	17.5 14.5	ns	2-4
t _{PLH} t _{PHL}	Propagation Delay C _n to C _n + 4	2.5 3.5	5.6 6.3	8.0 9.0	2.0 2.0	9.0 10.0	ns	2-4
t _{PLH} t _{PHL}	Propagation Delay C _n to OVR	3.5 2.5	8.0 7.1	11.0 10.0	3.5 2.5	13.0 11.0	ns	2-4
t _{PLH} t _{PHL}	Propagation Delay A _i or B _j to OVR	7.0 3.0	11.5 8.0	15.5 10.5	7.0 3.0	16.5 11.5	ns	2-4