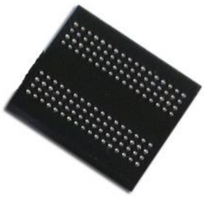
DDR3 SDRAM MEMORY

3D3D8G32WB1741
3D3D8G32YB1741
Datasheet

8Gb DDR3 SDRAM organized as 256Mx32

FEATURES

- JEDEC Standard ball-out
- Combines two 4 Gb x 16 devices
- VDD/VDDQ = 1.35V (1.283V to 1.45V) or 1.5V (1.425V to 1.575V)
- Differential clock inputs (CK, /CK) operation
- Posted CAS by programmable additive latency
- Burst length: 8 (BL8) and Burst Chop 4 (BC) modes
- Bi-directional Differential Data Strobe (DQS)
- DLL aligns DQ and DQS transitions with CK
- Commands entered on each positive CK transition.
- Data and data mask are referenced to both edges of a differential data strobe pair (Double data rate)
- Programmable read burst : interleave or nibble sequential
- Multi Purpose Register (MPR) for pre-defined pattern read out
- Programmable on-die termination (ODT)
- Refresh: Self-refresh, Auto Self-refresh and Partial array Self-refresh
- High Temperature Self-Refresh rate enable
- ZQ calibration for DQ drive and ODT
- Asynchronous RESET pin for Power-up initialization and reset function
- Clock rate available : 1333 and 1600 Mbps
- Industrial and Military temperature range.



Applications:

- Embedded Systems
- Workstations
- Server
- Super computers
- Test Systems

GENERAL DESCRIPTION

The 3D3D8G32WB1741 / 3D3D8G32YB1741 is a high speed stack multi-chip package integrated 4Gbits x 2 DDR3 SDRAM and fabricated with ultra high performance CMOS process containing 8G bits which is organized as 32Mbits x 8 banks by 32 bits.

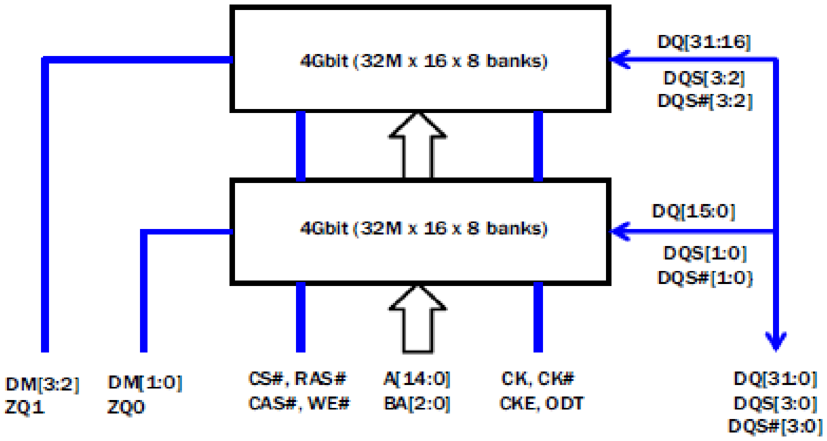
This synchronous device achieves a high speed double-data-rate transfer rates of up to 1600 Mb/sec/pin (DDR3-1600) for general applications. The chip is designed to comply with the following key DDR3 SDRAM features: (1) posted CAS by programmable additive latency, (2) On Die Termination (3) programmable driver strength data,(4) clock rate of 1600Mbps.

All the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising and /CK falling). All I/Os are synchronized with a pair of bidirectional differential data strobes (DQS and /DQS) in a source synchronous fashion. The address bus is used to convey row, column and bank address information in a /RAS and /CAS multiplexing style.

The 8Gb DDR3 devices operates with a single power supply: 1.35V or 1.5V for VDD and VDDQ.

This device is ideal for high density memory applications that require high speed transfer and compatibility with standard servers and networking equipment.

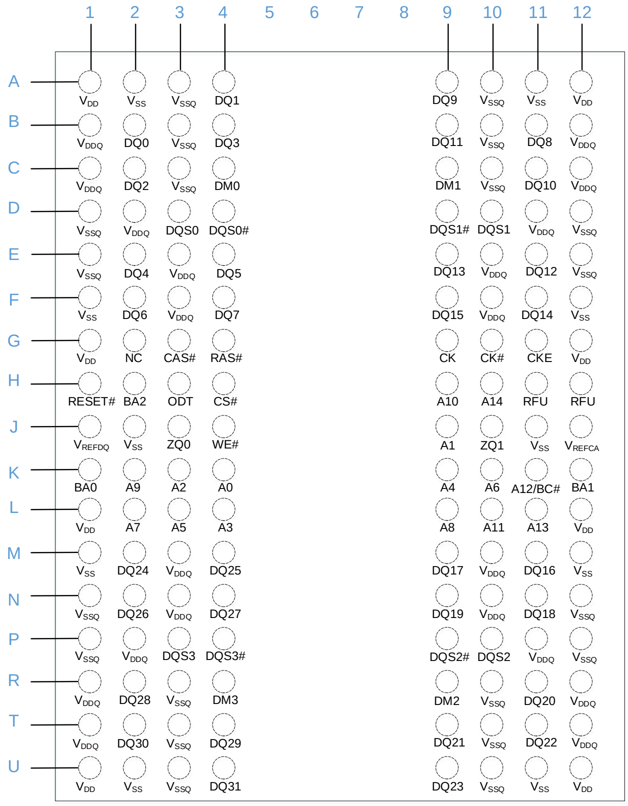
FUNCTIONAL BLOCK DIAGRAM



BALL ASSIGNMENTS

FBGA 136 (Pitch 0.80mm)

Top View (Viewed by Transparency)



	1	2	3	4	5	6	7	8	9	10	11	12
A	V_{DD}	V_{SS}	V_{SSQ}	DQ1					DQ9	V_{SSQ}	V_{SS}	V_{DD}
B	V_{DDQ}	DQ0	V_{SSQ}	DQ3					DQ11	V_{SSQ}	DQ8	V_{DDQ}
C	V_{DDQ}	DQ2	V_{SSQ}	DM0					DM1	V_{SSQ}	DQ10	V_{DDQ}
D	V_{SSQ}	V_{DDQ}	DQS0	DQS0#					DQS1#	DQS1	V_{DDQ}	V_{SSQ}
E	V_{SSQ}	DQ4	V_{DDQ}	DQ5					DQ13	V_{DDQ}	DQ12	V_{SSQ}
F	V_{SS}	DQ6	V_{DDQ}	DQ7					DQ15	V_{DDQ}	DQ14	V_{SS}
G	V_{DD}	NC	CAS#	RAS#					CK	CK#	CKE	V_{DD}
H	RESET#	BA2	ODT	CS#					A10	A14	RFU	RFU
J	V_{REFDQ}	V_{SS}	ZQ0	WE#					A1	ZQ1	V_{SS}	V_{REFCA}
K	BA0	A9	A2	A0					A4	A6	A12/BC#	BA1
L	V_{DD}	A7	A5	A3					A8	A11	A13	V_{DD}
M	V_{SS}	DQ24	V_{DDQ}	DQ25					DQ17	V_{DDQ}	DQ16	V_{SS}
N	V_{SSQ}	DQ26	V_{DDQ}	DQ27					DQ19	V_{DDQ}	DQ18	V_{SSQ}
P	V_{SSQ}	V_{DDQ}	DQS3	DQS3#					DQS2#	DQS2	V_{DDQ}	V_{SSQ}
R	V_{DDQ}	DQ28	V_{SSQ}	DM3					DM2	V_{SSQ}	DQ20	V_{DDQ}
T	V_{DDQ}	DQ30	V_{SSQ}	DQ29					DQ21	V_{SSQ}	DQ22	V_{DDQ}
U	V_{DD}	V_{SS}	V_{SSQ}	DQ31					DQ23	V_{SSQ}	V_{SS}	V_{DD}

FUNCTIONAL DESCRIPTION

The twin-die DDR3 SDRAM is a high-speed, CMOS dynamic random access memory device.

The DDR3 SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is an 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O balls. A single read or write access consists of a single 8*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O balls.

The differential data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the DDR3L SDRAM input receiver. DQS is center-aligned with data for WRITEs. The read data is transmitted by the DDR3 SDRAM and edge-aligned to the data strobes.

Read and write accesses to the DDR3 SDRAM are burst-oriented. Accesses start at a selected location and continue for a burst length of four or eight in a programmed sequence. Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed. The address bits (including CS*n*#, BA*n*, and A*n*) registered coincident with the READ or WRITE command are used to select the rank, bank, and starting column location for the burst access.

Industrial and Military Temperature

JEDEC specifications require the refresh rate to double when TC exceeds 85°C; this also requires use of the high-temperature self-refresh option.
Additionally, ODT resistance, IDD values, some IDD specifications and the input/output impedance must be derated when TC is < 0°C or > 95°C.

BGA 136-BALL DESCRIPTION

Symbol	Type	Function
CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#.
CKE	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is asynchronous for Self-Refresh exit. After VREFCA and VREFDQ have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, CK#, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS#	Input	Chip Select: All commands are masked when CS# is registered HIGH. CS# provides for external Rank selection on systems with multiple Ranks. CS# is considered part of the command code.
ODT	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQS, DQS#. The ODT pin will be ignored if MR1 is programmed to disable RTT.
RAS#. CAS#. WE#	Input	Command Inputs: RAS#, CAS# and WE# (along with CS#) define the command being entered.
DM0-DM3	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS.
BA0 - BA2	Input	Bank Address Inputs: BA0 - BA2 define to which bank an Active, Read, Write, or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.

A0 - A14	Input	Address Inputs: Provided the row address for Active commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/BC# have additional functions; see below). The address inputs also provide the op-code during Mode Register Set commands.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC#	Input	Burst Chop: A12 is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET#	Input	Active Low Asynchronous Reset: Reset is active when RESET# is LOW, and inactive when RESET# is HIGH. RESET# must be HIGH during normal operation. RESET# is a CMOS rail-to-rail signal with DC high and low at 80% and 20% of VDD.
DQ	Input / Output	Data Input/ Output: Bi-directional data bus.
DQS0-3, DQS#0-3	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS is paired with differential signals DQS# to provide differential pair signaling to the system during reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.
VDDQ	Supply	DQ Power Supply: 1.35V (3D3D8G32YB1741) or 1.5V (3D3D8G32WB1741)
VSSQ	Supply	DQ Ground
VDD	Supply	Power Supply: 1.35V (3D3D8G32YB1741) or 1.5V (3D3D8G32WB1741)
VSS	Supply	Ground
VREFDQ	Supply	Reference voltage for DQ
VREFCA	Supply	Reference voltage for CA
ZQ0, ZQ1	Supply	Reference Pin for ZQ calibration

Note: Input only pins (BA0-BA2, A0-A14 RAS#, CAS#, WE#, CS#, CKE, ODT, and RESET#) do not supply termination.

ADDRESSING PARAMETERS

Parameter	256M x 32
Configuration	32M x 32 x 8 banks
Row addressing	A[14:0] (32K)
Bank addressing	BA[2:0] (8)
Column addressing	A[9:0], (1K)
Page size	4KB

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit	Note
V_{DD} supply voltage relative to V_{SS}	V_{DD}	-0.4 ~ 1.975	V	1
V_{DDQ} supply voltage relative to V_{SSQ}	V_{DDQ}	-0.4 ~ 1. 975	V	
Voltage on any pin relative to V_S	V_{IN}, V_{OUT}	-0.4 ~ 1.975	V	
Storage temperature	T_{STG}	-55 ~ +150	°C	
Operating case temperature - Industrial	Tc	-40 ~ +85	°C	2,3,4
Operating case temperature - Specific	Tc	-40 ~ +95	°C	2,3,4
Operating case temperature - Military	Tc	-55 ~ +125	°C	2,3,4

Note :

1. V_{DD} and V_{DDQ} must be within 300mV of each other at all times, and V_{REF} must not be greater than 0.6 × V_{DDQ}. When V_{DD} and V_{DDQ} are <500mV, V_{REF} can be ≤300mV.

2. MAX operating case temperature. TC is measured in the center/top side of the package.

3. Device functionality is not guaranteed if the DRAM device exceeds the maximum TC during operation.

4. The Auto-Refresh command interval can be kept at normal value tREFI = 7.8µs with Tc ≤ 85°C. For operation above 85°C case temperature, Refresh command must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9µs is required. If the Self-Refresh operation is utilized above 85°C case temperature, it is mandatory to either use the Manual Self-Refresh mode with extended temperature range capability (MR2 bit [A6, A7] = [0, 1]) or to enable the optional Auto Self-Refresh mode (MR2 bit [A6, A7] = [1, 0]).

PIN CAPACITANCE

Parameter	Symbol	Min	Max	Unit	Notes
Input/output capacitance (DQ, DMx,DQS, DQS#)	CIO	1,5	2,5	pF	1, 6
Input capacitance, CK and CK#	CCK	0,8	1,4	pF	1, 3
Input capacitance delta, CK and CK#	CDCK	0	0,15	pF	1, 2
Input capacitance delta DQS and DQS#	CDDQS	0	0,15	pF	1
Input capacitance, (CTRL, ADD, CMD input-only pins)	CI	0,75	1,3	pF	1
Input capacitance delta, (All CTRL input-only pins	CDI_CTRL	-0,4	0,2	pF	1, 4
Input capacitance, (address and command pins)	CI_ADD_CMD	-0,4	0,4	pF	1
Input capacitance delta, (All ADD/CMD input-only pins)	CDI_ADD_CMD	-0,4	0,4	pF	1, 5
Input/output capacitance delta (DQ, DM, DQS, DQS#)	CDIO	-0,5	0,3	pF	1, 7, 8
Input/output capacitance of ZQ pin	CZQ		3	pF	1, 7

Notes :

1. Although the DMx pins have different functions, the loading matches DQ and DQS
2. V_{DD}, V_{DDQ}, V_{SS}, V_{SSQ} applied and all other pins (except the pin under test) floating. V_{DD} = V_{DDQ} = 1.5V, VBIAS=V_{DDQ}/2
3. Absolute value of CK-CK#
4. CCK(min) will be equal to CIN(min)
5. CDI_CTRL= CI(CTRL)-0.5*(CI(CLK)+CI(CLK#))
6. CDI_ADD_CMD=CI_ADD_CMD-0.5*(CCK(CK)+CCK(CK#))
7. CDI_CTRL = CI(CTRL) - 0.5*(CCK(CK) + CCK(CK#))
8. CDIO=CIO(DQ, DM)-0.5*(CIO(DQS)+CIO(DQS#))
9. Maximum external load capacitance on ZQ pin: 5pF
10. DQ should be in high impendance state.

IDD SPECIFICATIONS AND CONDITIONS

$V_{DD} = V_{DDQ}$ = 1.35V (1.283V to 1.45V)

Symbol	Parameter	-1333	-1600	Units
IDD0	**Operating One Bank Active-Precharge Current:** CKE: High; External clock: On; tCK, nRC, nRAS, CL: see timing used table; BL: 8; AL: 0; CS: High between ACT and PRE; Command, Address: partially toggling; Data IO: FLOATING; DM:stable at 0; Bank Activity: Cycling with one bank active at a time; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	TBD	126	mA
IDD1	**Operating One Bank Active-Read-Precharge Current:** CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: see timing used table; BL: 81; AL: 0; CS#: High between ACT, RD and PRE; Command, Address, Data IO: partially toggling; DM: stable at 0; Bank Activity: Cycling with one bank active at a time; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	TBD	179	mA
IDD2P0	**Precharge Power-Down Current Slow Exit:** CKE: Low; External clock:On; tCK, CL: see timing used table; BL: 8; AL: 0; CS: stable at 1; Command, Address: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0; Precharge Power Down Mode: Slow Exit	TBD	18	mA
IDD2P1	**Precharge Power-Down Current Fast Exit:** CKE: Low; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; CS#: stable at 1; Command, Address: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0; Pre-charge Power Down Mode: Fast Exit	TBD	31	mA
IDD2N	**Precharge Standby Current:** CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; CS#: stable at 1; Command, Address: partially toggling; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	TBD	53	mA
IDD3P	**Active Power-Down Current:** CKE: Low; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; CS#: stable at 1; Command, Address: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	TBD	58	mA
IDD3N	**Active Standby Current:** CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; CS: stable at 1; Command, Address: partially toggling; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	TBD	84	mA

Symbol	Parameter	-1333	-1600	Units
IDD4W	**Operating Burst Write Current:** CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; CS#: High between WR; Command, Address: partially toggling; Data IO: seamless write data burst with different data between one burst and the next one; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at HIGH	TBD	341	mA
IDD4R	**Operating Burst Read Current:** CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; CS#: High between RD; Command, Address: partially toggling; Data IO: seamless read data burst with different data between one burst and the next one; DM: stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	TBD	341	mA
IDD5B	**Burst Refresh Current:** CKE: High; External clock: On; tCK, CL, nRFC: see timing used table; BL: 8; AL: 0; CS#: High between REF; Command, Address: partially toggling; Data IO: FLOATING; DM: stable at 0; Bank Activity: REF command every nRFC; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	TBD	470	mA
IDD6	**Self-Refresh Current: Normal Temperature Range** TCASE: 0-85°C; Auto Self-Refresh (ASR): Disabled; Self-Refresh Temperature Range (SRT): Normal; CKE: Low; External clock: Off; CK and CK#: LOW; CL: see timing used table; BL: 8; AL: 0; CS, Command, Address, Data IO: FLOATING; DM: stable at 0; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: FLOATING	TBD	27	mA
IDD6ET	**Self Refresh Current: Extended Temperature Range:** TCASE: 0-95°C; Auto Self-Refresh (ASR): Disabled; Self-Refresh Temperature Range (SRT): Extended; CKE: Low; External clock: Off; CK and CK: LOW; CL: see timing used table; BL: 8; AL: 0; CS, Command, Address, Data IO: FLOATING; DM: stable at 0; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: FLOATING	TBD	36	
IDD7	**Operating Bank Interleave Read Current** CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nFAW, CL: see timing used table; BL: 8; AL: CL-1; CS#: High between ACT and RDA; Command, Address: partially toggling; Data IO: read data bursts with different data between one burst and the next one; DM: stable at 0; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	TBD	418	mA

Symbol	Parameter	-1333	-1600	Units
IDD8	**RESET Low Current:** RESET: Low; External clock: off; CK and CK: LOW; CKE: FLOATING; CS, Command, Address, Data IO: FLOATING; ODT Signal : FLOATING	TBD	30	mA

Notes:

1. Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00B
2. Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT_Nom enable: set MR1 A[9,6,2]= 011B; RTT_Wr enable: set MR2 A[10,9] = 10B
3. Precharge Power Down Mode: set MR0 A12=0B for Slow Exit or MR0 A12=1B for Fast Exit
4. Auto Self-Refresh (ASR): set MR2 A6 = 0B to disable or 1B to enable feature
5. Self-Refresh Temperature Range (SRT): set MR2 A7=0B for normal or 1B for extended temperature range
6. Refer to DRAM supplier data sheet and/or DIMM SPD to determine if optional features or requirements are supported by DDR3 SDRAM
7. Read Burst type: Nibble Sequential, set MR0 A[3]=0B

Timing used for IDD and IDDQ Measurement – Loop Patterns

Speed	DDR3-1333	DDR3-1600	Unit
CL-nRCD, nRP	9-9-9	11-11-11	
tCK(min)	1.5	1.25	ns
CL	9	11	nCK
tRCD(min)	9	11	nCK
tRC(min)	33	39	nCK
tRAS(min)	24	28	nCK
tRP(min)	9	11	nCK
tFAW (2KB page size)	30	32	nCK
tRRD (2KB page size)	5	6	nCK
tRFC	234	280	nCK

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Rating			Units	Notes
		Min	Typ	Max		
VDD	Supply Voltage	1.283	1.35	1.45	V	1, 2, 3
		1.425	1.5	1.575		
VDDQ	Supply voltage for output	1.283	1.35	1.45	V	1, 2, 3
		1.425	1.5	1.575		

Notes: **1**. Under all conditions V_{DDQ} must be less than or equal to V_{DD}.

2. V_{DDQ} tracks with V_{DD}. AC parameters are measured with V_{DD} and V_{DDQ} tied together.

3. V_{DD} and V_{DDQ} rating are determinated by operation voltage.

INPUT OPERATING CONDITIONS

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Reference voltage for ADD, CMD inputs	VREFCA(DC)	0.49*VDD	0.51*VDD	V	1,2
Reference voltage for DQ, DM inputs	VREFDQ(DC)	0.49*VDD	0.51*VDD	V	1,2

Notes: **1**. The AC peak noise on VREF may not allow VREF to deviate from VREFCA(DC) by more than ±1% VDD (for reference approx. ±15mV).

2. For reference: Approx VDD/2 ±15mV.

OUTPUT CHARACTERISTICS AND OPERATING CONDITIONS

Parameter/Condition	Symbol	Value	Unit	Note
DC output high measurement level (for IV curve linearity)	VOH(DC)	0.8 x VDDQ	V	
DC output middle measurement level (for IV curve linearity)	VOM(DC)	0.5 x VDDQ	V	
DC output low measurement level (for IV curve linearity)	VOL(DC)	0.2 x VDDQ	V	
AC output high measurement level (for output SR)	VOH(AC)	VTT + 0.1 x VDDQ	V	1
AC output low measurement level (for output SR)	VOL(AC)	VTT - 0.1 x VDDQ	V	1
AC differential output high measurement level	VOHdiff(AC)	+0.2 x VDDQ	V	2
AC differential output low measurement level	VOLdiff(AC)	-0.2 x VDDQ	V	2

Notes: **1.** The swing of ±0.1 × VDDQ is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to VTT = VDDQ/2.

2. The swing of ±0.2 × VDDQ is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to VTT = VDDQ/2 at each of the differential outputs.

AC OPERATING TEST CONDITIONS (25°C)

Speed bin		DDR3-1333		DDR3-1600		Unit	Note
Cl-nRCD-nRP		9-9-9		11-11-11			
Parameter	Symbol	Min	Max	Min	Max		
Internal read command to first data	t_{AA}	13.5	20	13.75	20	ns	7
ACT to read or write delay time	t_{RCD}	13.5	-	13.75		ns	7
PRE command period	t_{RP}	13.5	-	13.75		ns	7
ACT to ACT or REF command time	t_{RC}	49.5	-	48.75		ns	7
ACT to PRE command period	t_{RAS}	36	$9*t_{REFI}$	35	$9*t_{REFI}$	ns	6
Average clock cycle CL=5, CWL=5	$t_{CK(AVG)}$	3.0	3.3	3.0	3.3	ns	1,2,3,4,5
Average clock cycle CL=6, CWL=5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	ns	1,2,3,4,5
Average clock cycle CL=7, CWL=6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	ns	1,2,3,4,5
Average clock cycle CL=8, CWL=6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	ns	1,2,3,4,5
Average clock cycle CL=9, CWL=7	$t_{CK(AVG)}$	1.5	< 1.875	1.5	< 1.875	ns	1,2,3,4,5
Average clock cycle CL=10, CWL=7	$t_{CK(AVG)}$	1.5	< 1.875	1.5	1.875	ns	1,2,3,4,5
Average clock cycle CL=11, CWL=8	$t_{CK(AVG)}$	-	-	1.25	1.5	ns	1,2,3,5
Supported CL settings		6,7,8,9,10		6,7,8,9,10,11		nCK	
SupportedCWL settings		5,6,7		5,6,7,8		nCK	

Notes:

1. The CL setting and CWL setting result in tCK(AVG).MIN and tCK(AVG).MAX requirements.When making a selection of tCK(AVG), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(AVG).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(AVG) value (2.5, 1.875, 1.5 or 1.25ns) when calculating CL [nCK] = tAA [ns] / tCK(AVG) [ns], rounding up to the next 'Supported.
3. tCK(AVG).MAX limits: Calculate tCK(AVG) = tAA.MAX / CL SELECTED and round the resulting tCK(AVG) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875ns or 1.5ns). This result is tCK(AVG).MAX corresponding to CL SELECTED.
4. Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to production tests but verified by design/characterization.
5. Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to production tests but verified by design/characterization.
6. tREFI depends on operating case temperature (Tcase).
7. For devices supporting optional downshift to CL=7 and CL=9, tAA/tRCD/tRPmin must be 13.125 ns. SPD settings must be programmed to match.

Parameter	Symbol	DDR3-1333		DDR3-1600		Unit	Note
		Min	Max	Min	Max		
Average Clock cycle time	t_{CK}(avg)	Refer to standard speed bins				ps	
Minimum Clock cycle (DLL off mode)	t_{CK} (DLL_off)	8	-	8	-	ns	6
Average High pulse width	t_{CH}(avg)	0.47	0.53	0.47	0.53	tCK(avg)	
Average Low pulse width	t_{CL}(avg)	0.47	0.53	0.47	0.53	tCK(avg)	
ACTIVE to ACTIVE command period	t_{RRD}	6	-	6	-	ns	
Four activate window	t_{FAW}	45	-	40	-	ns	
Control and Address input hold time (1.5V)	t_{IH}(base) DC100	140	-	120	-	ps	16
Control and address input setup time (1.5V)	t_{IS}(base) AC175	65	-	45	-	ps	16
Control and address setup time (1.5V)	t_{IS} (base) AC150	190	-	170	-	Ps	16,24
DQ and DM input hold time (1.5V)	t_{DH}(base) DC100	65	-	45	-	ps	17
DQ and DM input setup time (1.5V)	t_{DS}(base) AC150	30	-	10	-	ps	17
Control and address input pulse width for each input	t_{IPW}	620	-	560	-	ps	25
DQ and DM input pulse width for each input	t_{DIPW}	400	-	360	-	ps	25
DQ high impedance time	t_{HZ}(DQ)	-	250	-	225	ps	13,14
DQ low impedance time	t_{LZ}(DQ)	-500	250	-450	225	ps	13,14
DQS and DQS# low impedance time	t_{LZ}(DQS)	-500	250	-450	225	ps	13,14
DQS and DQS# high impedance time	t_{HZ}(DQS)	-	250	-	225		13,14
DQS, DQS# to DQ skew per group, per access	t_{DQSQ}	-	125	-	100	ps	12,13
CAS# to CAS# command delay	t_{CCD}	4	-	4	-	nCK	
DQ output hold time from DQS, DQS#	t_{QH}	0.38	-	0.38	-	tCK(avg)	12,13
DQS, DQS# rising edge output access time from rising CK, CK#	t_{DQSCK}	-255	255	-225	225	ps	12,13
DQS, DQS# rising edge to CK	t_{DQSS}	-0.25	0.25	-0.27	0.27	tCK(avg)	
DQS, DQS# input high pulse width	t_{DQSH}	0.45	0.55	0.45	0.55	tCK(avg)	27,28

Parameter	Symbol	DDR3-1333		DDR3-1600		Unit	Note
		Min	Max	Min	Max		
DQS, DQS# falling edge setup time from CK rising edge	t_{DSS}	0.2	-	0.18	-	tCK(avg)	29
DQS, DQS# falling edge hold time from CK rising edge	t_{DSH}	0.2	-	0.18	-	tCK(avg)	29
DQS, DQS# differential low pulse width	t_{DQSL}	0.45	0.55	0.45	0.55	tCK(avg)	26,28
DQS, DQS# differential high pulse width	t_{DQSH}	0.45	0.55	0.45	0.55	tCK(avg)	27,28
DQS, DQS# differential output high time	t_{QSH}	0.40	-	0.40	-	tCK(avg)	12,13
DQS, DQS# differential output low time	t_{QSL}	0.40	-	0.40	-	tCK(avg)	12,13
Mode register set command cycle time	t_{MRD}	4	-	4	-	nCK	
Mode register set command update delay	t_{MOD}	12nCK, 15ns	-	12nCK, 15ns	-		
DQS, DQS# read preamble time	t_{RPRE}	0.9	-	0.9	-	tCK(avg)	13,19
DQS, DQS# read postamble time	t_{RPST}	0.3	-	0.3	-	tCK(avg)	11,13
DQS, DQS# write preamble time	t_{WPRE}	0.9	-	0.9	-	tCK(avg)	1
DQS, DQS# write postamble time	t_{WPST}	0.3	-	0.3	-	tCK(avg)	1
Write recovery time	t_{WR}	15	-	15	-	ns	
Auto precharge write recovery+ precharge time	t_{DAL}(min)	WR + roundup[tRP / tCK(avg)]				nCK	
Multipurpose register recovery time	t_{MPRR}	1	-	1	-	nCK	22
Internal read command to precharge command delay	t_{RTP}	4nCK, 7.5ns	-	4nCK, 7.5ns	-		
Delay from internal write command to read	t_{WTR}	4nCK, 7.5ns	-	4nCK, 7.5ns	-		18
Minimum CKE low width for self refresh entry to exit timing	t_{CKESR}	t_{CKE}(min)+1nCK	-	t_{CKE}(min)+1nCK	-		
Valid clock requirement after self refresh entry or power down entry	t_{CKSRE}	5nCK, 10ns	-	5nCK, 10ns			
Valid clock requirement before self refresh exit or power down exit	t_{CKSRX}	5nCK, 10ns	-	5nCK, 10ns			

Parameter	Symbol	DDR3-1333		DDR3-1600		Unit	Note
		Min	Max	Min	Max		
Exit self refresh to commands not requiring a locked DLL	t_{XS}	5nCK, tRFC(min)+10 ns	-	5nCK, tRFC(min)+10ns	-		
Exit self refresh to commands requiring a locked DLL	t_{XSDLL}	t_{DLLK}(min)	-	t_{DLLK}(min)		nCK	
REF command to ACT or REF command time	t_{RFC}	350		350		ns	
Average periodic refresh interval 40°C ≤ Tc ≤ +85°C	t_{REFI}	-	7.8	-	7.8	µs	
Average periodic refresh interval 85°C ≤ Tc ≤ +95°C	t_{REFI}	-	3.9	-	3.9	µs	
CKE minimum pulse width	t_{CKE}	3nCK, 5.625ns	-	3nCK, 5ns	-		
Exit reset from CKE high to a valid command	t_{XPR}	5nCK, t_{RFC}(min)+10ns	-	5nCK, t_{RFC}(min)+10ns	-		
DLL lock time	t_{DLLK}	512	-	512	-	nCK	
Power down entry to exit timing	t_{PD}	t_{CKE}(min)	9*t_{REFI}	tCKE(min)	9*tREFI		15
Exit precharge power down with DLL frozen to commands requiring a locked DLL	t_{XPDLL}	10nCK, 24ns	-	10nCK, 24ns			2
Exit power down with DLL to any valid command; exit precharge power down with DLL frozen to commands not requiring a locked DLL	t_{XP}	3nCK, 6ns	-	3nCK, 6ns	-		
Timing of WR command to power down entry (BL8OTF, BL8MRS, BL4OTF)	t_{WRPDEN}	WL+4+ (t_{WR}/t_{CK}(avg))	-	WL+4+ (t_{WR}/t_{CK}(avg))	-	nCK	9
Timing of WR command to power down entry (BC4MRS)	t_{WRPDEN}	WL+2+ (t_{WR}/t_{CK}(avg))	-	WL+2+ (t_{WR}/t_{CK}(avg))	-	nCK	9
Timing of WRA command to power down entry (BL8OTF, BL8MRS, BL4OTF)	$t_{WRAPDEN}$	WL+4+WR+1	-	WL+4+WR+1	-	nCK	10
Timing of WR command to power down entry (BC4MRS)	$t_{WRAPDEN}$	WL+2+WR+1	-	WL+2+WR+1	-	nCK	10

Parameter	Symbol	DDR3-1333		DDR3-1600		Unit	Note
		Min	Max	Min	Max		
Timing of REF command to power down entry	$t_{REFDPEN}$	1	-	1	-	nCK	20,21
Timing of MRS command to power down entry	$t_{MRSPDEN}$	tMOD(min)	-	tMOD(min)	-		
Command pass disable delay	t_{CPDED}	1	-	1	-	nCK	
Timing of ACT to power down entry	$t_{ACTPDEN}$	1	-	1	-	nCK	20
Timing of PRE to command power down entry	t_{PRPDEN}	1	-	1	-	nCK	20
Timing of RD/RDA command to power down entrt	t_{RDPDEN}	RL+4+1	-	RL+4+1	-	nCK	
RTT turn-on	t_{AON}	-250	250	-225	225	ps	7
Asynchronous RTT turn-on delay (power down with DLL frozen)	t_{AONPD}	2	8.5	2	8.5	ns	
RTT_Nom and RTT_WR turn off time from ODTLoff reference	t_{AOF}	0.3	0.7	0.3	0.7	tCK(avg)	8
Asynchronous RTT turn off delay (power down with DLL frozen)	t_{AOFPD}	2	8.5	2	8.5	ns	
ODT high time without write command or with write command and BC4	ODTH4	4	-	4	-	nCK	
ODT high time with write command and BL8	ODTH8	6	-	6	-	nCK	
RTT dynamic change skew	t_{ADC}	0.3	0.7	0.3	0.7	tCK(avg)	
Power up and reset calibration time	t_{ZQINIT}	512	-	512	-	nCK	
Normal operation calibration time	t_{ZQOPER}	256	-	256	-	nCK	
Normal operation short calibration time	t_{ZQCS}	64	-	64	-	nCK	23
First DQS/DQS# rising edge after write leveling mode is programmed	t_{WLMRD}	40	-	40	-	nCK	3
DQS/DQS# delay after write leveling more is programmed	$t_{WLDDQSEN}$	25	-	25	-	nCK	3

Parameter	Symbol	DDR3-1333		DDR3-1600		Unit	Note
		Min	Max	Min	Max		
Write leveling setup time from rising CK/CK# crossing to rising DQS/DQS# crossing	t_{WLS}	195	-	165	-	ps	
Write leveling hold time from rising DQS/DQS# crossing to rising CK/CK# crossing	t_{WLH}	195	-	165	-	ps	
Write leveling output delay	t_{WLO}	0	9	0	7.5	ns	
Write leveling output error	t_{WLOE}	0	2	0	2	ns	
Absolute clock period	t_{CK}(abs)	t_{CK}(avg)min + t_{JIT}(per)min	t_{CK}(avg)max + t_{JIT}(per)max	t_{CK}(avg)min + t_{JIT}(per)min	t_{CK}(avg)max + t_{JIT}(per)max	ps	
Absolute clock high pulse width	t_{CH}(abs)	0.43	-	0.43	-	t_{CK}(avg)	30
Absolute clock low pulse width	t_{CL}(abs)	0.43	-	0.43	-	t_{CK}(avg)	31
Clock period jitter	t_{JIT}(per)	-80	80	-70	70	ps	
Clock period jitter during DLL locking time	t_{JIT}(per,lck)	-70	70	-60	60	ps	
Cycle to cycle clock jitter	t_{JIT}(cc)	-	160	-	140	ps	
Cycle to cycle clock jitter during DLL locking time	t_{JIT}(cc,lck)	-	140	-	120	ps	
Cumulative error across 2 cycles	t_{ERR}(2per)	-118	118	-103	103	ps	
Cumulative error across 3 cycles	t_{ERR}(3per)	-140	140	-122	122	ps	
Cumulative error across 4 cycles	t_{ERR}(4per)	-155	155	-136	136	ps	
Cumulative error across 5 cycles	t_{ERR}(5per)	-168	168	-147	147	ps	
Cumulative error across 6 cycles	t_{ERR}(6per)	-177	177	-155	155	ps	
Cumulative error across 7 cycles	t_{ERR}(7per)	-186	186	-163	163	ps	
Cumulative error across 8 cycles	t_{ERR}(8per)	-193	193	-169	169	ps	
Cumulative error across 9 cycles	t_{ERR}(9per)	-200	200	-175	175	ps	
Cumulative error across 10 cycles	t_{ERR}(10per)	-205	205	-180	180	ps	
Cumulative error across 11 cycles	t_{ERR}(11per)	-210	210	-184	184	ps	
Cumulative error across 12 cycles	t_{ERR}(12per)	-215	215	-188	188	ps	
Cumulative error across n= 13,14,…,49,50 cycles	t_{ERR}(nper)	t_{ERR}(nper)min= (1+0.68ln(n)) * t_{JIT}(per)min t_{ERR}(nper)max= (1+0.68ln(n)) * t_{JIT}(per)max				ps	32

Notes:

1. Actual value dependant upon measurement level definitions.
2. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
3. The max values are system dependent.
4. WR as programmed in mode register
5. Value must be rounded-up to next higher integer value
6. There is no maximum cycle time limit besides the need to satisfy the refresh interval, t_{REFI}.
7. ODT turn on time (min) is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time (max) is when the ODT resistance is fully on. Both are measured from ODTLon.
8. ODT turn-off time (min) is when the device starts to turn-off ODT resistance. ODT turn-off time (max) is bus is in high impedance. Both are measured from ODTLoff
9. t_{WR} is defined in ns, for calculation of t_{WRPDEN} it is necessary to round up t_{WR} / t_{CK} to the next integer.
10. WR in clock cycles as programmed in MR0.
11. The maximum read postamble is bound by t_{DQSCK}(min) plus t_{QSH}(min) on the left side and t_{HZ}(DQS)max on the right side.
12. Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by t.b.d.
13. Value is only valid for RON34
14. Single ended signal parameter. Refer to the section of t_{LZ}(DQS), t_{LZ}(DQ), t_{HZ}(DQS), t_{HZ}(DQ) notes for definition and measurement method.
15. t_{REFI} depends on operating case temperature (Tc).
16. t_{IS}(base) and t_{IH}(base) values are for 1V/ns CMD/ADD single-ended slew rate and 2V/ns CK, CK# differential slew rate. Note for DQ and DM signals, V_{REF}(DC) = V_{RefDQ}(DC). For input only pins except RESET#, V_{Ref}(DC) = V_{RefCA}(DC). See Address / Command Setup, Hold and Derating section.
17. t_{DS}(base) and t_{DH}(base) values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS, DQS# differential slew rate. Note for DQ and DM signals, V_{REF}(DC) = V_{RefDQ}(DC). For input only pins except RESET#, V_{Ref}(DC) = V_{RefCA}(DC). See Data Setup, Hold and Slew Rate Derating section.
18. Start of internal write transaction is defined as follows:
    a. For BL8 (fixed by MRS and on- the-fly): Rising clock edge 4 clock cycles after WL.
    b. For BC4 (on- the- fly): Rising clock edge 4 clock cycles after WL.
    c. For BC4 (fixed by MRS): Rising clock edge 2 clock cycles after WL.
19. The maximum read preamble is bound by t_{LZ}(DQS)min on the left side and t_{DQSCK}(max) on the right side
20. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
21. Although CKE is allowed to be registered LOW after a REFRESH command once $t_{REFPDEN}$(min) is satisfied, there are cases where additional time such as t_{XPDLL}(min) is also required
22. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
23. One ZQCS command can effectively correct a minimum of 0.5 % (ZQ Correction) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the ‘Output Driver Voltage and Temperature Sensitivity’ and ‘ODT Voltage and Temperature Sensitivity’ tables. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters. One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{ZQCorrection}{(Tsens \times Tdriftrate) + (Vsens \times Vdriftrate)}$$

where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities

24. The t_{IS}(base) AC150 specifications are adjusted from the t_{IS}(base) specification by adding an additional 100 ps of derating to accommodate for the lower alternate threshold of 150 mV and another 25 ps to account for the earlier reference point [(175 mv - 150 mV) / 1 V/ns].

25. Pulse width of a input signal is defined as the width between the first crossing of VREF(DC) and the consecutive crossing of V_{REF}(DC).

26. t_{DQSL} describes the instantaneous differential input low pulse width on DQS - DQS#, as measured from one falling edge to the next consecutive rising edge.

27. t_{DQSH} describes the instantaneous differential input high pulse width on DQS - DQS#, as measured from one rising edge to the next consecutive falling edge.

28. t_{DQSH},act + t_{DQSL},act = 1 t_{CK},act ; with t_{XYZ},act being the actual measured value of the respective timing parameter in the application.

29. t_{DSH},act + t_{DSS},act = 1 tCK,act ; with t_{XYZ},act being the actual measured value of the respective timing parameter in the application.

30. t_{CH}(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.

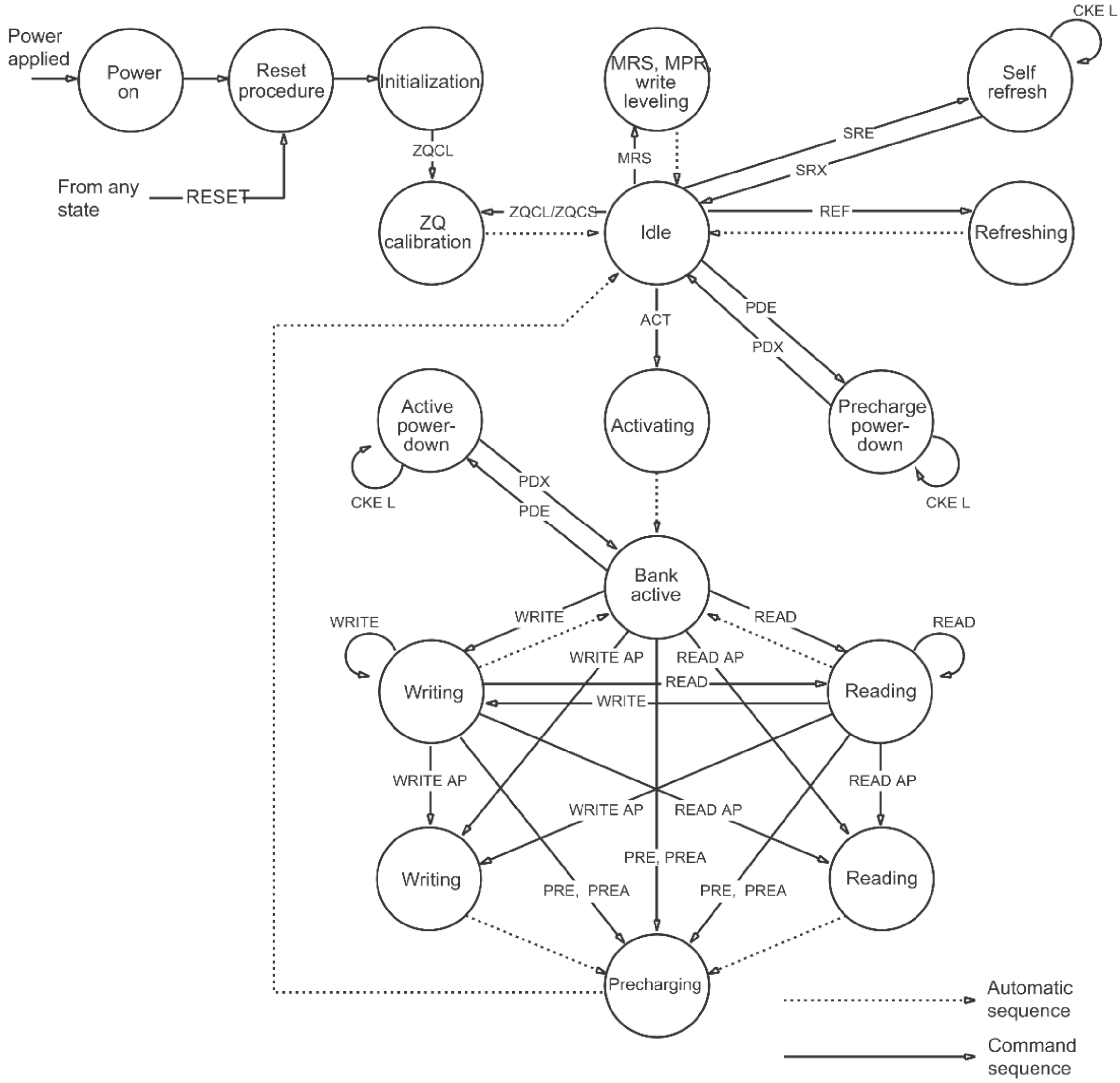
31. t_{CL}(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.

32. n = from 13 cycles to 50 cycles. This row defines 38 parameters.

33. Tc ≤ 85°C.

34. Required for operation at Tc > 85°C.

SIMPLIFIED STATE DIAGRAM



Abbreviation	Function	Abbreviation	Function	Abbreviation	Function
ACT	Activate	READ	RD, RDS4, RDS8	PDE	Enter Power down
PRE	Precharge	READ AP	RDA, RDAS4, RDAS8	PDX	Exit Power down
PREA	Precharge All	WRITE	WR, WRS4, WRS8	SRE	Self refresh entry
MRS	Mode Register set	WRITE AP	WRA, WRAS4, WRAS8	SRX	Self refresh exit
REF	Refresh	RESET	Start Reset Procedure	MPR	Multi purpose register
ZQCL	ZQ long calibration	ZQCS	ZQ short calibration		

COMMAND TRUTH TABLE

Function	Symbol	CKE		CS#	RAS#	CAS#	WE#	BA0-BA2	A13-A14	A12-BC#	A10-AP	A0-A9,A11	Notes
		n-1	n										
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				
Refresh	REF	H	H	L	L	L	H	V	V	V	V	V	
Self Refresh entry	SRE	H	L	L	L	L	H	V	V	V	V	V	7,9,12
Self refresh exit	SRX	L	H	H	X	X	X	X	X	X	X	X	7,8,9,12
				L	H	H	H	V	V	V	V	V	
Single bank precharge	PRE	H	H	L	L	H	L	BA	V	V	L	V	
Precharge all banks	PREA	H	H	L	L	H	L	V	V	V	H	V	
Bank activate	ACT	H	H	L	L	H	H	BA	Row address (RA)				
Write (Fixed BL8 or BL4)	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	
Write (BL4, on the fly)	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA	
Write (BL8, on the fly)	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA	
Write with Auto precharge (fixed BL8 or BL4)	WRA	H	H	L	H	L	L	BA	RFU	V	H	CA	
Write with auto precharge (BL4, on the fly)	WRAS4	H	H	L	H	L	L	BA	RFU	L	H	CA	
Write with auto precharge (BL8, on the fly)	WRAS8	H	H	L	H	L	L	BA	RFU	H	H	CA	
Read (fixed BL8 or BL4)	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	
Read (BL4, on the fly)	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA	
Read (BL8, on the fly)	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA	
Read with auto precharge (fixed BL8 or BL4)	RDA	H	H	L	H	L	H	BA	RFU	V	H	CA	
Read with auto precharge (BL4, on the fly)	RDAS4	H	H	L	H	L	H	BA	RFU	L	H	CA	
Read with auto precharge (BL8, on the fly)	RDAS8	H	H	L	H	L	H	BA	RFU	H	H	CA	
No operation	NOP	H	H	L	H	H	H	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	11
Power down entry	PDE	H	L	L	H	H	H	V	V	V	V	V	6,12
				H	X	X	X	X	X	X	X	X	
Power down exit	PDX	L	H	L	H	H	H	V	V	V	V	V	6,12
				H	X	X	X	X	X	X	X	X	
ZQ calibration long	ZQCL	H	H	L	H	H	L	X	X	X	H	X	
ZQ calibration short	ZQCS	H	H	L	H	H	L	X	X	X	L	X	

Notes:

1. All DDR3 SDRAM commands are defined by states of CS#, RAS#, CAS#, WE# and CKE at the rising edge of the clock. The MSB of BA, RA and CA are device density and configuration dependant.
2. RESET# is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.
3. Bank addresses (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.
4. “V” means “H or L (but a defined logic level)” and “X” means either “defined or undefined (like floating) logic level”.
5. Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-Fly BL will be defined by MRS.
6. The Power Down Mode does not perform any refresh operation.
7. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
8. Self Refresh Exit is asynchronous.
9. V_{REF}(Both V_{REFDQ} and V_{REFCA}) must be maintained during Self Refresh operation.
10. The No Operation command should be used in cases when the DDR3 SDRAM is in an idle or wait state. The purpose of the No Operation command (NOP) is to prevent the DDR3 SDRAM from registerng any unwanted commands between operations. A No Operation command will not terminate a pervious operation that is still executing, such as a burst read or write cycle.
11. The Deselect command performs the same function as No Operation command.
12. Refer to the CKE Truth Table for more detail with CKE transition.

CKE TRUTH TABLE

Current state	CKE		Command (N)^3 RAS#, CAS#, WE#, CS#	Action (N)^3	Notes
	N-1	N			
Power down	L	L	X	Maintain power down	14,15
	L	H	Deselect or nop	Power down exit	11,14
Self –refresh	L	L	X	Maintain self refresh	15,16
	L	H	Deselect or nop	Self refresh exit	8,12,16
Bank active	H	L	Deselect or nop	Active power down entry	11,13,14
Reading	H	L	Deselect or nop	Power down entry	11,13,14,17
Writing	H	L	Deselect or nop	Power down entry	11,13,14,17
Precharging	H	L	Deselect or nop	Power down entry	11,13,14,17
Refreshing	H	L	Deselect or nop	Precharge power down entry	11
All banks Idle	H	L	Deselect or nop	Precharge power down entry	11,13,14,18
	H	L	Refresh	Self refresh	9,13,18
For more details with all signals see “Command truth table”					10

Notes:

1. CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.
2. Current state is defined as the state of the DDR3 SDRAM immediately prior to clock edge N.
3. COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N), ODT is not included here.
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self- Refresh.
6. CKE must be registered with the same value on t_{CKE}min consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the t_{CKE}min clocks of registeration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of t_{IS} + t_{CKE}min + t_{IH}.
7. DESELECT and NOP are defined in the Command Truth Table.
8. On Self-Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the t_{XS} period. Read or ODT commands may be issued only after t_{XSDLL} is satisfied.
9. Self-Refresh mode can only be entered from the All Banks Idle state.
10. Must be a legal command as defined in the Command Truth Table.
11. Valid commands for Power-Down Entry and Exit are NOP and DESELECT only.
12. Valid commands for Self-Refresh Exit are NOP and DESELECT only.
13. Self-Refresh can not be entered during Read or Write operations. For a detailed list of restrictions See self-Refresh Operation an power down modes
14. The Power-Down does not perform any refresh operations.
15. “X” means “don’t care“ (including floating around VREF) in Self-Refresh and Power-Down. It also applies to Address pins.
16. V_{REF} (Both V_{REFDQ} and V_{REFCA}) must be maintained during Self-Refresh operation.

17. If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power-Down is entered, otherwise Active Power-Down is entered.

18. ‘Idle state’ is defined as all banks are closed (t_{RP}, t_{DAL}, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (t_{MRD}, t_{MOD}, t_{RFC}, t_{ZQinit}, t_{ZQoper}, t_{ZQCS}, etc.) as well as all Self-Refresh exit and Power-Down Exit parameters are satisfied (t_{XS}, t_{XP}, t_{XPDLL}, etc).

POWER-UP AND INITIALIZATION

The following sequence is required for POWER UP and Initialization.

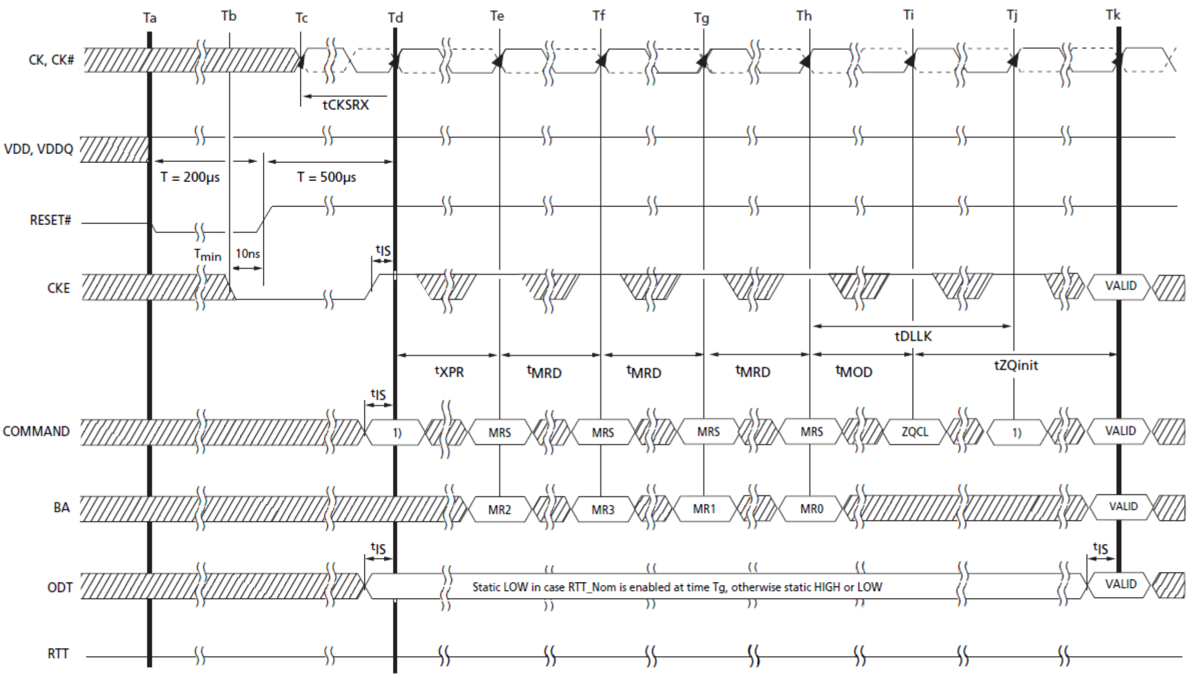
1. Apply power (RESET# is recommended to be maintained below 0.2 x V_{DD}; all other inputs may be undefined). RESET# needs to be maintained for minimum 200 µs with stable power. CKE is pulled “Low” anytime before RESET# being de-asserted (min. time 10 ns). The power voltage ramp time between 300 mv to V_{DD}min must be no greater than 200 ms; and during the ramp, $V_{DD} > V_{DDQ}$ and $(V_{DD} - V_{DDQ}) < 0.3$ volts.
   - V_{DD} and V_{DDQ} are driven from a single power converter output, AND
   - The voltage levels on all pins other than V_{DD}, V_{DDQ}, V_{SS}, V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side and must be larger than or equal to V_{SSQ} and V_{SS} on the other side. In addition, V_{TT} is limited to 0.95 V max once power ramp is finished, AND
   - V_{REF} tracks $V_{DDQ}/2$.

   or

   - Apply V_{DD} without any slope reversal before or at the same time as V_{DDQ}.
   - Apply V_{DDQ} without any slope reversal before or at the same time as V_{TT} & V_{REF}.
   - The voltage levels on all pins other than V_{DD}, V_{DDQ}, V_{SS}, V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side and must be larger than or equal to V_{SSQ} and V_{SS} on the other side.
2. After RESET# is de-asserted, wait for another 500 µs until CKE becomes active. During this time, the DRAM will start internal state initialization; this will be done independently of external clocks.
3. Clocks (CK, CK#) need to be started and stabilized for at least 10 ns or 5 t_{CK} (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding set up time to clock (tIS) must be met. Also, a NOP or Deselect command must be registered (with t_{IS} set up time to clock) before CKE goes active. Once the CKE is registered “High” after Reset, CKE needs to be continuously registered “High” until the initialization sequence is finished, including expiration of t_{DLLK} and t_{ZQ}init.
4. The DDR3 SDRAM keeps its on-die termination in high-impedance state as long as RESET# is asserted. Further, the SDRAM keeps its on-die termination in high impedance state after RESET# deassertion until CKE is registered HIGH. The ODT input signal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of t_{DLLK} and t_{ZQ}init.
5. After CKE is being registered high, wait minimum of Reset CKE Exit time, t_{XPR}, before issuing the first MRS command to load mode register. (t_{XPR}=max (t_{XS} ; 5 x t_{CK})
6. Issue MRS Command to load MR2 with all application settings. (To issue MRS command for MR2, provide “Low” to BA0 and BA2, “High” to BA1.)
7. Issue MRS Command to load MR3 with all application settings. (To issue MRS command for MR3, provide “Low” to BA2, “High” to BA0 and BA1.)
8. Issue MRS Command to load MR1 with all application settings and DLL enabled. (To issue "DLL Enable" command, provide "Low" to A0, "High" to BA0 and "Low" to BA1-BA2).
9. Issue MRS Command to load MR0 with all application settings and “DLL reset”. (To issue DLL reset command, provide "High" to A8 and "Low" to BA0-2).
10. Issue ZQCL command to starting ZQ calibration.

11. Wait for both t_{DLLK} and t_{ZQ}init completed.
12. The DDR3 SDRAM is now ready for normal operation.

RESET AND POWER INITIALIZATION SEQUENCE



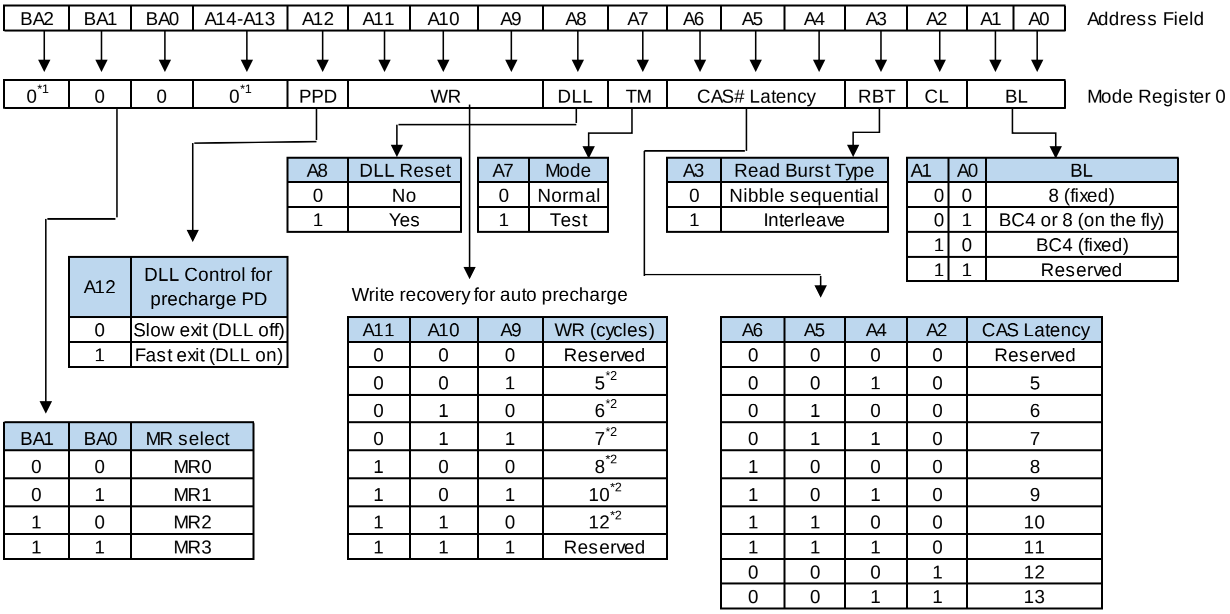
NOTE 1. From time point “Td” until “Tk” NOP or DES commands must be applied between MRS and ZQCL commands.

⸾ TIME BREAK ▨ DON’T CARE

MODE REGISTER DEFINITION

Mode Register MR0

The mode register MR0 stores the data for controlling various operating modes of DDR3 SDRAM. It controls burst length, read burst type, CAS latency, test mode, DLL reset, WR and DLL control for precharge Power-Down, which include various vendor specific options to make DDR3 SDRAM useful for various applications. The mode register is written by asserting low on CS#, RAS#, CAS#, WE#, BA0, BA1, and BA2, while controlling the states of address pins according to the below figure.



Address Field	BA2	BA1	BA0	A14-A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode Register 0	0^{*1}	0	0	0^{*1}	PPD	WR			DLL	TM	CAS# Latency			RBT	CL	BL	

A8	DLL Reset
0	No
1	Yes

A7	Mode
0	Normal
1	Test

A3	Read Burst Type
0	Nibble sequential
1	Interleave

A1	A0	BL
0	0	8 (fixed)
0	1	BC4 or 8 (on the fly)
1	0	BC4 (fixed)
1	1	Reserved

A12	DLL Control for precharge PD
0	Slow exit (DLL off)
1	Fast exit (DLL on)

Write recovery for auto precharge

A11	A10	A9	WR (cycles)
0	0	0	Reserved
0	0	1	5^{*2}
0	1	0	6^{*2}
0	1	1	7^{*2}
1	0	0	8^{*2}
1	0	1	10^{*2}
1	1	0	12^{*2}
1	1	1	Reserved

A6	A5	A4	A2	CAS Latency
0	0	0	0	Reserved
0	0	1	0	5
0	1	0	0	6
0	1	1	0	7
1	0	0	0	8
1	0	1	0	9
1	1	0	0	10
1	1	1	0	11
0	0	0	1	12
0	0	1	1	13

BA1	BA0	MR select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

Notes:

*__1__. BA2, A13, A14 are reserved for future use and must be programmed to 0 during MRS

***2**. WR(write recovery for autoprecharge)min in clock cycles is calculated by dividing t_{WR}(in ns) by t_{CK}(in ns) and rounding up to the next integer: WRmin[cycles] = Roundup(t_{WR}[ns]/t_{CK}[ns]). The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with t_{RP} to determine t_{DAL}.

Burst length, Type and Order

Accesses within a given burst may be programmed to sequential or interleaved order. The burst type is selected via bit A3. The ordering of accesses within a burst is determined by the burst length, burst type, and the starting column address as shown in the table below. The burst length is defined by bits A0-A1. Burst length options include fixed BC4, fixed BL8, and 'on the fly' which allows BC4 or BL8 to be selected coincident with the registration of a Read or Write command via A12/BC#.

Burst length	Read/Write	Starting column address (A2,A1,A0)	Burst type = sequential A3=0	Burst type = interleaved A3=1	Notes
4 (Burst chop)	READ	0 0 0	0,1,2,3,T,T,T,T	0,1,2,3,T,T,T,T	1,2,3
		0 0 1	1,2,3,0,T,T,T,T	1,0,3,2,T,T,T,T	1,2,3
		0 1 0	2,3,0,1,T,T,T,T	2,3,0,1,T,T,T,T	1,2,3
		0 1 1	3,0,1,2,T,T,T,T	3,2,1,0,T,T,,T,T	1,2,3
		1 0 0	4,5,6,7,T,T,T,T	4,5,6,7,T,T,T,T	1,2,3
		1 0 1	5,6,7,4,T,T,T,T	5,4,7,6,T,T,T,T	1,2,3
		1 1 0	6,7,4,5,T,T,T,T	6,7,4,5,T,T,T,T	1,2,3
		1 1 1	7,4,5,6,T,T,T,T	7,6,5,4,T,T,T,T	1,2,3
	WRITE	0,V,V	0,1,2,3,X,X,X,X	0,1,2,3,X,X,X,X	1,2,4,5
		1,V,V	4,5,6,7,X,X,X,X	4,5,6,7,X,X,X,X	1,2,4,5
8	READ	0 0 0	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2
		0 0 1	1,2,3,0,5,6,7,4	1,0,3,2,5,4,7,6	2
		0 1 0	2,3,0,1,6,7,4,5	2,3,1,0,6,7,4,5	2
		0 1 1	3,0,1,2,7,4,5,6	3,2,1,0,7,6,5,4	2
		1 0 0	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3	2
		1 0 1	5,6,7,4,1,2,3,0	5,4,7,6,1,0,3,2	2
		1 1 0	6,7,4,5,2,3,0,1	6,7,4,5,2,3,0,1	2
		1 1 1	7,4,5,6,3,0,1,2	7,6,5,4,3,2,1	2
	WRITE	V,V,V	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2,4

Notes:

1. In case of burst length being fixed to 4 by MR0 setting, the internal write operation starts two clock cycles earlier than for the BL8 mode. This means that the starting point for t_{WR} and t_{WTR} will be pulled in by two clocks. In case of burst length being selected on-the-fly via A12/BC#, the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for t_{WR} and t_{WTR} will not be pulled in by two clocks.
2. 0...7 bit number is value of CA[2:0] that causes this bit to be the first read during a burst.
3. T: Output driver for data and strobes are in high impedance.
4. V: a valid logic level (0 or 1), but respective buffer input ignores level on input pins.
5. X: Don't Care

CAS Latency

The CAS Latency is defined by MR0 (bits A9-A11) as shown in Figure 9. CAS Latency is the delay, in clock cycles, between the internal Read command and the availability of the first bit of output data. DDR3 SDRAM does not support any half-clock latencies. The overall Read Latency (RL) is defined as Additive Latency (AL) + CAS Latency (CL); RL = AL + CL.

Test Mode

The normal operating mode is selected by MR0 (bit A7 = 0) and all other bits set to the desired values. Programming bit A7 to a ‘1’ places the DDR3 SDRAM into a test mode that is only used by the DRAM Manufacturer and should NOT be used. No operations or functionality is specified if A7 = 1.

DLL Reset

The DLL Reset bit is self-clearing, meaning that it returns back to the value of ‘0’ after the DLL reset function has been issued. Once the DLL is enabled, a subsequent DLL Reset should be applied. Any time that the DLL reset function is used, t_{DLLK} must be met before any functions that require the DLL can be used (i.e., Read commands or ODT synchronous operations).

Write Recovery

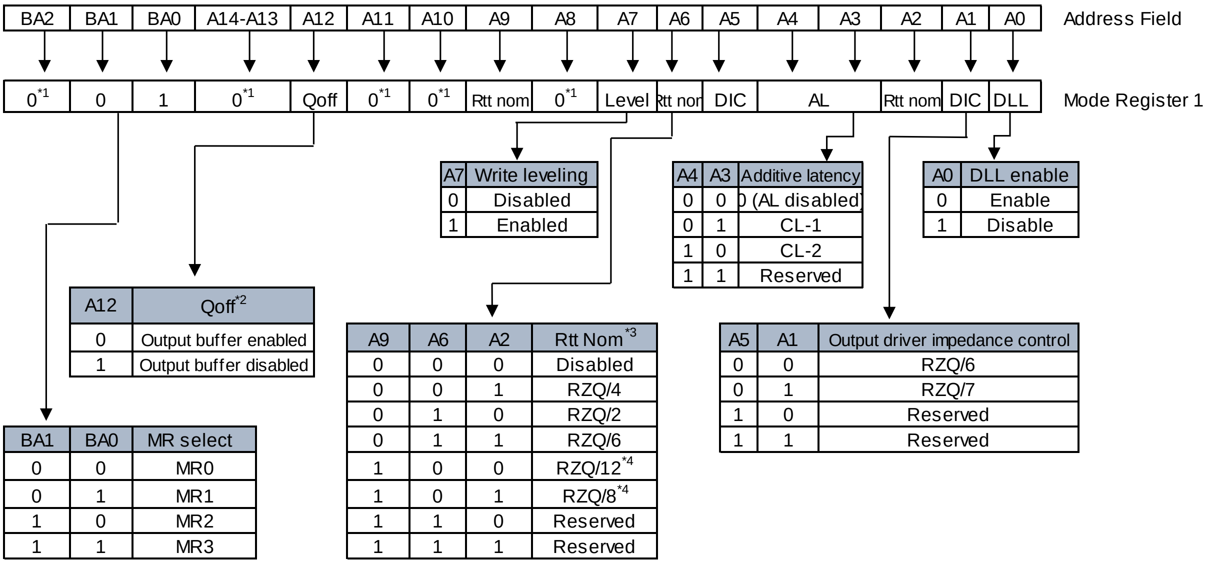
The programmed WR value MR0 (bits A9, A10, and A11) is used for the auto precharge feature along with t_{RP} to determine t_{DAL}. WR (write recovery for auto-precharge) min in clock cycles is calculated by dividing t_{WR} (in ns) by t_{CK} (in ns) and rounding up to the next integer: WRmin[cycles] = Roundup(t_{WR}[ns]/ t_{CK}[ns]). The WR must be programmed to be equal to or larger than t_{WR}(min).

Precharge PD PLL

MR0 (bit A12) is used to select the DLL usage during precharge power-down mode. When MR0 (A12 = 0), or ‘slow-exit’, the DLL is frozen after entering precharge power-down (for potential power savings) and upon exit requires t_{XPDLL} to be met prior to the next valid command. When MR0 (A12 = 1), or ‘fast-exit’, the DLL is maintained after entering precharge power-down and upon exiting power-down requires t_{XP} to be met prior to the next valid command.

Mode Register MR1

The Mode Register MR1 stores the data for enabling or disabling the DLL, output driver strength, Rtt_Nom impedance, additive latency, Write leveling enable, T_{DQS} enable and Qoff. The Mode Register 1 is written by asserting low on CS#, RAS#, CAS#, WE#, high on BA0 and low on BA1 and BA2, while controlling the states of address pins according to the figure below.



Address Field	BA2	BA1	BA0	A14-A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode Register 1	0*1	0	1	0*1	Qoff	0*1	0*1	Rtt nom	0*1	Level	Rtt nor	DIC	AL	AL	Rtt nom	DIC	DLL

A7	Write leveling
0	Disabled
1	Enabled

A4	A3	Additive latency
0	0	0 (AL disabled)
0	1	CL-1
1	0	CL-2
1	1	Reserved

A0	DLL enable
0	Enable
1	Disable

A12	Qoff*2
0	Output buffer enabled
1	Output buffer disabled

A9	A6	A2	Rtt Nom *3
0	0	0	Disabled
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/12*4
1	0	1	RZQ/8*4
1	1	0	Reserved
1	1	1	Reserved

A5	A1	Output driver impedance control
0	0	RZQ/6
0	1	RZQ/7
1	0	Reserved
1	1	Reserved

BA1	BA0	MR select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

Notes:

***1.** BA2, A13, A14, A11, A10 and A8 are reserved for future use and must be programmed to 0 during MRS,

***2.** Output disabled – D_{QS}, D_{QSS}, D_{QSS}#

***3.** In Write leveling mode (MR1[bit7]=1) with MR1[bit12]=1, all RTT_Nom settings are allowed; in write leveling mode (MR1[bit7]=1) with MR1[bit12]=0, only RTT_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed.

***4.** If RTT_Nom is used during write, only the values RZQ/2, RZQ/4 and RZQ/6 are allowed.

RZQ=240 Ohms

DLL Enable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. During normal operation (DLL-on) with MR1 (A0 = 0), the DLL is automatically disabled when entering Self-Refresh operation and is automatically re-enabled upon exit of Self-Refresh operation. Any time the DLL is enabled and subsequently reset, t_{DLLK} clock cycles must occur before a Read or synchronous ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the t_{DQSCK}, t_{AON} or t_{AOF} parameters. During t_{DLLK}, CKE must continuously be registered high. DDR3 SDRAM does not require DLL for any Write operation, except when RTT_WR is enabled and the DLL is required for proper ODT operation. For more detailed information on DLL Disable operation refer to “DLL-off Mode.

The direct ODT feature is not supported during DLL-off mode. The on-die termination resistors must be disabled by continuously registering the ODT pin low and/or by programming the RTT_Nom bits MR1{A9,A6,A2} to {0,0,0} via a mode register set command during DLL-off mode. The dynamic ODT feature is not supported at DLL-off mode. User must use MRS command to set Rtt_WR, MR2 {A10, A9} = {0,0}, to disable Dynamic ODT externally.

ODT Rtt Values

DDR3 SDRAM is capable of providing two different termination values (Rtt_Nom and Rtt_WR). The nominal termination value Rtt_Nom is programmed in MR1. A separate value (Rtt_WR) may be programmed in MR2 to enable a unique Rtt value when ODT is enabled during writes. The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled.

Additive Latency

Additive Latency (AL) operation is supported to make command and data bus efficient for sustainable bandwidths in DDR3 SDRAM. In this operation, the DDR3 SDRAM allows a read or write command (either with or without auto-precharge) to be issued immediately after the active command. The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of the AL and CAS Latency (CL) register settings. Write Latency (WL) is controlled by the sum of the AL and CAS Write Latency (CWL) register settings

Write Leveling

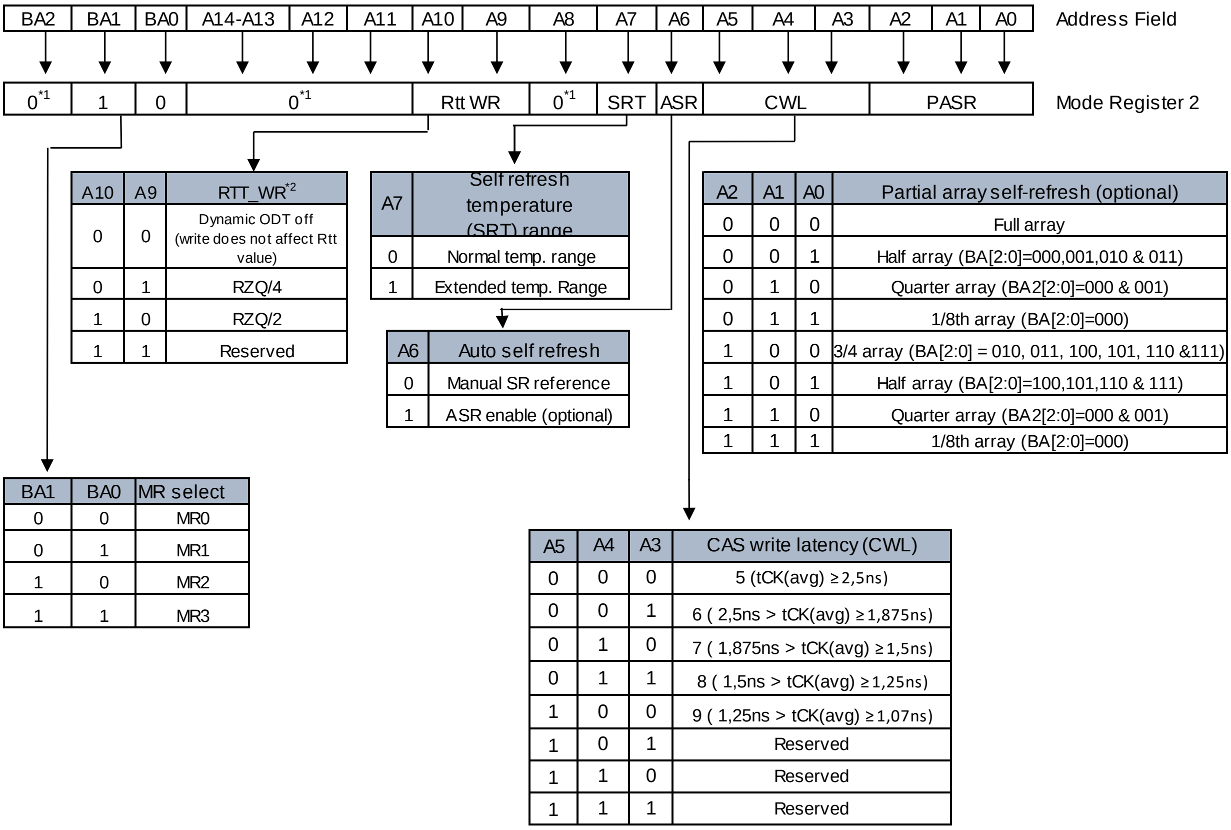
Additive Latency (AL) operation is supported to make command and data bus efficient for sustainable bandwidths in DDR3 SDRAM. In this operation, the DDR3 SDRAM allows a read or write command
For better signal integrity, DDR3 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has the benefit of reducing the number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the Controller to maintain t_{DQSS}, t_{DSS}, and t_{DSH} specification. Therefore, the DDR3 SDRAM supports a ‘write leveling’ feature to allow the controller to compensate for skew.

Output Disable

The DDR3 SDRAM outputs may be enabled/disabled by MR1 (bit A12) as shown in Figure 10. When this feature is enabled (A12 = 1), all output pins (DQs, DQS, DQS#, etc.) are disconnected from the device, thus removing any loading of the output drivers. This feature may be useful when measuring module power, for example. For normal operation, A12 should be set to ‘0’.

Mode Register MR2

The Mode Register MR2 stores the data for controlling refresh related features. Rtt_WR impedance, and CAS write latency. The Mode Register 2 is written by asserting low on CS#, RAS#, CAS#, WE#, high on BA1 and low on BA0 and BA2, while controlling the states of address pins according to the table below.



	BA2	BA1	BA0	A14-A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Address Field	BA2	BA1	BA0	A14-A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode Register 2	0^{*1}	1	0	0^{*1}			Rtt WR		0^{*1}	SRT	ASR	CWL			PASR		

A10	A9	RTT_WR*2
0	0	Dynamic ODT off (write does not affect Rtt value)
0	1	RZQ/4
1	0	RZQ/2
1	1	Reserved

A7	Self refresh temperature (SRT) range
0	Normal temp. range
1	Extended temp. Range

A6	Auto self refresh
0	Manual SR reference
1	ASR enable (optional)

A2	A1	A0	Partial array self-refresh (optional)
0	0	0	Full array
0	0	1	Half array (BA[2:0]=000,001,010 & 011)
0	1	0	Quarter array (BA2[2:0]=000 & 001)
0	1	1	1/8th array (BA[2:0]=000)
1	0	0	3/4 array (BA[2:0] = 010, 011, 100, 101, 110 &111)
1	0	1	Half array (BA[2:0]=100,101,110 & 111)
1	1	0	Quarter array (BA2[2:0]=000 & 001)
1	1	1	1/8th array (BA[2:0]=000)

BA1	BA0	MR select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A5	A4	A3	CAS write latency (CWL)
0	0	0	5 (tCK(avg) ≥ 2,5ns)
0	0	1	6 (2,5ns > tCK(avg) ≥ 1,875ns)
0	1	0	7 (1,875ns > tCK(avg) ≥ 1,5ns)
0	1	1	8 (1,5ns > tCK(avg) ≥ 1,25ns)
1	0	0	9 (1,25ns > tCK(avg) ≥ 1,07ns)
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Notes:

***1**. BA2, A14~A11 and A8 are reserved for future use and must be programmed to 0 during MRS,

***2**. the Rtt_WR value can be applied during writes even when Rtt_Nom is disabled.

During write leveling, Dynamic ODT is not available

Partial Array self-refresh

DDR3 SDRAM is capable of providing two different Optional in DDR3 SDRAM: Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material. If PASR (Partial Array Self-Refresh) is enabled, data located in areas of the array beyond the specified address range will be lost if Self-Refresh is entered. Data integrity will be maintained if t_{REFI} conditions are met and no Self-Refresh command is issued.

CAS Write Latency

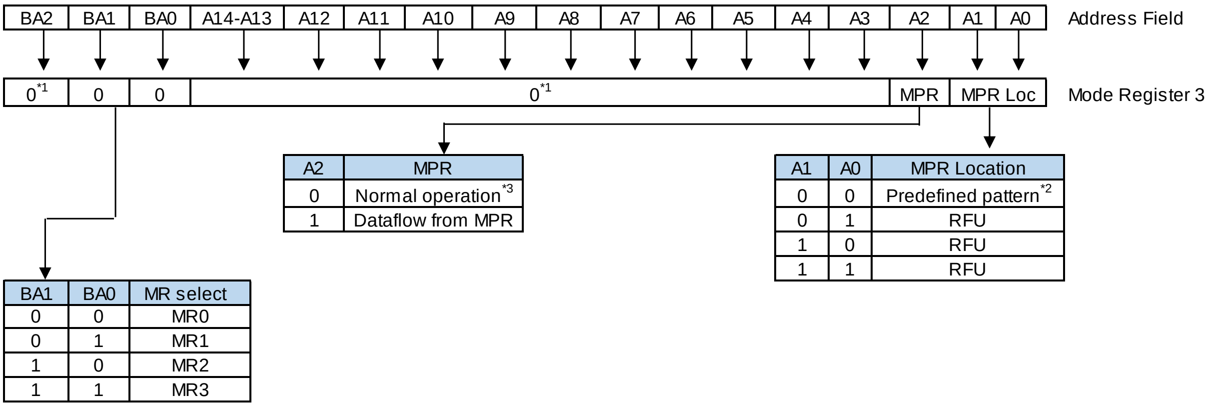
The CAS Write Latency is defined by MR2 (bits A3-A5). CAS Write Latency is the delay, in clock cycles, between the internal Write command and the availability of the first bit of input data. DDR3 SDRAM does not support any half-clock latencies. The overall Write Latency (WL) is defined as Additive Latency (AL) + CAS Write Latency (CWL); WL = AL + CWL.

Dynamic ODT (Rtt_WR)

DDR3 SDRAM introduces a new feature “Dynamic ODT”. In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command. MR2 Register locations A9 and A10 configure the Dynamic ODT setings. In Write leveling mode, only RTT_Nom is available

Mode Register MR3

The Mode Register MR3 controls Multi purpose registers. The Mode Register 3 is written by asserting low on CS#, RAS#, CAS#, WE#, high on BA1 and BA0, and low on BA2 while controlling the states of address pins according to the table below.



A2	MPR
0	Normal operation[*3]
1	Dataflow from MPR

A1	A0	MPR Location
0	0	Predefined pattern[*2]
0	1	RFU
1	0	RFU
1	1	RFU

BA1	BA0	MR select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

Notes:

*1. BA2, A14~A3 are reserved for future use and must be programmed to 0 during MRS.

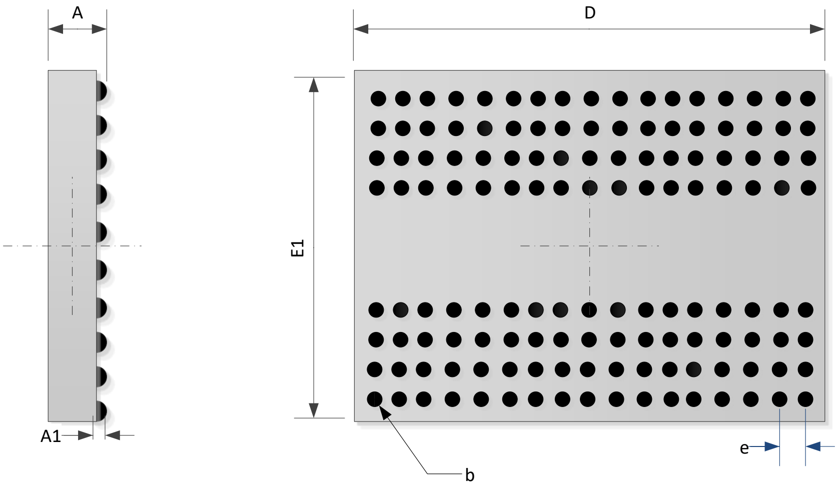
***2**. The predefined control pattern will be used for read synchronization.

***3**. When MPR control is set for normal operation, MR3 A[2] then MR3 A[1:0] will be ignored.

Multi purpose Register (MPR)

The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence. To enable the MPR, a MODE Register Set (MRS) command must be issued to MR3 Register with bit A2 = 1. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP met). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi Purpose Register. When the MPR is enabled, only RD or RDA commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3 bit A2 = 0). Power-Down mode, Self-Refresh, and any other non-RD/RDA command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode

MECHANICAL DRAWING



REF.	Dimensions in mm	
	Min	Max
A	1.00	1.20
A1	0.30	0.38
b	0.40	0.50
D	13.90	14.10
E1	11.90	12.10
e	0.80 BSC	

ORDERING INFORMATION

Part Number	Voltage (V)	Case Temperature range (°C)	Package	Description
3D3D8G32WB1741 IB	1.5	-40°C to +85°C	BGA 136 with SAC302 balls	DDR3 8Gb x32 Industrial temperature RoHs balls
3D3D8G32YB1741 IB	1.35			
3D3D8G32WB1741 IB 00L	1.5		BGA 136 with Sn63Pb37 balls	DDR3 8Gb x32 Specific temperature SnPb balls
3D3D8G32YB1741 IB 00L	1.35			
3D3D8G32WB1741 SB	1.5	-40°C to +95°C	BGA 136 with SAC302 balls	DDR3 8Gb x32 Specific temperature RoHs balls
3D3D8G32YB1741 SB	1.35			
3D3D8G32WB1741 SB 00L	1.5		BGA 136 with Sn63Pb37 balls	DDR3 8Gb x32 Specific temperature SnPb balls
3D3D8G32YB1741 SB 00L	1.35			
3D3D8G32WB1741 MB	1.5	-55°C to +125°C	BGA 136 with SAC302 balls	DDR3 8Gb x32 Military temperature RoHs balls
3D3D8G32YB1741 MB	1.35			
3D3D8G32WB1741 MB 00L	1.5		BGA 136 with Sn63Pb37 balls	DDR3 8Gb x32 Military temperature SnPb balls
3D3D8G32YB1741 MB 00L	1.35			

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