Signetics

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Status	Product Specification
FAST Products	

FAST 74F579 Counter

8-Bit Bidirectional Binary Counter (3-state)

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F579	115MHz	100mA

FEATURES

- **Fully synchronous operation**
- **Multiplexed 3-state I/O ports for bus oriented applications**
- **Built in cascading carry capability**
- **U/$\overline{D}$ pin to control direction of counting**
- **Separate pins for Master Reset and Synchronous operation**
- **Center power pins to reduce effects of package inductance**
- **Count frequency 115MHz typ**
- **Supply current 100mA typ**
- **See 'F269 for 24 pin separate I/O port version**
- **See 'F779 for 16 pin version**

DESCRIPTION

The 74F579 is a fully synchronous 8-stage Up/Down Counter with multiplexed 3-state I/O ports for bus-oriented applications. It features a preset capability for programmable operation, carry look-ahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, except for the case of asynchronous reset, are initiated by the rising edge of the clock. $\overline{TC}$ output is not recommended for use as a clock or asynchronous reset due to the possibility of decoding spikes.

ORDERING INFORMATION

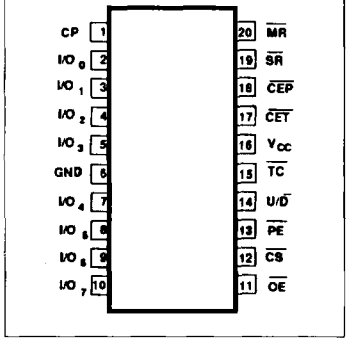
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic Dip	N74F579N
20-Pin Plastic SOL	N74F579D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

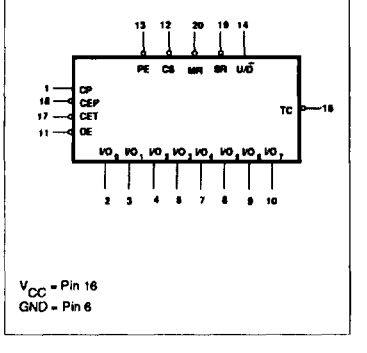
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I/O_n	Data inputs	3.5/1.0	70μA/0.6mA
	Data outputs	150/40	3.0mA/24mA
$\overline{PE}$	Parallel Enable input (active Low)	1.0/1.0	20μA/0.6mA
U/$\overline{D}$	Up/Down count control input	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Master Reset input (active Low)	1.0/1.0	20μA/0.6mA
$\overline{SR}$	Synchronous Reset input (active Low)	1.0/1.0	20μA/0.6mA
$\overline{CEP}$	Count Enable Parallel input (active Low)	1.0/1.0	20μA/0.6mA
$\overline{CET}$	Count Enable Trickle input (active Low)	1.0/1.0	20μA/0.6mA
$\overline{CS}$	Chip Select input (active Low)	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20μA/0.6mA
CP	Clock input	1.0/1.0	20μA/0.6mA
$\overline{TC}$	Terminal count output (active Low)	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

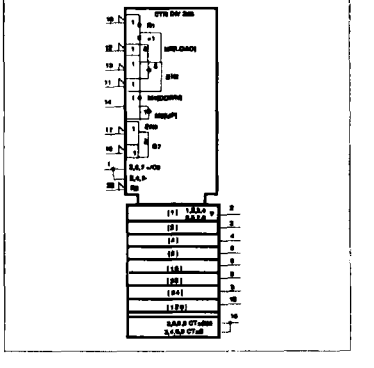
PIN CONFIGURATION



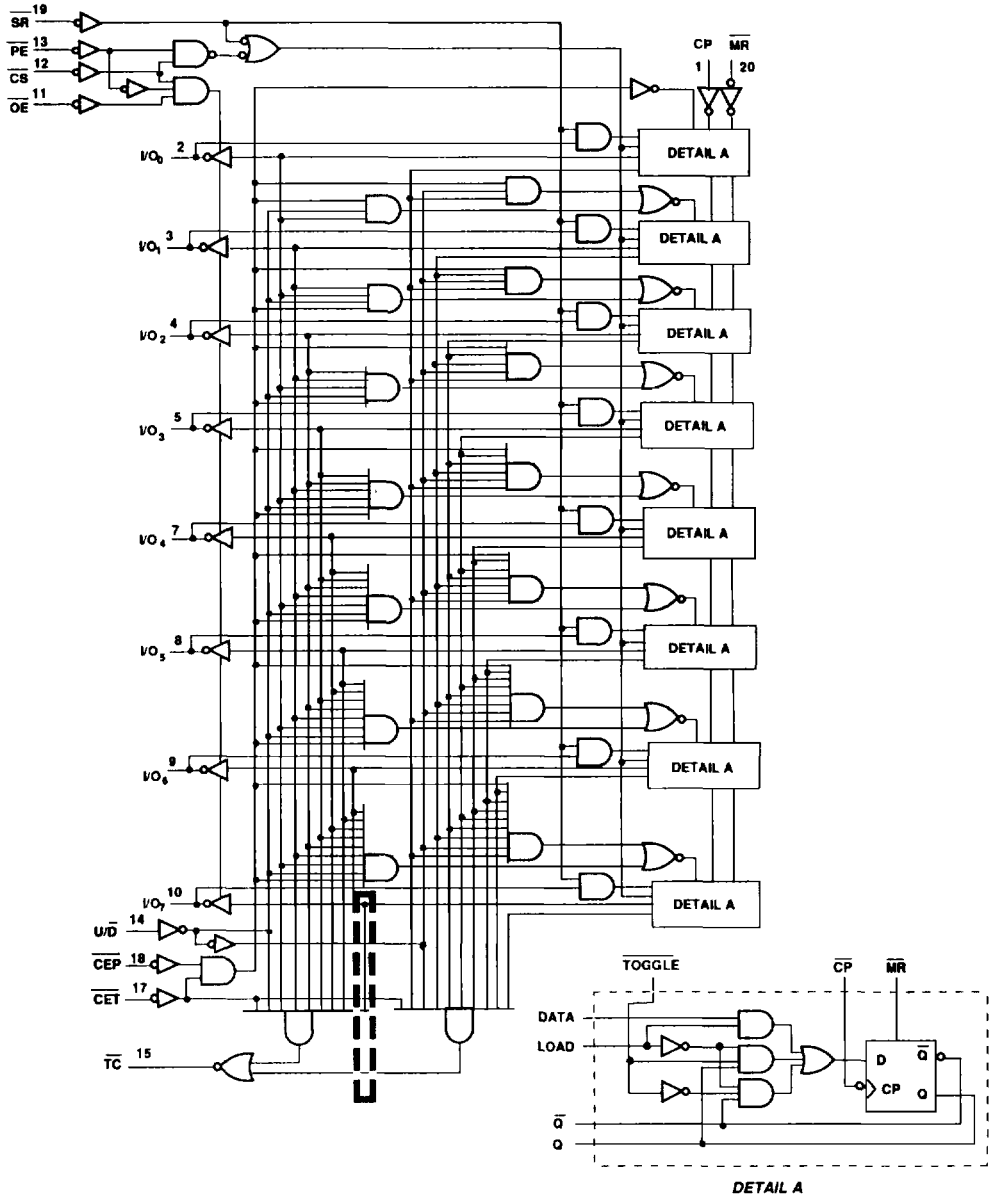
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



V_{CC} =pin16
GND=pin 6

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	115		80		MHz
t_{PLH} t_{PHL}	Propagation delay CP to I/O_n	Waveform 1	5.0 5.0	7.5 7.5	10.5 10.5	5.0 5.0	11.5 11.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$	Waveform 1	5.5 5.5	7.5 7.5	10.0 10.0	5.0 5.0	11.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ to $\overline{TC}$	Waveform 4	3.5 4.5	5.5 6.5	8.0 8.0	3.5 4.5	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$	Waveform 3	3.5 3.5	5.5 6.0	7.0 8.0	3.5 3.5	8.5 8.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to I/O_n	Waveform 2	5.0	7.0	9.0	5.0	10.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{CS}$ to I/O_n	Waveform 6 Waveform 7	4.0 5.5	5.0 7.0	8.5 10.5	3.5 5.0	10.0 11.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{CS}$ to I/O_n	Waveform 6 Waveform 7	3.0 5.0	5.0 7.5	7.5 9.5	3.0 4.5	9.0 11.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{PE}$ to I/O_n	Waveform 6 Waveform 7	3.0 5.0	4.5 6.5	8.0 10.0	3.0 4.5	9.0 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{PE}$ to I/O_n	Waveform 6 Waveform 7	3.0 2.5	4.0 4.0	7.5 7.5	3.0 2.0	9.0 8.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to I/O_n	Waveform 6 Waveform 7	2.5 4.5	4.0 5.5	7.0 9.0	2.5 4.0	8.5 10.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to I/O_n	Waveform 6 Waveform 7	1.0 2.0	2.5 4.0	4.0 7.0	1.0 2.0	5.5 8.0	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low I/O_n to CP	Waveform 5	3.0 3.0			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I/O_n to CP	Waveform 5	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $U/\overline{D}$ to CP	Waveform 5	8.0 8.0			9.0 9.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $U/\overline{D}$ to CP	Waveform 5	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$, $\overline{SR}$ or $\overline{CS}$ to CP	Waveform 5	9.5 9.5			10.0 10.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$, $\overline{SR}$ or $\overline{CS}$ to CP	Waveform 5	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP	Waveform 5	5.0 9.0			5.5 10.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I/O_n to CP	Waveform 5	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	4.5 4.5			4.5 4.5		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 2	3.0			3.0		ns
t_{REC}	Recovery time, $\overline{MR}$ to CP	Waveform 2	4.0			4.5		ns