

HD74LS91 8-bit Shift Registers

This serial-in, serial-out, 8-bit shift register is composed of eight R-S master-slave flip-flops, input gating, and a clock drive. Single-rail data and input control are gated through inputs A and B and an internal inverter to form the complementary inputs to the first bit of the shift register. Drive for the internal common clock line is provided by an inverting clock driver. This clock pulse inverter/driver causes these circuits to shift information one bit on the positive edge of an input clock pulse.

FUNCTION TABLE

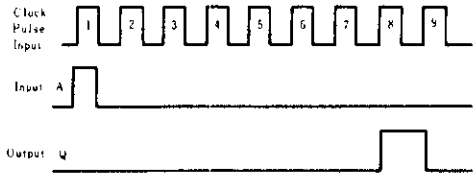
Inputs		Outputs	
t_n		t_{n+8}	
A	B	Q_H	$\bar{Q}_H$
H	H	H	L
L	X	L	H
X	L	L	H

Notes) H; high level, L; low level, X; irrelevant
 t_n ; Reference bit time, clock low
 t_{n+8} ; Bit time after 8 low-to-high clock transitions.

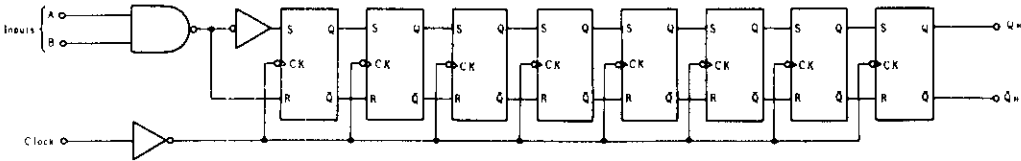
RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	max	Unit
Clock pulse width	t_w	25	—	ns
Setup time	t_{su}	25	—	ns
Hold time	t_h	5	—	ns

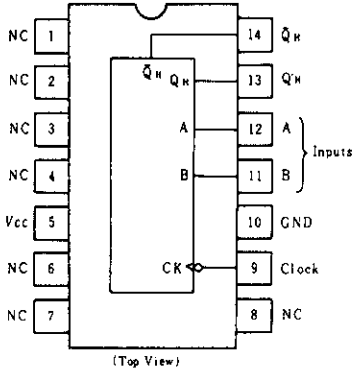
TIMING CHART



BLOCK DIAGRAM



PIN ARRANGEMENT



■ ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^\circ\text{C}$)

Item	Symbol	Test Conditions	min	typ*	max	Unit
Input voltage	V_{IH}		2.0		—	V
	V_{IL}		—	—	0.8	V
Output voltage	V_{OH}	$V_{CC} = 4.75\text{V}$, $V_{IH} = 2\text{V}$, $V_{IL} = 0.8\text{V}$, $I_{OH} = -400\mu\text{A}$	2.7		—	V
	V_{OL}	$V_{CC} = 4.75\text{V}$, $V_{IH} = 2\text{V}$, $V_{IL} = 0.8\text{V}$	—	—	0.4	V
					0.5	
Input current	I_{IH}	$V_{CC} = 5.25\text{V}$, $V_I = 2.7\text{V}$	—	—	20	μA
	I_{IL}	$V_{CC} = 5.25\text{V}$, $V_I = 0.4\text{V}$	—	—	0.4	mA
	I_I	$V_{CC} = 5.25\text{V}$, $V_I = 7\text{V}$	—	—	0.1	mA
Short circuit output current	I_{OS}	$V_{CC} = 5.25\text{V}$	-20	—	-100	mA
Supply current	I_{CC}^{**}	$V_{CC} = 5.25\text{V}$	—	12	20	mA
Input clamp voltage	V_{IK}	$V_{CC} = 4.75\text{V}$, $I_{IS} = 18\text{mA}$	—	—	-1.5	V

* $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$

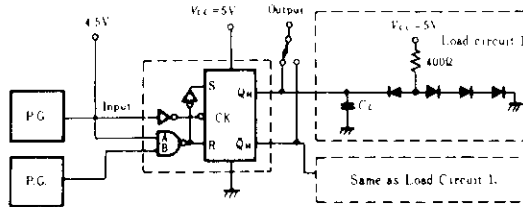
** I_{CC} is measured after the eighth clock pulse with the output open and A and B inputs grounded.

■ SWITCHING CHARACTERISTICS ($V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$)

Item	Symbol	Test Conditions	min	typ	max	Unit
Maximum clock frequency	f_{max}		10	18	—	MHz
Propagation delay time	t_{PLH}	$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$	—	24	40	ns
	t_{PHL}		—	27	40	ns

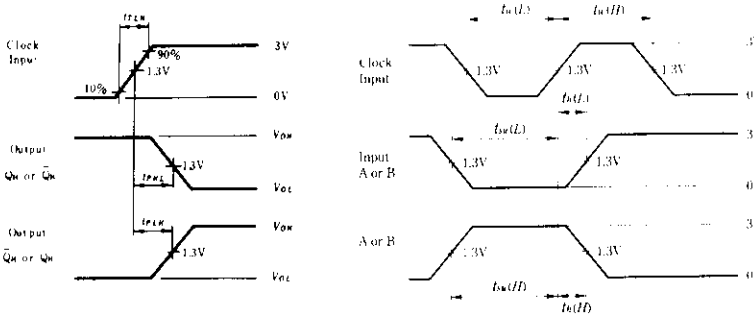
■ TESTING METHOD

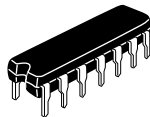
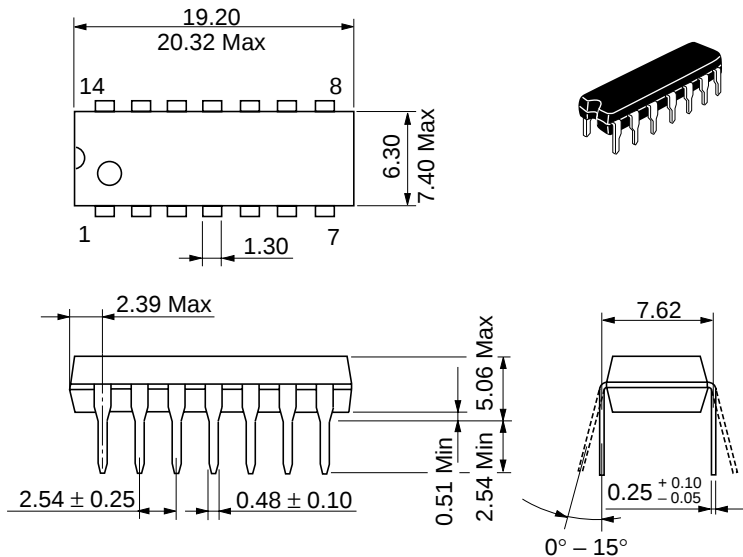
1) Test Circuit



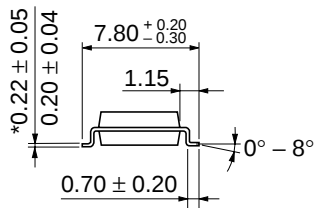
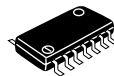
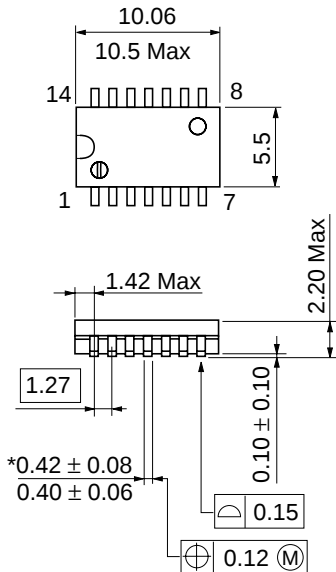
- Notes) 1. Input pulse: $t_{TLH} \leq 15\text{ns}$, $t_{THL} \leq 6\text{ns}$, $PRR = 1\text{MHz}$, duty cycle=50%
 2. C_L includes probe and jig capacitance.
 3. All diodes are 1S2074 Φ .

Waveform



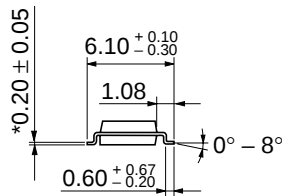
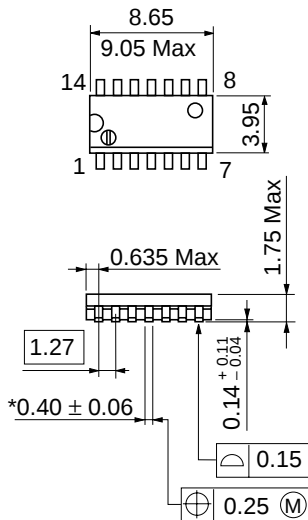


Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.97 g



Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.23 g

*Dimension including the plating thickness
Base material dimension



Hitachi Code	FP-14DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.13 g

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