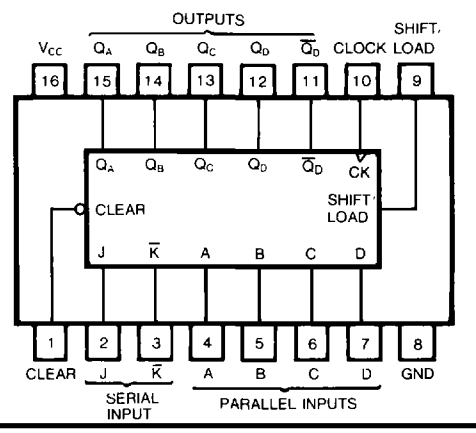
GD54/74LS195A

4-BIT PARALLEL ACCESS SHIFT REGISTERS

Features

- Synchronous parallel load
- Positive-edge-triggered clocking
- Parallel inputs and outputs from each flip-flop
- Direct overriding clear
- J and $\overline{K}$ inputs to first stage
- Complementary outputs from last stage
- For use in high-performance.
  accumulators/processors
  serial-to-parallel, parallel-to-serial converters
- Typical clock frequecy 39 MHz
- Typical power dissipation 70mW

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

General Description

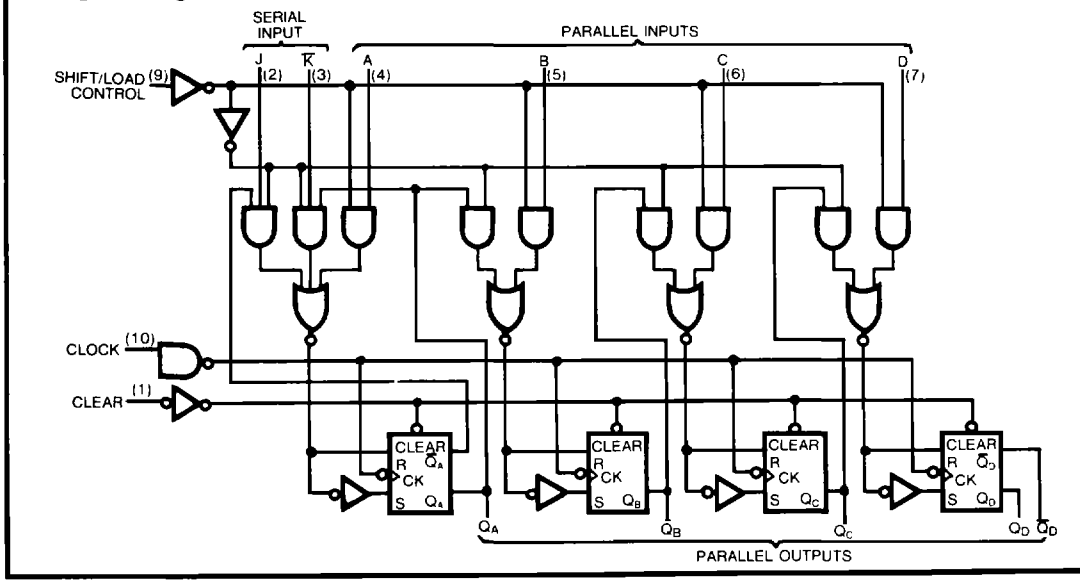
These 4-bit registers feature parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The registers have two modes of operation:

Parallel (broadside) load
Shift (in the direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, D, or T-type flip-flop as shown in the function table.

Logic Diagram



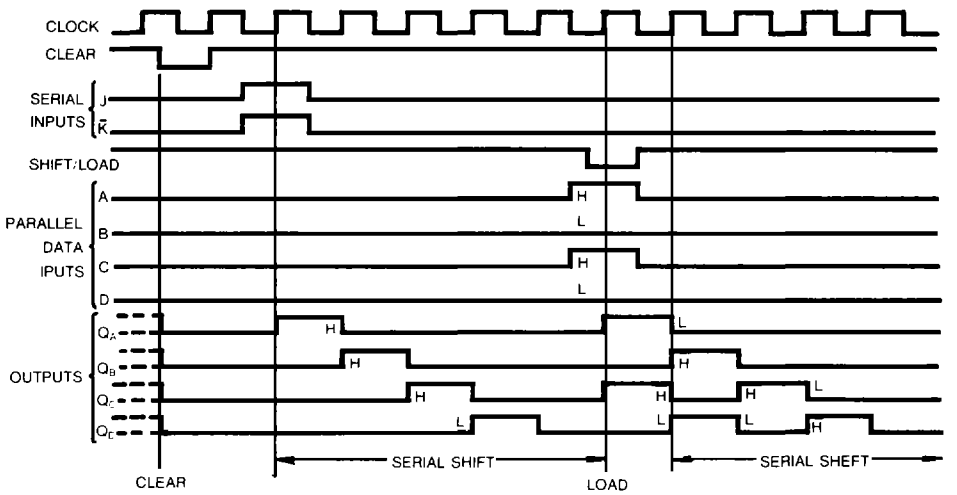
Function Table

Inputs									Outputs				
Clear	Shift/ Load	Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	d
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	Q_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H=High Level (steady state) L=Low Level (steady state), X=Don't Care (any input, including transitions)
↑=Transition from low to high level
a,b,c,d=The level of steady state input at A, B, C or D, respectively
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0}=The level of Q_A, Q_B, Q_C or Q_D respectively, before the indicated steady state input conditions were established
Q_{An}, Q_{Bn}, Q_{Cn}= The level of Q_C, Q_B, Q_C, respectively, before the most recent transition of the clock

Timing Diagram

TYPICAL CLEAR, SHIFT, AND LOAD SEQUENCES



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54, 74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
f_{clock}	Clock frequency		0		30	MHz
t_w	Pulse Width	Clock	16			ns
		Clear	12			
t_{su}	Setup Time	Shift/Load	25			ns
		Data	15			
t_H	Hold Time		0			ns
t_{REL}	Shift/Load Release Time		10			ns
	Clear Release Time		25			
T_A	Operatig free-air teperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IL}=Max, I_{OH}=Max, V_{IH}=Min		54	2.5	3.4		V
				74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54, 74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input curret at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=Max (Note 3)				14	21	mA

Note 1 All typical values are at V_{CC}=5V, T_A=25°C
Note 2 Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second
Note3 With all outputs open, SHIFT/LOAD grounded, and 4 5V applied to the J, $\overline{K}$, and data inputs, I_{CC} is measured by applying a momentary ground then 4 5V to the CLEAR and then applying a momentary ground then 4 5V to the CLOCK

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

SYMBOL	PARAETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency		30	39		MHz
t_{PHL}	Propagation delay time, high-to-low-level Q outputs from clear input	$C_L=15pF$, $R_L=2k\Omega$		19	30	ns
t_{PLH}	Propagation delay time, low-to-high-level Q outputs from clock input			14	22	ns
t_{PHL}	Propagation delay time, high-to low-level Q outputs from clock input			17	26	ns

#For load circuit and voltage waveforms, see page 3-11.