GEC PLESSEY

SEMICONDUCTORS

SL2521B

1.3GHz DUAL WIDEBAND LOGARITHMIC AMPLIFIER

(NOT RECOMMENDED FOR NEW DESIGNS – TO BE REPLACED BY SL2524)

The SL2521 is a revolutionary monolithic integrated circuit designed on an advanced 3 micron oxide isolated bipolar process. The amplifier is a successive detection type which provides linear gain and accurate logarithmic signal compression over a wide bandwidth.

When six stages (three SL2521s) are cascaded the strip can be used for IFs between 30-650MHz whilst achieving greater than 65dB dynamic range with a log accuracy of $<\pm1.0$dB. The balanced limited output also offers accurate phase information with input amplitude. One log strip therefore offers limited IF output, phase and video information.

The device is also available as the SL2522BC which has guaranteed operation over the full Military Temperature Range and is screened to MIL-STD-883C Class B. Data is available separately.

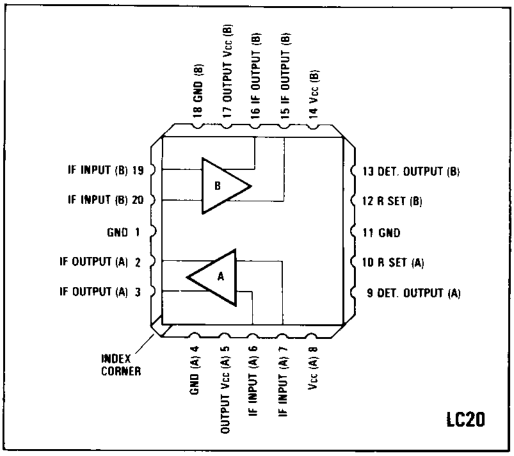

Fig.1 Pin connections - top view

FEATURES

- 1.3GHz Bandwidth (-3dB)
- Balanced IF Limiting
- 3ns Rise Times/5ns Fall Times (Six Stages)
- 20ns Pulse Handling (Six Stages)
- Temperature Stabilised
- Full Military Temperature Range/Surface Mountable

APPLICATIONS

- Ultra Wideband Log Receivers
- Channelised Receivers
- Monopulse Applications

ORDERING INFORMATION

SL2521 B LC
Military version available:
SL2522 AC LC
SL2522 BC LC

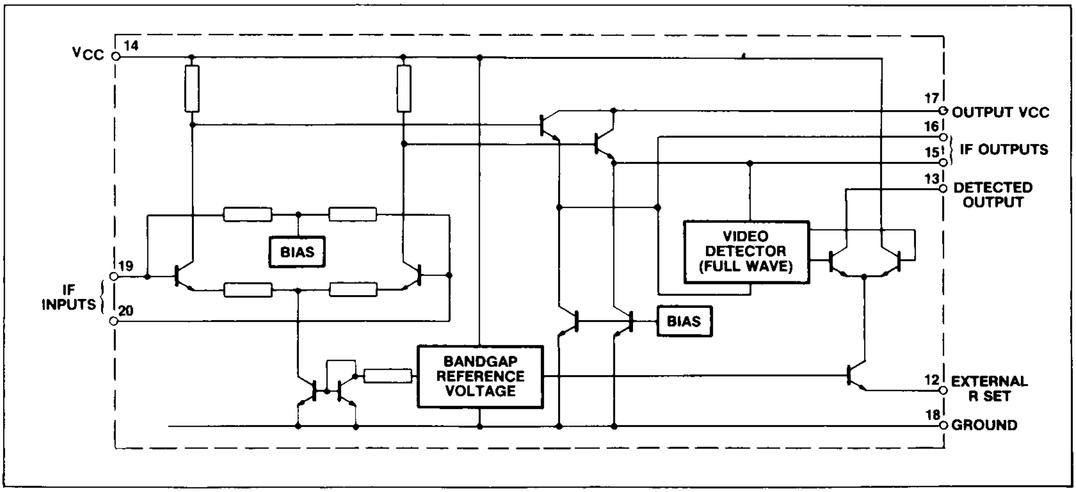

Fig.2 Circuit diagram (single stage B only)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Frequency = 200MHz, T_{amb} = -30°C to +85°C, Input voltage = -30dBm, V_{CC} = 6V ± 0.1V, Source Impedance = 50Ω, Test Circuit = Fig.3, R_{set} = 300Ω. Tested as a dual stage.

Characteristics	Value						Units	Conditions	Notes
	50Ω Load			1kΩ Load					
	Min.	Typ.	Max.	Min.	Typ.	Max.			
Small signal gain (dual stage, single ended)	9.2	10.7	12.2	14.8	16.5	18.3	dB	T_{amb} = -30°C frequency = 200MHz	2
	9.8	11.0	12.2	15.8	17.0	18.2	dB	T_{amb} = +25°C frequency = 200MHz	
	9.7	11.2	12.4	15.8	17.3	18.8	dB	T_{amb} = +85°C frequency = 200MHz	2
	9.9	11.5	13.2	16.1	18.1	20.1	dB	T_{amb} = -30°C frequency = 500MHz	2
	10.2	11.4	12.7	16.3	18.0	19.8	dB	T_{amb} = +25°C frequency = 500MHz	
	9.7	11.2	12.7	15.6	17.6	19.6	dB	T_{amb} = +85°C frequency = 500MHz	2
Detected output current (max)	3.05	3.25	3.45	3.20	3.45	3.70	mA	T_{amb} = -30°C,V_{in} = 0dBm,f = 200MHz	2
	3.15	3.3	3.45	3.30	3.5	3.70	mA	T_{amb} = +25°C,V_{in} = 0dBm,f = 200MHz	
	3.10	3.3	3.50	3.30	3.55	3.80	mA	T_{amb} = +85°C,V_{in} = 0dBm,f = 200MHz	2
	2.8	3	3.2	2.8	3	3.2	mA	T_{amb} = -30°C,V_{in} = 0dBm,f = 500MHz	2
	2.9	3.05	3.45	2.8	3	3.2	mA	T_{amb} = +25°C,V_{in} = 0dBm,f = 500MHz	
	2.85	3.03	3.65	2.8	3	3.2	mA	T_{amb} = +85°C,V_{in} = 0dBm,f = 500MHz	2
Detected output current (no signal)				0.9	1.1	1.3	mA	T_{amb} = -30°C	2
				0.95	1.1	1.25	mA	T_{amb} = +25°C	
				0.9	1.1	1.3	mA	T_{amb} = +85°C	2
Upper cut off frequency (RF)				900	1100		MHz	-3dB w.r.t. 200MHz,T_{amb} = +25°C	1
Lower cut off frequency (RF)					0.35	1	MHz		
Detector cut off frequency					700		MHz	50% O/P current w.r.t. 200MHz	
Limited IF O/P voltage				105	120	145	mV	I/P voltage = 0dBm,T_{amb} = +25°C	
Phase variation with input level (normalised to -30dBm)		±2	±6				Degree	Frequency = 70MHz, -55 to +3dBm	
		±2	±6				Degree	Frequency = 200MHz, -55 to +3dBm	
Limited O/P var with temp.		±12	±25				mV		
Noise figure		12			9		dB		
Max I/P before overload					15		dBm		
Input impedance					1		kΩ	1kΩ in parallel with 2pF	
Output impedance					40		Ω		
Supply current			90		75	90	mA		
Variation of max detected current with V_{CC}					5		%/V	T_{amb} = +25°C	
Variation of small signal gain with V_{CC}					0.5		dB/V	T_{amb} = +25°C	

NOTES
1. Parameter guaranteed but not tested.
2. Tested at 25°C only, but guaranteed at temperature.

GENERAL DESCRIPTION

The SL2521 is primarily intended for use in Radar and EW receivers. Six stages (3 chip carriers) can be cascaded to form a very wideband logarithmic amplifier offering >65dB of input dynamic range, with pulse handling of better than 25ns. (See Figs.4 and 5.)

A six stage strip also offers balanced IF limiting, linearity (log accuracy) of <±1.0dB, temperature stabilisation and programmable detector characteristics.

The detector has an external resistor set pin which allows the major characteristics of the detector to be programmed. With a six stage strip it is possible to vary the value of R_{set} on each detector and so improve the overall log error/linearity.

The detector is full wave and good slew rates are achieved with 2ns rise and 5ns fall times (no video filter). The video bandwidth for a six stage strip is typically 600MHz (-3dB).

The amplifier also offers balanced IF limiting, low phase shift versus input amplitude, and at an IF of 120MHz, less than 7° of phase change is achievable over the input level of -55dBm to +5dBm.

The IF and Video ports can be used simultaneously so offering phase, frequency and pulse (video) information. A slight loss of dynamic range (2dB) will be observed when the IF ports are used in conjunction with the video.

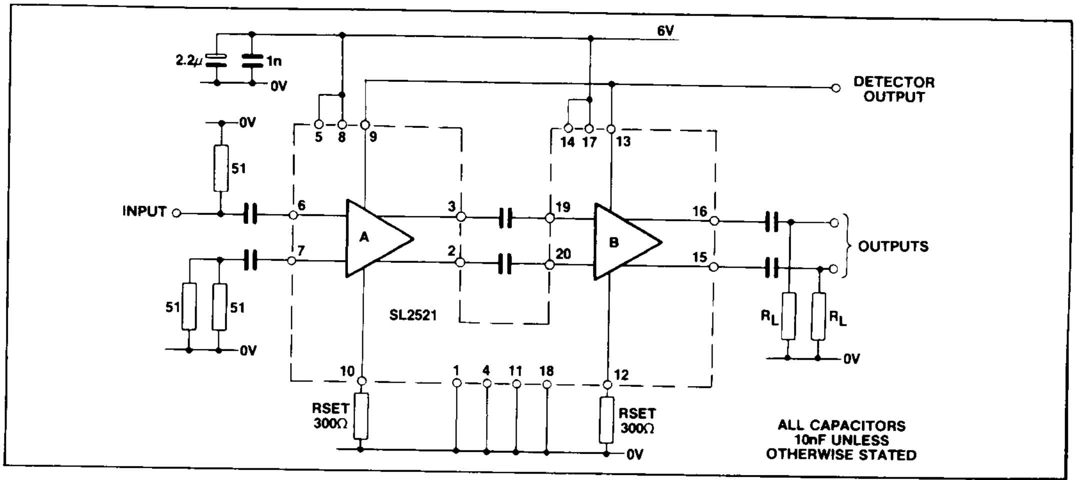

Fig.3 Test circuit

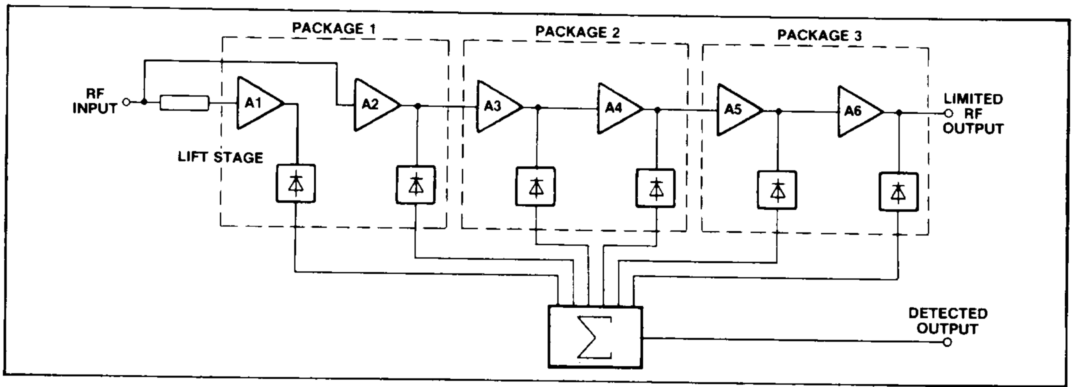

Fig.4 Schematic diagram showing configuration of SD amplifier

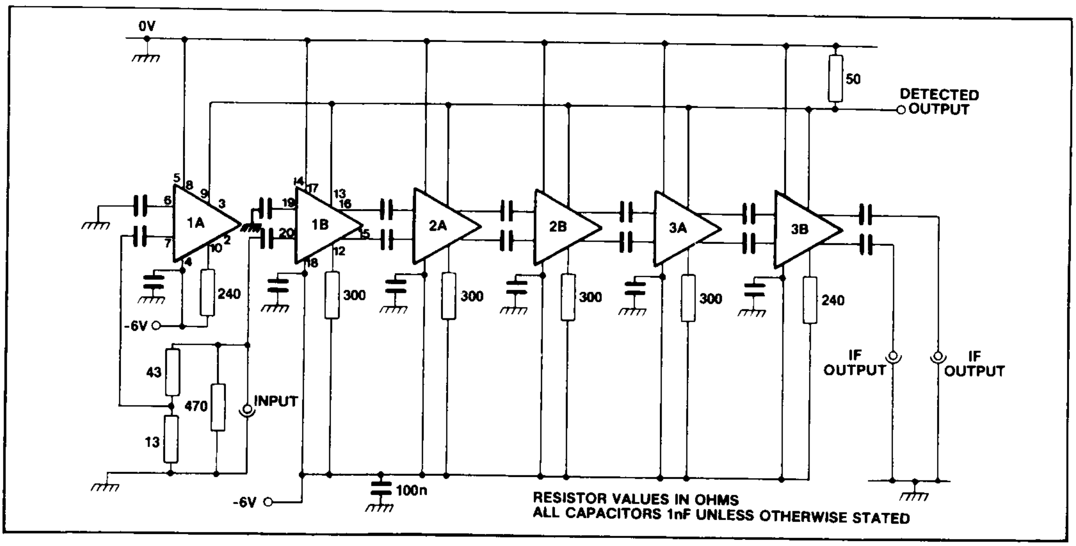

Fig. 5 Circuit diagram for 6-stage log strip (results shown in Figs. 18 to 35 were achieved with this circuit)

TYPICAL CHARACTERISTICS FOR A DUAL STAGE AMPLIFIER (i.e. 1 SL2521)

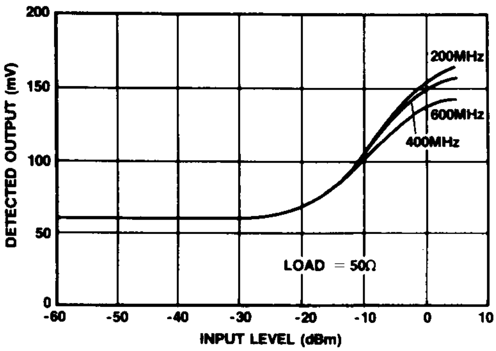

Fig.6 Detected O/P Vs input level at 200,400,600MHz for R_L = 50Ω

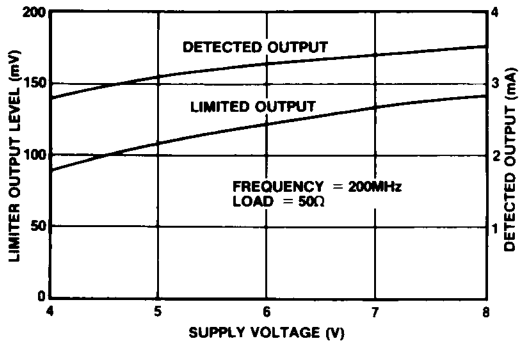

Fig.7 Output levels Vs supply voltage

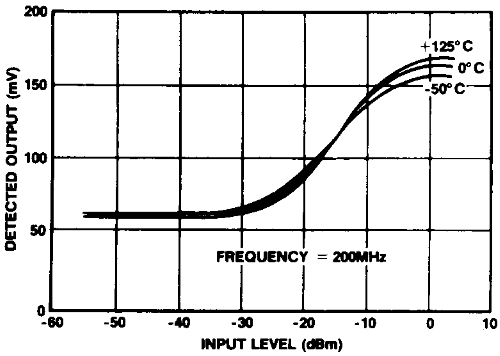

Fig.8 Detected output Vs input level and temperature

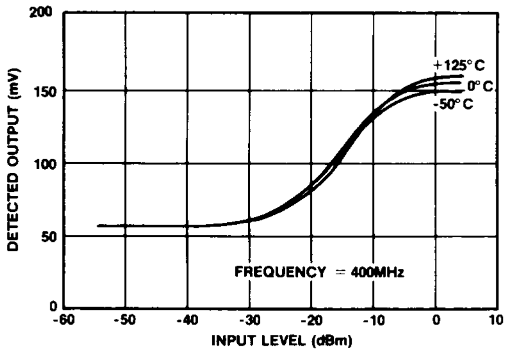

Fig.9 Detected output Vs input level and temperature

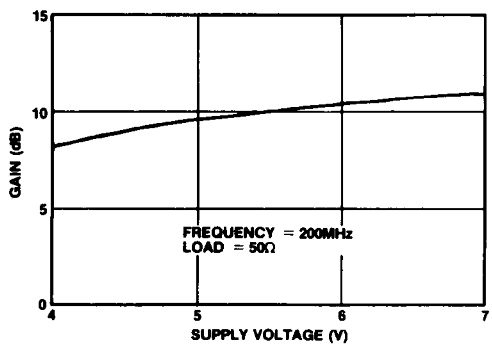

Fig.10 Gain Vs supply voltage

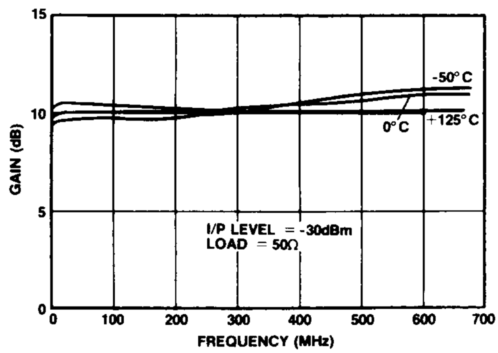

Fig.11 Gain Vs frequency of 2 amplifiers (1 SL2521)

TYPICAL CHARACTERISTICS FOR A DUAL STAGE AMPLIFIER

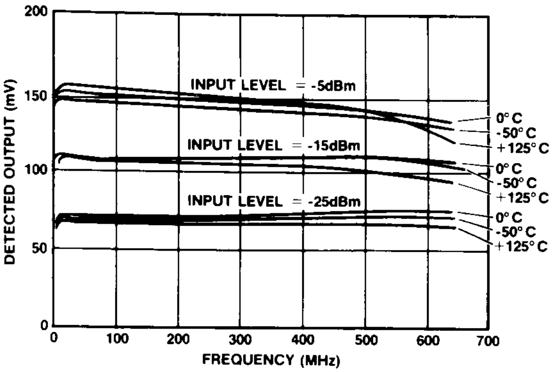

Fig.12 Detected output level Vs frequency and temperature

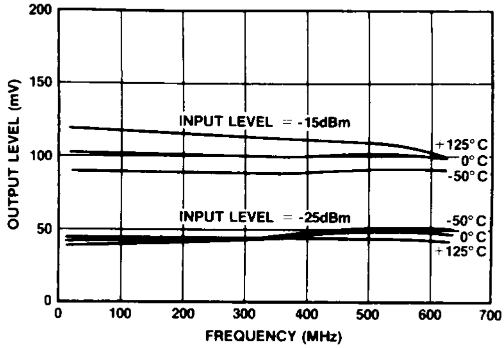

Fig.13 Limited output level Vs frequency and temperature

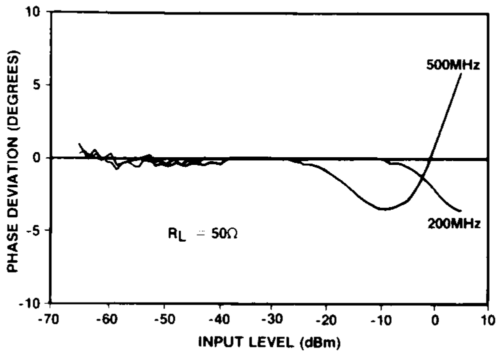

Fig.14 Normalised phase Vs input level at 200 and 500MHz for R_L = 50Ω

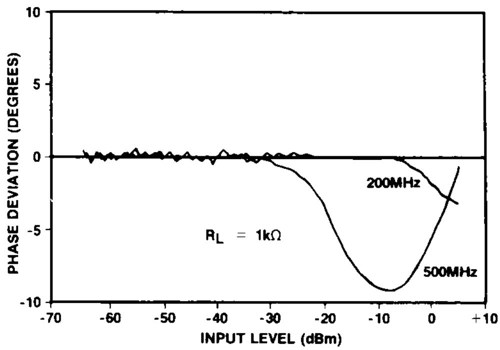

Fig.15 Normalised phase Vs input level at 200 and 500MHz for R_L = 1kΩ

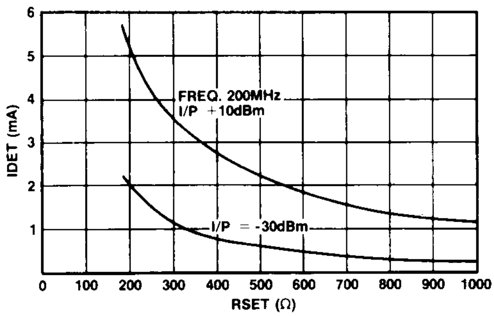

Fig.16 Detector current Vs R_{set} at 200MHz

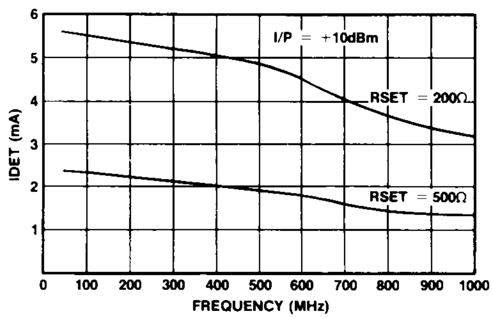

Fig.17 Detector current Vs frequency at R_{set} = 200Ω and 500Ω

TYPICAL CHARACTERISTICS FOR A SIX STAGE STRIP, USING THE VIDEO OUTPUT

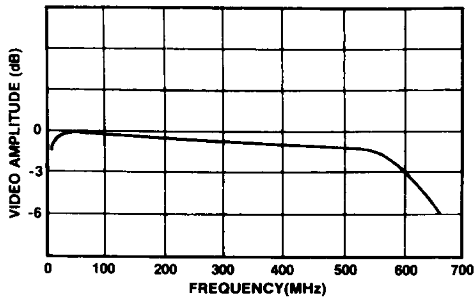

Fig.18 Video bandwidth (detector)

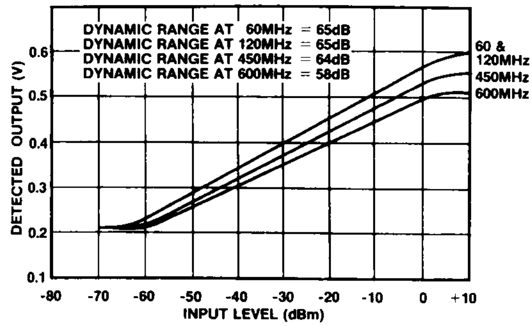

Fig.19 Video output Vs CW input at 60, 120, 450 and 600MHz at 25° C

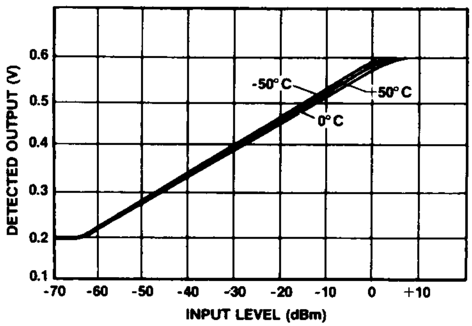

Fig.20 Detected output Vs input level and temperature at 60, 120MHz

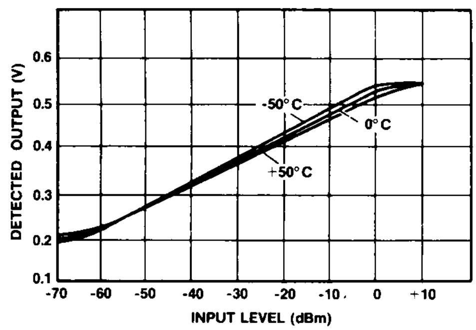

Fig.21 Detected output Vs input level and temperature at 450MHz

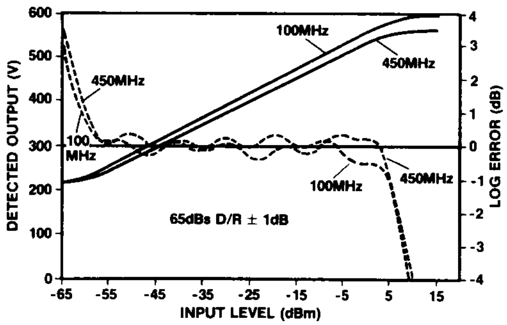

Fig.22 Detected O/P and log linearity at 450 and 100MHz

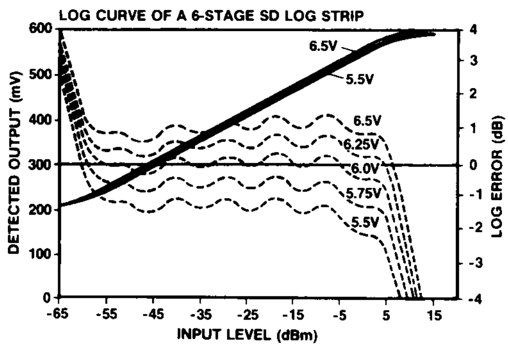

Fig.23 Logarithmic output Vs Vcc

SL2521: PULSE FIDELITY FOR A SIX STAGE STRIP

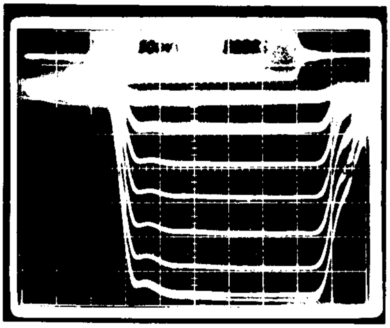

Fig.24 60ns I/P pulse. With low pass video filter. Horizontal = 10ns/div. Vertical = 50mV/div. Input level -70dBm to -10dBm

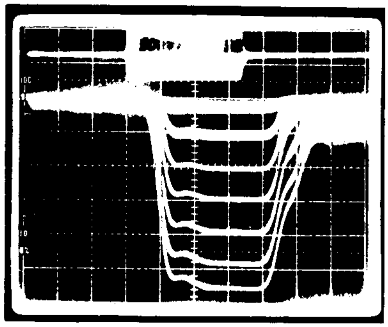

Fig.25 As Fig.25 with 35ns input pulse (Slight glitch on front edge is due to underdamping of video filter)

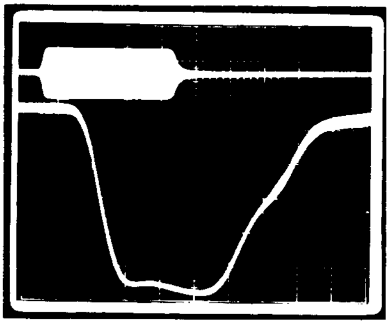

Fig.26 20ns input pulse. Showing input and output pulse with low pass video filter. Horizontal = 5ns/div. Vertical = 50mV/div; -10dBm input.

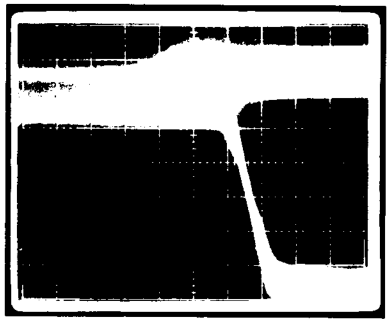

Fig.27 20ns input pulse. No video filter leading edge only. Horizontal = 2ns/div; -10dBm input level.

SL2521: LIMITING CHARACTERISTICS

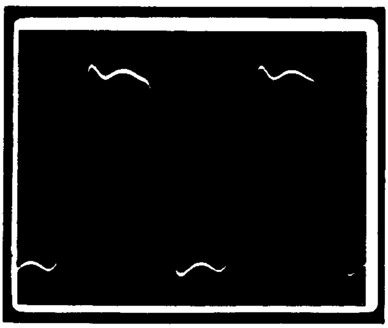

Fig.28 Hard limiting output at 200MHz with +10dBm input level

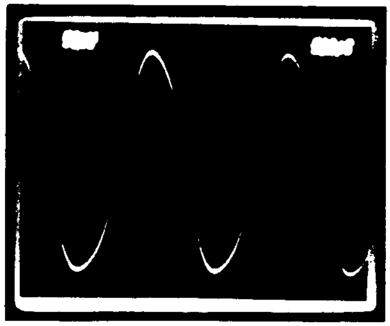

Fig.29 Hard limiting output at 500MHz with +10dBm input level

TYPICAL CHARACTERISTICS OF A SIX STAGE STRIP AS A LOW PHASE SHIFT WIDEBAND LIMITER

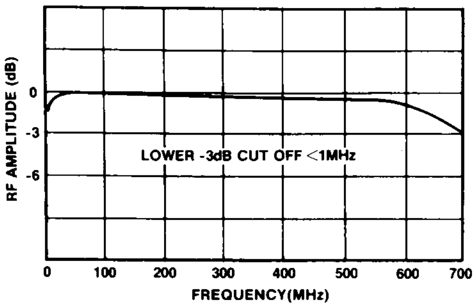

Fig.30 IF bandwidth measured from output 1. Output 2 terminated into 50Ω

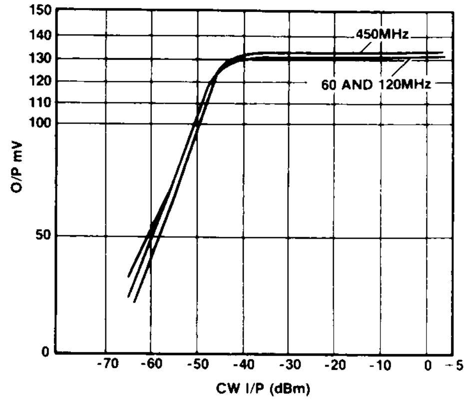

Fig.31 IF limiting characteristic at 60, 120 and 450MHz

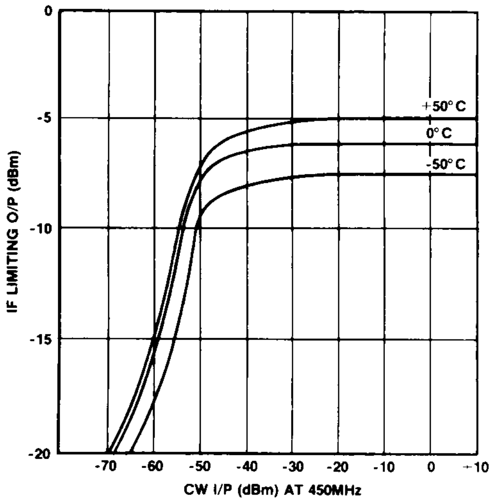

Fig.32 Limiting characteristic Vs temperature at 450MHz

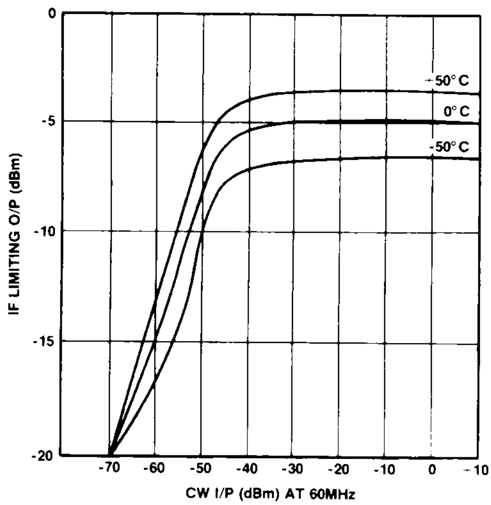

Fig.33 Limiting characteristic Vs temperature at 60MHz

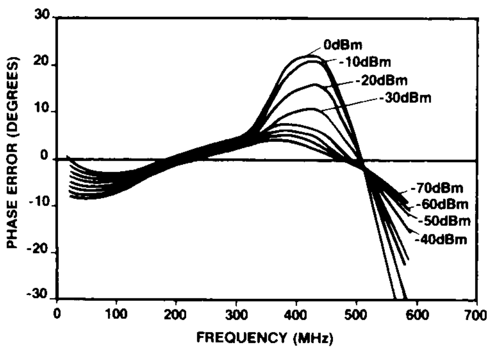

Fig.34 Departure from linear phase

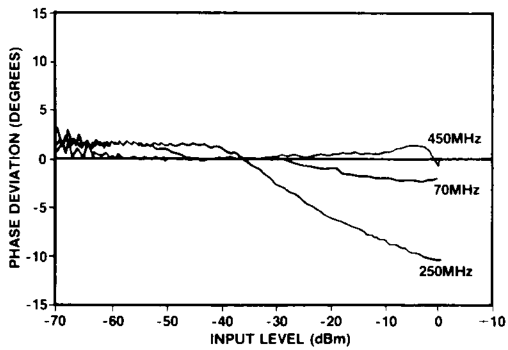

Fig.35 Normalised phase Vs input level

WIDEBAND LIMITER CHARACTERISTICS

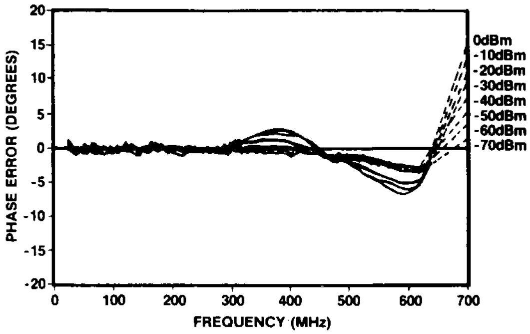

Fig.36 Phase tracking Vs frequency of two SD log strips (typical)

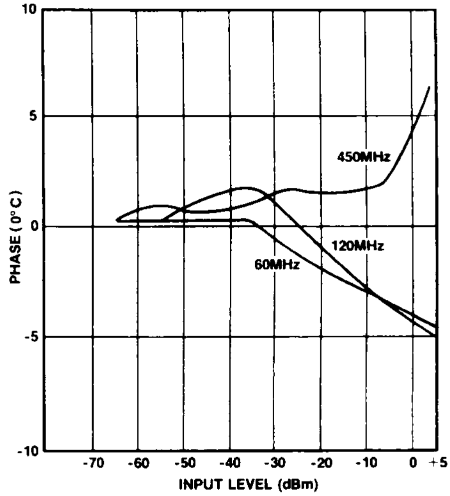

Fig.37 Phase change Vs input level at 60, 120 and 450MHz

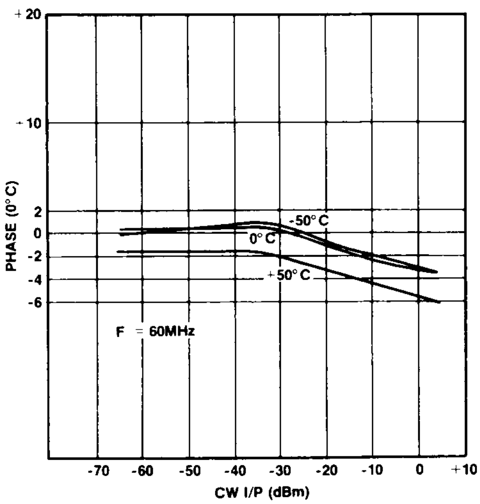

Fig.38 Phase change Vs temperature at 60MHz

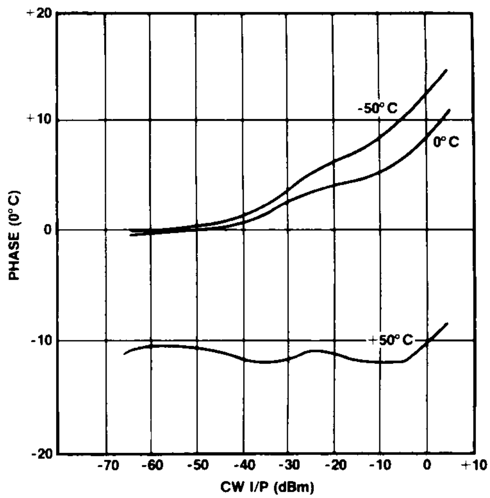

Fig.39 Phase change Vs temperature at 450MHz

IMPEDANCE OR ADMITTANCE CO-ORDINATES

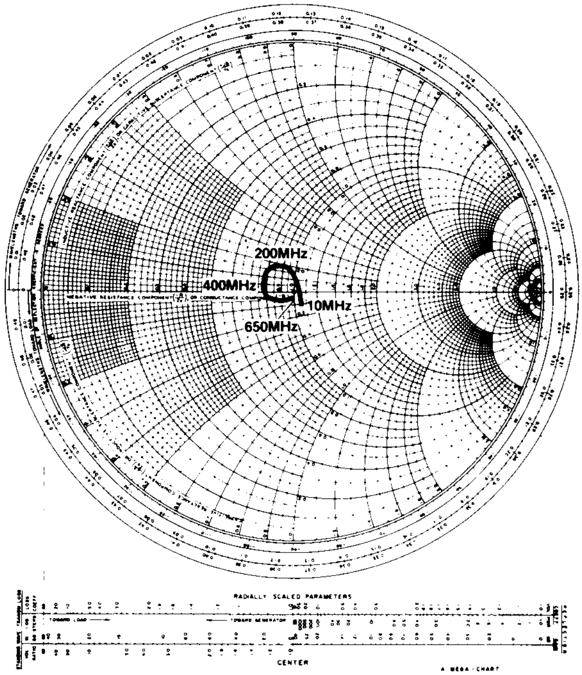

Fig.40 Output impedance (typical)

IMPEDANCE OR ADMITTANCE CO-ORDINATES

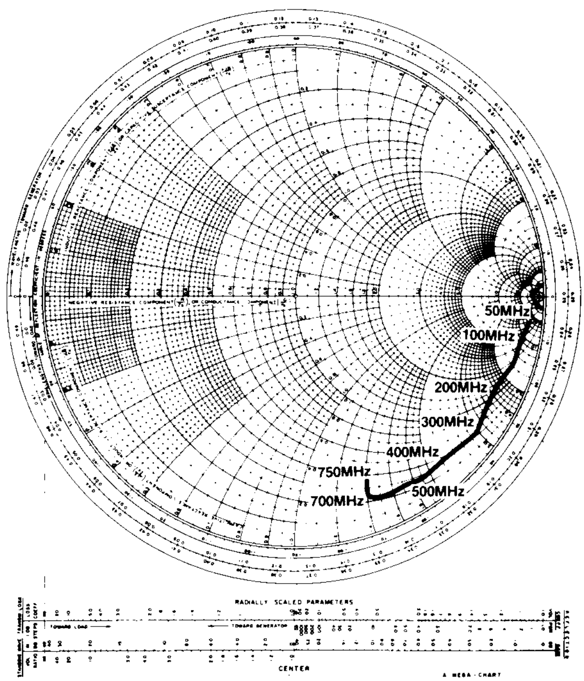

Fig.41 Input impedance (typical)