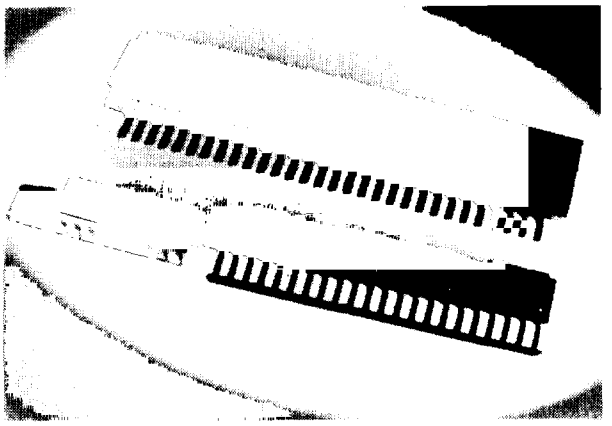
ACCUTEK

HIGH DENSITY DYNAMIC RANDOM ACCESS MEMORY MODULES



DESCRIPTION

The Accutek family of high density dynamic RAM modules are comprised of 64K x 1 or 256K x 1 dynamic RAMs packaged in LCCs or PLCCs along with chip capacitors, mounted to multi-layer ceramic or PWB substrates. These modules are intended for applications where board space is limited or large amounts of memory are required in a compact space.

FEATURES

* Utilizes industry standard 64K or 256K dynamic RAMs in PLCCs or LCCs
* Includes decoupling capacitors
* Jedec approved pinouts
* Row Access Time - Cycle Time
  100 ns max - 200 ns min
  120 ns max - 240 ns min
  150 ns max - 260 ns min
* Single +5V supply (10% tolerance)
* Direct interfacing with TTL logic family
* RAS only and hidden refresh capability
* Read-modify-write and page mode capability
* Common I/O capability using early write operations
* Available with nibble mode capability (specify)
* Available screened to mil-std-883C class B on some modules

HIGH DENSITY DYNAMIC RAM SELECTION GUIDE

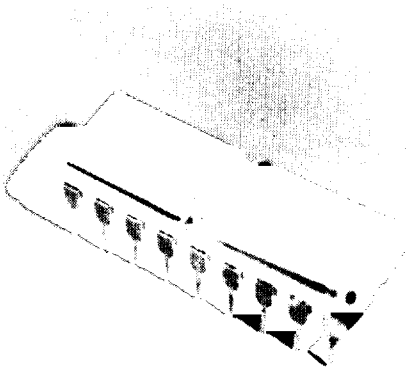
This data sheet contains descriptions of the following high density modules with mechanical and functional properties.

Based upon the 64K DRAM Component			
Part #	Organization	Form	Package
AK41128H	128K x 1	18 pin DIP	D18C-1
AK42064H	64K x 2	18 pin DIP	D18C-1
AK41256S	256K x 1	22 pin SIP	S22C-1
AK44064S	64K x 4	22 pin SIP	S22C-1
AK48064S	64K x 8	30 pad SIMM	S30P-1
AK49064S	64K x 9	30 pad SIMM	S30P-1

Based upon the 256K DRAM Component			
Part #	Organization	Form	Package
AK41512H	512K x 1	18 pin DIP	D18C-2
AK42256H	256K x 2	18 pin DIP	D18C-2
AK411024S	1MEG x 1	22 pin SIP	S22C-2
AK44256S	256K x 4	22 pin SIP	S22C-2
AK48256S	256K x 8	20 pad SIMM	S30P-1
AK49256S	265K x 9	30 pad SIMM	S30P-1

ACCUTEK

AK41128H
131,072 x 1 bit NMOS Dynamic Random Access Memory



PACKAGE D18C-1

DESCRIPTION

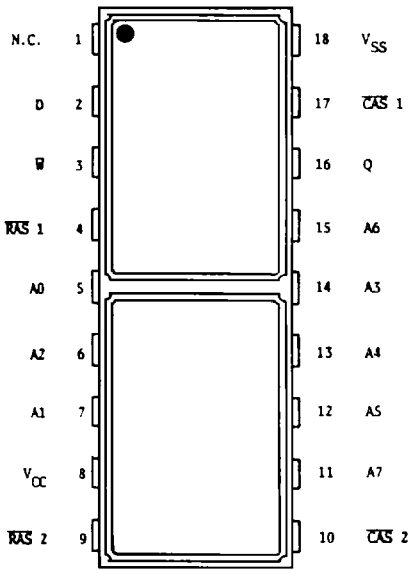
The Accutek AK41128H high density memory module is a random access memory organized in 128K x 1 bit words. The assembly consists of two standard 64K x 1 DRAMs in leadless chip carrier mounted to a multi-layer ceramic 18 pin DIP. This packaging approach provides an almost 2 to 1 density increase.

The operation of the AK41128H is identical to two 64K dynamic RAMs. The data inputs are common and data outputs are common with control by utilizing separate RAS and separate CAS for each device.

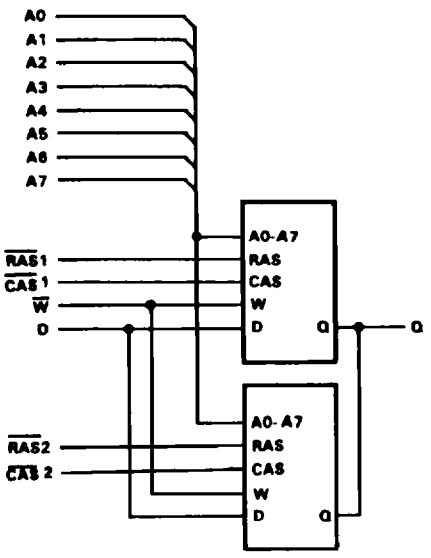
FEATURES

* 131,072 x 1 bit organization
* 18 pin Dual In-line Package
* Common D and Q lines with separate RAS and CAS
* Refresh period 2ms/128 cycle
  or 4ms/256 cycle
* 270 mW active 40 mW standby (max)
* Available with Pin 1 RFSH for internal refresh address counter (specify)
* Available screened to mil-std-883C
* Upward compatable with AK41512H
* Downward compatable with AK41032H (Mostek MK4332)

PIN ASSIGNMENT



FUNCTIONAL DIAGRAM

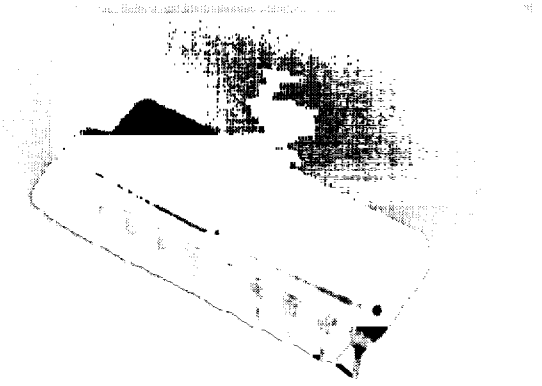


PIN NOMENCLATURE

A_0-A_7	Address Inputs
D	Data Input
Q	Data Output
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Write Enable
VCC	5V Supply
VSS	Ground

ACCUTEK

AK42064H
65,536 x 2 bit NMOS Dynamic Random Access Memory



PACKAGE D18C-1

DESCRIPTION

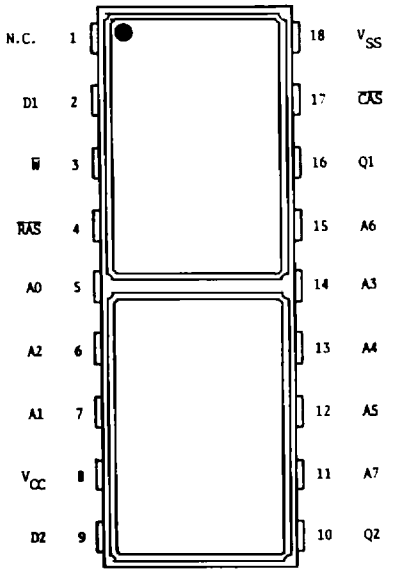
The Accutek AK42064H high density memory module is a random access memory organized in 64K x 2 bit words. The assembly consists of two standard 64K x 1 DRAMs in leadless chip carrier mounted to a multi-layer ceramic 18 pin DIP. This packaging approach provides an almost 2 to 1 density increase.

The operation of the AK42064H is identical to two 64K dynamic RAMs. The data input and data output pins are separate for each device with common RAS and common CAS.

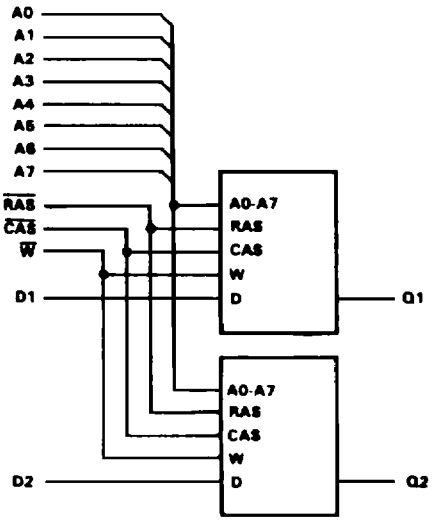
FEATURES

* 65,536 x 2 bit organization
* 18 pin Dual In-line Package
* Separate D and Q line for each device with common RAS and CAS control
* Refresh period 2ms/128 cycle
  or 4ms/256 cycle
* 500 mW active 40 mW standby (max)
* Available with Pin 1 RFSH for internal refresh address counter (specify)
* Available screened to mil-std-883C
* Upward compatable with AK42256H

PIN ASSIGNMENT



FUNCTIONAL DIAGRAM

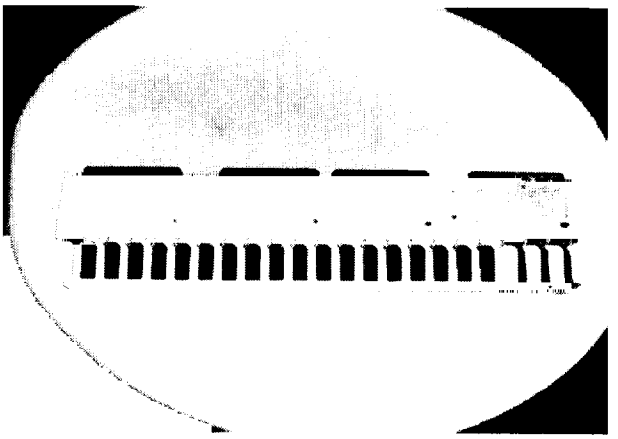


PIN NOMENCLATURE

A_0-A_7	Address Inputs
D	Data Input
Q	Data Output
CAS	Column Address Strobe
RAS	Row Address Strobe
W	Write Enable
VCC	5V Supply
VSS	Ground

ACCUTEK

AK41256S
262,144 x 1 bit NMOS Dynamic Random Access Memory



PACKAGE S22C-1

DESCRIPTION

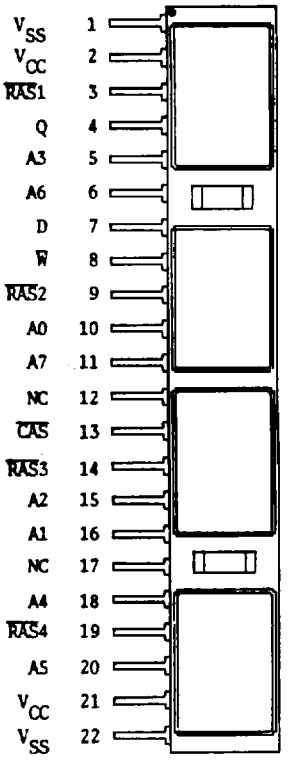
The Accutek AK41256S high density memory module is a random access memory organized in 256K x 1 bit words. The assembly consists of four standard 64K x 1 DRAMs in leadless chip carrier mounted to a multi-layer ceramic 22 pin SIP. This packaging approach provides a 4 to 1 density increase.

The operation of the AK41256S is identical to four 64K dynamic RAMs. The data inputs are common and data outputs are common with control by utilizing separate RAS for each device.

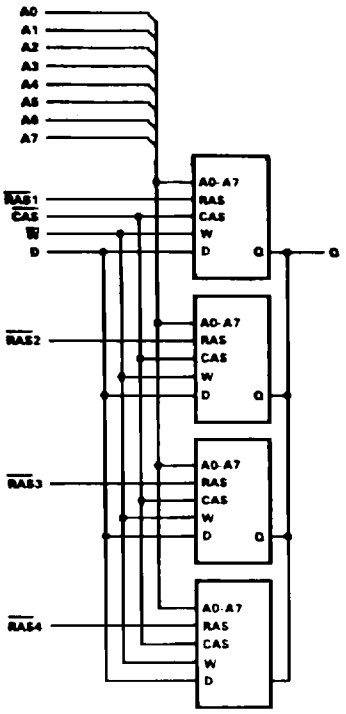
FEATURES

* 262,144 x 1 bit organization
* 22 pin Single In-line Package
* Common D and Q lines with separate RAS
* Refresh period 2ms/128 cycle
  or 4ms/256 cycle
* 310 mW active 80 mW standby (max)
* Available with Pin 17 RFSH for internal refresh address counter (specify)
* Available screened to mil-std-883C
* Upward compatable with AK411024S

PIN ASSIGNMENT



FUNCTIONAL DIAGRAM

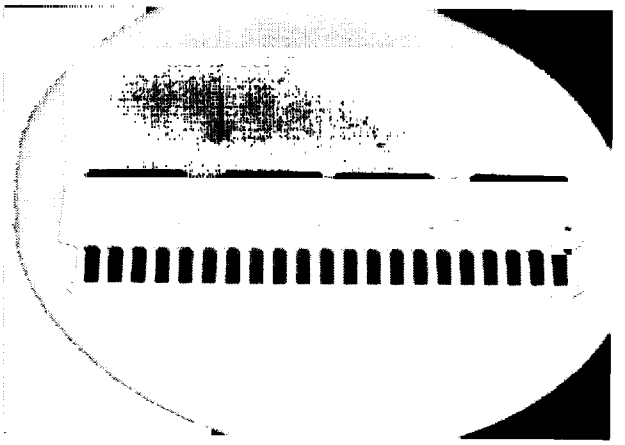


PIN NOMENCLATURE

A_0-A_7	Address Inputs
D	Data Input
Q	Data Output
CAS	Column Address Strobe
RAS	Row Address Strobe
W	Write Enable
VCC	5V Supply
VSS	Ground

ACCUTEK

AK44064S
65,536 x 4 bit NMOS Dynamic Random Access Memory



PACKAGE S22C-1

DESCRIPTION

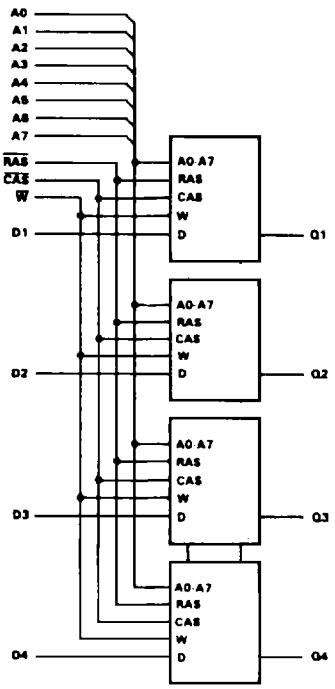
The Accutek AK44064S high density memory module is a Random Access Memory organized in 64K x 4 bit words. The assembly consists of four standard 64K x 1 DRAMs in leadless chip carrier mounted to a multi-layer ceramic 22 pin SIP. This packaging approach provides a 4 to 1 density increase.

The operation of the AK44064S is identical to four 64K Dynamic RAMs. The data input and data output pins are separate for each device with common RAS and common CAS control.

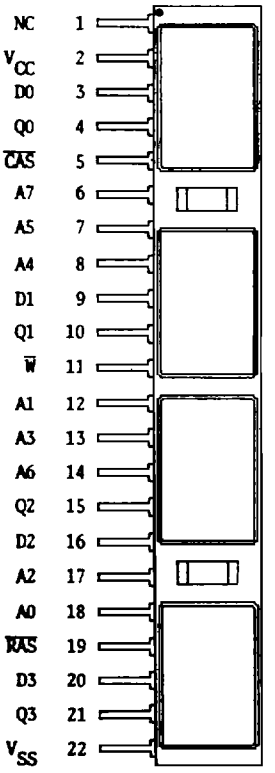
FEATURES

* 65,536 x 4 bit organization
* 22 pin Single In-line Package
* JEDEC approved pinout
* Separate D and Q lines for each device with common RAS and CAS control
* 1.0 Watt active and 80 mW standby (max)
* Available with Pin 1 RFSH for interal refresh accress counter (specify)
* Available screened to mil-std-883C
* Upward compatable with AK44256S
* Downward compatable with AK44016S

FUNCTIONAL DIAGRAM



PIN ASSIGNMENT



PIN NOMENCLATURE

A_0-A_7	Address Inputs
D	Data Input
Q	Data Output
CAS	Column Address Strobe
RAS	Row Address Strobe
W	Write Enable
VCC	5V Supply
VSS	Ground

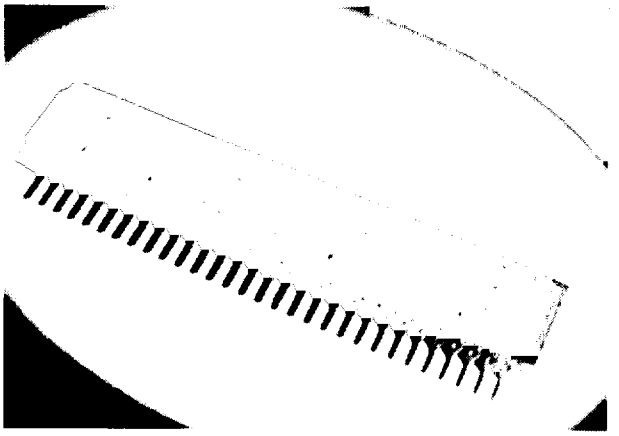
ACCUTEK

AK48064S
65,536 x 8 bit NMOS Dynamic Random Access Memory

DESCRIPTION

The Accutek AK48064S high density memory module is a random access memory organized in 64K x 8 bit words. The assembly consists of eight standard 64K x 1 DRAMs in plastic leaded chip carrier (SOJ) mounted to a printed wiring board 30 pad (SIMM) SIP. This packaging approach provides a 6 to 1 density increase over standard DIP packaging.

The operation of the AK48064S is identical to eight 64K dynamic RAMs. The data input is tied to the data output and brought out separately for each device, with common RAS and CAS control. This common I/O feature dictates the use of early-write cycles to prevent contention of D and Q.

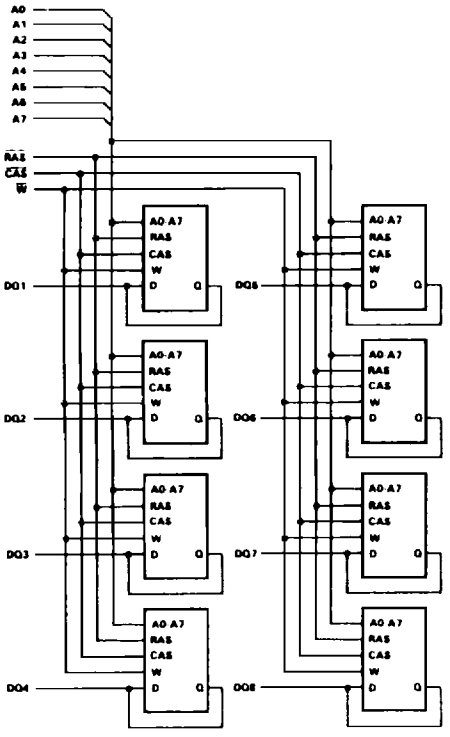


PACKAGE S30P-1

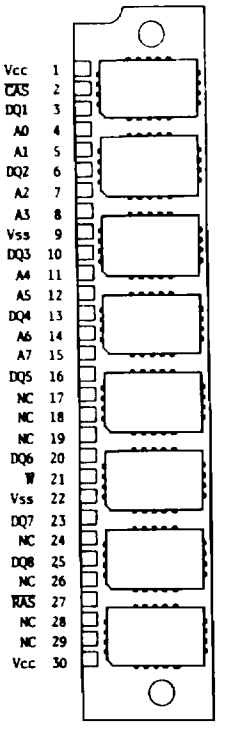
FEATURES

* 65,536 x 8 bit organization
* 30 Pad (SIMM) Single In-line Memory Module packaging
* JEDEC approved pinout
* Each device has common D and Q lines with common RAS and CAS control
* 2.0 Watt active and 160 mW standby (max)
* Operating free air temperature: 0^{o}c to 70^{o}
* Upward compatable with AK48256S and AK481024S
* Available in leadless or leaded version

FUNCTIONAL DIAGRAM



PIN ASSIGNMENT



PIN NOMENCLATURE

A_0-A_7	Address Inputs
DQ	Data In/Data Out
CAS	Column Address Strobe
RAS	Row Address Strobe
W	Write Enable
VCC	5V Supply
VSS	Ground

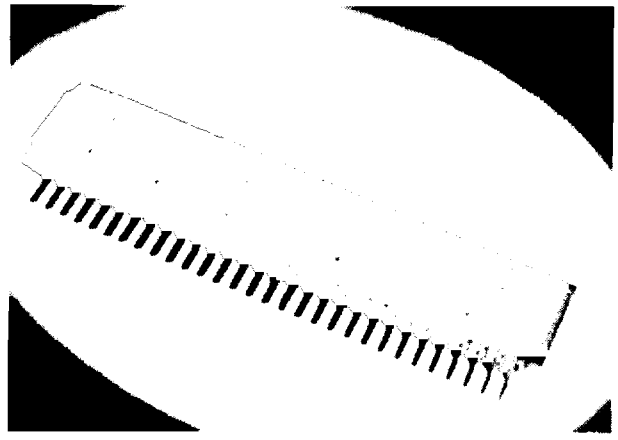
ACCUTEK

AK49064S
65,536 x 9 bit NMOS Dynamic Random Access Memory

DESCRIPTION

The Accutek AK49064S high density memory module is a random access memory organized in 64K x 9 bit words. The assembly consists of nine 64K x 1 DRAMs in plastic leaded chip carrier (SOJ) mounted to a printed wiring board 30 pad (SIMM) SIP. This packaging approach provides a 6 to 1 density increase over standard DIP packaging.

The operation of the AK49064S is identical to nine 64K dynamic RAMs. For the lower eight bits, the data input is tied to the data output and brought out separately for each device, with common RAS anc CAS control. This common I/O feature dictates the use of early-write cycles to prevent contention of D and Q. For the ninth bit, the data input (D9) and data output (Q9) pins are brought out separately and controlled by a separate CAS 9 for that bit. Bit nine is generally used parity.

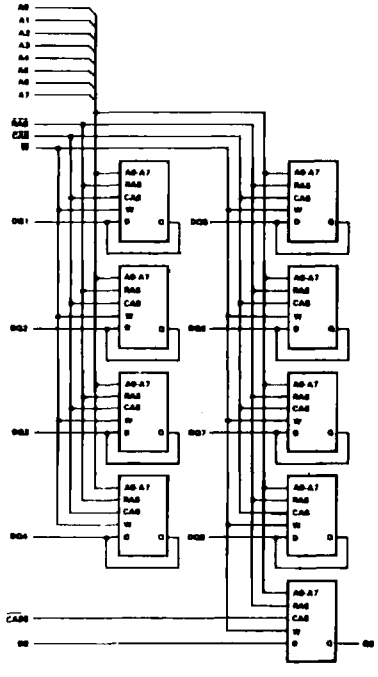


PACKAGE S30P-1

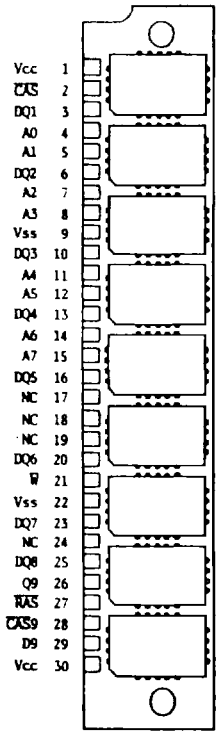
FEATURES

* 65,536 x 9 bit organization
* 30 pad (SIMM) Single In-line Memory Module packaging
* JEDEC approved pinout
* Common CAS and common RAS control for eight common D and Q lines
* Separate CAS control for one separate pair of D and Q lines
* 2.25 Watt active and 180 mW standby (max)
* Operating free air temperature $0^{o}c$ to $70^{o}c$
* Upward compatable with AK49256S and AK491024S
* Available in leadless or leaded version

FUNCTIONAL DIAGRAM



PIN ASSIGNMENT



PIN NOMENCLATURE

A_0-A_7	Address Inputs
DQ	Data In/Data Out
CAS	Column Address Strobe
RAS	Row Address Strobe
W	Write Enable
VCC	5V Supply
VSS	Ground

ABSOLUTE MAXIMUM RATINGS (See note)

Rating	Symbol	AK41128H AK42064H Value	AK41256S AK44064S Value	AK48064S AK49064S Value	Unit
Voltage on any pin related to V_{SS}	V_{IN}, V_{OUT}	-1 to +7.0	-1 to +7.0	-1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1 to +7.0	-1 to +7.0	-1 to +7.0	V
Storage Temperature LCC/Ceramic	T_{stg}	-55 to +150	-55 to +150		oC
PLCC/PCB		-55 to +125	-55 to +125	-55 to +125	
Power Dissipation	PD	1.0	2.0	4.0	W
Short Circuit Output Current	IOS	50	50	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may effect device reliability. This device contains circuity to protect the inputs against damage due to high static voltage or electric fields. It is advised that normal precautions be taken to avoid application of any voltage higher that maximum rated voltage to this high impedance circuit.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Value			Unit	Operating Temperature
		Min	Typ	Max		
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0oC to 70oC
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	-	6.5	V	
Input Low Voltage, all inputs	V_{IL}	-1.0	-	0.8	V	

CAPACITANCE (T_A=25^{o}C)

Parameter	Symbol	Maximum Value						Unit
		AK41128	AK42064	AK41256	AK44064	AK48064	AK49064	
Input Capacitance D	C_{IND}	12	5	12	5	5	5	pF
Input Capacitance A_0 ~ A_7	C_{INA}	12	12	22	22	44	49	pF
Input Capacitance $\overline{CAS}$, $\overline{W}$	C_{INC}	18	18	34	34	68	76	pF
Output Capacitance Q	C_{OUT}	16	7	30	7	7	7	pF
Input Capacitance $\overline{RAS}$	C_{INR}	8	18	8	34	68	76	pF

DC CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	AK41128		AK42064		AK41256		AK44064		AK48064		AK49064		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
OPERATING CURRENT* Average Power Supply Current (RAS, CAS cycling; t_{RC}=min.)(minimum cycle time)	I_{CC1}	-	54	-	100	-	62	-	200	-	400	-	450	mA
STANDBY CURRENT* Average Power Supply Current (RAS/CAS = V_{IH})	I_{CC2}	-	8	-	8	-	16	-	16	-	32	-	36	mA
REFERSH CURRENT* Average Power Supply Current (CAS = V_{IH}; RAS cycling, t_{RC}=min.)(minimum cycle time)	I_{CC3}	-	42	-	76	-	50	-	152	-	304	-	342	mA
PAGE MODE CURRENT* Average Power Supply Current (RAS = V_{IL}, CAS cycling; t_{PC}=min.)(minimum cycle time)	I_{CC4}	-	39	-	70	-	47	-	140	-	280	-	315	mA
INPUT LEAKAGE CURRENT, any input (0V≤V_{IN}≤5.5V, V_{CC}=5.5V, V_{SS}=0V, all other pins not under test=0V)	I_{IL}	-20	20	-20	20	-40	40	-40	40	-80	80	-90	90	uA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V≤V_{OUT}≤5.5V)	I_{OL}	-20	20	-10	-10	-40	40	-10	10	-10	10	-10	10	uA
OUTPUT LEVEL Output High Voltage (I_{OH}=-5.0mA)	V_{OH}	2.4	-	2.4	-	2.4	-	2.4	-	2.4	-	2.4	-	V
OUTPUT LEVEL, Output Low Voltage (I_{OL}=4.2mA)	V_{OL}	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	V

Note: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

AC CHARACTERISTICS (Recommended operation conditions unless otherwise noted.)

Parameter	Notes	Symbol		100NS		120NS		150NS		Unit
		Alternate	*Standard	Min	Max	Min	Max	Min	Max	
Time between Refresh		tREF	TRVRV	-	2	2	-	2	-	ms
Random Read/Write Cycle Time		tRC	TRELREL	200	-	230	-	260	-	ns
Read-Write Cycle Time		tRWC	TRELREL	230	-	265	-	280	-	ns
Page Mode Cycle Time		tPC	TCELCEL	105	-	120	-	145	-	ns
Page Mode Read-Write Cycle Time		tPRWC	TCEHCEK	135		155		180		ns
Access Time from RAS	(4),(6)	tRAC	TRELQV	-	100	-	120	-	150	ns
Access Time from CAS	(5),(6)	tCAC	TCELQV	-	50	-	60	-	75	ns
Output Buffer Turn off Delay		tOFF	TCEHQZ	0	30	0	35	0	40	ns
Transition Time		tT	TT	3	50	3	50	3	50	ns
RAS Precharge Time		tRP	TREHREL	90	-	100	-	100	-	ns
RAS Pulse Width		tRAS	TRELREH	100	10000	120	10000	150	10000	ns
RAS HOld Time		tRSH	TCELREH	50	-	60	-	75	-	ns
CAS Precharge Time (Page mode only)		tCP	TCEHCEL	45	-	50	-	60	-	ns
CAS Precharge Time (All cycles except page mode)		tCPN	TCEHCEL	25	-	30	-	30	-	ns
CAS Pulse Width		tCAS	TCELCEH	50	10000	60	10000	75	10000	ns
CAS HOld Time		tCSH	TRELCEH	100	-	120	-	150	-	ns
RAS to CAS Delay Time		tRCD	TRELCEL	20	50	20	60	25	75	ns
CAS to RAS Precharte Time		tCRP	TCEHREL	0	-	0	-	0	-	ns
Row Address Set Up Time		tASR	TAVREL	0	-	0	-	0	-	ns
Row Address Hold Time		tRAH	TRELAX	10	-	10	-	15	-	ns
Column Address Set Up Time		tASC	TAVCEL	0	-	0	-	0	-	ns
Column Address Hold Time		tCAH	TCELAX	15	-	15	-	20	-	ns
Read Command Set Up Time		tRCS	TWHCEL	0	-	0	-	0	-	ns
Read Command Hold Time Reference to CAS	(9)	tRCH	TCEHWX	0	-	0	-	0	-	ns
Read Command Hold Time Referenced to RAS	(9)	tRRH	TREHWX	20	-	20	-	20	-	ns
Write Command Set Up Time	(8)	tWCS	TWLCEL	0	-	0	-	0	-	ns
Write Command Hold Time		tCH	TCELWH	20	-	25	-	30	-	ns
Write Command Pulse Width		tWP	TWLWH	20	-	25	-	30	-	ns
Write Command to RAS Lead Time		tRWL	TWLREH	35	-	40	-	45	-	ns
Write Command to CAS Lead Time		tCWL	TWLCEH	35	-	40	-	45	-	ns
Data In Set Up Time		tDS	TCVCEL	0	-	0	-	0	-	ns
Data In Hold Time		tDH	TCELDX	20	-	25	-	30	-	ns
CAS to W Delay		tCWD	TCELWL	40	-	50	-	60	-	ns
RAS to W Delay		tRWD	TRELWL	90	-	110	-	120	-	ns

NOTES

1. An initial pause of 200uS is required after power-up followed by any 8 RAS cycles before proper device operation is achieved.

2. AC characteristics assume t_T = 5nS

3. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH}(min.) andV_{IL}(max.)

4. t_{RCD} is specified as a reference point only. If $t_{RCD} \leq t_{RCD}$(max.) the specified maximum value of t_{RAC}(max.) can be met. If $t_{RCD} > t_{RCD}$(max.) then t_{RAC} is increased by the amount that t_{RCD} exceeds t_{RCD}(max.)

5. Assumes that $t_{RCD} \geq t_{RCD}$(max.).

6. Measured with a load equivilent to 2 TTL loads and 100pF.

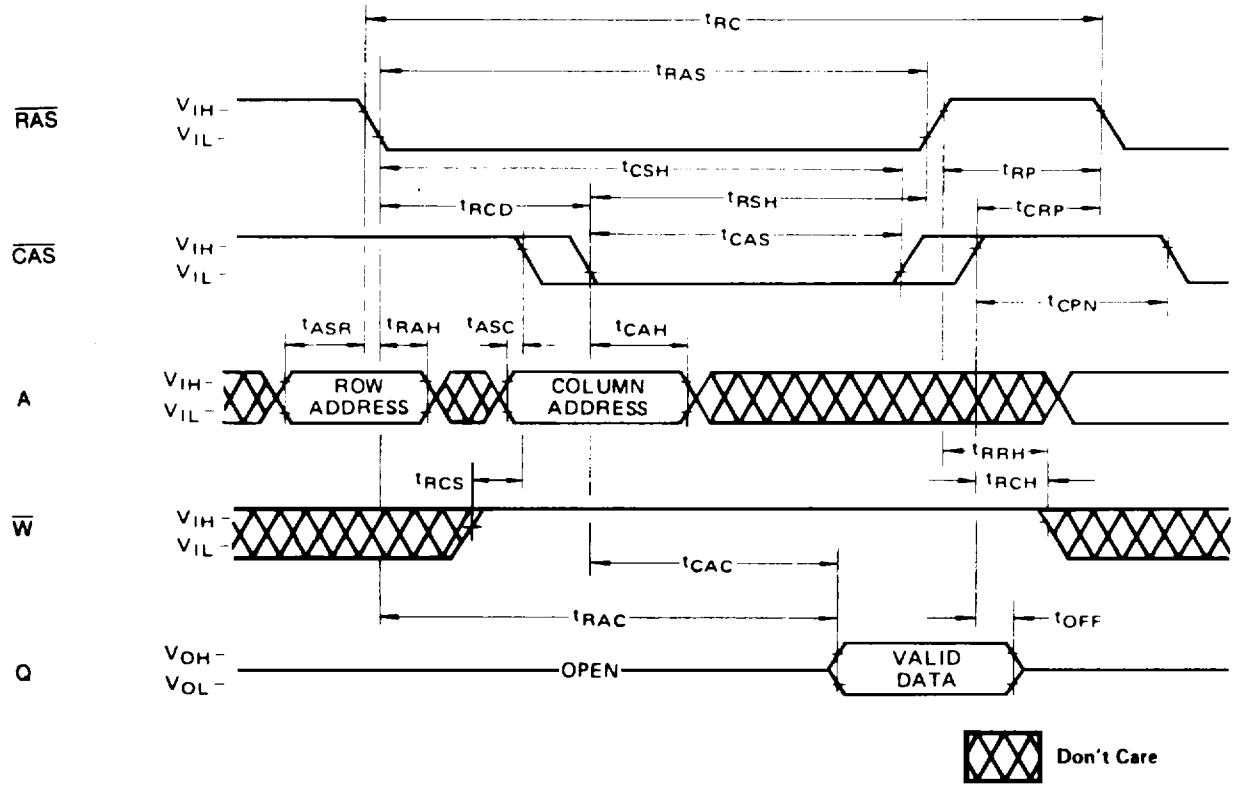
7. t_{RCD}(min.)=t_{RAH}(min.)+2t_T+t_{ASC}(min.); t_T=5nS.

8. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early-write cycle, and the data out pin will remain open circuit (high impedance) throughout entire cycle.

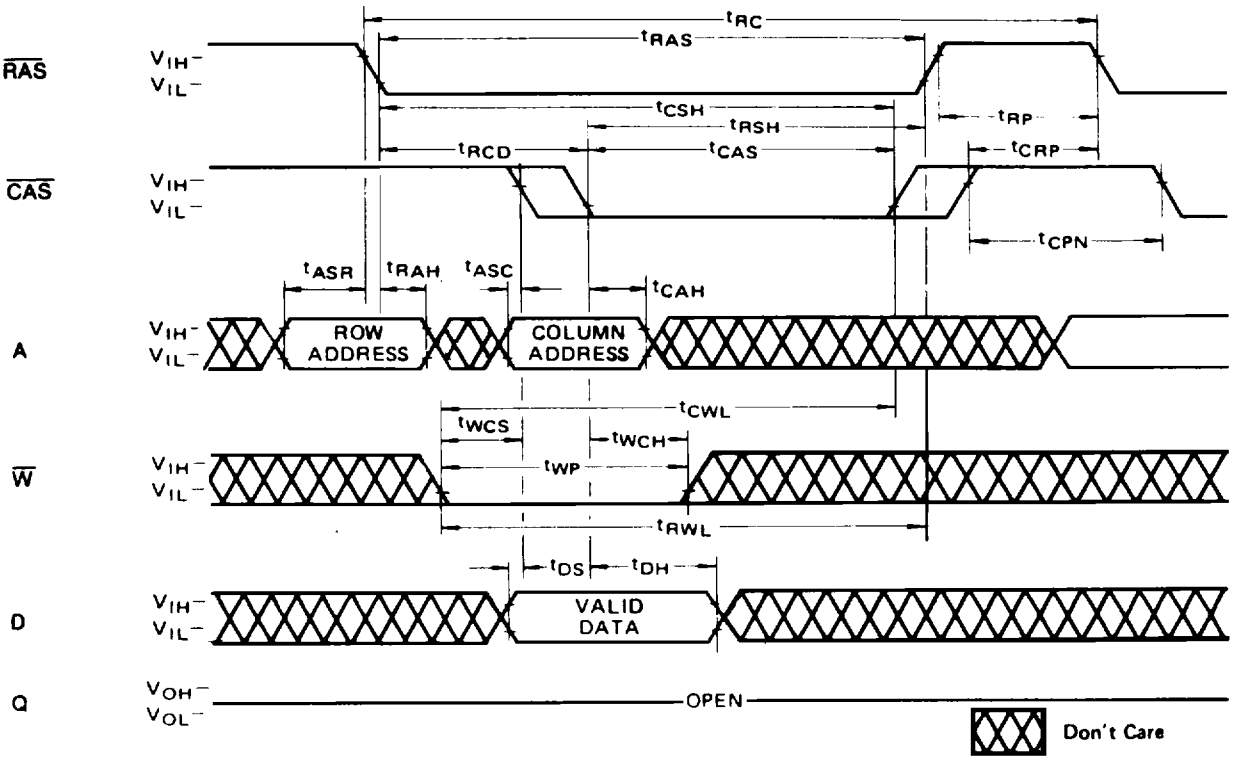
   If $t_{CWD} \geq t_{CWD}$(min.) and $t_{RWD} \geq t_{RWD}$(min.), the cycle is a read-write cycle and data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out is indeterminate.

9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

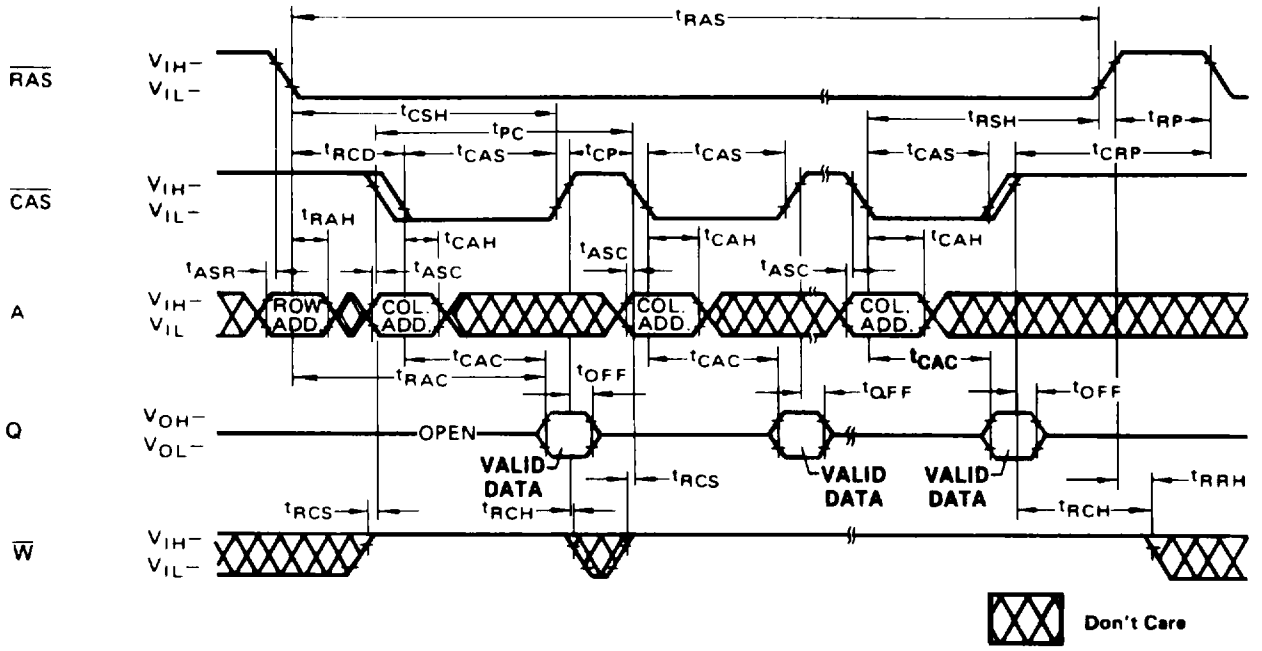
READ CYCLE



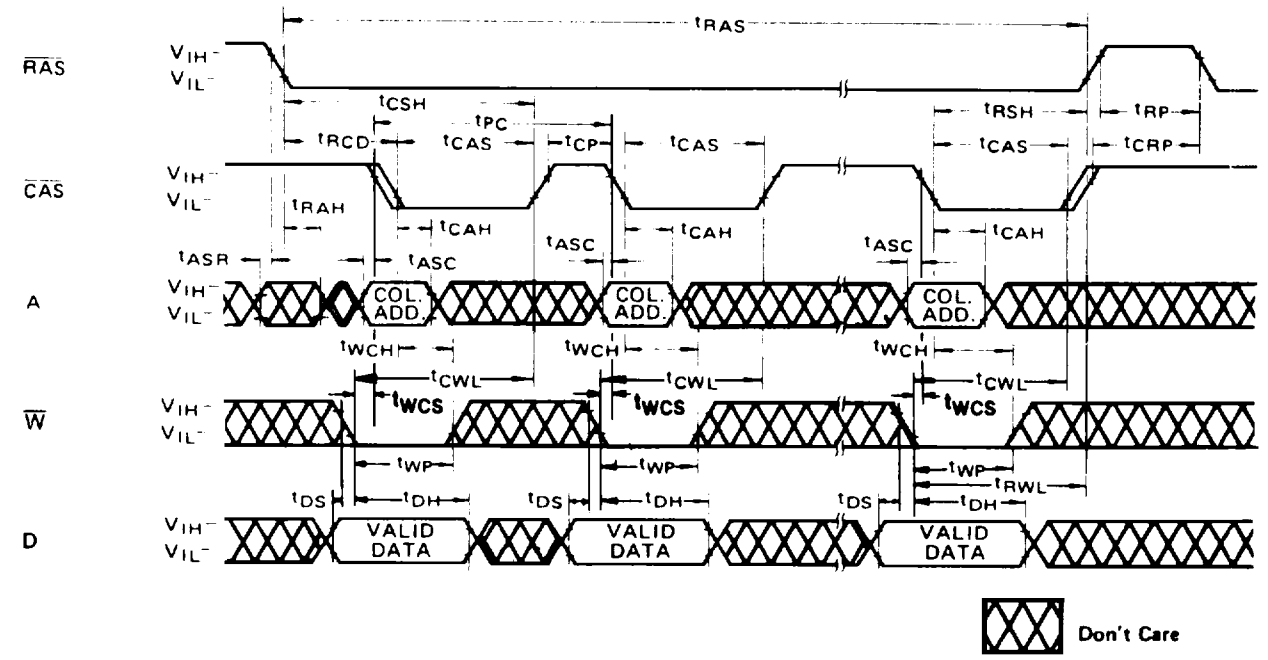
WRITE CYCLE (EARLY WRITE)



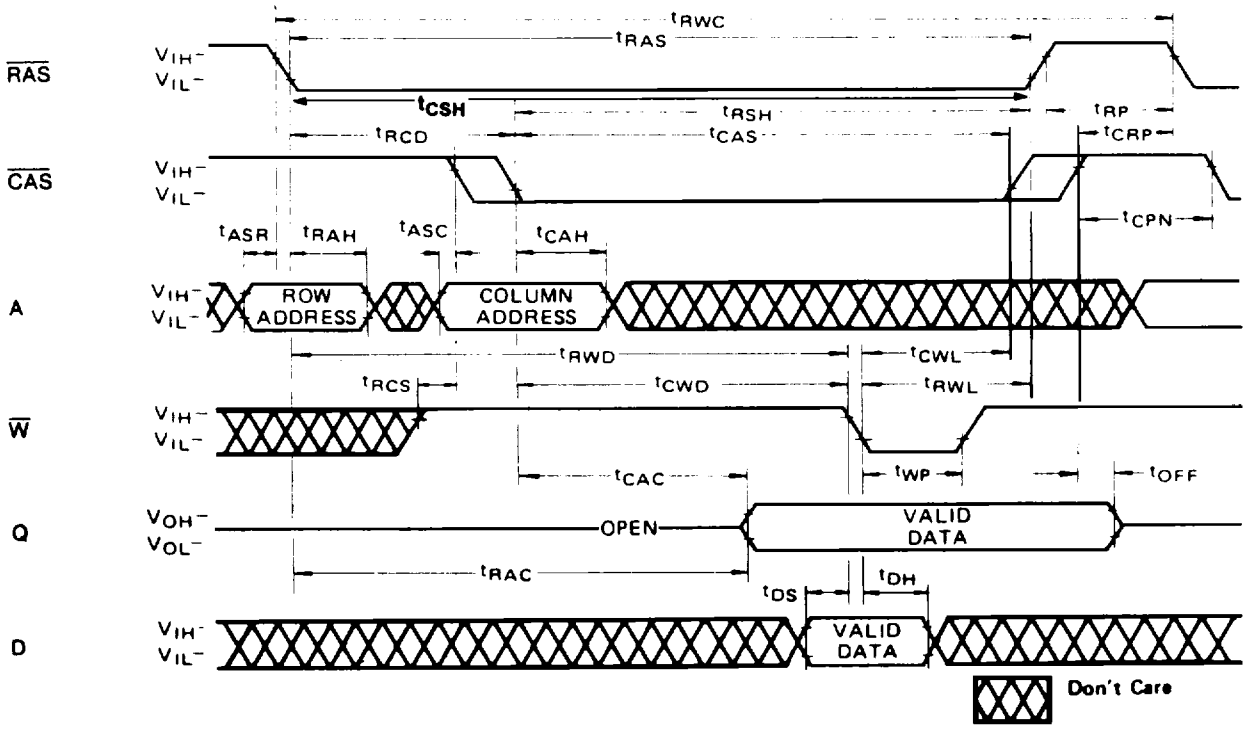
PAGE MODE READ CYCLE



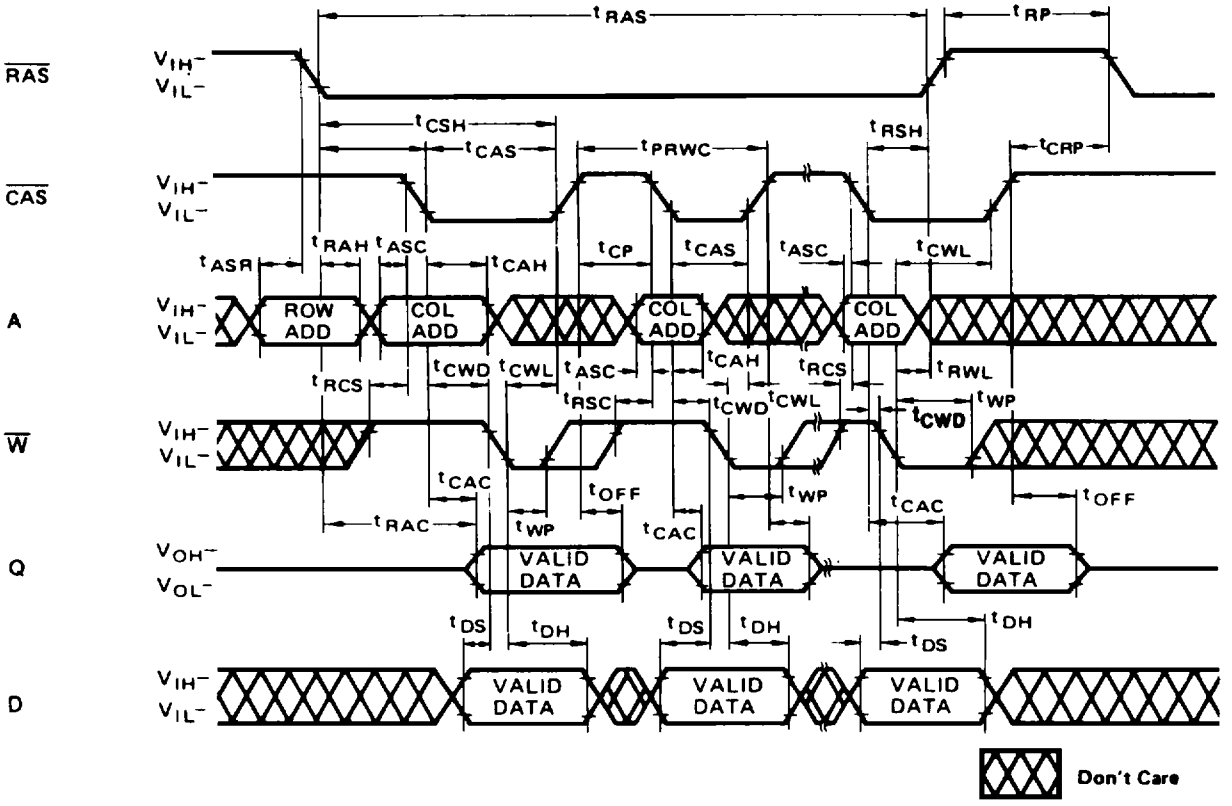
PAGE MODE WRITE CYCLE



READ-WRITE/READ-MODIFY-WRITE CYCLE

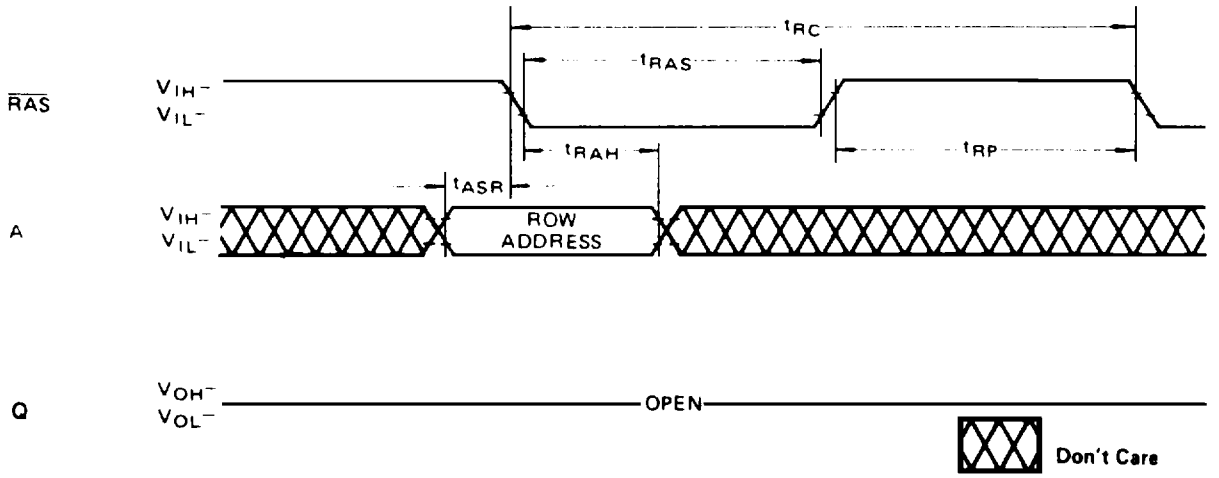


PAGE MODE READ-WRITE CYCLE

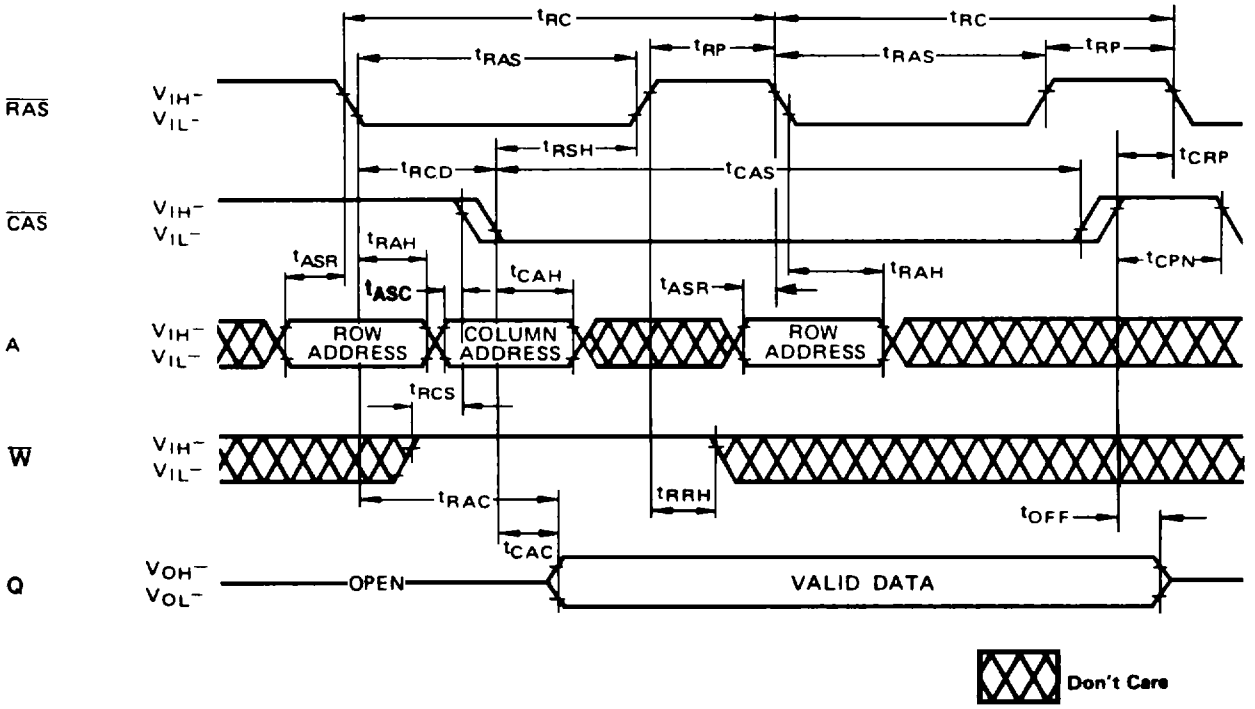


$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE: $\overline{CAS}$ = V_{IH}, $\overline{W}$, D = Don't Care



HIDDEN $\overline{RAS}$-ONLY REFRESH CYCLE



OPERATION

Address Inputs

A total of sixteen binary input address bits are required to decode any one of 65,536 storage cell locations within each of the 64K DRAMs. Eight row-address bits are established on the input pins (A_0 through A_7) and latched with Row Address Strobe ($\overline{RAS}$). The eight column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-address.

Write Enable

The read mode or write mode is selected with the $\overline{W}$ input. A logic high (1) on $\overline{W}$ dictates read mode; logic low (0) dicatates when read mode is selected.

Data Input

Data is written into the selected cell during a write or read-write cycle. The last falling edge of $\overline{W}$ or $\overline{CAS}$ is a strobe for the Data In (D) register. In a write cycle, if $\overline{W}$ is brought low (write mode) before $\overline{CAS}$, D is strobed by CAS, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{W}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D is strobed by $\overline{W}$ and set-up and hold times are referenced to $\overline{W}$.

Data Output

Data-out is the same polarity as data-in. The output is is a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data Remains valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid. The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads.

Page Mode

Page mode operation permits strobing the row-address into the high density memory while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

RAS Only Refresh

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 128 row-addresses (A_0 ~ A_6) at least every two milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_7. $\overline{RAS}$-only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 128 row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

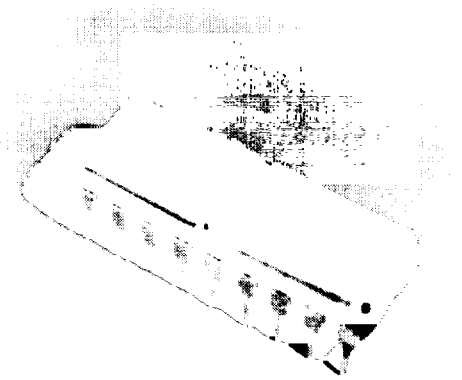
Hidden Refresh

A $\overline{RAS}$-ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.

Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} from a previous memory read cycle.

ACCUTEK

AK41512H
524,288 x 1 bit NMOS Dynamic Random Access Memory



PACKAGE D18C-2

DESCRIPTION

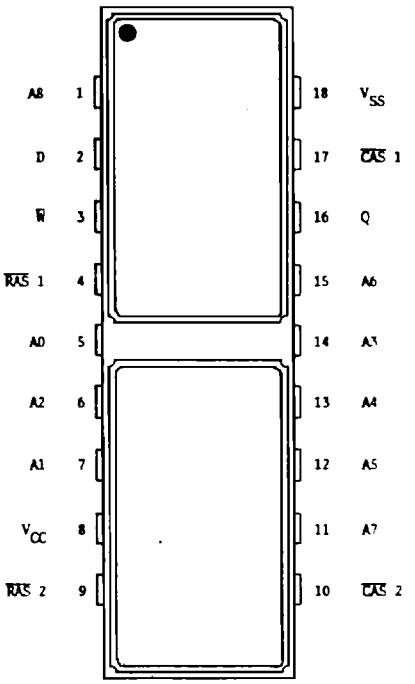
The Accutek AK41512H high density memory module is a random access memory organized in 512K x 1 bit words. The assembly consists of two standard 256K x 1 DRAMs in leadless chip carrier mounted to a multi-layer ceramic 18 pin DIP. This packaging approach provides an almost 2 to 1 density increase.

The operation of the AK41512H is identical to two 256K dynamic RAMs. The data inputs are common and data outputs are common with control by utilizing separate RAS and separate CAS for each device.

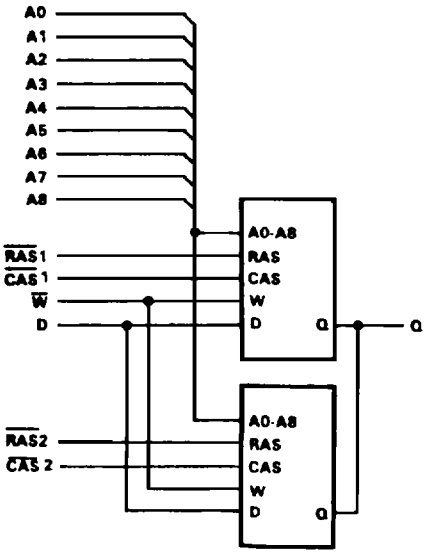
FEATURES

* 524,288 x 1 bit organization
* 18 pin Dual In-line Package (1.080 x .300 inch)
* Common D and Q lines with separate RAS and CAS
* Refresh period 4ms/256 cycle
* 375 mW active 45 mW standby (max)
* Available with CAS-before-RAS refresh (specify)
* Available screened to mil-std-883C
* Downward compatable with AK41128H

PIN ASSIGNMENT



FUNCTIONAL DIAGRAM

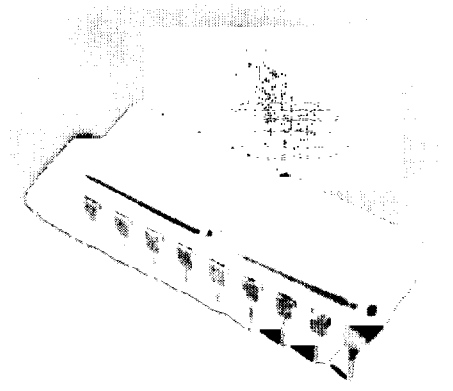


PIN NOMENCLATURE

A_0-A_8	Address Inputs
D	Data Input
Q	Data Output
CAS	Column Address Strobe
RAS	Row Address Strobe
W	Write Enable
VCC	5V Supply
VSS	Ground

ACCUTEK

AK42256H
262,144 x 2 bit NMOS Dynamic Random Access Memory



PACKAGE D18C-2

DESCRIPTION

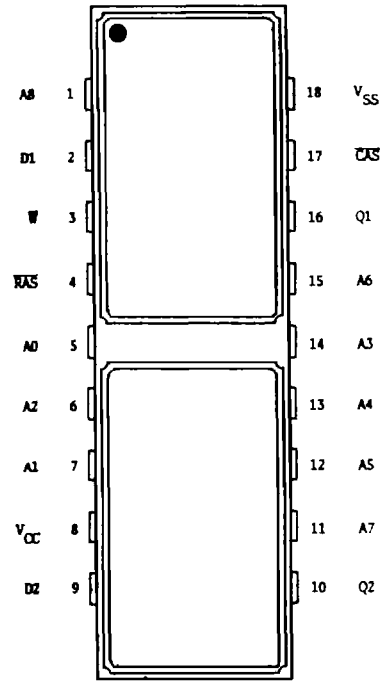
The Accutek AK42256H high density memory module is a random access memory organized in 256K x 2 bit words. The assembly consists of two standard 256K x 1 DRAMs in leadless chip carrier mounted to a multi-layer ceramic 18 pin DIP. This packaging approach provides an almost 2 to 1 density increase.

The operation of the AK42256H is identical to two 256K dynamic RAMs. The data input and data output pins are separate for each device with common RAS and common CAS.

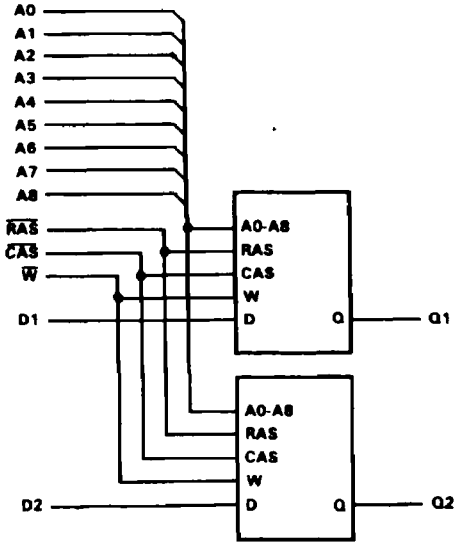
FEATURES

* 262,144 x 2 bit organization
* 18 pin Dual In-line Package (1.080 x .300 inch)
* Separate D and Q line for each device with common RAS and CAS control
* Refresh period 4ms/256 cycle
* 700 mW active 45 mW standby (max)
* Available with CAS-before RAS refresh (specify)
* Available screened to mil-std-883C
* Downward compatable with AK42064H

PIN ASSIGNMENT



FUNCTIONAL DIAGRAM

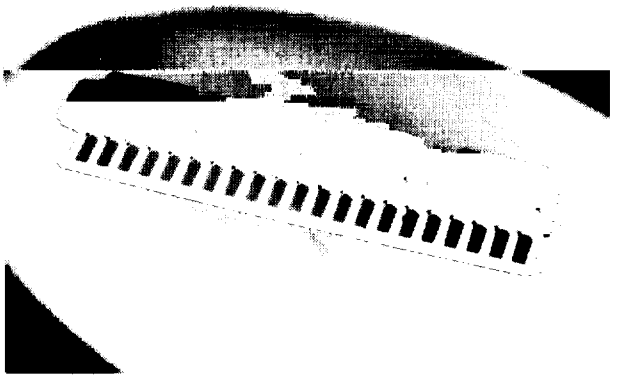


PIN NOMENCLATURE

A_0-A_8	Address Inputs
D	Data Input
Q	Data Output
CAS	Column Address Strobe
RAS	Row Address Strobe
W	Write Enable
VCC	5V Supply
VSS	Ground

ACCUTEK

AK411024S
1,048,576 x 1 bit NMOS Dynamic Random Access Memory



PACKAGE S22C-2

DESCRIPTION

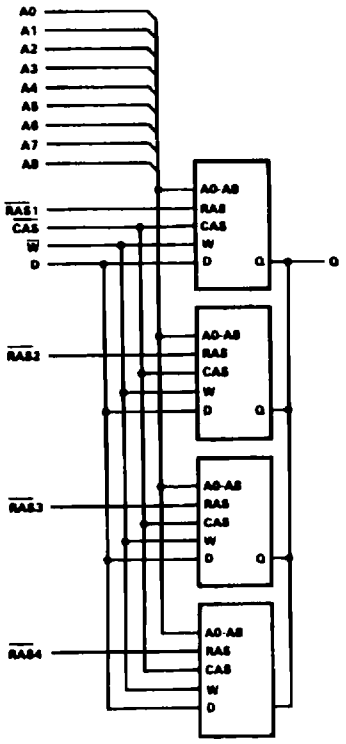
The Accutek AK411024S high density memory module is a random access memory organized in 1 Meg x 1 bit words. The assembly consists of four standard 256K x 1 DRAMs in leadless chip carrier mounted to a multi-layer ceramic 22 pin SIP. This packaging approach provides a 4 to 1 density increase over standard dip packaging.

The operation of the AK411024S is identical to four 256K dynamic RAMs. The data inputs are common and data outputs are common with control by utilizing separate RAS for each device.

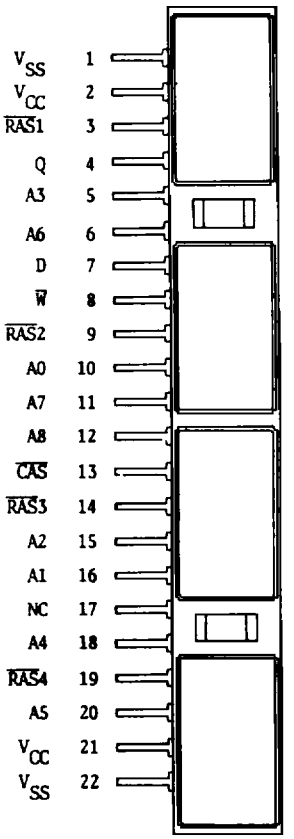
FEATURES

* 1,048,576 x 1 bit organization
* 22 pin Single In-line Package (2.400 x .200 x .335 inch)
* Common D and Q lines with separate RAS
* Refresh period 4ms/256 cycle
* 420 mW active 90 mW standby (max)
* Available with CAS-before-RAS refresh (specify)
* Available screened to mil-std-883C
* Upward compatable with AK414096S
* Downward compatable with AK41256S

FUNCTIONAL DIAGRAM



PIN ASSIGNMENT

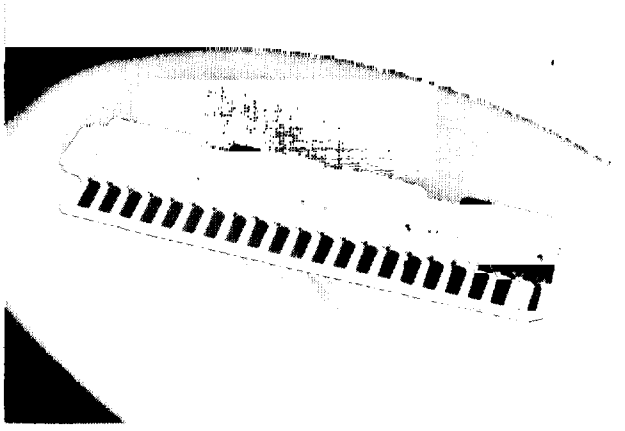


PIN NOMENCLATURE

A_0-A_8	Address Inputs
D	Data Input
Q	Data Output
CAS	Column Address Strobe
RAS	Row Address Strobe
W	Write Enable
VCC	5V Supply
VSS	Ground

ACCUTEK

AK44256S
262,144 x 4 bit NMOS Dynamic Random Access Memory



PACKAGE S22C-2

DESCRIPTION

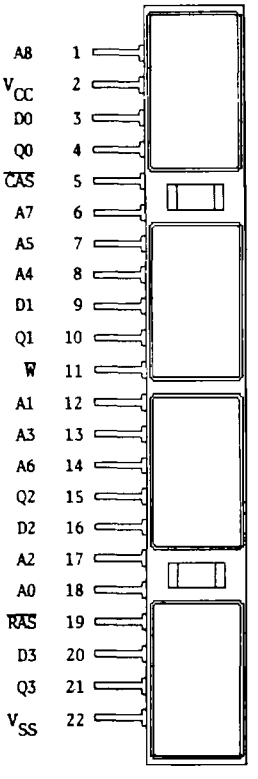
The Accutek AK44256S high density memory module is a Random Access Memory organized in 256K x 4 bit words. The assembly consists of four standard 256K x 1 DRAMs in leadless chip carrier mounted to a multi-layer ceramic 22 pin SIP. This packaging approach provides a 4 to 1 density increase over standard dip packaging.

The operation of the AK44256S is identical to four 256K Dynamic RAMs. The data input and data output pins are separate for each device with common RAS and common CAS control.

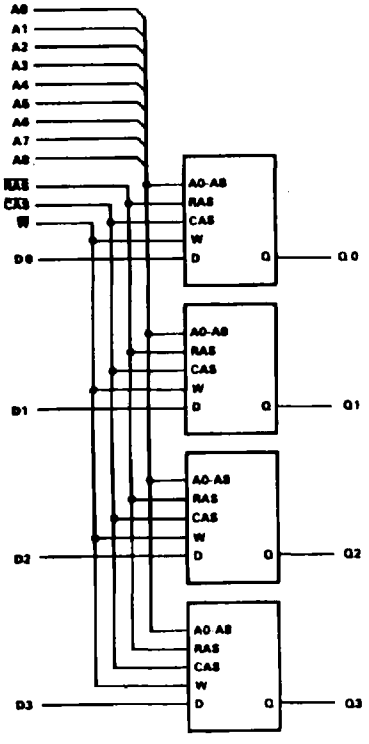
FEATURES

* 262,144 x 4 bit organization
* 22 pin Single In-line Package
* (2.400 x .200 x .345 inch)
* JEDEC approved pinout
* Separate D and Q lines for each device with common RAS and CAS control
* 1.4 Watt active and 90 mW standby (max)
* Available with CAS-before-RAS refresh (specify)
* Available screened to mil-std-883C
* Downward compatable with AK44064S

PIN ASSIGNMENT



FUNCTIONAL DIAGRAM

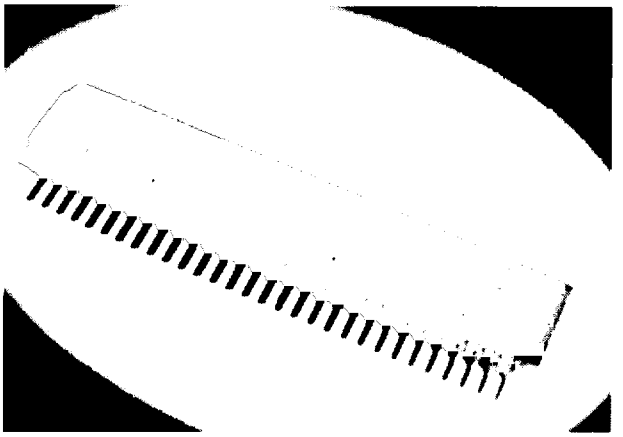


PIN NOMENCLATURE

A_0-A_8	Address Inputs
D	Data Input
Q	Data Output
CAS	Column Address Strobe
RAS	Row Address Strobe
W	Write Enable
VCC	5V Supply
VSS	Ground

ACCUTEK

AK48256S
262,144 x 8 bit NMOS Dynamic Random Access Memory



PACKAGE S30P-1

DESCRIPTION

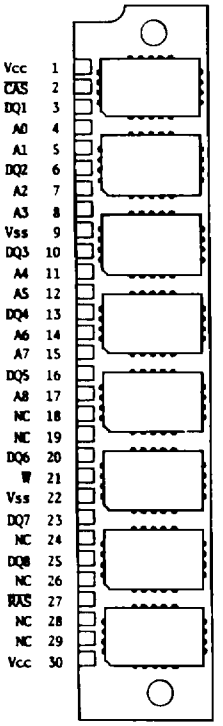
The Accutek AK48256S high density memory module is a random access memory organized in 256K x 8 bit words. The assembly consists of eight standard 256K x 1 DRAMs in plastic leaded chip carrier (SOJ) mounted to a printed wiring board 30 pad (SIMM) SIP. This packaging approach provides a 6 to 1 density increase over standard DIP packaging.

The operation of the AK48256S is identical to eight 256K dynamic RAMs. The data input is tied to the data output and brought out separately for each device, with common RAS and CAS control. This common I/O feature dictates the use of early-write cycles to prevent contention of D and Q.

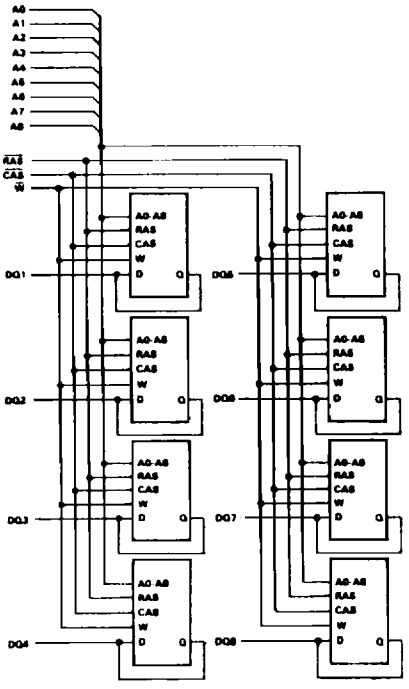
FEATURES

* 262,144 x 8 bit organization
* 30 Pad (SIMM) Single In-line Memory Module packaging
* JEDEC approved pinout
* Each device has common D and Q lines with common RAS and CAS control
* Available with CAS-before-RAS refresh (specify)
* 2.8 Watt active and 180 mW standby (max)
* Operating free air temperature: 0°c to 70°
* Upward compatable with AK481024S
* Downward compatable with AK48064S
* Available in leadless or leaded version

PIN ASSIGNMENT



FUNCTIONAL DIAGRAM



PIN NOMENCLATURE

DQ	Data In/Data Out
A_0-A_8	Address Inputs
CAS	Column Address Strobe
RAS	Row Address Strobe
W	Write Enable
VCC	5V Supply
VSS	Ground

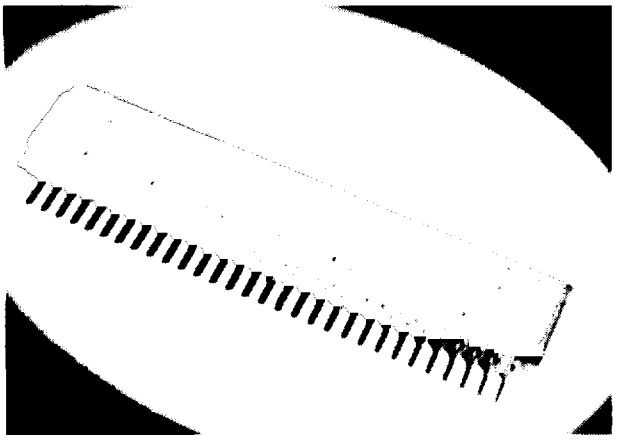
ACCUTEK

AK49256S
262,144 x 9 bit NMOS Dynamic Random Access Memory

DESCRIPTION

The Accutek AK49256S high density memory module is a random access memory organized in 256K x 9 bit words. The assembly consists of nine 256K x 1 DRAMs in plastic leaded chip carrier (SOJ) mounted to a printed wiring board 30 pad (SIMM) SIP. This packaging approach provides a 6 to 1 density increase over standard DIP packaging.

The operation of the AK49256S is identical to nine 256K dynamic RAMs. For the lower eight bits, the data input is tied to the data output and brought out separately for each device, with common RAS and CAS control. This common I/O feature dictates the use of early-write cycles to prevent contention of D and Q. For the ninth bit, the data input (D9) and data output (Q9) pins are brought out separately and controlled by a separate CAS 9 for that bit. Bit nine is generally used for parity.

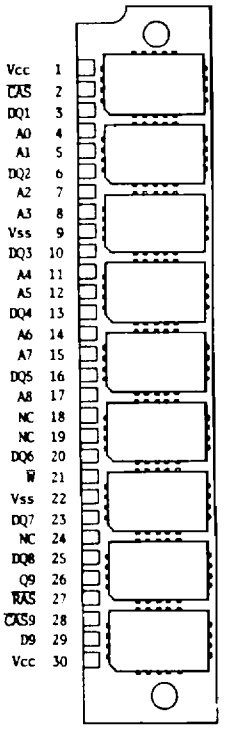


PACKAGE S30P-1

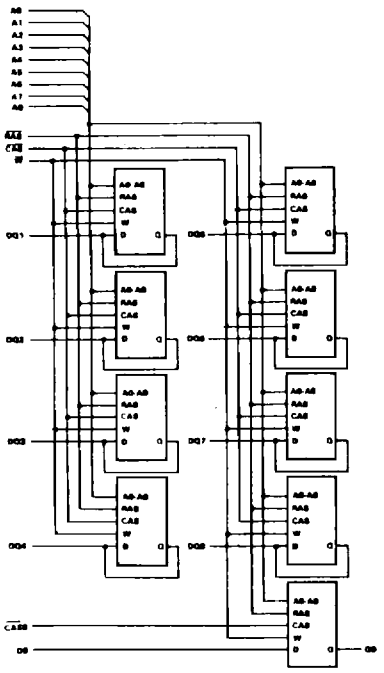
FEATURES

* 262,144 x 9 bit organization
* 30 pad (SIMM) Single In-line Memory Module packaging
* JEDEC approved pinout
* Common CAS and common RAS control for eight common D and Q lines
* Separate CAS control for one separate pair of D and Q lines
* Available with CAS-before-RAS refresh (specify)
* 3.15 Watt active and 205 mW standby (max)
* Operating free air temperature 0°c to 70°c
* Upward compatable with AK491024S
* Downward compatable with AK49064S
* Available in leadless or leaded version

PIN ASSIGNMENT



FUNCTIONAL DIAGRAM



PIN NOMENCLATURE

DQ	Data In/Data Out
A_0-A_8	Address Inputs
CAS	Column Address Strobe
RAS	Row Address Strobe
W	Write Enable
VCC	5V Supply
VSS	Ground

ABSOLUTE MAXIMUM RATINGS (See note)

Rating	Symbol	AK41512H AK42256H Value	AK411024S AK44256S Value	AK48256S AK49256S Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1 to +7.0	-1 to +7.0	-1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1 to +7.0	-1 to +7.0	-1 to +7.0	V
Storage Temperature LCC/Ceramic	T_{stg}	-55 to +150	-55 to +150		oC
PLCC/PWB		-55 to +125	-55 to +125	-55 to +125	
Power Dissipation	PD	1.0	2.0	4.0	W
Short Circuit Output Current	I_{OS}	50	50	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may effect device reliability. This device contains circuity to protect the inputs against damage due to high static voltage or electric fields. It is advised that normal precautions be taken to avoid application of any voltage higher that maximum rated voltage to this high impedance circuit.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Value			Unit	Operating Temperature
		Min	Typ	Max		
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0oC to 70oC
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	-	6.5	V	
Input Low Voltage, all inputs	V_{IL}	-1.0	-	0.8	V	

CAPACITANCE (T_A=25°C)

Parameter	Symbol	Maximum Value						Unit
		AK41512	AK42256	AK411024	AK44256	AK48256	AK49256	
Input Capacitance D	C_{IND}	16	7	30	7	7	7	pF
Input Capacitance A_0 ~ A_8	C_{INA}	16	16	30	30	60	67	pF
Input Capacitance $\overline{CAS}$, $\overline{W}$	C_{INC}	22	22	42	42	84	94	pF
Output Capacitance Q	C_{OUT}	16	7	30	7	7	7	pF
Input Capacitance $\overline{RAS}$	C_{INR}	10	22	10	42	84	94	pF

DC CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	AK41512		AK42256		AK411024		AK44256		AK48256		AK49256		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC}=min.)(minimum cycle time)	I_{CC1}	-	74.5	-	140	-	83.5	-	280	-	560	-	630	mA
STANDBY CURRENT* Average Power Supply Current ($\overline{RAS}$/$\overline{CAS}$ = V_{IH})	I_{CC2}	-	9	-	9	-	18	-	18	-	36	-	40.5	mA
REFERSH CURRENT* Average Power Supply Current ($\overline{CAS}$ = V_{IH}; $\overline{RAS}$ cycling, t_{RC}=min.)(minimum cycle time)	I_{CC3}	-	64.5	-	120	-	73.5	-	240	-	480	-	540	mA
PAGE MODE CURRENT* Average Power Supply Current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC}=min.)(minimum cycle time)	I_{CC4}	-	39.5	-	70	-	48.5	-	140	-	280	-	315	mA
INPUT LEAKAGE CURRENT, any input (0V≤V_{IN}≤5.5V, V_{CC}=5.5V, V_{SS}=0V, all other pins not under test=0V)	I_{IL}	-20	20	-20	20	-40	40	-40	40	-80	80	-90	90	uA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V≤V_{OUT}≤5.5V)	I_{OL}	-20	20	-10	-10	-40	40	-10	10	-10	10	-10	10	uA
OUTPUT LEVEL Output High Voltage (I_{OH}=-5.0mA)	V_{OH}	2.4	-	2.4	-	2.4	-	2.4	-	2.4	-	2.4	-	V
OUTPUT LEVEL, Output Low Voltage (I_{OL}=4.2mA)	V_{OL}	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	V

Note: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

AC CHARACTERISTICS (Recommended operation conditions unless otherwise noted.)

Parameter	Notes	Symbol		100NS		120NS		150NS		Unit
		Alternate	*Standard	Min	Max	Min	Max	Min	Max	
Time between Refresh		tREF	TRVRV	-	4	-	4	-	4	ms
Random Read/Write Cycle Time		tRC	TRELREL	210	-	230	-	260	-	ns
Read-Write Cycle Time		tRWC	TRELREL	210	-	230	-	260	-	ns
Access Time from RAS	(4),(6)	tRAC	TRELQV	-	100	-	120	-	150	ns
Access Time from CAS	(5),(6)	tCAC	TCELQV	-	50	-	60	-	75	ns
Output Buffer Turn off Delay		tOFF	TCEHQZ	0	25	0	25	0	30	ns
Transition Time		tT	TT	3	50	3	50	3	50	ns
RAS Precharge Time		tRP	TREHREL	90	-	100	-	100	-	ns
RAS Pulse Width		tRAS	TRELREH	110	100000	120	100000	150	100000	ns
RAS Hold Time		tRSH	TCELREH	60	-	60	-	75	-	ns
CAS Pulse Width		tCAS	TCELCEH	60	100000	60	100000	75	100000	ns
CAS Hold Time		tCSH	TRELCEH	110	-	120	-	150	-	ns
RAS to CAS Delay Time	(4),(7)	tRCD	TRELCEL	20	50	22	60	25	75	ns
Cas to RAS Set Up Time		tCRS	TCEXREL	15	-	20	-	20	-	ns
Row Address Set Up Time		tASR	TAVRELH	0	-	0	-	0	-	ns
Row Address Hold Time		tRAH	TRELAX	10	-	12	-	15	-	ns
Column Address Set Up Time		tASC	TAVCEL	0	-	0	-	0	-	ns
Column Address Hold Time		tCAH	TCELAX	15	-	20	-	25	-	ns
Read Command Set Up Time		tRCS	TWHCEL	0	-	0	-	0	-	ns
Read Command Hold Time Referenced to CAS	(10)	tRCH	TCEHWX	0	-	0	-	0	-	ns
Read Command Hold Time Referenced to RAS	(10)	tRRH	TREHWX	20	-	20	-	20	-	ns
Write Command Set Up Time	(8)	tWCS	TWLCEL	0	-	0	-	0	-	ns
Write Command Pulse Width		tWP	TWLWH	15	-	20	-	25	-	ns
Write Command Hold Time		tWCH	TCELWH	15	-	20	-	25	-	ns
Write Command to RAS Lead Time		tRWL	TWLREH	40	-	50	-	60	-	ns
Write Command to CAS Lead Time		tCWL	TWLCEH	40	-	50	-	60	-	ns
Data In Set Up Time		tDS	TDVCEL	0	-	0	-	0	-	ns
Data In Hold Time		tDH	TCELDX	15	-	20	-	25	-	ns
CAS to W Delay	(8)	tCWD	TCELWL	15	-	20	-	25	-	ns
Refresh Set Up Time for CAS Referenced to RAS		tFCS	TCELREL	20	-	25	-	30	-	ns
Refresh Hold Time for CAS Referenced to RAS		tFCH	TRELCEX	20	-	25	-	30	-	ns
Page Mode Read/Write Cycle Time		tPC	TCELCEL	100	-	120	-	150	-	ns
Page Mode Read-Write Cycle Time		tPRWC	TCEHCEH	100	-	120	-	150	-	ns
Page Mode CAS Precharge Time		tCP	TCEHCEL	40	-	50	-	65	-	ns
Refresh Counter Test RAS Pulse Width	(9)	tTRAS	TRELREH	230	10000	265	10000	320	-	ns
Refresh Counter Test Cycle Time	(9)	tRTC	TRELREL	330	-	375	-	430	-	ns
RAS Precharge to CAS Active Time		tRPC	TREHCEL	20	-	20	-	20	-	ns
Refresh Counter Test CAS Precharge Time	(9)	tCPT	TCEHCEL	50	-	60	-	70	-	ns
CAS Precharge Time for CAS before RAS Refresh Cycle		tCPR	TCEHCEL	20	-	25	-	30	-	ns

NOTES: *These symbols are described in IEEE SD. 662-1980: IEEE Standard terminology for semiconductor memory.

NOTES

1. An initial pause of 200uS is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.

   If the internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh initialization cycles are required.

2. AC characteristics assume t_T = 5nS

3. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH}(min.) and V_{IL}(max.)

4. tRCD is specified as a reference point only. If $t_{RCD} \leq t_{RCD}$(max.) the specified maximum value of t_{RAC}(max.) can be met. If $t_{RCD} > t_{RCD}$(max.) then t_{RAC} is increased by the amount that t_{RCD} exceeds t_{RCD}(max.)

5. Assumes that $t_{RCD} > t_{RCD}$(max.).

6. Measured with a load equivilent to 2 TTL loads and 100pF.

7. t_{RCD}(min.)=t_{RAH}(min.)+2t_T+t_{ASC}(min.); tT=5nS.

8. t_{WCS} and t_{CWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early-write cycle, and the data out pin will remain open circuit (high impedance) throughout entire cycle.

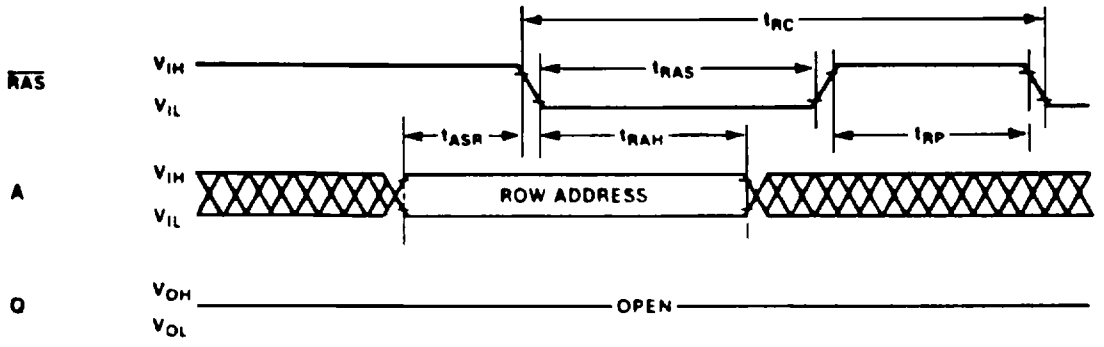
   If $t_{CWD} \geq t_{CWD}$(min.) the cycle is a read-write cycle and data out contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out is indeterminate.

9. Test mode write cycle only.

10. Either t_{RCH} or t_{RRH} must be satsified for a read cycle.

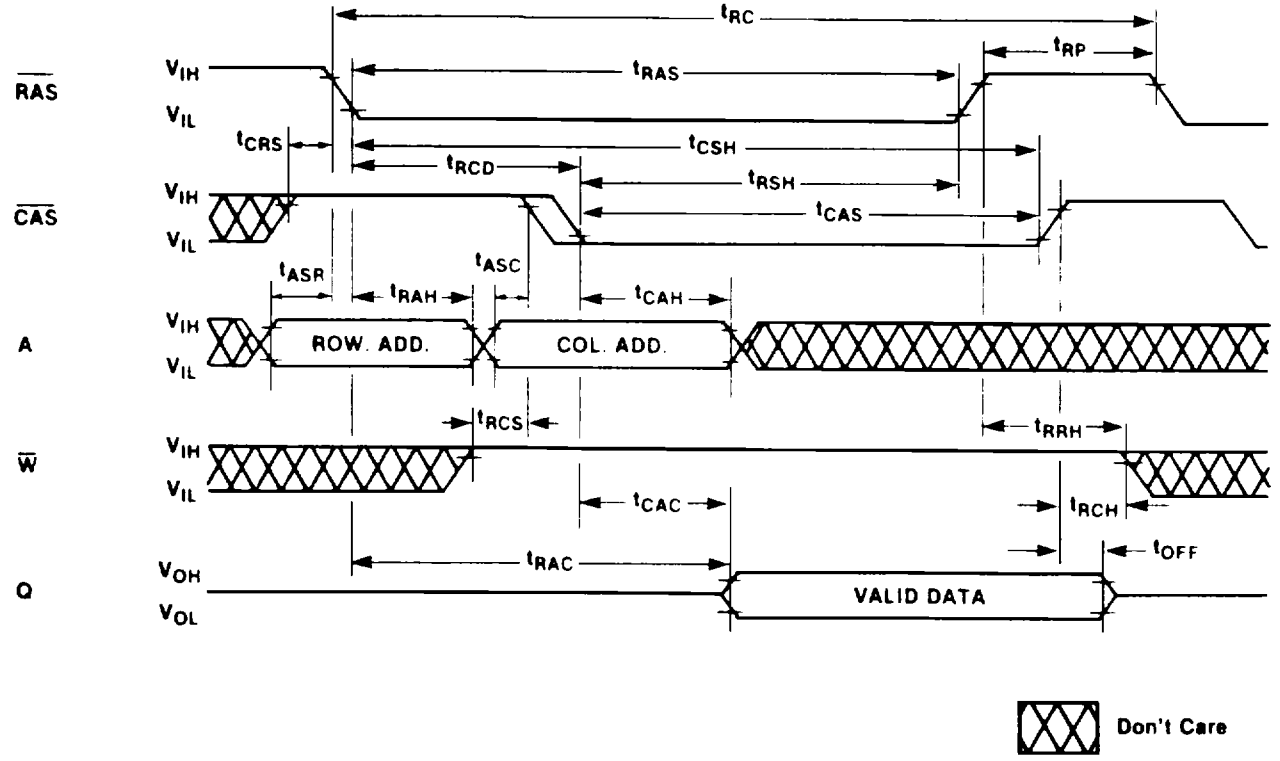
Timing Diagrams

"$\overline{RAS}$-Only" Refresh Cycle

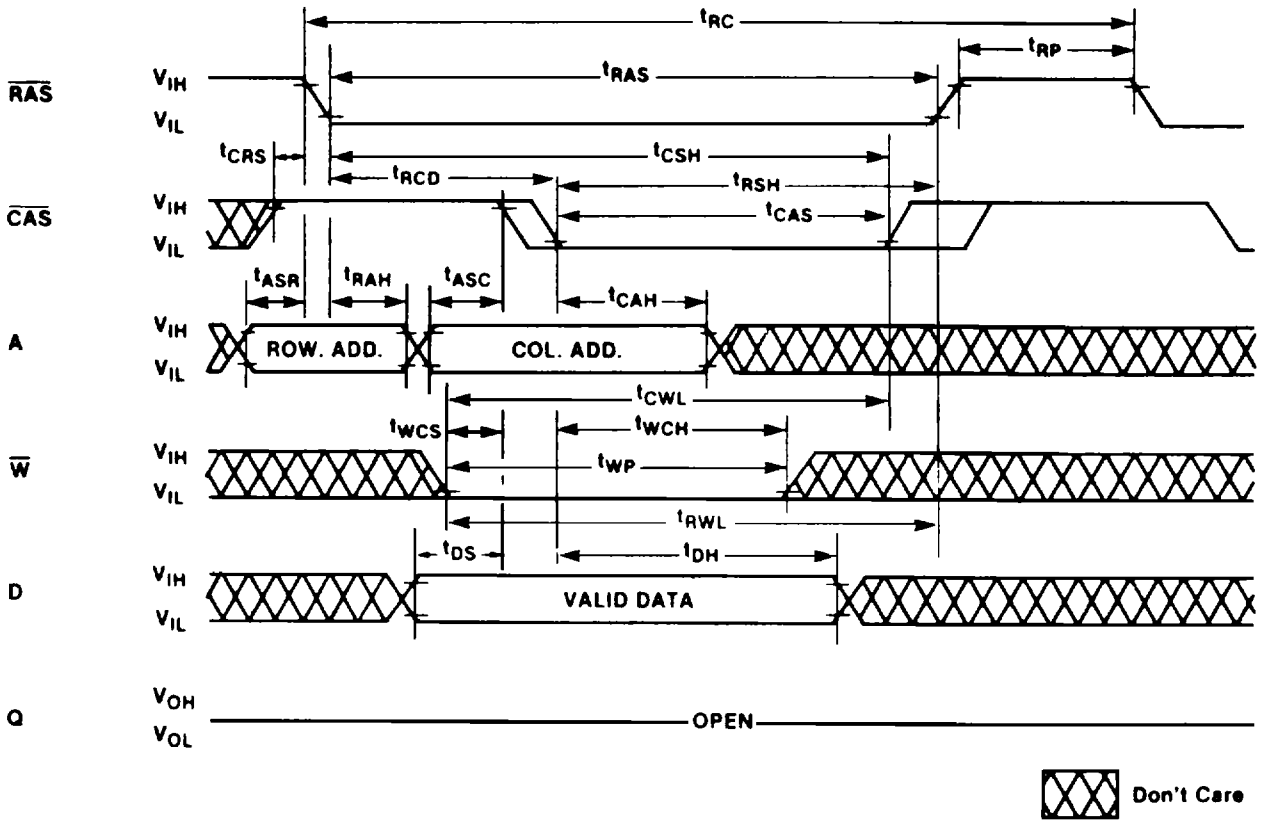


NOTE: $\overline{CAS}$ = V_{IH}. W, D = Don't Care

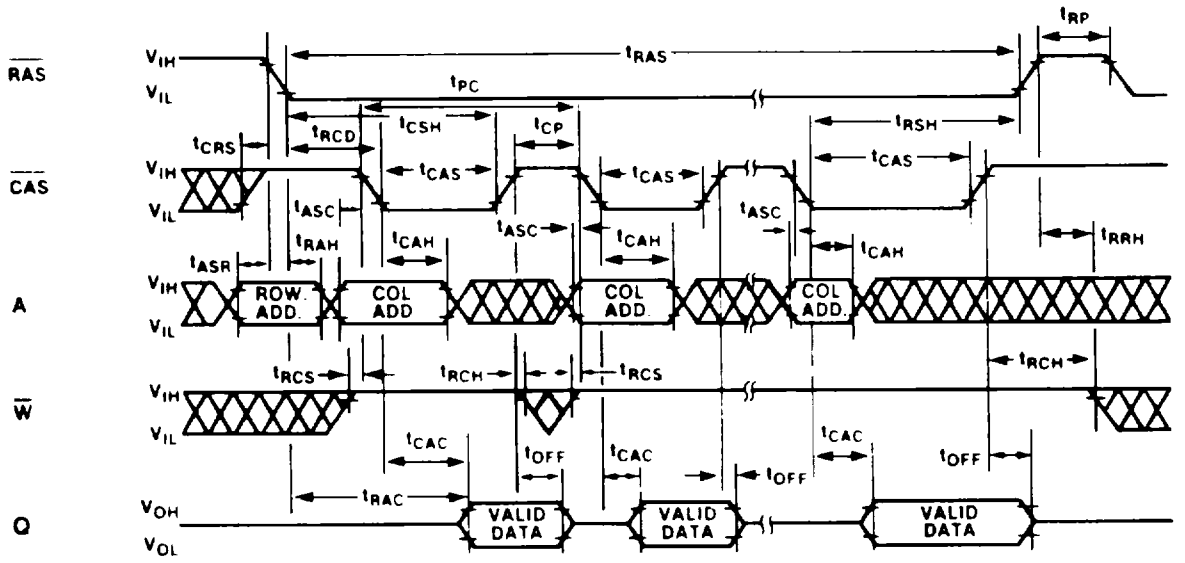
Read Cycle



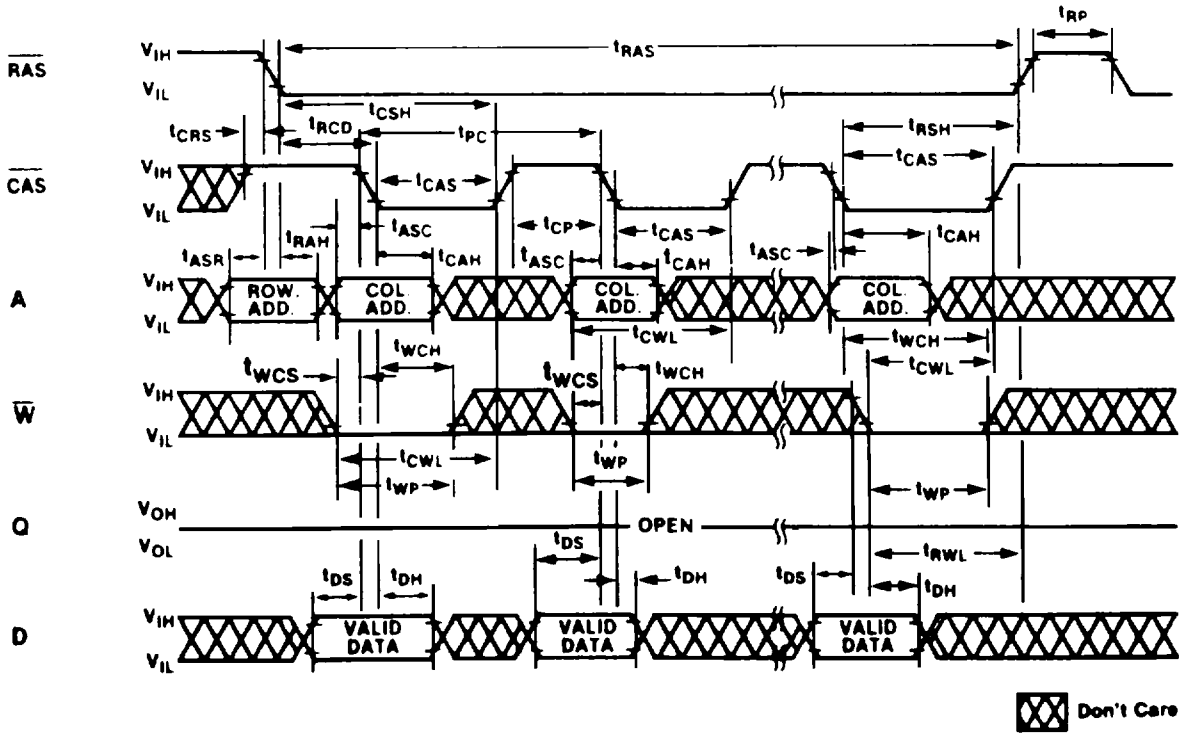
Write Cycle (Early Write)



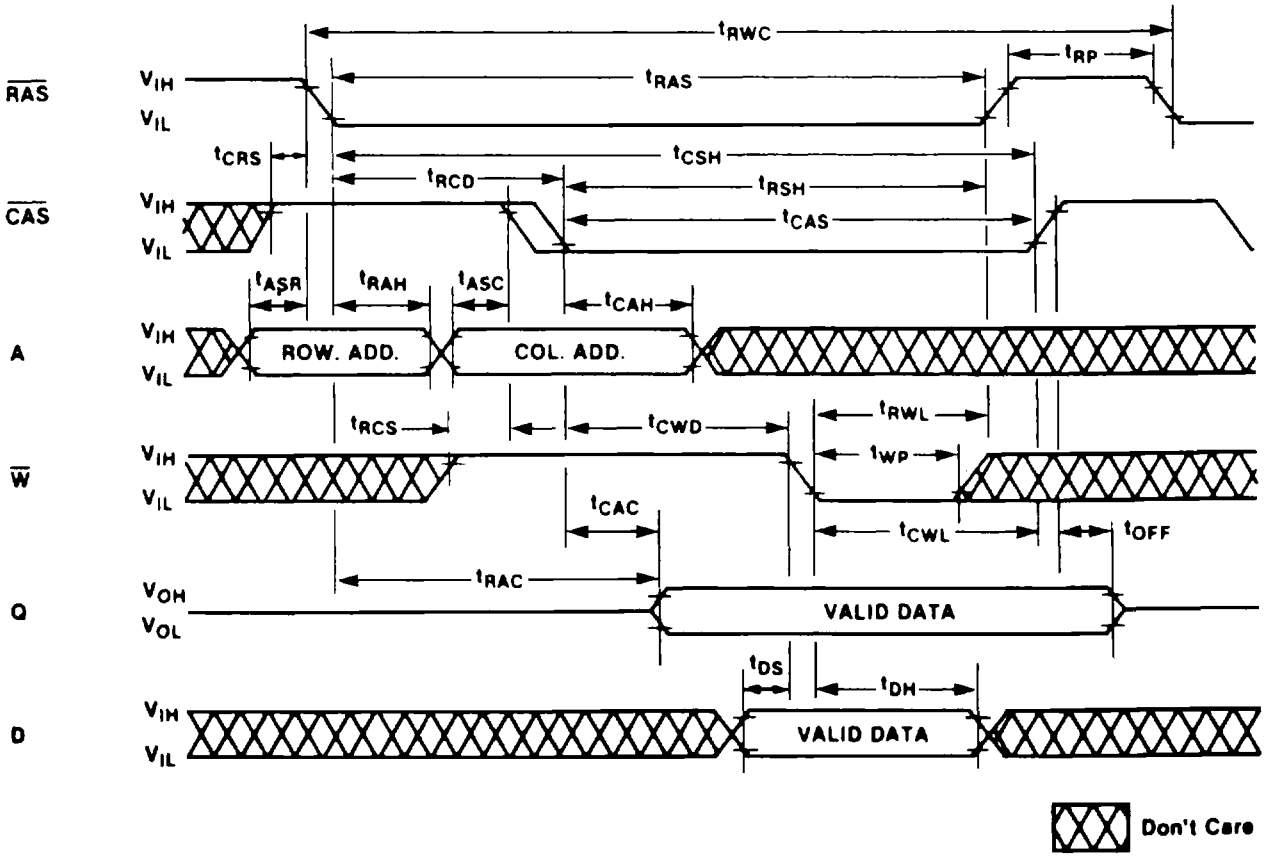
Page Mode Read Cycle



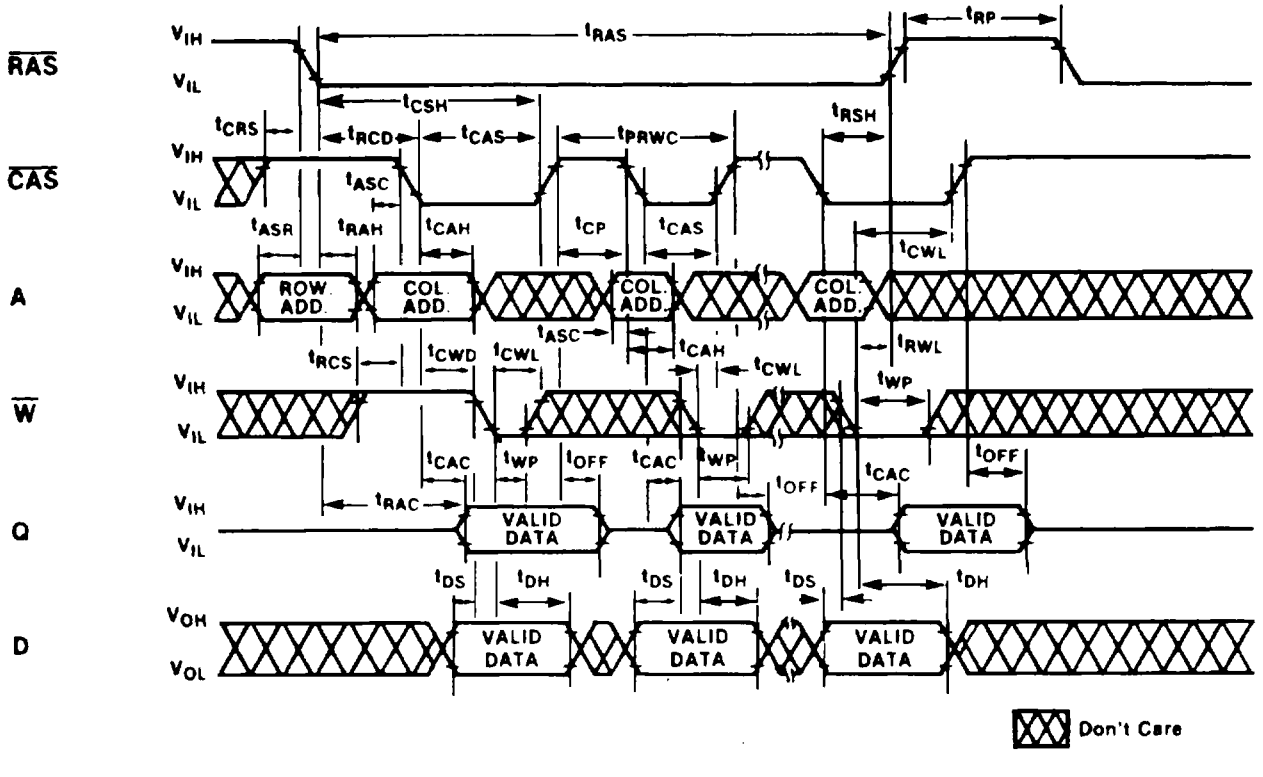
Page Mode Write Cycle



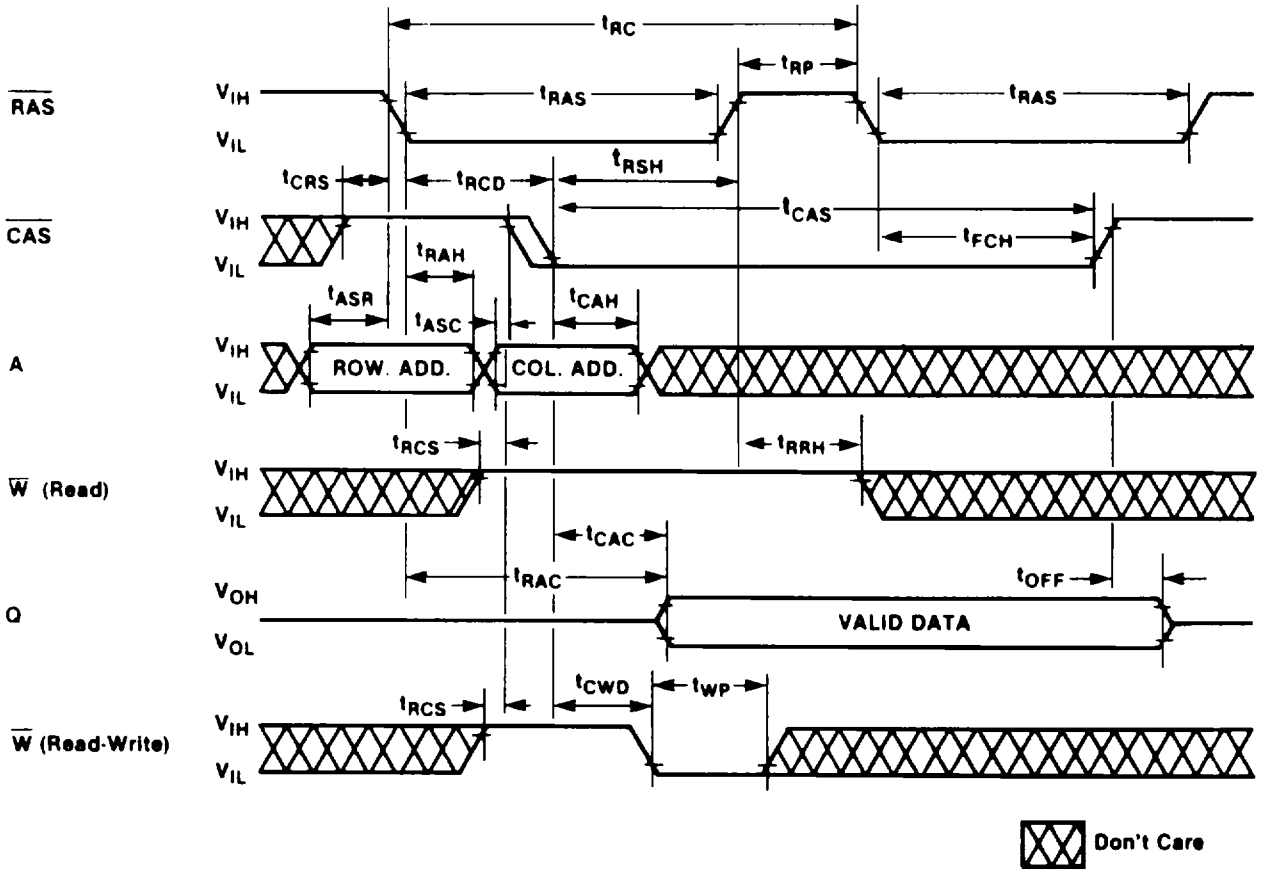
Read-Write/Read-Modify-Write Cycle



Page Mode Read-Write Cycle

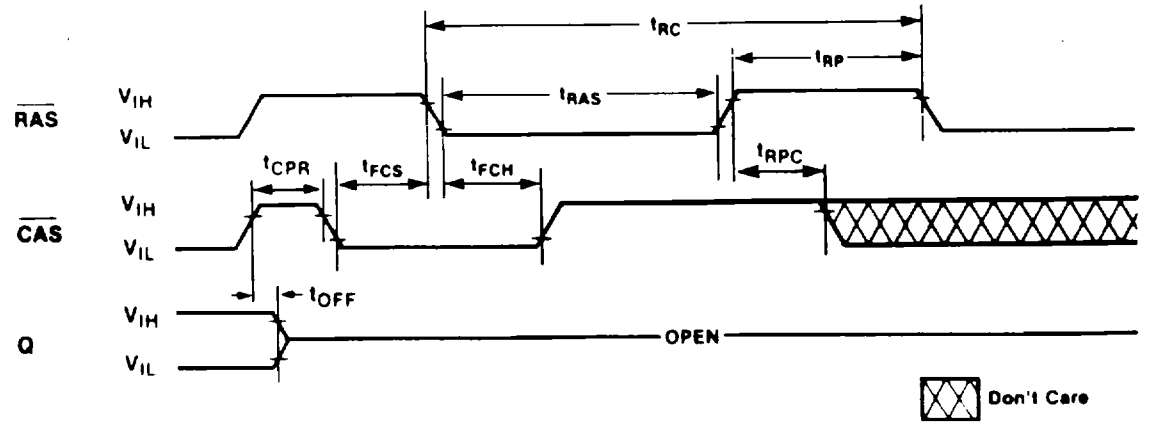


Hidden Refresh Cycle



"CAS-Before-RAS" Refresh Cycle

(when specified)



NOTE: A, W, D = Don't Care

OPERATION

The high density DRAM modules can operate under the condition of tRCD(max.) = tCAC, thus providing optimal timing for address multiplexing. These devices have minimal hold times for Addresses (tCAH), Write-Enable (tWCH) and Data-in (tDH). The hold times of the Column Address, D and W as well as tCWD (CAS to W Delay) are not restricted by tRCD.

The output buffer is controlled by the state of W when CAS goes low. When W is low during a CAS transition to low, the device goes into an early-write mode in which the output floats and the common I/O bus can be used. When W goes low after tCWD following a CAS transition to low, the device goes into the delayed write mode. The output then contains the data from the selected cell and the data from D is written into that cell.

Address Inputs

A total of eighteen binary input address bits are required to decode any one of 262,144 storage cell locations within each of the 256K DRAMs. Nine row-address bits are established on the input pins (A_0 through A_8) and latched with Row Address Strobe (RAS). The nine column-address bits are established on the input pins and latched with the Column Address Strobe (CAS). All input addresses must be stable on or before the falling edge of RAS. CAS is internally inhibited (or "gated") by RAS to permit triggering of CAS as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-address.

Write Enable

The read mode or write mode is selected with the W input. A logic high (1) on W dictates read mode; logic low (0) dicatates when read mode is selected.

Data Input

Data is written into the selected cell during a write or read-write cycle. The last falling edge of W or CAS is a strobe for the Data In (D) register. In a write cycle, if W is brought low (write mode) before CAS, D is strobed by CAS, and the set-up and hold times are referenced to CAS. In a read-write cycle, W will be delayed until CAS has made its negative transition. Thus D is strobed by W and set-up and hold times are referenced to W.

Data Output

Data-out is the same polarity as data-in. The output is is a high impedance state until CAS is brought low. In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of RAS when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of CAS when the transition occurs after t_{RCD} (max). Data Remains valid until CAS is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid. The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads.

Page Mode

Page mode operation permits strobing the row-address into the high density memory while maintaining RAS at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of RAS is saved. Access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

RAS-Only Refresh

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses (A_0 ~ A_7) at least every four milliseconds. RAS-only refresh avoids any output during refresh because the output buffer is in the high impedance state unless CAS is brought low. Strobing each of 256 row-addresses with RAS will cause all bits in each row to be refreshed. RAS-only refresh results in a substantial reduction in power dissipation.

Hidden Refresh

A RAS-ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.

Hidden Refresh is performed by holding CAS at V_{IL} from a previous memory read cycle.

CAS-before-RAS Refresh (specified option)

CAS-before-RAS refreshing is available as an option on 256K DRAM based modules. If CAS is held low for the specified period (tFCS) before RAS goes low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next CAS-before-RAS refresh operation.

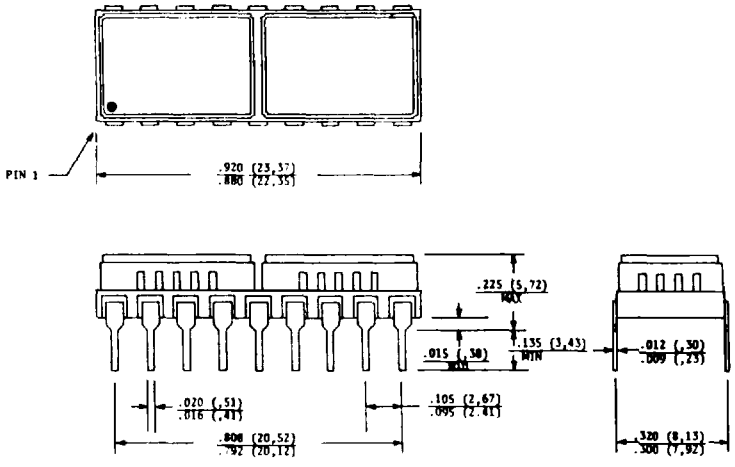
Nibble Mode (specified option)

Nibble mode operation allows faster successive data operation on 4 bits. The first of 4 bits is accessed in the usual manner with read data coming out at tCAC time. By keeping RAS low, CAS can be cycled up and then down, to read or write the next three pages at a high data rate (faster than tCAC). Row and column addresses need only be supplied for first access of the cycles. From then on, the falling edge of CAS will activate the next bit. After four bits have been accessed, the next bit will be the same as the first bit accessed(wrap-around method). A8 determines the starting point of the circular 4 nibble bits. Row A8 and column A8 provide the two binary bits needed to select one of four bits. From then on, successive bits come out in a binary fashion; 00 -> 01 -> 10 -> 11 with A8 row being the least significant address.

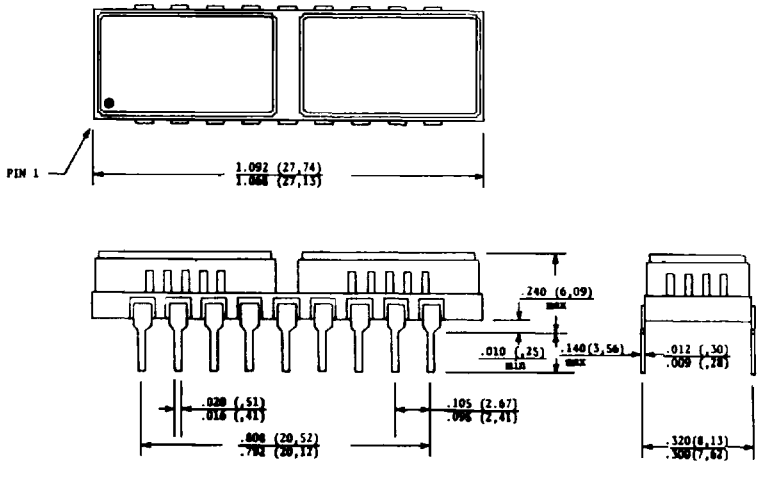
A nibble cycle can be a read, write, or late write cycle. Any combinations of reads and writes or late writes will be allowed. The circular wrap-around will continue for as long as RAS is kept low.

MECHANICAL DIMENSIONS inches (millimeters)

D18C-1

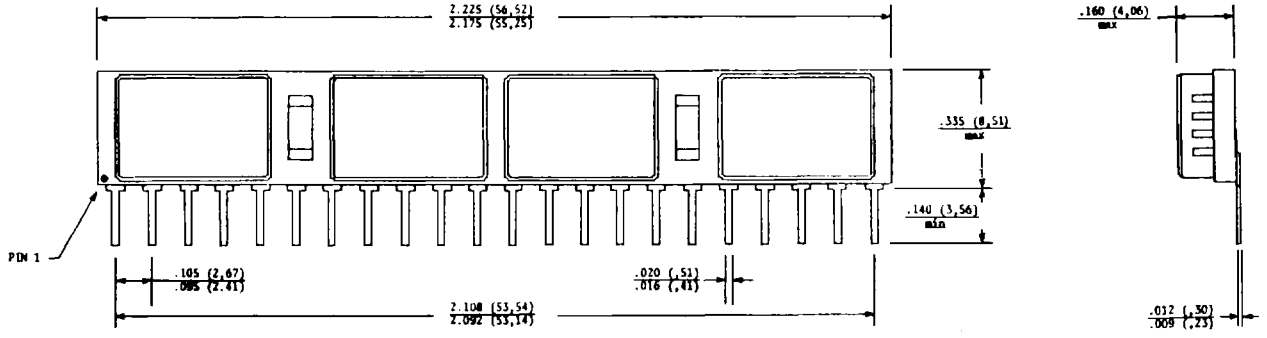


D18C-2

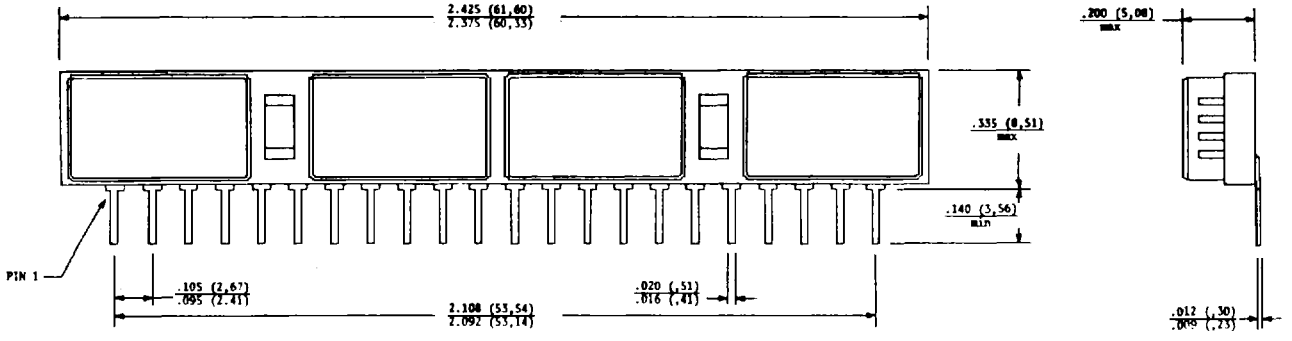


MECHANICAL DIMENSIONS inches (millimeters)

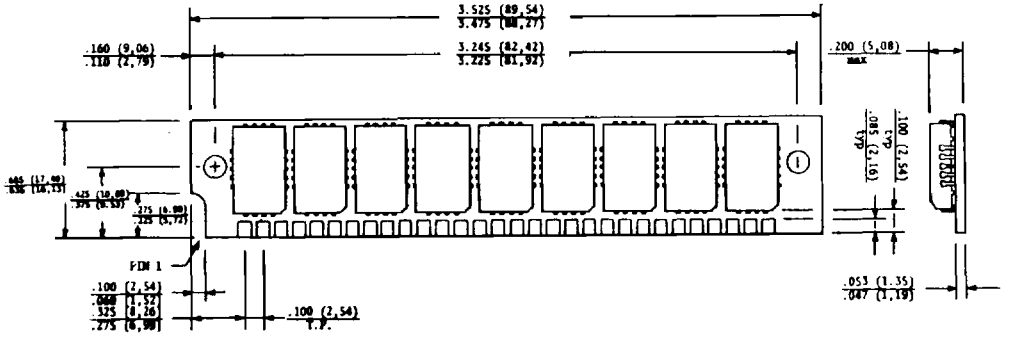
S22C-1



S22C-2



S30P-1



ORDERING INFORMATION

PART NUMBER CODING INTERPRETATION

Position:	1	2	3	4	5	6	7	8	9

1 - Product
AK = Accutek Memory

2 - Type
2 = EPROM
4 = Dynamic RAM
6 = Static RAM
7 = Dual Port RAM
8 = EEPROM

3 - Organization/Word Width
1 = by 1
2 = by 2
4 = by 4
8 = by 8
9 = by 9

4 - Size/Bits Depth
016 = 16K
064 = 64K
256 = 256K
1024 = 1MEG
4096 = 4MEG

5 - Package Type
S = Single In-Line Package (SIP)
P = Plastic DIP
H = Hermetic Ceramic DIP
D = Dual In-Line Package (DIP)

6 - Special Designation
P = Page Mode
N = Nibble Mode
X = Burned In
R = RFSH or CAS-before-RAS refresh

7 - Separator
~ = Commercial (0° to +70°C)
M = Military Equivalent Screened (-55° to +125°C)
I = Industrial Temperature Tested (-45° to +85°C)

8 - Speed (first two significant digits)
45 = 45ns
55 = 55ns
07 = 70ns
10 = 100ns
12 = 120ns
15 = 150ns
20 = 200ns
etc,

9 - Power
Blank = Standard
LP = Low Power

Examples:

AK44256SP-12
256K x 4 Dynamic Ram, SIP, page mode,
Commercial, 120ns Access Time

AK41512HPM15
512K x 1 Dynamic Ram, Hermetic, DIP, page mode,
Military, 150ns Access Time

ACCUTEK MICROCIRCUIT CORPORATION
72 Cherry Hill Drive
Cherry Hill Research Park
Beverly, MA 01915

617-927-4900
TWX 710-347-1660
Telecopier 617-927-0381