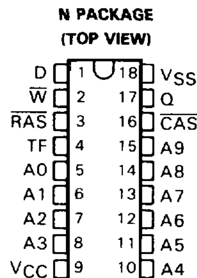
MAY 1986—REVISED MAY 1988

- **1,048,576 × 1 Organization**
- **Single 5-V Supply (10% Tolerance)**
- **Performance Ranges:**

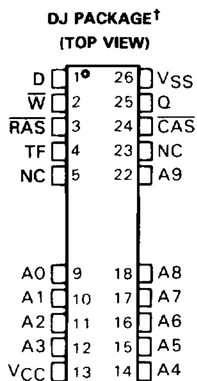
	ACCESS TIME $t_{a(R)}$ (t_{RAC}) (MAX)	ACCESS TIME $t_{a(C)}$ (t_{CAC}) (MAX)	ACCESS TIME $t_{a(CA)}$ (t_{CAA}) (MAX)	READ OR WRITE CYCLE (MIN)
TMS4C102_-10	100 ns	25 ns	45 ns	190 ns
TMS4C102_-12	120 ns	30 ns	55 ns	220 ns
TMS4C102_-15	150 ns	40 ns	70 ns	260 ns

- **TMS4C1024—Enhanced Page Mode Operation for Faster Memory Access**
  - **Higher Data Bandwidth than Conventional Page-Mode Parts**
  - **Random Single-Bit Access Within a Row with a Column Address**
- **TMS4C1025—4-Bit Nibble Mode Operation**
  - **Four Sequential Single Bit Access Within a Row By Toggling $\overline{CAS}$**
- **TMS4C1027—Static Column Decode Mode Operation**
  - **Random Single-Bit Access Within a Row with Only a Column Address Change**
- **One of TI's CMOS Megabit DRAM Family Including:**
  TMS44C256—256K × 4 Enhanced Page Mode
  TMS44C257—256K × 4 Static Column Decode
- **$\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . . 512-Cycle Refresh in 8 ms (Max)**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **Texas Instruments EPIC™ CMOS Process**
- **All Inputs/Outputs and Clocks Are TTL Compatible**
- **High-Reliability Plastic 18-Pin 300-Mil-Wide DIP or 20/26-Lead Surface Mount (SOJ) Packages**
- **Operating Free-Air Temperature 0°C to 70°C**
- **Operations of TI's Megabit CMOS DRAMs Can Be Controlled by TI's SN74ALS6301 and SN74ALS6302 Dynamic RAM Controllers**

N PACKAGE
(TOP VIEW)



DJ PACKAGE†
(TOP VIEW)



†The packages shown here are for pinout reference only. The DJ package is actually 75% of the length of the N package.

PIN NOMENCLATURE	
A0-A9	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data In
NC	No Connection
Q	Data Out
$\overline{RAS}$	Row-Address Strobe
TF	Test Function
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

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description

The TMS4C1024, TMS4C1025, and TMS4C1027 are high-speed, 1,048,576-bit dynamic random-access memories, organized as 1,048,576 words of one bit each. They employ state-of-the-art EPIC™ (Enhanced Process Implanted CMOS) technology for high performance, reliability, and low power at a low cost.

These devices feature maximum $\overline{RAS}$ access times of 100 ns, 120 ns and 150 ns. Maximum power dissipation is as low as 330 mW operating and 16.5 mW standby on 120 ns devices.

The EPIC™ technology permits operation from a single 5-V supply, reducing system power supply and decoupling requirements, and easing board layout. I_{CC} peaks are 140 mA typical, and a − 1-V input voltage undershoot can be tolerated, minimizing system noise considerations.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS4C102_ are offered in 18-pin plastic dual-in-line (N-suffix) and 20/26-lead plastic surface mount SOJ (DJ suffix) packages. These packages are guaranteed for operation from 0°C to 70°C.

operation

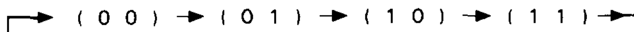
enhanced page mode (TMS4C1024)

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page cycle time used. With minimum $\overline{CAS}$ page cycle time, all 1024 columns specified by column addresses A0 through A9 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the TMS4C1024 to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as "enhanced page mode." Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after $t_{a(C)}$ max (access time from $\overline{CAS}$ low), if $t_{a(CA)}$ max (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of $t_{a(C)}$ or $t_{a(CP)}$ (access time from rising edge of $\overline{CAS}$).

nibble mode (TMS4C1025)

Nibble-mode operation allows high-speed read, write, or read-write-modify-write access of 1 to 4 bits of data. The first bit is accessed in the normal manner with read data coming out at $t_{a(C)}$ time as long as $t_{a(R)}$ and $t_{a(CA)}$ are satisfied. The next sequential bits can be read or written by cycling $\overline{CAS}$ while $\overline{RAS}$ remains low. The first bit is determined by the row and column addresses, which need to be supplied only for the first access. Row A9 and column A9 provide the two binary bits for initial selection, with row A9 being the least-significant address and column A9 being the most significant. Thereafter, the falling edge of $\overline{CAS}$ will access the next bit of the circular 4-bit nibble in the following sequence.



Data written in a sequence of more than 4 consecutive cycles shall be capable of being read back without exiting from the nibble mode. In a sequence of consecutive nibble-mode cycles the control of the high-impedance state for the data out (Q) pin is determined by each individual cycle. This facilitates fully mixed nibble-mode cycles (e.g., read/write/read-modify-write/read etc.).

static column decode mode (TMS4C1027)

The static column decode mode of operation allows high-speed read, write, or read-modify-write by reducing the number of required signal setup, hold, and transition timings. This is achieved by first addressing the row and column in the normal manner, but after the first access, maintaining $\overline{CAS}$ low. Subsequently changing the column address produces valid data at $t_{a(CA)}$. The first bit is accessed in the normal manner with read coming out at $t_{a(R)}$ time. Similarly, write or read-modify-write cycle times can be achieved with appropriate toggling of $\overline{W}$. The addresses are latched during the write operation, but at the completion of the internal write operation the addresses are unlatched.

address (A0 through A9) (TMS4C1024, TMS4C1025)

Twenty address bits are required to decode 1 of 1,048,576 storage cell locations. Ten row-address bits are set up on inputs A0 through A9 and latched onto the chip by the row-address strobe ($\overline{RAS}$). The ten column-address bits are set up on pins A0 through A9 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the output buffer, as well as latching the address bits into the column-address buffer.

address (A0 through A9) (TMS4C1027)

Twenty address bits are required to decode 1 of 1,048,576 storage cell locations. Ten row-address bits are set up on inputs A0 through A9 and latched onto the chip by the row-address strobe ($\overline{RAS}$). The ten column-address bits are set up on pins A0 through A9. Row addresses must be stable on or before the falling edges of $\overline{RAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. In a write cycle, the later of $\overline{CAS}$ or $\overline{W}$ latches the column address bits.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle, permitting common I/O operation.

data in (D)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output becomes valid after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ and $t_{a(CA)}$ are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In a delayed-write or read-modify-write cycle, the output will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least once every eight milliseconds to retain data. This can be achieved by strobing each of the 512 rows (A0-A8). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level,

thus conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{\mathrm{RAS}}$-only refresh. Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{\mathrm{CAS}}$ at V_{IL} after a read operation and cycling $\overline{\mathrm{RAS}}$ after a specified precharge period, similar to a $\overline{\mathrm{RAS}}$-only refresh cycle.

$\overline{\mathrm{CAS}}$-before-$\overline{\mathrm{RAS}}$ refresh

$\overline{\mathrm{CAS}}$-before-$\overline{\mathrm{RAS}}$ refresh is utilized by bringing $\overline{\mathrm{CAS}}$ low earlier than $\overline{\mathrm{RAS}}$ [see parameter $t_{d(CLRL)R}$] and holding it low after $\overline{\mathrm{RAS}}$ falls [see parameter $t_{d(RLCH)R}$]. For successive $\overline{\mathrm{CAS}}$-before-$\overline{\mathrm{RAS}}$ refresh cycles, $\overline{\mathrm{CAS}}$ can remain low while cycling $\overline{\mathrm{RAS}}$. The external address is ignored and the refresh address is generated internally. The external address is also ignored during the hidden refresh cycles.

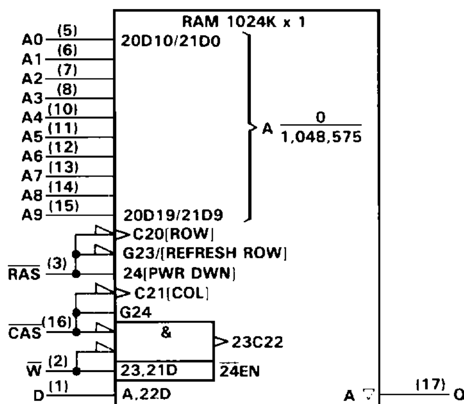
power up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved.

test-function pin

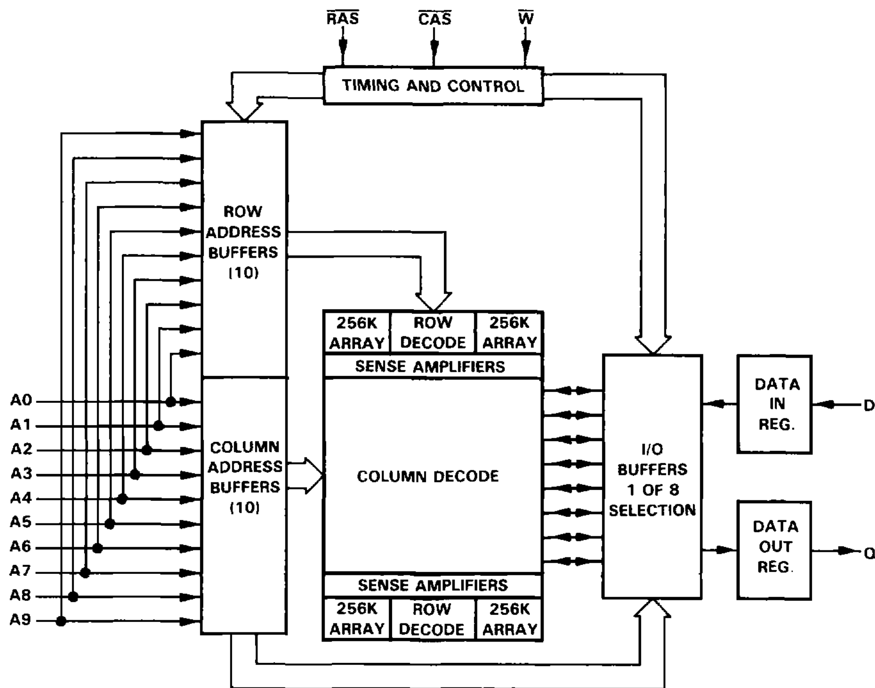
During normal device operation the TF pin must either be disconnected or biased at a voltage less than or equal to V_{CC}.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown are for the 18-pin dual-in-line package.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin . . . . −1 V to 7 V
Voltage range on V_{CC} . . . . −1 V to 7 V
Short circuit output current . . . . 50 mA
Power dissipation . . . . 1 W
Operating free-air temperature range . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS4C1024-10 TMS4C1025-10 TMS4C1027-10		TMS4C1024-12 TMS4C1025-12 TMS4C1027-12		TMS4C1024-15 TMS4C1025-15 TMS4C1027-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{CC} = 5.5 V, All other pins = 0 V to V_{CC}		±10		±10		±10	μA
I_O	Output current (leakage)	V_O = 0 V to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		±10		±10		±10	μA
I_{CC1}	Read or write cycle current	Minimum cycle, V_{CC} = 5.5 V		70		60		55	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V		3		3		3	mA
I_{CC3}	Average refresh current	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high		65		55		50	mA
I_{CC4}	Average page current (TMS4C1024)	$t_{c(P)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		45		35		30	mA
I_{CC5}	Average nibble current (TMS4C1025)	$t_{c(N)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling for 4 cycles		45		40		30	mA
I_{CC6}	Average static column decode current (TMS4C1027)	$t_{c(rdW)SC}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		45		35		30	mA

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capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz (see Note 3)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		6	pF
$C_{i(D)}$	Input capacitance, data input		5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		7	pF
$C_{i(W)}$	Input capacitance, write-enable input		7	pF
C_o	Output capacitance		7	pF

NOTE 3: V_{CC} equal to 5.0 V ± 0.5 V and the bias on pins under test is 0.0 V.

switching characteristics over recommended supply voltage range and operating free-air temperature range (see Figure 1)

PARAMETER		ALT. SYMBOL	TMS4C102_-10		TMS4C102_-12		TMS4C102_-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$ low†	t_{CAC}		25		30		40	ns
$t_{a(CA)}$	Access time from column-address†	t_{CAA}		45		55		70	ns
$t_{a(R)}$	Access time from $\overline{RAS}$ low†	t_{RAC}		100		120		150	ns
$t_{a(CP)}$	Access time from column precharge (TMS4C1024 only)	t_{CAP}		50		60		75	ns
$t_{a(C)N}$	Access time from $\overline{CAS}$ low (TMS4C1025 only)	t_{NCAC}		20		25		35	ns
$t_{a(WHQ)}$	Access time from $\overline{W}$ high (TMS4C1027 only)	t_{WRA}		30		35		40	ns
$t_{a(WLQ)}$	Access time from $\overline{W}$ low (TMS4C1027 only)	t_{ALW}		95		115		120	ns
$t_{h(CAQ)}$	Static column decode mode output hold time after address change (TMS4C1027 only)	t_{AOH}	5		5		5		ns
$t_{h(WQ)}$	Static column decode mode output hold time after $\overline{W}$ low (TMS4C1027 only)	t_{WOH}	0		0		0		ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high (see Note 4)†	t_{OFF}	0	25	0	30	0	35	ns

†Parameters apply uniformly to TMS4C1024, TMS4C1025, TMS4C1027.
NOTE 4: $t_{dis(CH)}$ is specified when the output is no longer driven.

PARAMETER MEASUREMENT INFORMATION

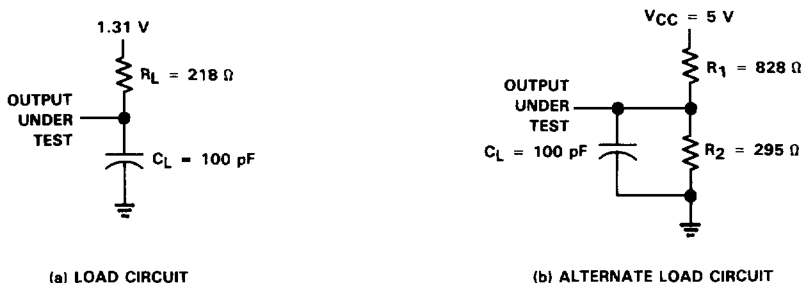

FIGURE 1. LOAD CIRCUITS FOR TIMING PARAMETERS

timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TMS4C1024-10		TMS4C1024-12		TMS4C1024-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time (see Note 6)	t_{RC}	190		220		260		ns
$t_{c(W)}$	Write cycle time	t_{WC}	190		220		260		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	220		255		305		ns
$t_{c(P)}$	Page-mode read or write cycle time (see Note 7)	t_{PC}	55		65		80		ns
$t_{c(PM)}$	Page-mode read-modify-write cycle time	t_{PCM}	85		100		125		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CP}	10		15		25		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 8)	t_{CAS}	25	10,000	30	10,000	40	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge)	t_{RP}	80		90		100		ns
$t_{w(RL)}$	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	t_{RAS}	100	10,000	120	10,000	150	10,000	ns
$t_{w(RL)P}$	Page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	t_{RASP}	100	100,000	120	100,000	150	100,000	ns
$t_{w(WL)}$	Write pulse duration	t_{WP}	15		20		25		ns
$t_{su(CA)}$	Column-address setup time before $\overline{CAS}$ low	t_{ASC}	0		0		0		ns
$t_{su(RA)}$	Row-address setup time before $\overline{RAS}$ low	t_{ASR}	0		0		0		ns
$t_{su(D)}$	Data setup time (see Note 10)	t_{DS}	0		0		0		ns
$t_{su(rd)}$	Read setup time before $\overline{CAS}$ low	t_{RCS}	0		0		0		ns
$t_{su(WCL)}$	$\overline{W}$-low setup time before $\overline{CAS}$ low (see Note 11)	t_{WCS}	0		0		0		ns
$t_{su(WCH)}$	$\overline{W}$-low setup time before $\overline{CAS}$ high	t_{CWL}	25		30		40		ns
$t_{su(WRH)}$	$\overline{W}$-low setup time before $\overline{RAS}$ high	t_{RWL}	25		30		40		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	20		20		25		ns
$t_{h(RA)}$	Row-address hold time after $\overline{RAS}$ low	t_{RAH}	15		15		20		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low (see Note 12)	t_{AR}	70		80		100		ns
$t_{h(D)}$	Data hold time (see Note 10)	t_{DH}	20		25		30		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low (see Note 12)	t_{DHR}	70		85		110		ns
$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ high (see Note 15)	t_{RCH}	0		0		0		ns
$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ high (see Note 15)	t_{RRH}	10		10		10		ns
$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low (see Note 11)	t_{WCH}	20		25		30		ns
$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low (see Note 12)	t_{WCR}	70		85		100		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	100		120		150		ns
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	25		30		40		ns
$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Note 13)	t_{CWD}	25		30		40		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	t_{RCD}	25	80	25	95	30	115	ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column-address (see Note 14)	t_{RAD}	20	55	20	65	25	80	ns

Continued next page.

NOTES:

5. Timing measurements in this table are referenced to V_{IL} max and V_{IH} min.
6. All cycle times assume t_t = 5 ns.
7. To guarantee $t_{c(P)}$ min, $t_{su(CA)}$ should be greater than or equal to $t_{w(CH)}$.
8. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed.
9. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed.
10. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
11. Early write operation only.
12. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
13. Read-modify-write operation only.
14. Maximum value specified only to guarantee access time.
15. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.

timing requirements over recommended supply voltage range and operating free-air temperature range (concluded)

		ALT. SYMBOL	TMS4C1024-10		TMS4C1024-12		TMS4C1024-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{d(CARH)}$	Delay time, column-address to $\overline{RAS}$ high	t_{RAL}	45		55		70		ns
$t_{d(CACH)}$	Delay time, column-address to $\overline{CAS}$ high	t_{CAL}	45		55		70		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 13)	t_{RWD}	100		120		150		ns
$t_{d(CAWL)}$	Delay time, column address to $\overline{W}$ low (see Note 13)	t_{AWD}	45		55		70		ns
$t_{d(RLCH)R}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high, (see Note 16)	t_{CHR}	25		25		30		ns
$t_{d(CLRL)R}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low, (see Note 16)	t_{CSR}	10		10		15		ns
$t_{d(RHCL)R}$	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	t_{RPC}	0		0		0		ns
t_{rf}	Refresh time interval	t_{REF}		8		8		8	ms
t_t	Transition time	t_T	3	50	3	50	3	50	ns

NOTES: 13. Read-modify-write operation only.
16. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.

timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TMS4C1025-10		TMS4C1025-12		TMS4C1025-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time (see Note 6)	t_{RC}	190		220		260		ns
$t_{c(W)}$	Write cycle time	t_{WC}	190		220		260		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	220		255		305		ns
$t_{c(N)}$	Nibble-mode read or write cycle time	t_{NC}	40		50		70		ns
$t_{c(rdW)N}$	Nibble-mode read-modify-write cycle time	t_{NRMW}	65		75		110		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CP}	10		15		25		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 8)	t_{CAS}	20	10,000	25	10,000	35	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge)	t_{RP}	80		90		100		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low (see Note 9)	t_{RAS}	100	10,000	120	10,000	150	10,000	ns
$t_{w(WL)}$	Write pulse duration	t_{WP}	15		20		25		ns
$t_{su(CA)}$	Column-address setup time before $\overline{CAS}$ low	t_{ASC}	0		0		0		ns
$t_{su(RA)}$	Row-address setup time before $\overline{RAS}$ low	t_{ASR}	0		0		0		ns
$t_{su(D)}$	Data setup time (see Note 10)	t_{DS}	0		0		0		ns
$t_{su(rd)}$	Read setup time before $\overline{CAS}$ low	t_{RCS}	0		0		0		ns
$t_{su(WCL)}$	$\overline{W}$-low setup time before $\overline{CAS}$ low (see Note 11)	t_{WCS}	0		0		0		ns
$t_{su(WCH)}$	$\overline{W}$-low setup time before $\overline{CAS}$ high	t_{CWL}	20		25		35		ns
$t_{su(WRH)}$	$\overline{W}$-low setup time before $\overline{RAS}$ high	t_{RWL}	20		25		35		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	20		20		25		ns
$t_{h(RA)}$	Row-address hold time after $\overline{RAS}$ low	t_{RAH}	15		15		20		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low (see Note 12)	t_{AR}	70		80		100		ns
$t_{h(D)}$	Data hold time (see Note 10)	t_{DH}	20		25		35		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low (see Note 12)	t_{DHR}	70		85		110		ns
$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ high	t_{RCH}	0		0		0		ns
$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ high	t_{RRH}	10		10		10		ns
$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low (see Note 11)	t_{WCH}	20		25		30		ns
$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low (see Notes 11 and 12)	t_{WCR}	70		85		100		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	100		120		150		ns
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	20		25		35		ns
$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Note 13)	t_{CWD}	20		25		35		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	t_{RCD}	25	80	25	95	30	115	ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column-address (see Note 14)	t_{RAD}	20	55	20	65	25	80	ns

Continued next page.

NOTES:

5. Timing measurements in this table are referenced to V_{IL} max and V_{IH} min.
6. All cycle times assume t_t = 5 ns.
8. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed.
9. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed.
10. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
11. Early write operation only.
12. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
13. Read-modify-write operation only.
14. Maximum value specified only to guarantee access time.

timing requirements over recommended supply voltage range and operating free-air temperature range (concluded)

		ALT. SYMBOL	TMS4C1025-10		TMS4C1025-12		TMS4C1025-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{d(CARH)}$	Delay time, column-address to $\overline{RAS}$ high	t_{RAL}	45		55		70		ns
$t_{d(CACH)}$	Delay time, column-address to $\overline{CAS}$ high	t_{CAL}	45		55		70		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 13)	t_{RWD}	100		120		150		ns
$t_{d(CAWL)}$	Delay time, column address to $\overline{W}$ low (see Note 13)	t_{AWD}	45		55		70		ns
$t_{d(RLCH)R}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 16)	t_{CHR}	25		25		30		ns
$t_{d(CLRL)R}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 16)	t_{CSR}	10		10		15		ns
$t_{d(RHCL)R}$	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	t_{RPC}	0		0		0		ns
t_{rf}	Refresh time interval	t_{REF}		8		8		8	ms
t_t	Transition time	t_T	3	50	3	50	3	50	ns

NOTES: 13. Read-modify-write operation only.
16. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.

timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TMS4C1027-10 MIN	TMS4C1027-10 MAX	TMS4C1027-12 MIN	TMS4C1027-12 MAX	TMS4C1027-15 MIN	TMS4C1027-15 MAX	UNIT
$t_{c(rd)}$	Read cycle time (see Note 6)	t_{RC}	190		220		260		ns
$t_{c(W)}$	Write cycle time	t_{WC}	190		220		260		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	220		255		305		ns
$t_{c(rd)SC}$	Static column decode mode read cycle time	t_{SCR}	50		60		90		ns
$t_{c(W)SC}$	Static column decode mode write cycle time	t_{SCW}	50		60		90		ns
$t_{c(rdW)SC}$	Static column decode mode, read-modify-write cycle time	t_{SCRDW}	100		120		150		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CP}	10		15		25		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 8)	t_{CAS}	25	10,000	30	10,000	40	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge)	t_{RP}	80		90		100		ns
$t_{w(RL)}$	Non-static column decode mode pulse duration, $\overline{RAS}$ low (see Note 9)	t_{RAS}	100	10,000	120	10,000	150	10,000	ns
$t_{w(RL)P}$	Static column decode mode pulse duration, $\overline{RAS}$ low (see Note 9)	t_{RASP}	100	100,000	120	100,000	150	100,000	ns
$t_{w(WL)}$	Write pulse duration	t_{WP}	15		20		25		ns
$t_{w(CA)}$	Static column decode mode column-address pulse duration	t_{ADP}	45		55		70		ns
$t_{w(WH)}$	Static column decode mode $\overline{W}$ high pulse duration, inactive	t_{WI}	10		15		25		ns
$t_{su(CA)}$	Column-address setup time before $\overline{CAS}$, $\overline{W}$ low (see Note 10)	t_{ASC}	0		0		0		ns
$t_{su(CAR)}$	Column-address setup time before $\overline{RAS}$	t_{CAR}	50		60		75		ns
$t_{su(RA)}$	Row-address setup time before $\overline{RAS}$ low	t_{ASR}	0		0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		0		ns
$t_{su(rd)}$	Read setup time before $\overline{CAS}$ low	t_{RCS}	0		0		0		ns
$t_{su(WCL)}$	$\overline{W}$-low setup time before $\overline{CAS}$ low (see Note 11)	t_{WCS}	0		0		0		ns
$t_{su(WCH)}$	$\overline{W}$-low setup time before $\overline{CAS}$ high	t_{CWL}	25		30		40		ns
$t_{su(WRH)}$	$\overline{W}$-low setup time before $\overline{RAS}$ high	t_{RWL}	25		30		40		ns
$t_{su(WHCH)}$	Setup time, $\overline{W}$ high to $\overline{CAS}$ high for early write, high impedance	t_{WH}	0		0		0		ns
$t_{h(CA)}$	Column-address hold time after $\overline{CAS}$, $\overline{W}$ low (see Note 10)	t_{CAH}	20		20		25		ns
$t_{h(RA)}$	Row-address hold time after $\overline{RAS}$ low	t_{RAH}	15		15		20		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low (see Note 18)	t_{AR}	100		120		150		ns

Continued next page.

NOTES:

5. Timing measurements in this table are referenced to V_{IL} max and V_{IH} min.
6. All cycle times assume t_t = 5 ns.
8. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed.
9. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed.
10. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
11. Early write operation only.
18. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.

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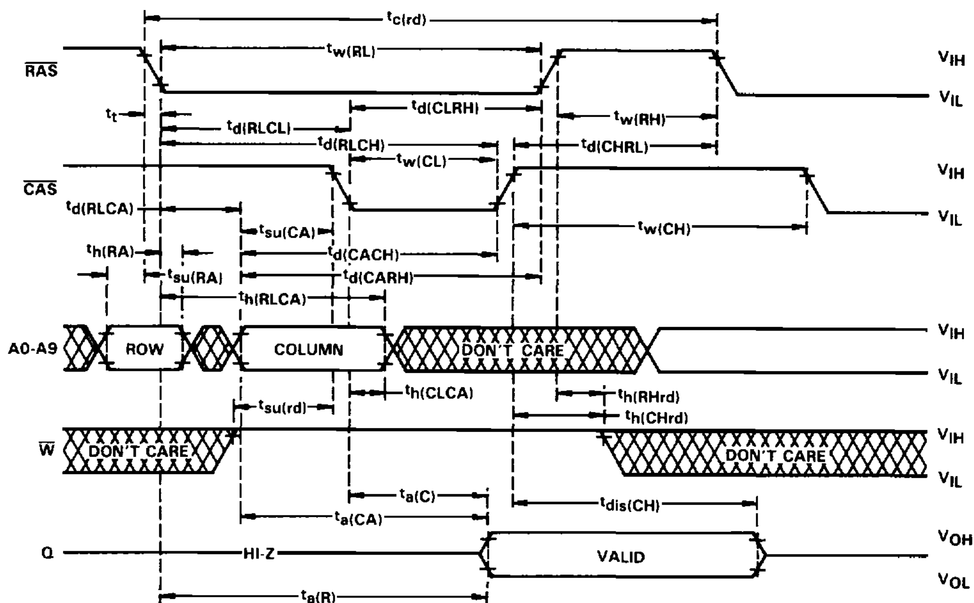
timing requirements over recommended supply voltage range and operating free-air temperature range (concluded)

		ALT. SYMBOL	TMS4C1027-10		TMS4C1027-12		TMS4C1027-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{h(D)}$	Data hold time (see Note 10)	t_{DH}	20		25		30		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low (see Note 17)	t_{DHR}	70		85		110		ns
$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ high (see Note 18)	t_{RCH}	0		0		0		ns
$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ high (see Note 18)	t_{RRH}	10		10		10		ns
$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low (see Note 11)	t_{WCH}	20		25		30		ns
$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low (see Note 17)	t_{WCR}	70		85		100		ns
$t_{h(RHCA)}$	Column-address hold time after $\overline{RAS}$ high	t_{AH}	10		15		15		ns
$t_{h(WLCA2)}$	Static column decode mode second column-address hold time after $\overline{W}$ low (see Note 13)	t_{AHLW}	95		115		135		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	100		120		150		ns
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	25		30		40		ns
$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Note 13)	t_{CWD}	25		30		40		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	t_{RCD}	25	80	25	95	30	115	ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column address (see Note 14)	t_{RAD}	20	55	20	65	25	80	ns
$t_{d(WLCA)}$	Delay time, $\overline{W}$ low to column address	t_{LWAD}	25	50	30	60	35	70	ns
$t_{d(CARH)}$	Delay time, column-address to $\overline{RAS}$ high	t_{RAL}	45		55		70		ns
$t_{d(CACH)}$	Delay time, column-address to $\overline{CAS}$ high	t_{CAL}	45		55		70		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 13)	t_{RWD}	100		120		150		ns
$t_{d(RLWL2)}$	Static column decode mode delay time, $\overline{RAS}$ low to second $\overline{W}$ low	t_{RSW}	100		120		150		ns
$t_{d(CAWL)}$	Delay time, column address to $\overline{W}$ low (see Note 13)	t_{AWD}	45		55		70		ns
$t_{d(WQ)}$	Delay time, $\overline{W}$ high to output transition from high impedance to active	t_{OW}	0		0		0		ns
$t_{d(RLCH)R}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high, (see Note 16)	t_{CHR}	25		25		30		ns
$t_{d(CLRL)R}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 16)	t_{CSR}	10		10		15		ns
$t_{d(RHCL)R}$	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 16)	t_{RPC}	0		0		0		ns
t_{rf}	Refresh time interval	t_{REF}		8		8		8	ms
t_t	Transition time	t_T	3	50	3	50	3	50	ns

NOTES:

10. Referenced to later of $\overline{CAS}$ or $\overline{W}$ in write operations.
11. Early write operation only.
13. Read-modify-write operation only.
14. Maximum value specified only to guarantee access time.
16. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.
17. The minimum value is measured when $t_{d(RLCA)}$ is set to $t_{d(RLCA)}$ min as a reference.
18. Either $t_{h(RDrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.

read cycle timing



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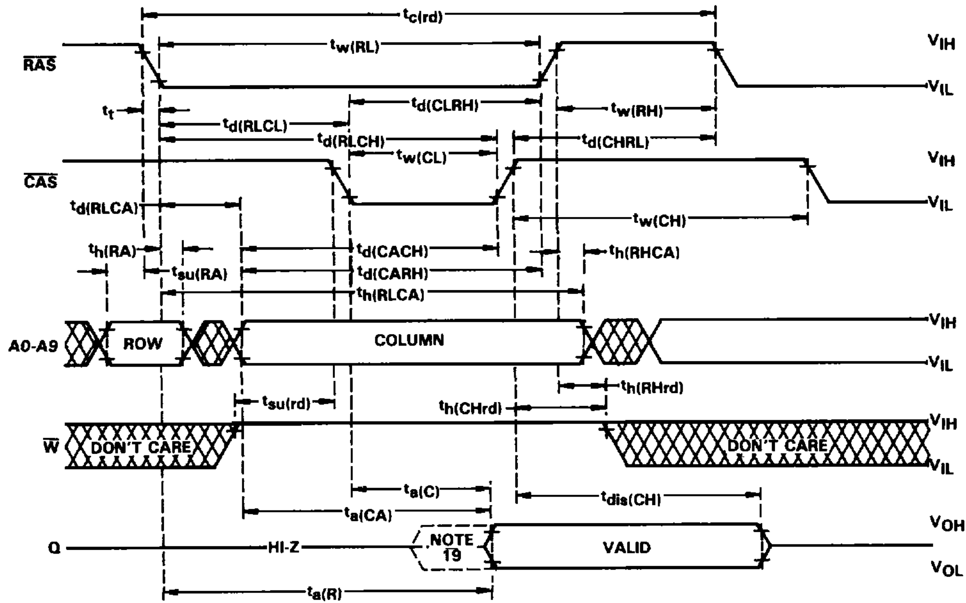
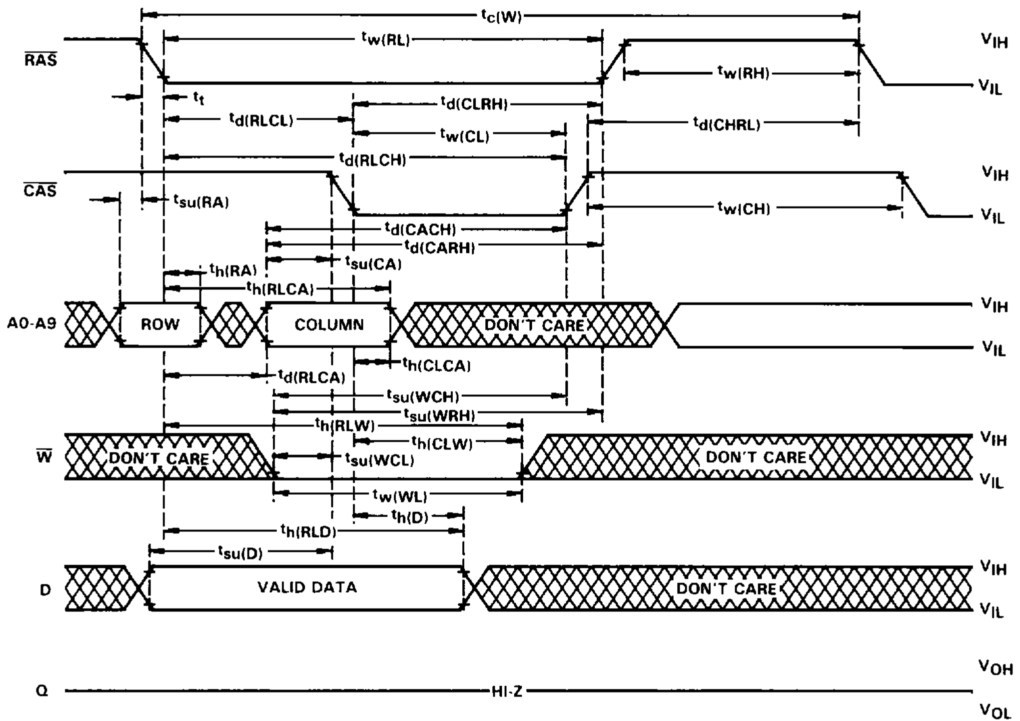
read cycle timing

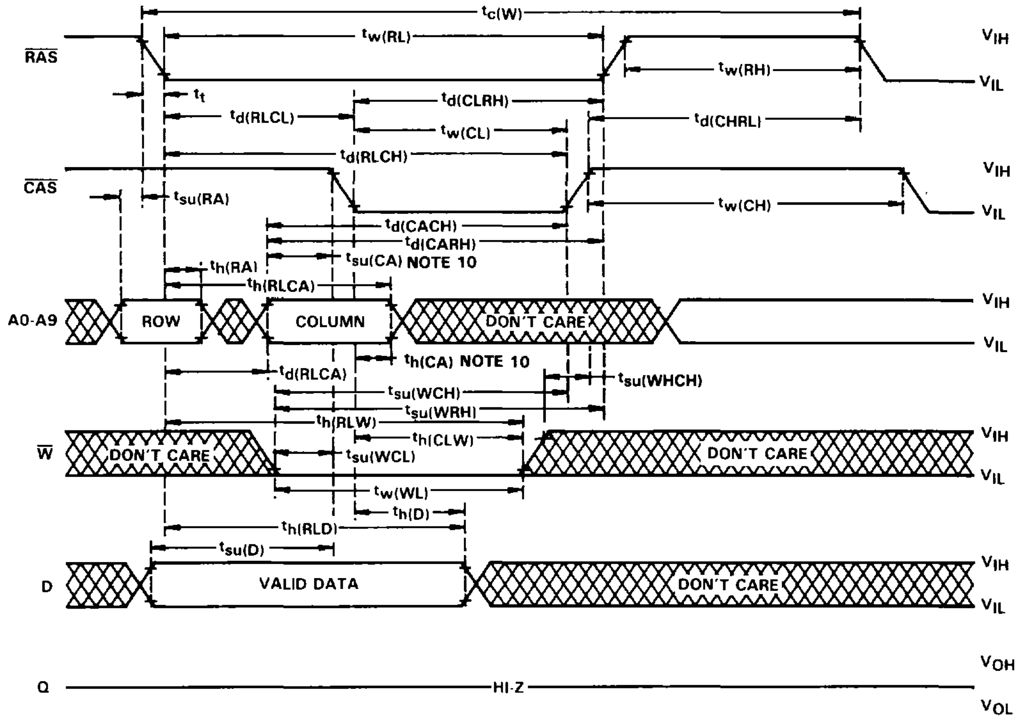


NOTE 19: Output may go from high impedance to an invalid state prior to the specified access time.

early write cycle timing

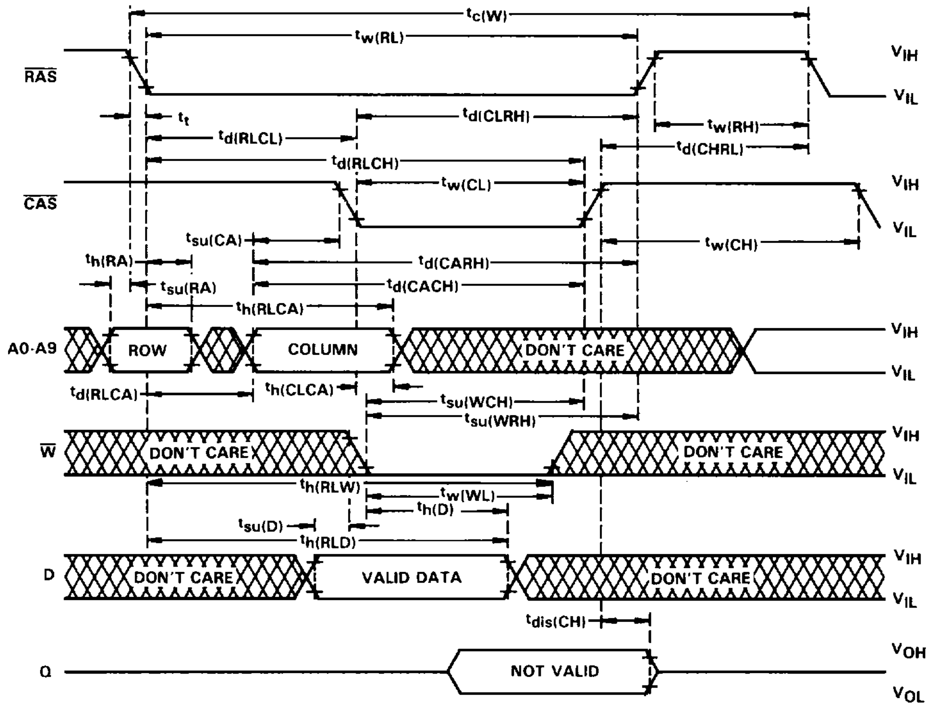


early write cycle timing



NOTE 10: Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in the write operations.

write cycle timing



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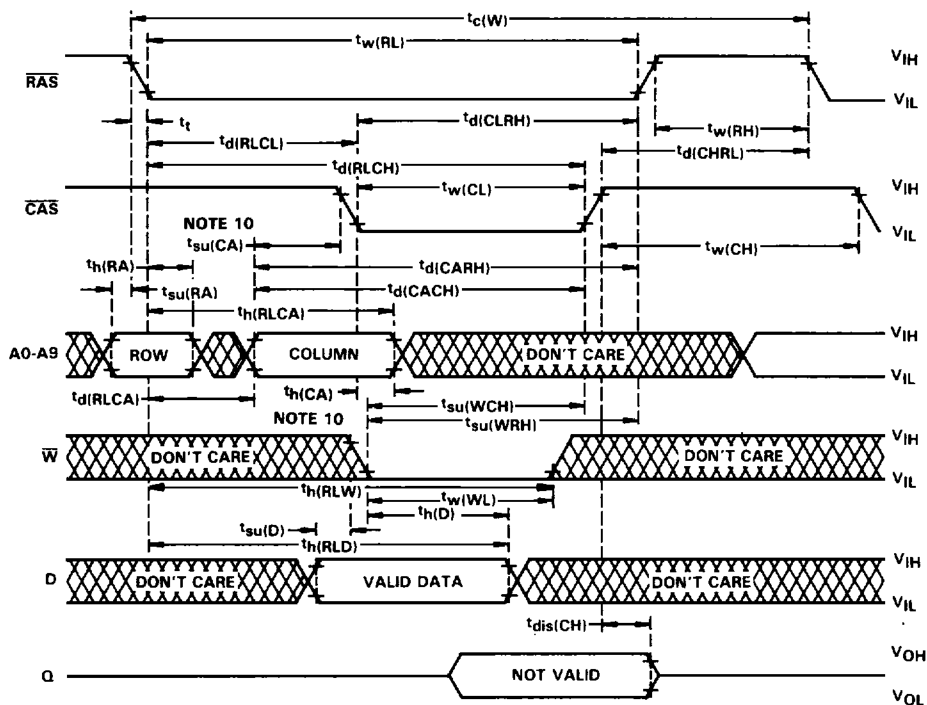
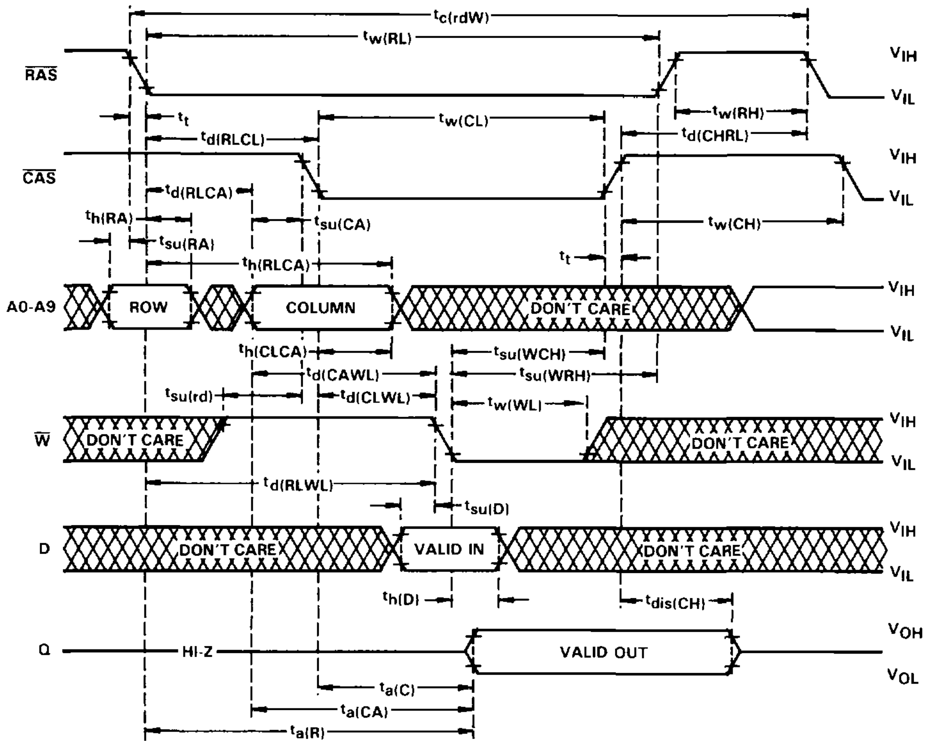
write cycle timing

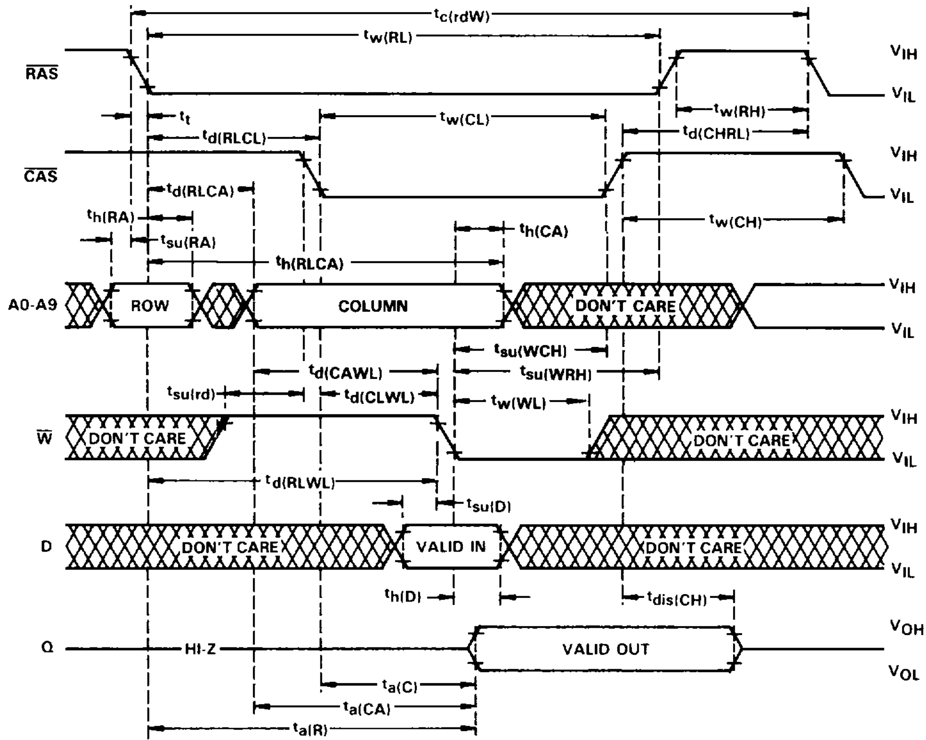


NOTE 10: Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in the write operation.

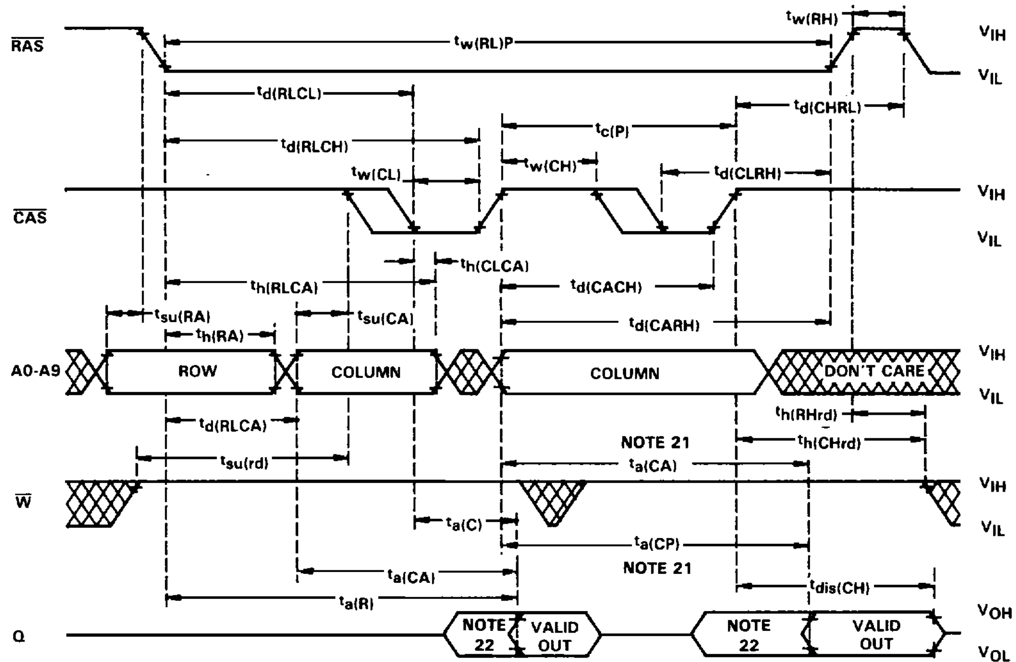
read-write/read-modify-write cycle timing



read-write/read-modify-write cycle timing



enhanced page-mode read cycle timing

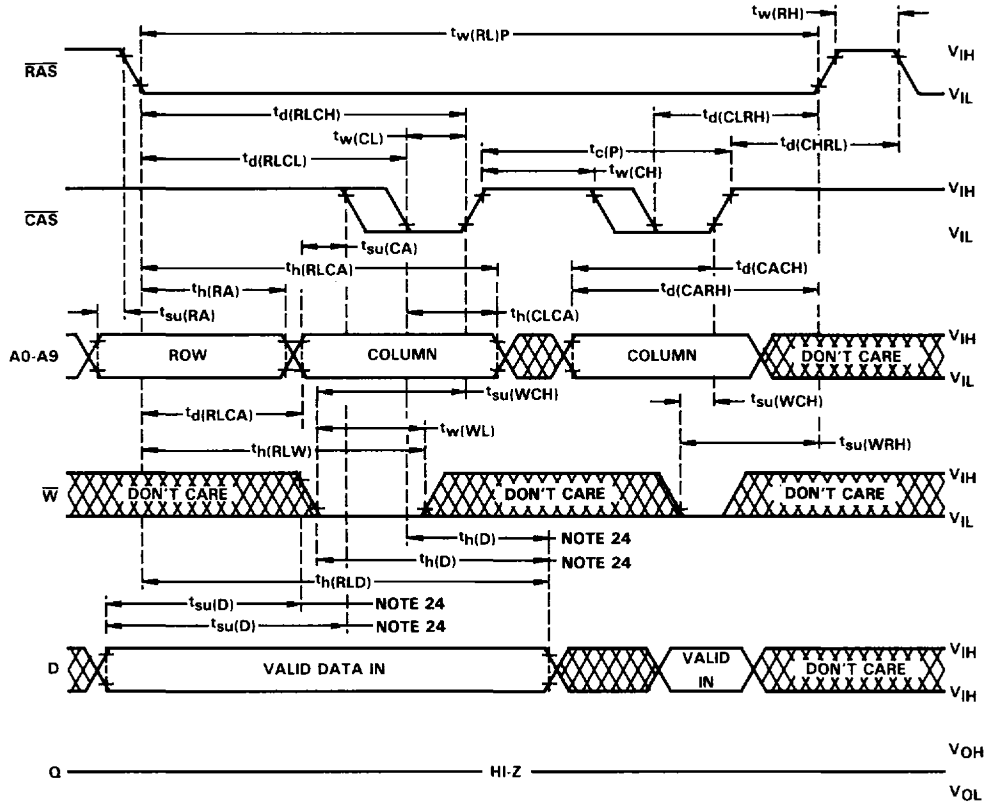


NOTES: 20. A write cycle or a read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.

21. Access time is $t_{a(CP)}$ or $t_{a(CA)}$ dependent.

22. Output may go from three-state to an invalid data state prior to the specified access time.

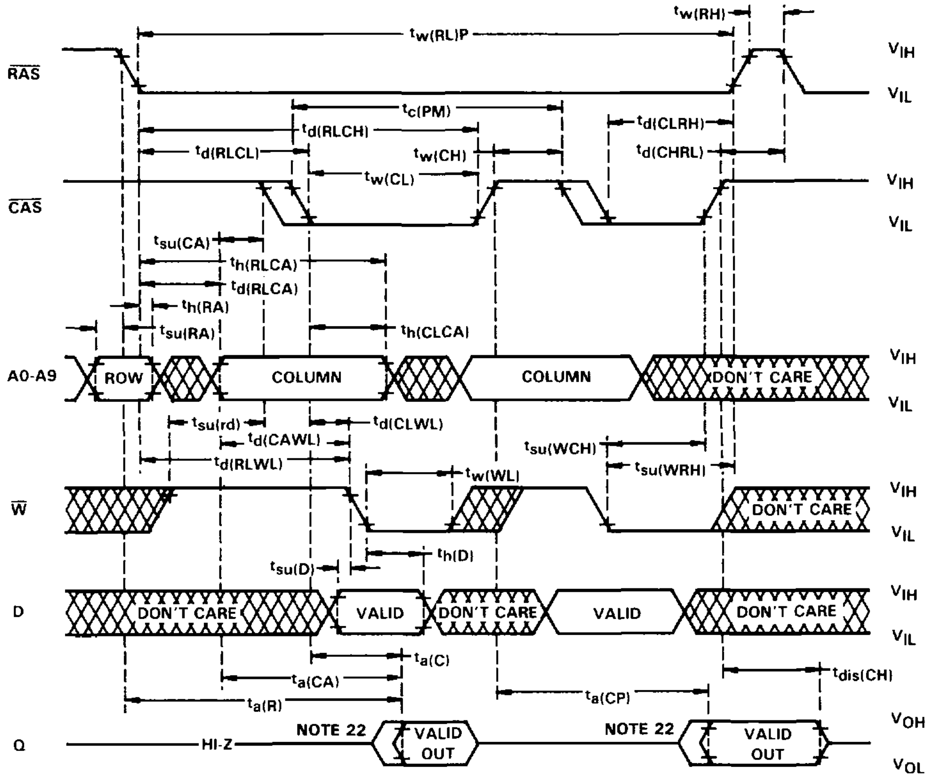
enhanced page-mode write cycle timing



NOTES: 23. A read cycle or a read-modify-write cycles can be intermixed with write cycle as long as read and read-modify-write timing specifications are not violated.

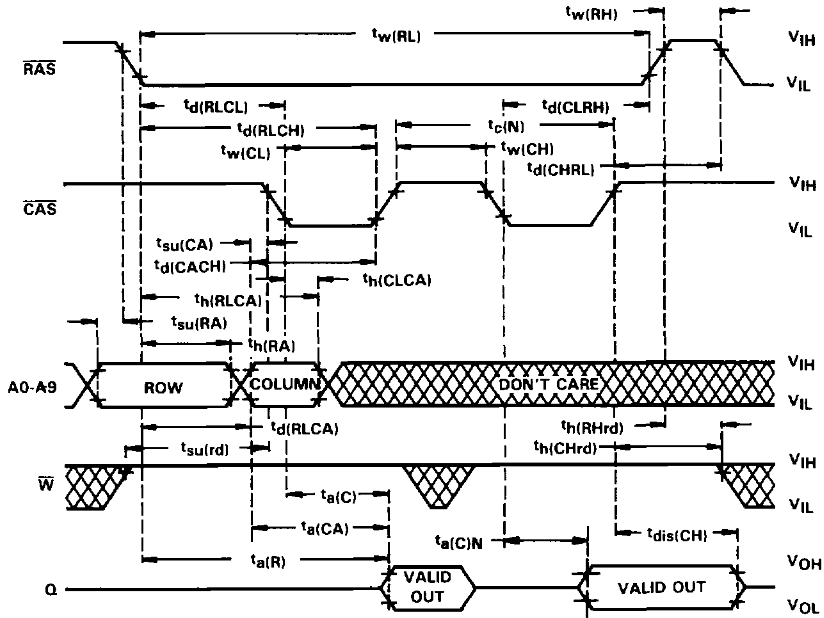
24. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.

enhanced page-mode read-modify-write cycle timing

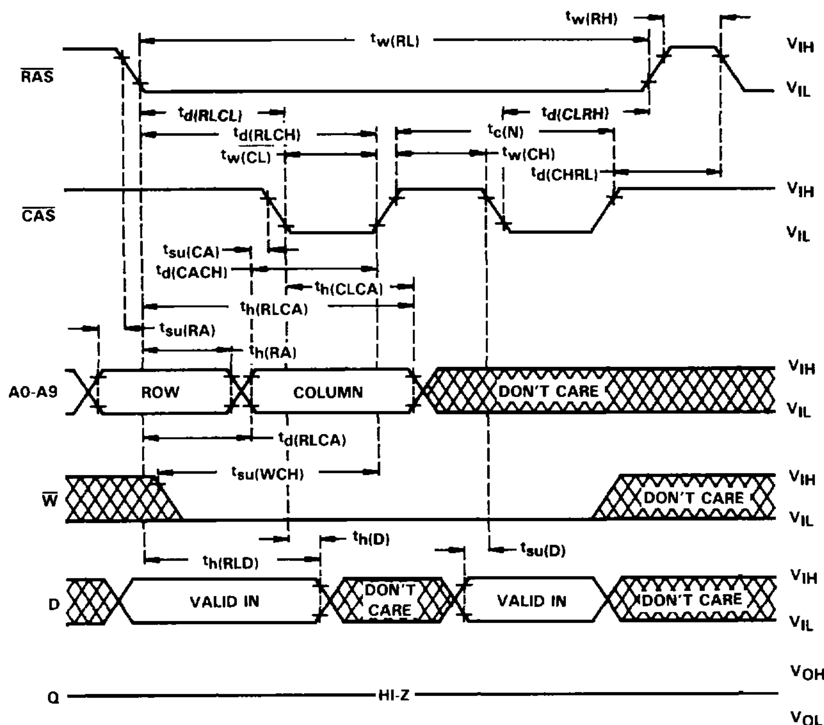


NOTES: 22. Output may go from three-state to an invalid data state prior to the specified access time.
25. A read or write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

nibble-mode read cycle timing



nibble-mode write cycle timing



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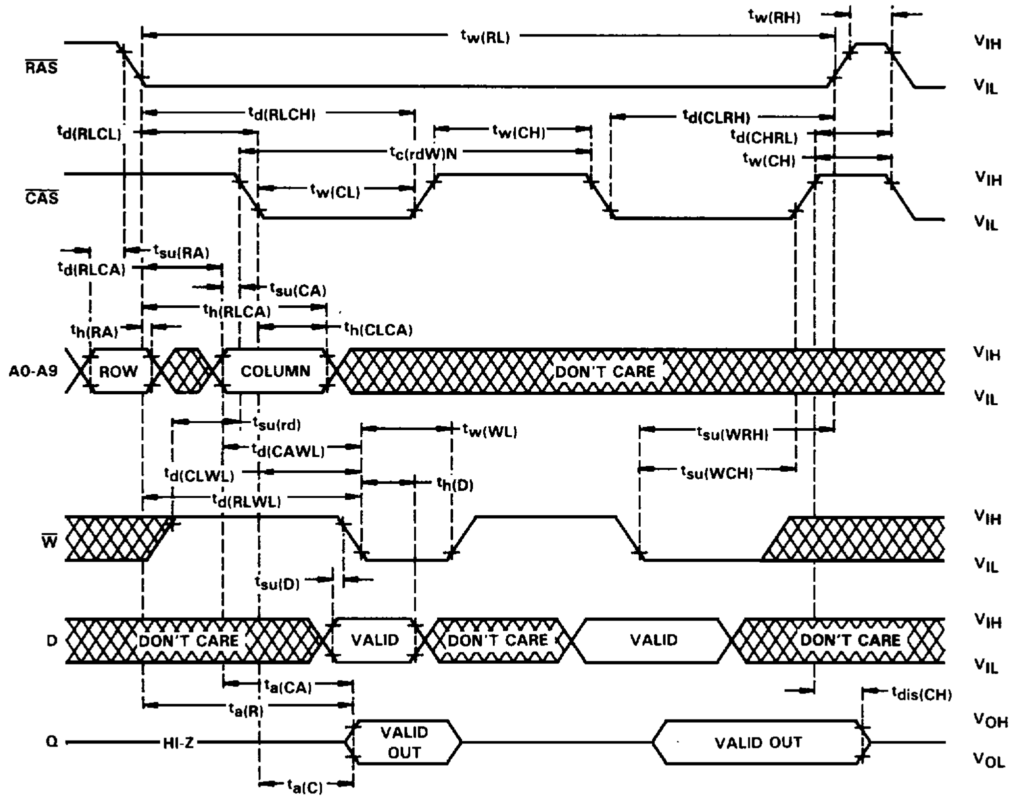
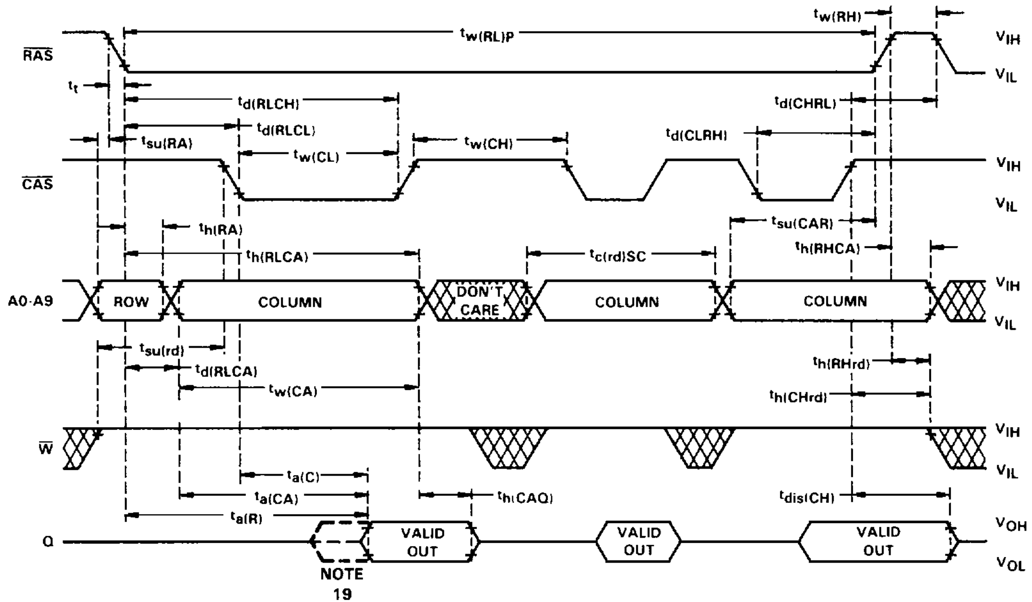
nibble-mode read-modify-write cycle timing

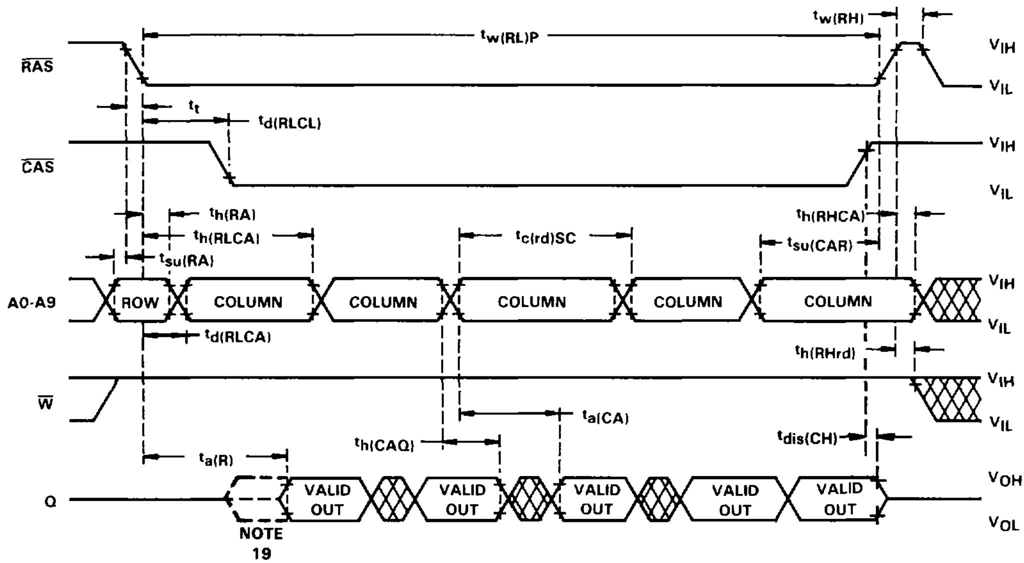


static column decode mode read timing with $\overline{\text{CAS}}$ cycling



NOTE 19: Output may go from high impedance to an invalid data state prior to the specified access time.

static column decode mode read cycle timing



NOTE 19: Output may go from high impedance to an invalid data state prior to the specified access time.

static column decode mode early write cycle timing

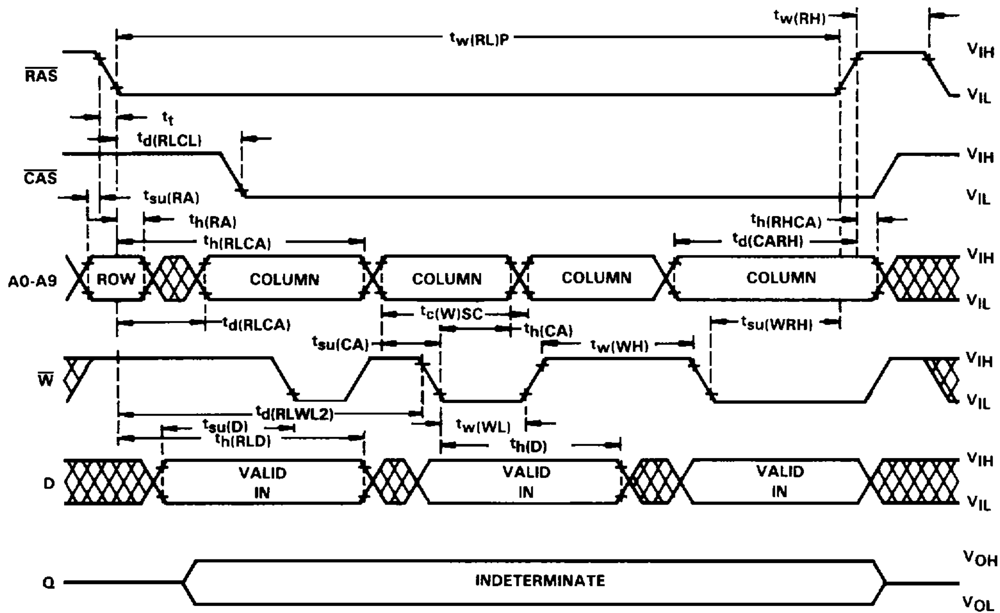
RAS
CAS
A0-A9
W
D
Q

$t_{w(RL)P}$ $t_{w(RH)}$ t_t $t_{d(RLCH)}$ $t_{w(CL)}$ $t_{d(RLCL)}$ $t_{d(CLRH)}$ $t_{d(CHRL)}$ $t_{w(CH)}$ $t_{su(RA)}$ $t_{h(RA)}$ $t_{h(RLCA)}$ $t_{h(CA)}$ $t_{su(CA)}$ $t_{su(WHCH)}$ $t_{h(RHCA)}$ $t_{d(CARH)}$ $t_{c(W)SC}$ $t_{su(WCH)}$ $t_{su(WRH)}$ $t_{d(RLCA)}$ $t_{d(RLWL2)}$ $t_{w(WH)}$ $t_{su(D)}$ $t_{h(D)}$ $t_{w(WL)}$ $t_{h(RLD)}$

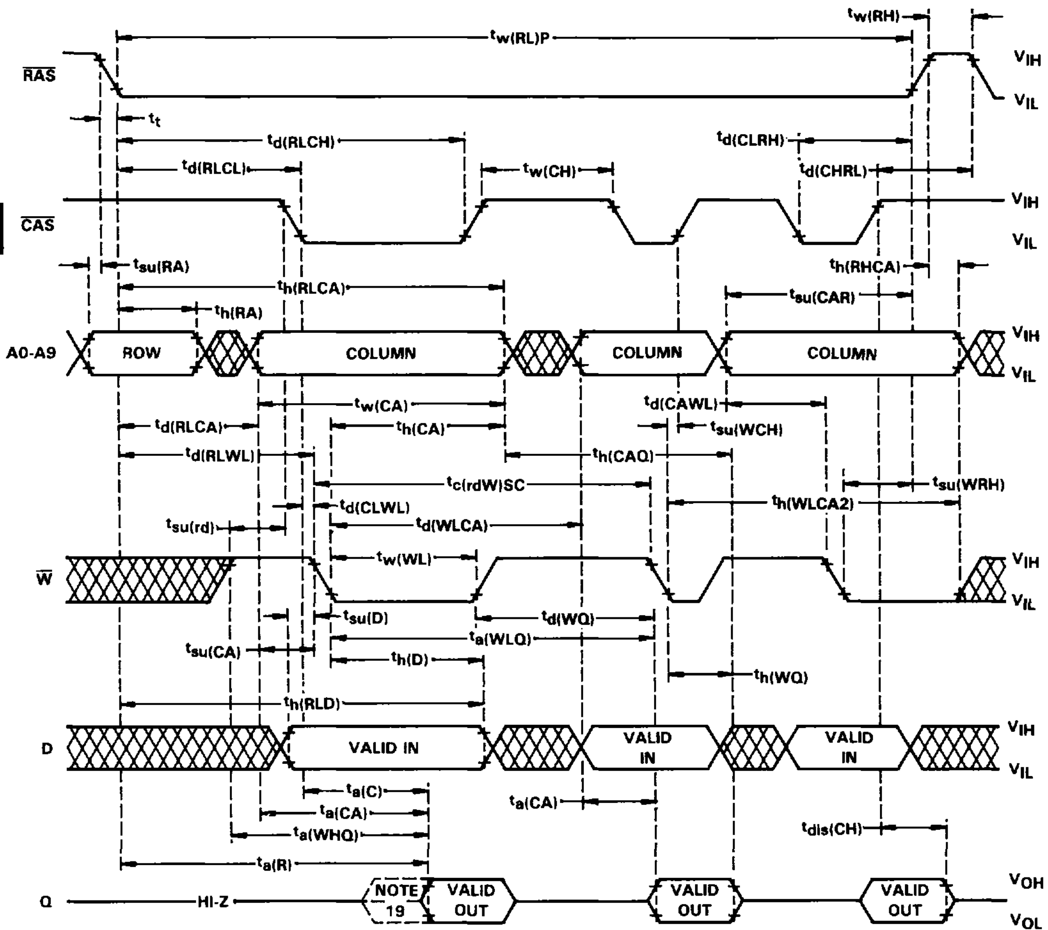
ROW COLUMN COLUMN COLUMN
VALID IN DON'T CARE VALID IN DON'T CARE VALID IN
HI-Z

V_{IH} V_{IL} V_{OH} V_{OL}

static column decode mode write cycle timing

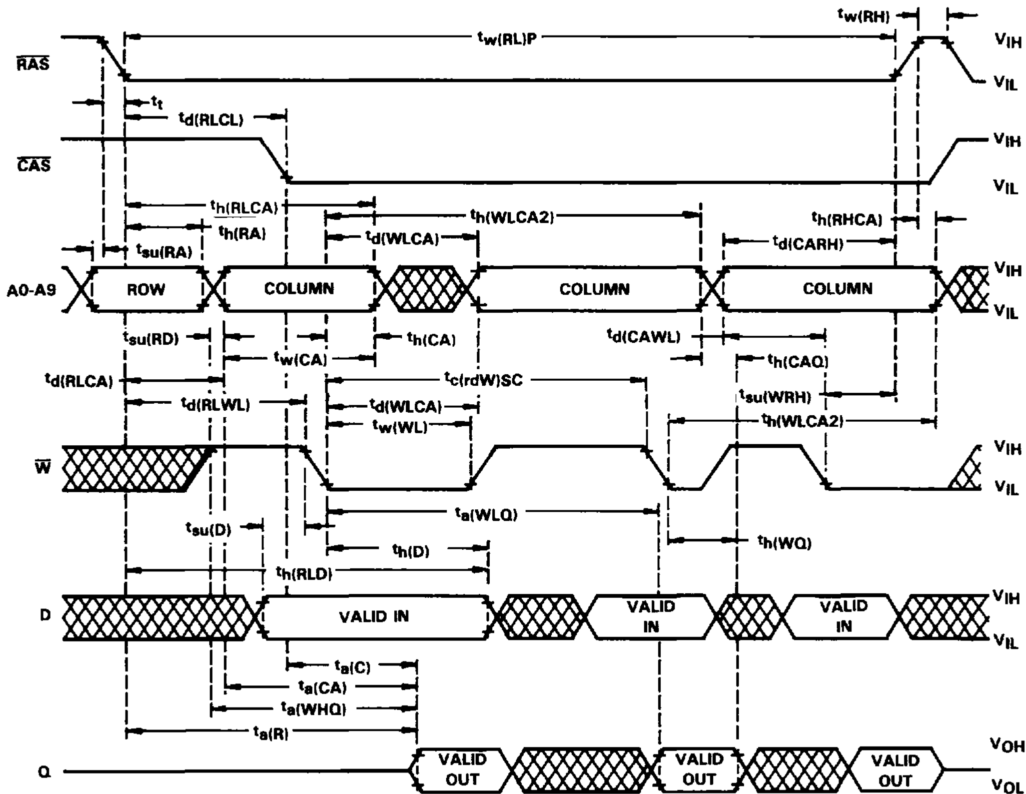


static column decode mode read-modify-write cycle timing with $\overline{CAS}$ cycling

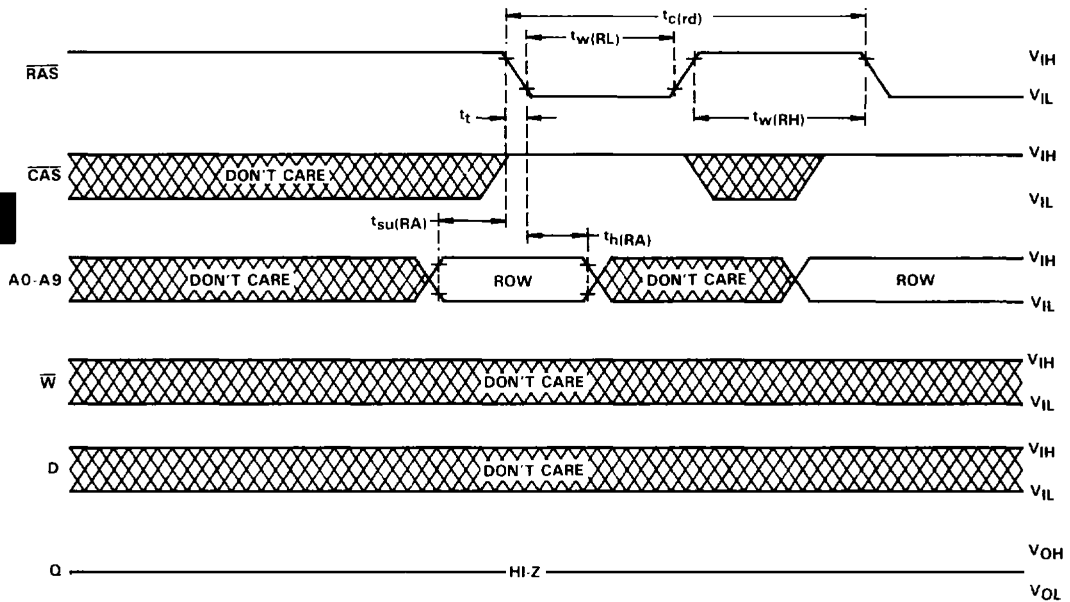


NOTE 19: Output may go from high impedance to an invalid data state prior to the specified access time.

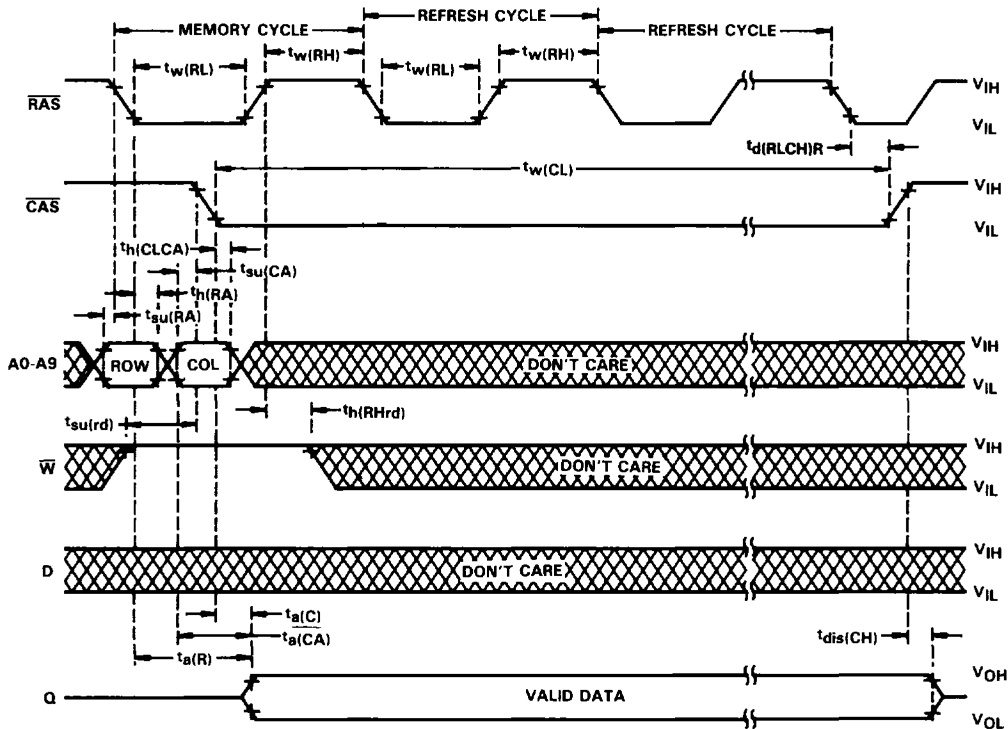
static column decode mode with read-modify-write cycle timing



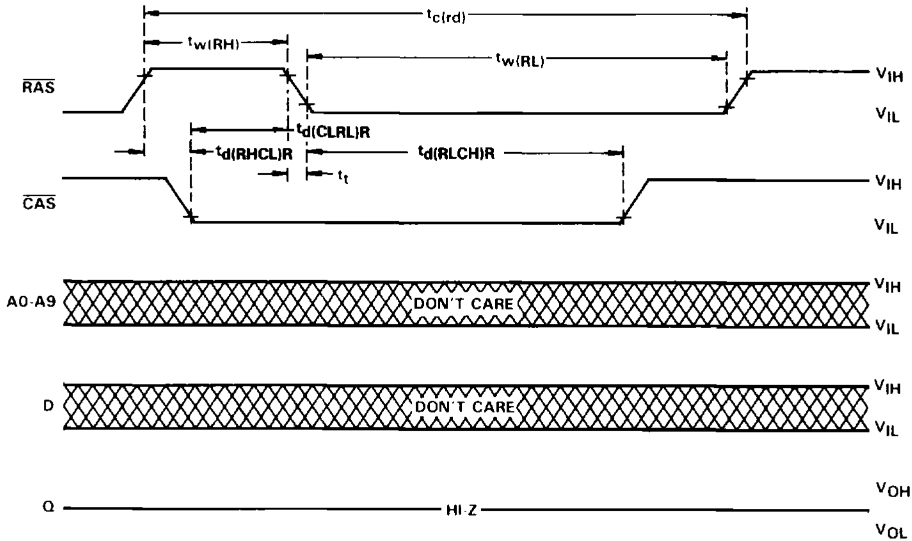
$\overline{\text{RAS}}$ only refresh timing



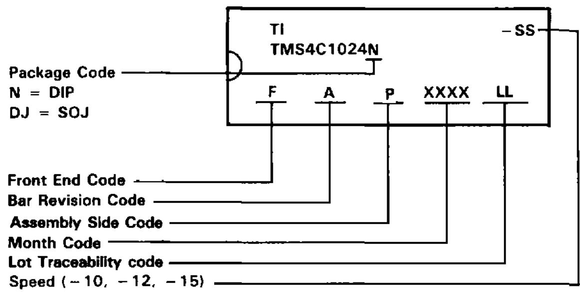
hidden refresh cycle



automatic (CAS-before-RAS) refresh timing



device symbolization



SUPPORT LITERATURE AVAILABLE

The following literature is available from Texas Instruments for assistance in DRAM design. Please contact your local TI sales office to obtain a copy.

1 MEGABIT DRAM FAMILY DATA SHEETS

- TMS44C256 — Specifications for the 1 Megabit DRAM organized 256K × 4 with enhanced page mode access. (SMGS256)
- TMS44C257 — Specifications for the 1 Megabit DRAM organized 256K × 4 with static column decode. (SMGS257)

Single-In-Line Package Memory Modules

- TM024GAD8, TM024EAD9 — Specifications for the socketable 1 Megabit × 8 and 1 Megabit × 9 Single-In-line Package memory modules. (SMMS102C)
- TM024HAC4 — Specifications for the leaded 1 Megabit × 4 Single-In-line Package memory module. (SMMS104A)

DESIGN CONSIDERATIONS

- Megabit DRAM Topology — The information in this report is useful in developing algorithms for cell sensitivity tests on TI's 1 Megabit DRAM configurations. (SMGA001)

TECHNICAL ARTICLE REPRINTS

- 1 Megabit Memories Demand New Design Choices — Discusses technical, technological, operational, and packaging issues pertaining to Megabit DRAMs. (SMZY018)
- 1-Megabit DRAMs Spark Tech Advances — Chip designers are proposing technological changes promising to significantly alter the design and layout landscape of the next generation of memory boards. (SMZY020)