

FEATURES

- handles high input levels cleanly (up to 100 mVRMS)
- low THD and IMD distortion
- unique twin average detectors
- dual channel signal processing
- adjustable AGC threshold levels
- highpass filter with adjustable corner frequency
- 2:1 compression of high frequencies

STANDARD PACKAGING

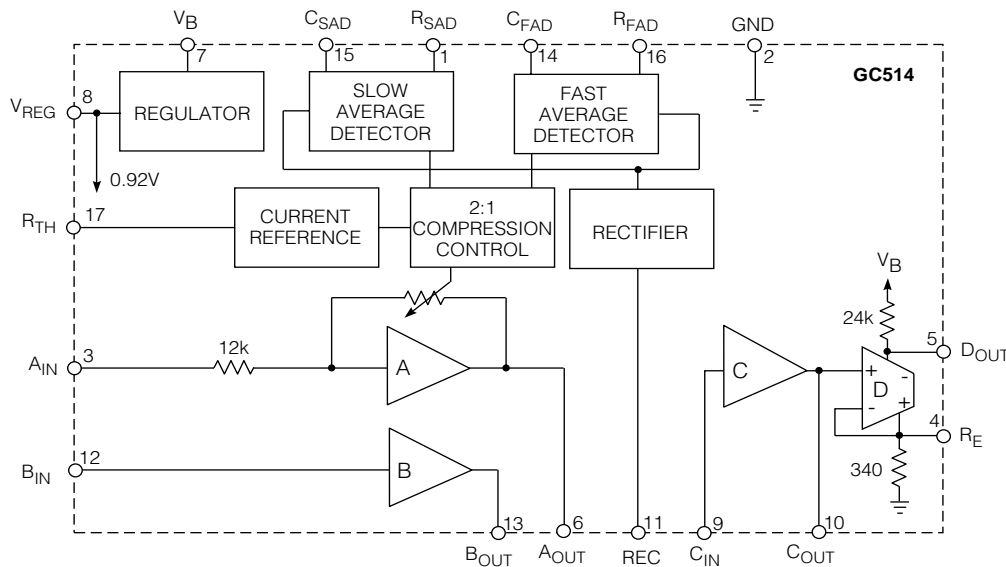
- Chip (84 X 112 mils)
Au Bump

DESCRIPTION

The GC514 integrated circuit is a dynamically adaptive loudness growth equalizer. Its gain and frequency response are dependent on the user's environment and provide treble increase at low levels (TILL). The unique twin average detector circuit dramatically reduces pumping effects and is optimized for mild-to-moderate hearing loss.

GC514 has two signal paths for dual channel processing incorporating four amplifying stages (A, B, C, D) and an AGC processing circuit.

Stage A is a highpass channel with 2:1 compression. Stage B is a wideband buffer. The sum of the two paths gives a high frequency boost to low level signals which gradually compresses to a flat response at high input levels. Stage C is used for volume control adjustment, while stage D is a class A power amplifier with receiver bias current adjustment.



All resistors in ohms, all capacitors in farads unless otherwise stated.
Patent Pending.

FUNCTIONAL BLOCK DIAGRAM

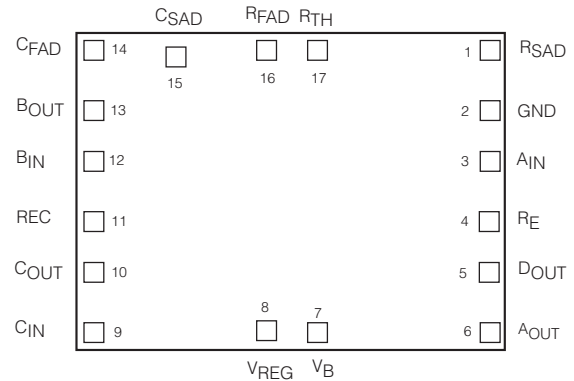
ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE / UNITS
Supply Voltage	5 VDC
Power Dissipation	25 mW
Operating Temperature Range	-10° C to 40° C
Storage Temperature Range	-20° C to 70° C

CAUTION
CLASS 1 ESD SENSITIVITY



CHIP PAD CONNECTION



ELECTRICAL CHARACTERISTICS

Conditions: Frequency = 1 kHz, Temperature = 25°C, Supply Voltage $V_B = 1.3$ V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Amplifier Current	I_{AMP}	$V_{IN} = 0$ VRMS	120	230	330	μ A
Minimum Voltage	V_B		1.1	-	-	V
STAGE A						
Input Impedance	$Z_{IN A}$		-	12	-	k Ω
Maximum Gain (no compression)	$A_{MAX A}$	S3, S4 closed; $V_{IN} = -80$ dBV	24.5	26.5	30	dB
Minimum Gain	$A_{MIN A}$	$V_{IN} = -20$ dBV	-	-11	-	dB
Gain in Compression	$A_{COMP A}$	S3 closed; $V_{IN} = -80$ dBV	16.7	18.2	19.7	dB
High Level Distortion	THD _A	$V_{IN} = -20$ dBV	-	0.4	2.0	%
Compression Ratio	COMP	$V_{IN} = -80$ dBV and -60 dBV	1.74:1	1.95:1	2.11:1	Ratio
AGC						
Threshold	V_{THR}		-	-94	-	dBV
STAGE B						
Input Bias Current	$I_{BIAS B}$		0	25	55	nA
Output Source Capacity	$I_{SOURCE B}$	$V_{P12} = 0.4$ V; $V_{P13} = 0.5$ V	15	30	-	μ A
Output Voltage Sink	$V_{SINKLOW B}$	Note 1	200	300	500	mV
STAGE C						
Input Bias Current	$I_{BIAS C}$		-25	-	25	nA
Output Source Capacity	$I_{SOURCE C}$	$V_{P9} = 0.4$ V; $V_{P10} = 0.5$ V	15	30	-	μ A
Output Voltage Sink	$V_{SINKLOW C}$	Note 2	200	300	500	mV
STAGE D						
Minimum Transducer Current	I_{TRMIN}		130	160	190	μ A
Maximum Current Sink	I_{SINK}	S1 closed	3	6	-	mA
Output Impedance	Z_{OUT}		20	24	28	k Ω
Emitter Bias Voltage	V_{RE}		48	52	56	mV
REGULATOR						
Regulator Voltage	V_{REG}		0.89	0.92	0.97	V
Supply Rejection	PSRR		-	57	-	dB

All parameters and switches remain as shown in the Test Circuit unless otherwise stated in CONDITIONS column

V_{QX} quiescent (unbias) voltage measured on the pin, (nothing connected to the pin)

V_{PX} actual voltage measured on the pin at given condition (X is pin number)

Notes: 1. $V_{SINKLOW B} = V_{Q13} - V_{P13}$ [$I_{P12} = 1$ μ A, $I_{P13} = 15$ μ A]

2. $V_{SINKLOW C} = V_{Q10} - V_{P10}$ [$I_{P9} = 1$ μ A, $I_{P10} = 15$ μ A]

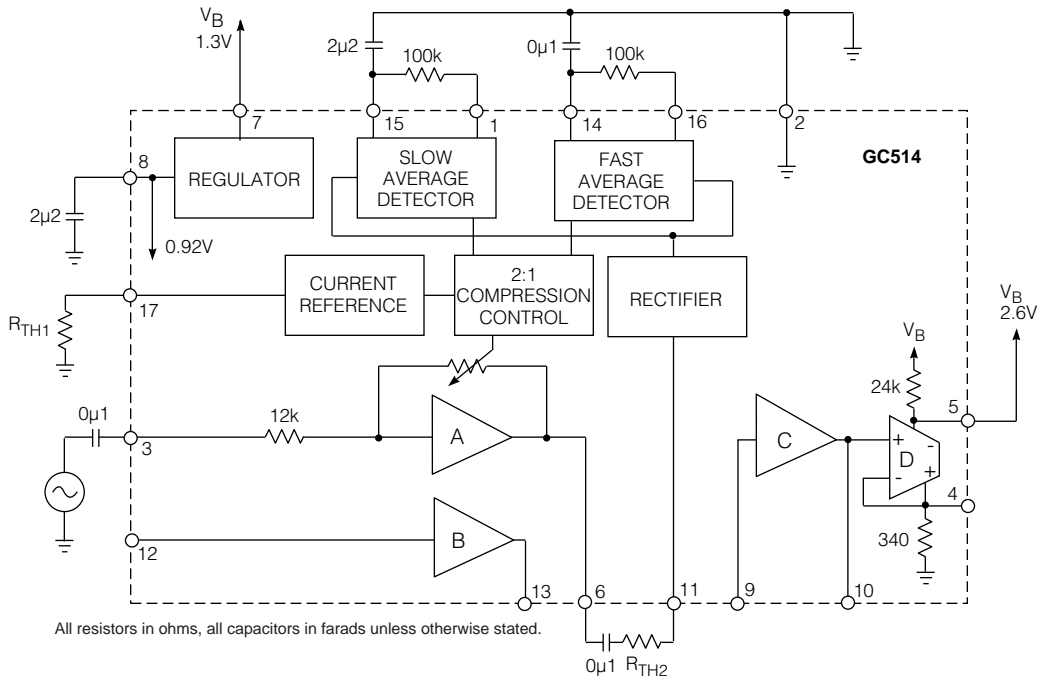


Fig. 3 Characterization Circuit (used to generate curves)

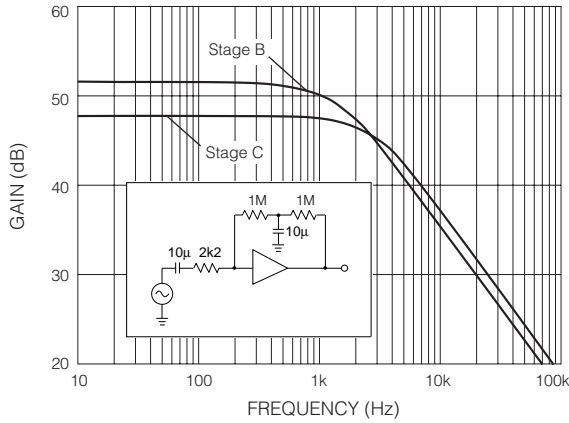


Fig. 4 Preamplifier Open Loop Voltage Gain

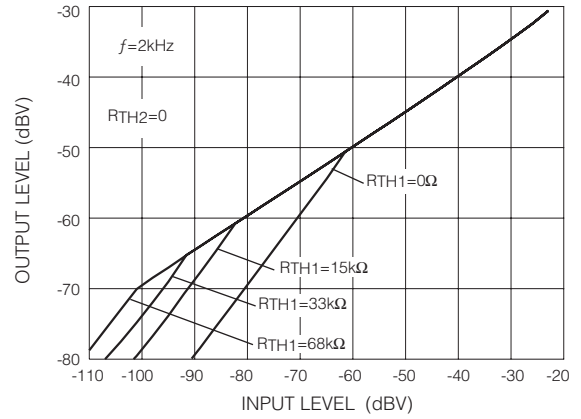


Fig. 5 Stage A Transfer Functions for Different R_{TH1} Resistors

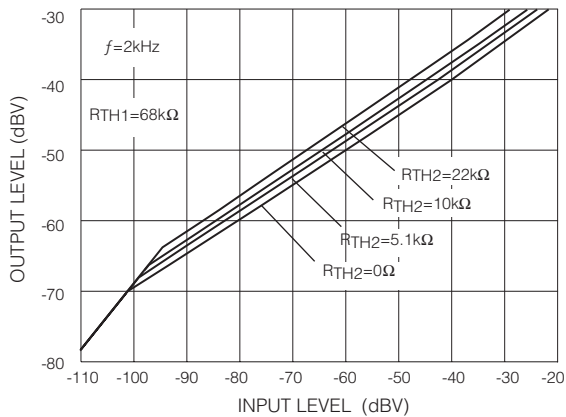


Fig. 6 Stage A I/O Transfer Functions for Different R_{TH2} Resistors

DOCUMENT IDENTIFICATION: DATA SHEET
The product is in production. Genum reserves the right to make changes at any time to improve reliability, function or design, in order to provide the best product possible.

REVISION NOTES:
Updated to Data sheet