**PRELIMINARY**

# microSSD™
# 4Gbyte Solid State Disk

- Extended Temp (-20°C to +85°C) Operation
- Industry Standard ATA/IDE Bus Interface
  – Host Interface: 16-bit access
  – Supports up to PIO Mode-6
  – Supports up to Multi-word DMA Mode-4
  – Supports up to Ultra DMA Mode-6
- 4Gbytes of Storage Capacity*
- Low Power, 3.3V Power Supply
- Low Current Operation:
  – Active mode: 115 mA typical
  – Sleep mode: 700 µA typical
- Power Management Unit
  – Immediate disabling of unused circuitry with out host intervention
  – Zero wake-up latency
- Expanded Data Protection
  – WP#/PD# pin configurable by firmware for prevention of data overwrites
  – Data security through user-selectable protection zones with advanced NAND management technology
- 20-byte Unique ID for Enhanced Security
  – Factory Pre-programmed 10-byte Unique ID
  – User-Programmable 10-byte ID

- Integrated Voltage Detector
  – Prevents inadvertent Write operations due to unexpected power-down or brownout.
- Pre-programmed Embedded Firmware
  – Executes industry standard ATA/IDE commands
  – Implements advanced wear-leveling algorithms to substantially increase the longevity of flash media
  – Embedded Flash File System
- Robust Built-in ECC
  – Corrects up to 24 random bits of error
- Multi-tasking Technology Enables Fast Sustained Write Performance
  – Up to 7 MByte/sec
- Fast Sustained Read Performance
  – Up to 28 MByte/sec
- 91-ball PBGA package
  – 14mm x 24mm x 1.3mm

## OPTIONS
## MARKING

- Plastic 91-Ball PBGA           PBG
  (Sn / Pb or RoHS Compliant Available)

- Operating Temperature Ranges
  - Extended Temp (-20°C to 85°C)

## SPEEDS / MODES

| Sustained Read | Sustained Write | Mode | | |
| --- | --- | --- | --- | --- |
| | | PIO | Ultra DMA | Multi-Word DMA |
| 28 MB/s | 7 MB/s | 6 | 6 | 4 |

*Actual usable capacity may be less

## OVERVIEW

The AS3uSSD4GB28MPBG microSSD™ solid-state drive (SSD) combines a NAND controller and 4 GBytes of NAND flash in a multi-chip package. It provides complete ATA/IDE hard disk drive functionality in a small package for easy, space saving mounting to a system motherboard. This makes the AS3uSSD4GB28MPBG microSSD the ideal data storage solution for mobile and embedded electronic products that require smaller and more reliable storage.

For more products and information
please visit our web site at
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## PRODUCT DESCRIPTION

The AS3uSSD4GB28MPBG microSSD™ solid-state drive (SSD) is a high-performance, fully-integrated, embedded flash solid state drive. It combines an integrated NAND Controller and 4 GByte of MLC NAND Flash in a multi-chip package. This product is ideal for solid state mass storage applications offering new and expanded functionality while enabling cost effective designs.

ATA-based solid state mass storage technology is widely used in portable and desktop computers, digital cameras, music players, handheld data collection scanners, cellular phones, PCS phones, PDAs, handy terminals, personal communicators, robotics, audio recorders, monitoring devices, and set-top boxes.

Micross microSSD is a solid state drive designed for embedded ATA/IDE protocol systems and supports standard ATA/IDE protocol with up to PIO Mode-6, Multi-word DMA Mode-4 and Ultra DMA Mode-6 interface. The built in microcontroller and file management firmware communicates with ATA standard interfaces; thereby eliminating the need for additional or proprietary software, such as Flash File System (FFS), on the host.

The AS3uSSD4GB28MPBG microSSD's provide complete IDE Hard Disk Drive functionality and compatibility in a 14mm x 24mm PBGA package for easy, space saving mounting to a system motherboard. It is a perfect solution for portable, consumer electronic products requiring smaller and more reliable data storage.

The microSSD provides a WP#/PD# pin to protect critical information stored in the flash media from unauthorized overwrites.

Pre-programmed with a 10-byte unique serial ID, microSSD allows users to program an additional 10 Bytes of ID space to create a unique, 20-byte ID for greater system security.

microSSD is available with advanced NAND management technology, a NAND memory management technology that enhances data security, significantly improves endurance, and accurately predicts the minimum life span of NAND flash devices. Advanced NAND management technology combines NAND controller hardware error correction, advanced wear leveling algorithms, and bad block management to extend the life of the product.

<span style="color:red">**PRELIMINARY**</span>

## GENERAL DESCRIPTION

Each microSSD contains an integrated NAND Controller and NAND Flash die in a PBGA package. Refer to Figure 1 for the microSSD block diagram.

### Performance-optimized microSSD

The heart of the microSSD is the NAND Controller which translates standard ATA signals into flash media data and control signals. The following components contribute to the microSSD's operation.

### Microcontroller Unit (MCU)

The 32-bit RISC architecture transfers the ATA/IDE commands into data and control signals required for flash media operation.

### Power Management Unit (PMU)

The power management unit controls the power consumption of the microSSD. The PMU dramatically reduces the power consumption of the microSSD by putting the part of the circuitry that is not in operation into sleep mode.

The Flash File System handles inadvertent power interrupts and has auto-recovery capability to insure microSSD data integrity. For regular power management, the Host must send an Idle_Immediate command and wait for command ready before powering down the microSSD.

### SRAM Buffer

A contributor to the microSSD performance is an SRAM buffer. The buffer optimizes the host's data transfer to and from the flash media.

### Embedded Flash File System

The embedded flash file system is an integral part of the microSSD. It contains MCU firmware that performs the following tasks:
1. Translates host side signals into flash media writes and reads.
2. Provides flash media wear leveling to spread the flash writes across all memory address space to increase the longevity of flash media.
3. Keeps track of data file structures.
4. Stores the data in Flash media upon completion of a Write command. The microSSD does not do Post-Write operations, except when the write cache is enabled by the Host command.

### Serial Communication Interface (SCI)

The Serial Communication Interface (SCI) is designed for manufacturing error reporting. During the design process, always provide access to the SCI interface in the PCB design to aid in design validation.

### Multi-tasking Interface

The multi-tasking interface enables fast, sustained write performance by allowing concurrent Read, Program, and Erase operations to multiple flash media devices.

**Error Correction Code (ECC)**
High performance is achieved through optimized hardware error detection and correction.

**Internal Direct Memory Access (DMA)**
The microSSD uses internal DMA allowing instant data transfer from buffer to flash media. This implementation eliminates microcontroller overhead associated with the traditional, firmware-based approach, thereby increasing the data transfer rate.

## NAND Flash
The microSSD family utilize standard NAND Flash for data storage. Because the re-flow process can alter the microSSD content, do not program the AS3uSSD4GB28MPBG NAND before the reflow process.

**Advanced NAND Management Technology**
Advanced NAND management technology balances the wear on erased blocks with an advanced wear-leveling scheme which provides a minimum of 7 million host write cycles. Advanced NAND management technology tracks the number of program/erase cycles within a group. When the host updates data, higher priority is given to the less frequently written erase blocks; thereby, evenly distributing host writes within a wear-leveling group.

Advanced NAND management technology enhances microSSD security with password protection and four independent protection zones which can be set to Read-only or Hidden.

## FUNCTIONAL BLOCKS
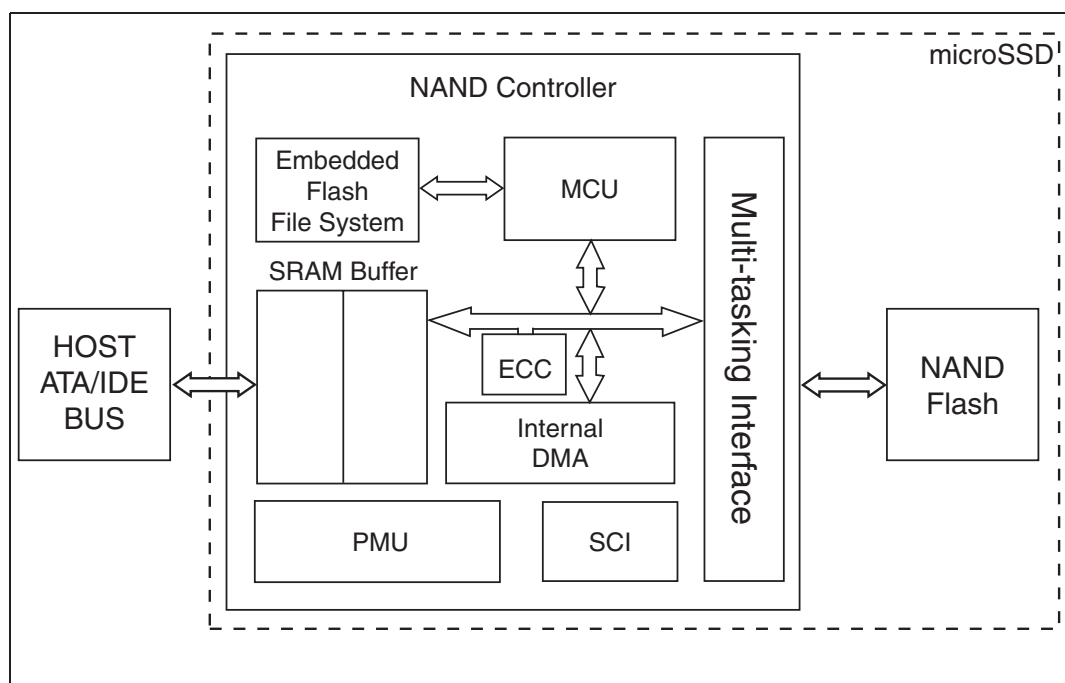


**Figure 1:**microSSD Block Diagram

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## PIN ASSIGNMENTS

The signal/pin assignments are listed in Figure 2. Low active signals have a "#" suffix. Pin types are Input, Output, or Input/Output. Signals whose source is the host are designated as inputs while signals that the microSSD sources are outputs.

The microSSD functions in ATA mode, which is compatible with IDE hard disk drives.



**Figure 2:** Pin Assignments for 91-Ball PBGA

## Table 1:Pin Assignments (1 of 3)

| Symbol | Pin No. 91 PBGA | Pin Type | I/O Type | Name and Functions |
|---|---|---|---|---|
| **Host Side Interface** | | | | |
| A2 | K8 | | | |
| A1 | K3 | I | I1Z | A[2:0] are used to select one of eight registers in the Task File. |
| A0 | L2 | | | |
| D15 | H8 | | | |
| D14 | G9 | | | |
| D13 | G8 | | | |
| D12 | H7 | | | |
| D11 | F9 | | | |
| D10 | F8 | | | |
| D9 | E8 | | | |
| D8 | F7 | I/O | I1Z/O2 | D[15:0] Data bus |
| D7 | F4 | | | |
| D6 | H4 | | | |
| D5 | E3 | | | |
| D4 | H3 | | | |
| D3 | F3 | | | |
| D2 | G3 | | | |
| D1 | F2 | | | |
| D0 | G2 | | | |
| DMACK# | K2 | I | I2U | DMA Acknowledge - input from host |
| DMARQ | J3 | O | O2 | DMA Request to host |
| CS1FX# | L3 | | | CS1FX# is the chip select for the task file registers |
| CS3FX# | L8 | I | I2Z | CS3FX# is used to select the alternate status register and the Device Control register. |
| CSEL | L9 | I | I1U | This internally pulled-up signal is used to configure this device as a Master or a Slave. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave. The pin setting should remain the same from Power-on to Power-down. |
| IORD# | H2 | I | I2Z | IORD#: This is an I/O Read Strobe generated by the host. When Ultra DMA mode is not active, this signal gates I/O data from thedevice. (This pin supports three functions) |
| | | | | HDMARDY#: In Ultra DMA mode when DMA Read is active, this signal is asserted by the host to indicate that the host is ready to receive Ultra DMA data-in bursts. The host may negate HDMARDY# to pause an Ultra DMA transfer. |
| | | | | HSTROBE: When DMA Write is active, this signal is the data-out strobe generated by the host. Both the rising and falling edges of HSTROBE cause data to be latched by the device. The host may stop generating HSTROBE edges to pause an Ultra DMA data-out burst. |

## Table 1:Pin Assignments (2 of 3)

| Symbol | Pin No. 91 PBGA | Pin Type | I/O Type | Name and Functions |
|---|---|---|---|---|
| IOWR# | H9 | I | I2Z | IOWR#: This is an I/O Write Strobe generated by the host. When Ultra DMA mode is not active, this signal is used to clock I/O data intothe device.  (This pin supports two functions) |
| | | | | STOP: When Ultra DMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA burst |
| IORDY | J4 | O | O2 | IORDY: When in PIO mode, the device is not ready to respond to a data transfer request. This signal is negated to extend the Host transfer cycle from the assertion of IORD# or IOWR#. However, it is never negated by this controller. (This pin supports three functions) |
| | | | | DDMARDY#: When Ultra DMA mode DMA Write is active, this signal is asserted by the device to indicate that the device is ready to receive Ultra DMA data-in bursts. The device may negate DDMARDY# to pause an Ultra DMA transfer. |
| | | | | DSTROBE: When Ultra DMA mode DMA Read is active, this signal is the data-out strobe generated by the device. Both the rising and falling edges of DSTROBE cause data to be latched by the host. The device may stop generating DSTROBE edges to pause an Ultra DMA data-out burst. |
| IOCS16# | J8 | O | O3 | This output signal is asserted low when the device is indicating a word data transfer cycle. |
| INTRQ | J2 | O | O2 | This signal is the active high Interrupt Request to the host. |
| PDIAG# | K9 | I/O | I1U/O1 | The Pass Diagnostic signal in the Master/Slave handshake protocol. |
| DASP# | D9 | I/O | I1U/O4 | The Drive Active/Slave Present signal in the Master/Slave handshake protocol. |
| RESET# | E4 | I | I2U | This input pin is the active low hardware reset from the host. |
| **Serial Communication Interface (SCI)** | | | | |
| SCID$_{OUT}$ | D8 | O | O2 | SCI interface data output |
| SCID$_{IN}$ | D7 | I | I1U | SCI interface data input |
| SCICLK | E7 | I | I1D | SCI interface clock |
| **Miscellaneous** | | | | |
| WP#/PD# | F6 | I | I2U | The WP#/PD# pin can be used for either the Write Protect mode or Power-down mode, but only one mode is active at any time. The Write Protect or Power-down modes can be selected through the host command. The Write Protect mode is the factory default setting. |
| V$_{SS}$[1] | G4, G6, G7, K4, K6, K7, J9 | PWR | | Ground |
| V$_{DD}$[1] | E9, K5, L5, M2 | PWR | | V$_{DD}$ (3.3V) |

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## Table 1:Pin Assignments (3 of 3)

| Symbol | Pin No. 91 PBGA | Pin Type | I/O Type | Name and Functions |
|---|---|---|---|---|
| DNU | A1, A2, A9, A10, B1, B9, B10, D2, D3, D4, D5, D6, E5, E6, F5, G5, J7, L4, L6, L7, M3, M4, M5, M6, M7, M8, N2, N3, N4, N5, N6, N7, N8, N9, R1, R2, R9, R10, T1, T2, T9, T10 | | | Do not use. |

1.Any $V_{SS\ or}\ V_{DD}$ pin must not be left open or floating.

## Capacity Specification

Table 2 shows the default capacity and specific settings for heads, sectors, and cylinders. At production time, the manufacturer can change the default settings in the drive ID table by changing the Cylinders-Heads Sectors configuration. If the total number of bytes configured is less than the default amount, the remaining space could be used as spare blocks to increase the flash drive endurance. It should also be noted that if the initialized total flash drive capacity exceeds the total bytes shown in Table 2, the flash drive endurance will be reduced.

## Table 2:Default microSSD Settings

| Capacity | Total Bytes | Cylinders | Heads | Sectors | Max LBA |
|----------|-------------|-----------|-------|---------|---------|
| 4 Gbyte | 3,657,056,256 | 7086 | 16 | 63 | 7,142,688 |

## Table 3:Sustained Performance

| Product | Write Performance | Read Performance |
|---------|-------------------|------------------|
| AS3uSSD4GB28MPBG | Up to 7 MByte/sec | Up to 28 MByte/sec |

## Table 4:Supported ATA Modes

| Product | PIO | MWDMA | UltraDMA |
|---------|-----|-------|----------|
| AS3uSSD4GB28MPBG | Up to Mode-6 | Up to Mode-4 | Up to Mode-6 |

## Configurable Write Protect/Power-down Modes

The WP#/PD# pin can be used for either Write Protect mode or Power-down mode, but only one mode is active at any time. Either mode can be selected through the host command, Set-WP#/PD#-Mode.

Once the mode is set with this command, the device will stay in the configured mode until the next time this command is issued. Power-off or reset will not change the configured mode.

**Write Protect Mode**
When the device is configured in the Write Protect mode, the WP#/PD# pin offers extended data protection. This feature can be either selected through a jumper or host logic to protect the stored data from inadvertent system writes or erases, and viruses. The Write Protect feature protects the full address space of the data stored on the flash media.

In the Write Protect mode, assert the WP#/PD# pin prior to issuing all destructive commands: Erase-Sector, Format-Track, Write-DMA, Write-Multiple, Write-Sector(s), or Write-Verify. This will force the microSSD to reject any destructive commands from the ATA interface. All destructive commands will return 51H in the Status register and 04H in the Error register signifying an invalid command. All non-destructive commands will be executed normally.

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Micross Components reserves the right to change products or specifications without notice.

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## Power-down Mode

When the device is configured in the Power-down mode, if the WP#/PD# pin is asserted during a command, the microSSD stops the ongoing command and immediately enters power-down mode. Afterwards, the device will not accept any other commands. Both a software or a hardware reset will bring the device to normal operation with the WP#/PD# pin de-asserted.

## Power-on Initialization

microSSD is self-initialized during the first power-up. As soon as the power is applied to the microSSD it reports busy for typically up to seven seconds while performing bad blocks search and low level format. This initialization is a one time event.

During the first self-initialization, the microSSD firmware scans all connected flash media devices and reads their device ID. If the device ID matches the listed flash media devices, the microSSD performs drive recognition based on the algorithm provided by the flash media suppliers, including setting up the bad block table, executing all the necessary handshaking routines for flash media support, and, finally, performing the low-level format.

If the drive initialization fails, and a visual inspection is unable to determine the problem, Micross provides a comprehensive interface for manufacturing flow debug. This interface not only allows debug of the failure and manual reset of the initialization process, but also allows customization of user definable options.

## ATA/IDE Host Interface

The ATA/IDE host interface can be used for microSSD manufacturing support. Micross provides an example of a DOS- and Windows™-based solution (an executable routine) for manufacturing debug and rework.

## Serial Communication Interface (SCI)

For additional manufacturing flexibility, the SCI bus can be used for manufacturing error reporting and for accessing the status of the controller's internal activities. The SCI consists of 3 active signals: SCIDOUT, SCIDIN, and SCICLK. Always provide access to the SCI interface in the PCB design to aid in design validation.

## Lifetime Expectancy

microSSD with advanced NAND management technology significantly extends the life of a product with its extensive ECC and advanced wear-leveling. For applications where data security is essential, microSSD with advanced NAND management technology offers two additional protection features—protection zones and password protections.

Protection zones - Up to four independent protection zones can be enabled as either Read-only or Hid-den (Read/Write protected). If the zones are not enabled, the data is unprotected (default configuration).

Password Protection - Requires a customer-unique password to access information within the protected zones.

## Power-on and Brown-out Reset Characteristics

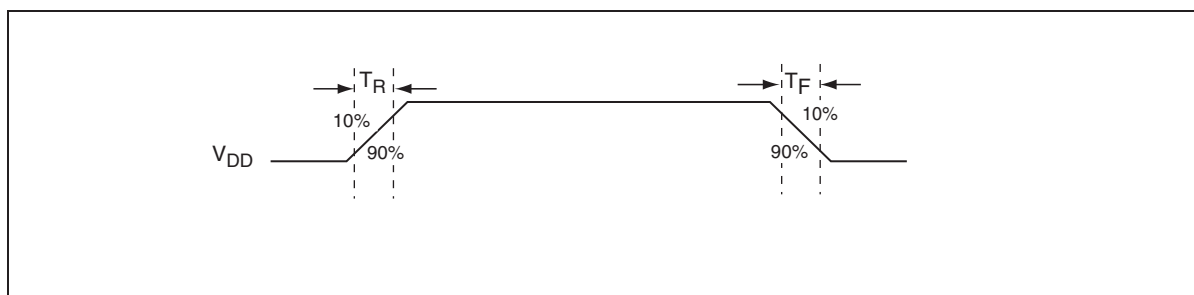Figure 3 and Table 5 detail the Power-on and Brown-out reset characteristics of the AS3uSSD4GB28MPBG.



**Figure 3:** Power-on and Brown-out Reset Timing

### Table 5: Power-on and Brown-out Reset Timing

| Item | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$ Rise Time | $T_R$ | | 250 | ms |
| $V_{DD}$ Fall Time | $T_F$ | | 250 | ms |

## I/O Transfer Function

The default operation for the microSSD is 16-bit. However, if the host issues a Set-Feature command to enable 8-bit mode, the  permits 8-bit microSSD data access.

The following table defines the function of various operations.

### Table 6: I/O Function

| Function Code | CS3FX# | CS1FX# | A0-A2 | IORD# | IOWR# | D15-D8 | D7-D0 |
|---|---|---|---|---|---|---|---|
| Invalid Mode | $V_{IL}$ | $V_{IL}$ | X | X | X | Undefined | Undefined |
| Standby Mode | $V_{IH}$ | $V_{IH}$ | X | X | X | High Z | High Z |
| Task File Write | $V_{IH}$ | $V_{IL}$ | 1-7H | $V_{IH}$ | $V_{IL}$ | X | Data In |
| Task File Read | $V_{IH}$ | $V_{IL}$ | 1-7H | $V_{IL}$ | $V_{IH}$ | High Z | Data Out |
| Data Register Write | $V_{IH}$ | $V_{IL}$ | 0 | $V_{IH}$ | $V_{IL}$ | In[1] | In |
| Data Register Read | $V_{IH}$ | $V_{IL}$ | 0 | $V_{IL}$ | $V_{IH}$ | Out[1] | Out |
| Control Register Write | $V_{IL}$ | $V_{IH}$ | 6H | $V_{IH}$ | $V_{IL}$ | X | Control In |
| Alt Status Read | $V_{IL}$ | $V_{IH}$ | 6H | $V_{IL}$ | $V_{IH}$ | High Z | Status Out |

1.If 8-bit data transfer mode is enabled.

   In 8-bit data transfer mode, High Byte is undefined for Data Out. For Data In, X can be VIH or VIL, but no other value.

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## Software Interface

### microSSD Command Description

This section defines the software requirements and the format of the commands the host sends to the microSSD. Commands are issued to the microSSD by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command register. With the exception of commands listed in Sections "Idle - 97H or E3H", "Set-Sleep-Mode - 99H or E6H",and "Set-WP#/PD#-Mode - 8BH", microSSD complies with ATA-7 Specifications.

### microSSD Command Set

Table 7 summarizes the microSSD command set.

### Table 7:microSSD Command Set (1 of 2)

| Command | Code | FR[1,2] | SC[2,3] | SN[2,4] | CY[2,5] | DH[6,7] | LBA[2,8] |
|---|---|---|---|---|---|---|---|
| Check-Power-Mode | E5H or 98H | - | - | - | - | D | - |
| Execute-Drive-Diagnostic | 90H | - | - | - | - | D | - |
| Flush-Cache | E7H | - | - | - | - | D | - |
| Flush-Cache-EXT | EAH | - | - | - | - | D | - |
| Identify-Drive | ECH | - | - | - | - | D | - |
| Idle | E3H or 97H | - | Y | - | - | D | - |
| Idle-Immediate | E1H or 95H | - | - | - | - | D | - |
| Initialize-Drive-Parameters | 91H | - | Y | - | - | Y | - |
| NOP | 00H | - | - | - | - | D | - |
| Read-Buffer | E4H | - | - | - | - | D | - |
| Read-DMA | C8H or C9H | - | Y | Y | Y | Y | Y |
| Read-DMA-EXT | 25H | - | Y | Y | Y | Y | Y |
| Read-Multiple | C4H | - | Y | Y | Y | Y | Y |
| Read-Multiple-EXT | 29H | - | Y | Y | Y | Y | Y |
| Read-Sector(s) | 20H or 21H | - | Y | Y | Y | Y | Y |
| Read-Sector(s)-EXT | 24H | - | Y | Y | Y | Y | Y |
| Read-Verify-Sector(s) | 40H or 41H | - | Y | Y | Y | Y | Y |
| Read-Verify-Sector(s)-EXT | 42H | - | Y | Y | Y | Y | Y |
| Recalibrate | 1XH | - | - | - | - | D | - |
| Security-Disable-Password | F6H | - | - | - | - | D | - |
| Security-Erase-Prepare | F3H | - | - | - | - | D | - |
| Security-Erase-Unit | F4H | - | - | - | - | D | - |
| Security-Freeze-Lock | F5H | - | - | - | - | D | - |
| Security-Set-Password | F1H | - | - | - | - | D | - |
| Security-Unlock | F2H | - | - | - | - | D | - |
| Seek | 7XH | - | - | Y | Y | Y | Y |
| Set-Features | EFH | Y | - | - | - | D | - |
| SMART | B0H | Y | Y | Y | Y | D | - |
| Set-Multiple-Mode | C6H | - | Y | - | - | D | - |

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## Table 7:microSSD Command Set (continued) (2 of 2)

| Command | Code | FR[1,2] | SC[2,3] | SN[2,4] | CY[2,5] | DH[6,7] | LBA[2,8] |
|---|---|---|---|---|---|---|---|
| Set-Sleep-Mode | E6H or 99H | - | - | - | - | D | - |
| Set-WP#/PD#-Mode | 8BH | Y | - | - | - | D | - |
| Standby | E2H or 96H | - | - | - | - | D | - |
| Standby-Immediate | E0H or 94H | - | - | - | - | D | - |
| Write-Buffer | E8H | - | - | - | - | D | - |
| Write-DMA | CAH or CBH | - | Y | Y | Y | Y | Y |
| Write-DMA-EXT | 35H | - | Y | Y | Y | Y | Y |
| Write-Multiple | C5H | - | Y | Y | Y | Y | Y |
| Write-Multiple-EXT | 39H | - | Y | Y | Y | Y | Y |
| Write-Sector(s) | 30H or 31H | - | Y | Y | Y | Y | Y |
| Write-Sector(s)-EXT | 34H | - | Y | Y | Y | Y | Y |
| Write-Verify | 3CH | - | Y | Y | Y | Y | Y |

1.FR - Features register
2.Y - The register contains a valid parameter for this command.
3.SC - Sector Count register
4.SN - Sector Number register
5.CY - Cylinder registers
6.For the Drive/Head register: Y means both the Drive and Head parameters are used; D means only the Drive parameter is valid and not the Head parameter.
7.DH - Drive/Head register
8.LBA - Logical Block Address mode supported (see command descriptions for use)

## Identify-Drive - ECH

| Bit -> | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Command (7) | ECH | | | | | | | |
| C/D/H (6) | X | | | Drive | X | | | |
| Cyl High (5) | X | | | | | | | |
| Cyl Low (4) | X | | | | | | | |
| Sec Num (3) | X | | | | | | | |
| Sec Cnt (2) | X | | | | | | | |
| Feature (1) | X | | | | | | | |

The Identify-Drive command enables the host to receive parameter information from the microSSD. This command has the same protocol as the Read Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table 8. All reserved bits or words are zero. Table 8 gives the definition for each field in the Identify-Drive information.

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### Table 8:Identify-Drive Information (1 of 2)

| Word Address | Default Value[1] | Total Bytes | Data Field Type Information |
|---|---|---|---|
| 0 | 044AH | 2 | General configuration bit |
| 1 | bbbbH[2] | 2 | Default number of cylinders |
| 2 | 0000H | 2 | Reserved |
| 3 | bbbbH[2] | 2 | Default number of heads |
| 4 | 0000H | 2 | Reserved |
| 5 | 0000H | 2 | Reserved |
| 6 | bbbbH[2] | 2 | Default number of sectors per track |
| 7-8 | bbbbH[3] | 4 | Number of sectors per device (Word 7 = MSW, Word 8 = LSW) |
| 9 | xxxxH | 2 | Vendor Unique |
| 10-14 | eeeeH[4] | 10 | User-programmable serial number in ASCII |
| 15-19 | ddddH[5] | 10 | Micross preset, unique ID in ASCII |
| 20 | 0000H | 2 | Retired |
| 21 | xxxxH | 2 | Vendor Unique |
| 22 | xxxxH | 2 | Vendor Unique |
| 23-26 | aaaaH[6] | 8 | Firmware revision in ASCII. Big Endian Byte Order in Word |
| 27-46 | ccccH[7] | 40 | User Definable Model number |
| 47 | 8000H | 2 | Maximum number of sectors on Read/Write-Multiple command |
| 48 | 0000H | 2 | Reserved |
| 49 | 0B00H | 2 | Capabilities |
| 50 | 0000H | 2 | Reserved |
| 51 | 0200H | 2 | PIO Data Transfer Cycle Timing Mode |
| 52 | 0000H | 2 | Reserved |
| 53 | 0007H | 2 | Translation parameters are valid |
| 54 | nnnnH | 2 | Current numbers of cylinders |
| 55 | nnnnH | 2 | Current numbers of heads |
| 56 | nnnnH | 2 | Current sectors per track |
| 57-58 | nnnnH | 4 | Current capacity in sectors (LBAs) (Word 57 = LSW, Word 58 = MSW) |
| 59 | 010xH | 2 | Multiple sector setting |
| 60-61 | nnnnH | 4 | Total number of sectors addressable in LBA mode |
| 62 | 0000H | 2 | Reserved |
| 63 | 0x07H | 2 | DMA data transfer is supported in NAND Controller |
| 64 | 0003H | 2 | Advanced PIO Transfer mode supported |
| 65 | 0078H | 2 | 120 ns cycle time support for Multi-word DMA Mode-2 |
| 66 | 0078H | 2 | 120 ns cycle time support for Multi-word DMA Mode-2 |
| 67 | 0078H | 2 | PIO Mode-4 supported |
| 68 | 0078H | 2 | PIO Mode-4 supported |
| 69-79 | 0000H | 22 | Reserved |
| 80 | 00FEH | 2 | ATA major version number |
| 81 | 0021H | 2 | ATA minor version number |
| 82 | 706BH | 2 | Features/command sets supported |
| 83 | 7408H | 2 | Features/command sets supported |
| 84 | 4000H | 2 | Features/command sets supported |
| 85-87 | xxxxH | 6 | Features/command sets enabled |
| 88 | 007FH | 2 | UDMA modes |

### Table 8:Identify-Drive Information (continued) (2 of 2)

| Word Address | Default Value[1] | Total Bytes | Data Field Type Information |
|---|---|---|---|
| 89 | xxxxH | 2 | Time required for security erase unit completion |
| 90 | xxxxH | 2 | Time required for enhanced security erase unit completion |
| 91 | 0000H | 2 | Advanced Power Management Level.  This always returns 000H |
| 92 | 0000H | 2 | Reserved |
| 93 | bbbbH | 2 | Hardware reset result |
| 94-99 | 0000H | 12 | Reserved |
| 100-103 | nnnnH | 8 | Maximum user LBA for 48-bit Address feature set |
| 104-127 | 0000H | 48 | Reserved |
| 128 | xxxxH | 2 | Security Status |
| 129-159 | 0000H | 62 | Vendor unique bytes |
| 160-216 | 0000H | 114 | Reserved |
| 217 | 0001H | 2 | Nominal media rotation rate of the device |
| 218-254 | 0000H | 74 | Reserved |

1. xxxx = Don't care. This field is subject to change by the host or the device.
2. bbbb - default value set by controller. The selections could be user programmable.
3. n - calculated data based on product configuration
4. eeee - the default value is '0000000000'
5. dddd - unique number of each device
6. aaaa - any unique SST firmware revision
7. cccc - default value is "xxxMB NANDrive" or "xxxGB microSSD" where xxx is the flash drive capacity.
         The user has an option to change the model number during manufacturing.

### Word 0: General Configuration
This field informs the host that this is a non-magnetic, hard sectored, removable storage device with a transfer rate greater than 10 MByte/sec and is not MFM encoded.

### Word 1: Default Number of Cylinders
This field contains the number of translated cylinders in the default translation mode. This value will be the same as the number of cylinders.

### Word 3: Default Number of Heads
This field contains the number of translated heads in the default translation mode.

### Word 6: Default Number of Sectors per Track
This field contains the number of sectors per track in the default translation mode.

### Word 7-8: Number of Sectors
This field contains the number of sectors per microSSD. This double word value is also the first invalid address in LBA translation mode. This field is only required by CF feature set support.

### Word 10-19: Serial Number
The contents of this field are right justified and padded with spaces (20H). The right-most ten bytes are a Micross preset, unique ID. The left-most ten bytes are a user-programmable value with a default value of "0000000000".

**Word 23-26: Firmware Revision**
This field contains the revision of the firmware for this product.

**Word 27-46: Model Number**
This field is reserved for the model number for this product.

**Word 47: Read-/Write-Multiple Sector Count**
This field contains the maximum number of sectors that can be read or written per interrupt using the Read-Multiple or Write-Multiple commands. Only a value of '1' is supported.

**Word 49: Capabilities**

Bit    Function
13     Standby Timer
       0: forces sleep mode when host is inactive.
11     IORDY Support
       1: microSSD supports PIO Mode-4.
9      LBA support
       1: microSSD supports LBA mode addressing.
8      DMA Support
       1: DMA mode is supported.

**Word 51: PIO Data Transfer Cycle Timing Mode**
This field contains the mode for PIO data transfer. microSSD supports PIO Mode-4.

**Word 53: Translation Parameters Valid**

Bit    Function
0      1: words 54-58 are valid and reflect the current number of cylinders, heads and sectors.
1      1: words 64-70 are valid to support PIO Mode-3 and -4.
2      1: words 88 are valid to support Ultra DMA data transfer.

**Word 54-56: Current Number of Cylinders, Heads, Sectors/Track**
These fields contains the current number of user addressable Cylinders, Heads, and Sectors/Track in the current translation mode.

**Word 57-58: Current Capacity**
This field contains the product of the current cylinders times heads times sectors.

**Word 59: Multiple Sector Setting**
This field contains a validity flag in the Odd Byte and the current number of sectors that can be transferred per interrupt for Read/Write Multiple in the Even Byte. The Odd Byte is always 01H which indicates that the Even Byte is always valid.

The Even Byte value depends on the value set by the Set Multiple command. The Even Byte of this word by default contains a 00H which indicates that Read/Write Multiple commands are not valid.

**Word 60-61: Total Sectors Addressable in LBA Mode**
This field contains the number of sectors addressable for the microSSD in LBA mode only.

**Word 63: Multi-word DMA Transfer Mode**
This field identifies the multi-word DMA transfer modes supported by the microSSD and indicates the mode that is currently selected. Only one DMA mode can be selected at any given time.

Bit      Function
15-11    Reserved
10       Multi-word DMA mode 2 selected
         1: Multi-word DMA mode 2 is selected and bits 8 and 9 are cleared to 0
         0: Multi-word DMA mode 2 is not selected.
9        Multi-word DMA mode 1 selected
         1: Multi-word DMA mode 1 is selected and 8 and 10 should be cleared to 0.
         0: Multi-word DMA mode 1 is not selected.
8        Multi-word DMA mode 0 selected
         1: Multi-word DMA mode 0 is selected and bits 9 and 10 are cleared to 0.
         0: Multi-word DMA mode 0 is not selected.
7-3      Reserved
2        Multi-word DMA mode 2 supported
         1: Multi-word DMA mode 2 and below are supported and Bits 0 and 1 are set to 1.
1        Multi-word DMA mode 1 supported
         1: Multi-word DMA mode 1 and below are supported.
0        Multi-word DMA mode 0 supported
         1: Multi-word DMA mode 0 is supported.

**Word 64: Advanced PIO Data Transfer Mode**
Bits [7:0] is defined as the PIO data and register transfer supported field. If this field is supported, bit 1of word 53 shall be set to one. This field is bit significant. Any number of bits may be set to one in this field by the device to indicate the PIO modes the device is capable of supporting. Of these bits, bits[7:2] are Reserved for future PIO modes.

Bit      Function
0        1:microSSD supports PIO Mode-3.
1        1: microSSD supports PIO Mode-4.

**Word 65: Minimum Multi-word DMA Transfer Cycle Time Per Word**
This field defines the minimum Multi-word DMA transfer cycle time per word. This field defines, in nanoseconds, the minimum cycle time that the microSSD supports when performing Multi-word DMA transfers on a per word basis. microSSD supports up to Multi-word DMA Mode-2, so this field is set to120ns.

Note: microSSD is capable of supporting Multi-word DMA Mode-4 cycle time of 80ns (0050H). Contact Micross sales for more details.

**Word 66: Device Recommended Multi-word DMA Cycle Time**
This field defines the microSSD recommended Multi-word DMA transfer cycle time. This field defines, in nano-seconds, the minimum cycle time per word during a single sector host transfer while performing a multiple sector READ DMA or WRITE DMA command for any location on the media under nominal conditions. If a host runs at a faster cycle rate by operating at a cycle time of less than this value, the microSSD may negate DMARQ for flow control. The rate at which DMARQ is negated could result in reduced throughput despite the faster cycle rate.

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**Word 66: Device Recommended Multi-word DMA Cycle Time (continued)**

Transfer at this rate does not ensure that flow control will not be used, but implies that higher performance may result. microSSD supports Multi-word DMAMode-2, so this field is set to 120ns.

<u>Note</u>: microSSD is capable of supporting Multi-word DMA Mode-4 cycle time of 80ns (0050H). Contact Micross sales for more details.

**Word 67: Minimum PIO Transfer Cycle Time Without Flow Control**

This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the device guarantees data integrity during the transfer without utilization of IORDY flow control. If this field is supported, Bit 1 of word 53 shall be set to one. microSSD supports PIO Mode-4, so this field is set to 120ns.

<u>Note</u>: microSSD is capable of supporting PIO Mode-6 cycle time of 80ns (0050H). Contact Micross sales for more details.

**Word 68: Minimum PIO Transfer Cycle Time With IORDY**

This field defines, in nanoseconds, the minimum cycle time that the device supports while performing data transfers while utilizing IORDY flow control. If this field is supported, Bit 1 of word 53 shall be set to one. microSSD supports PIO Mode-4, so this field is set to 120ns.

<u>Note</u>: microSSD is capable of supporting PIO Mode-6 cycle time of 80ns (0050H). Contact Micross sales for more details.

**Word 80: Major Version Number**

If not 0000H or FFFFH, the device claims compliance with the major version(s) as indicated by bits[6:1] being set to one. Since ATA standards maintain downward compatibility, a device may set more than one bit. AS3uSSD4GB28MPBG supports ATA-1 to ATA-7.

**Word 81: Minor Version Number**

If an implementer claims that the revision of the standard they used to guide their implementation does not need to be reported or if the implementation was based upon a standard prior to the ATA-3 standard, word 81 should be 0000H or FFFFH.
A value of 0021H reported in word 81 indicates ATA-7 T13/1532D volume 1, revision 4b guided the implementation.

**Words 82-84: Features/command sets supported**

Words 82, 83, and 84 indicate the features and command sets supported. A value of 706BH is reported.

**Word 82**

| <u>Bit</u> | <u>Function</u> |
| --- | --- |
| 15 | 0: Obsolete |
| 14 | 1: NOP command is supported |
| 13 | 1: Read Buffer command is supported |
| 12 | 1: Write Buffer command is supported |
| 11 | 0: Obsolete |
| 10 | 0: Host Protected Area feature set is not supported |

**Word 82 (continued)**

| Bit | Function |
|-----|----------|
| 9 | 0: Device Reset command is not supported |
| 8 | 0: Service interrupt is not supported |
| 7 | 0: Release interrupt is not supported |
| 6 | 1: Look-ahead is supported |
| 5 | 1: Write cache is supported |
| 4 | 0: Packet Command feature set is not supported |
| 3 | 1: Power Management feature set is supported |
| 2 | 0: Removable Media feature set is not supported |
| 1 | 1: Security Mode feature set is supported |
| 0 | 1: SMART feature set is supported |

**Word 83**

The values in this word should not be depended on by host implementers.

| Bit | Function |
|-----|----------|
| 15 | 0: Provides indication that the features/command sets supported words are not valid |
| 14 | 1: Provides indication that the features/command sets supported words are valid |
| 13 | 1: Flush Cache Ext command supported |
| 12 | 1: Mandatory Flush Cache command supported |
| 11 | 0: Device Configuration Overlay feature set not supported |
| 10 | 1: 48-bit Address feature set supported |
| 9 | 0: Reserved |
| 8 | 0: Set-Max security extension is not supported |
| 7-5 | 0: Reserved |
| 4 | 0: Removable Media Status feature set is not supported |
| 3 | 1: Advanced Power Management feature set is supported. However, it is No Operation (NOP) and word 91 will always return 0000H. |
| 2 | 0: CFA feature set is not supported |
| 1 | 0: Read DMA Queued and Write DMA Queued commands are not supported |
| 0 | 0: Download Microcode command is not supported |

**Word 84**

The values in this word should not be depended on by host implementers.

| Bit | Function |
|-----|----------|
| 15 | 0: Provides indication that the features/command sets supported words are valid |
| 14 | 1: Provides indication that the features/command sets supported words are valid |
| 13-0 | 0: Reserved |

**Words 85-87: Features/command sets enabled**
Words 85, 86, and 87 indicate features/command sets enabled. The host can enable/disable the features or command set only if they are supported in Words 82-84.

**Word 85**

Bit     Function
15      0: Obsolete
14      0: NOP command is not enabled
        1: NOP command is enabled
13      0: Read Buffer command is not enabled
        1: Read Buffer command is enabled
12      0:Write Buffer command is not enabled
        1: Write Buffer command is enabled
11      0: Obsolete
10      1: Host Protected Area feature set is enabled
9       0: Device Reset command is not enabled
8       0: Service interrupt is not enabled
7       0: Release interrupt is not enabled
6       0: Look-ahead is not enabled
        1: Look-ahead is enabled
5       0: Write cache is not enabled
        1: Write cache is enabled
4       0: Packet Command feature set is not enabled
3       0: Power Management feature set is not enabled
        1: Power Management feature set is enabled
2       0: Removable Media feature set is not enabled
1       0: Security Mode feature set has not been enabled via the Security Set Password command
        1: Security Mode feature set has been enabled via the Security Set Password command
0       0: SMART feature set is not enabled


**Word 86**

Bit     Function
15-14   0: Reserved
13      1: Flush Cache Ext command supported
12      1: Mandatory Flush Cache command supported
11      0: Device Configuration Overlay feature set not supported
10      1: 48-bit Address feature set supported
9       1: 48-bit Address feature set supported
8       1: Set-Max security extension supported
7-5     0: Reserved
4       0: Removable Media Status feature set is not enabled
3       0: Advanced Power Management feature set is not enabled
2       0: CFA feature set is disabled
1       0: Read DMA Queued and Write DMA Queued commands are not enabled
0       0: Download Microcode command is not enabled

**Word 87**
The values in this word should not be depended on by host implementers.
Bit     Function
15      0: Provides indication that the features/command sets supported words are valid
14      1: Provides indication that the features/command sets supported words are valid
13-0    0: Reserved

**Word 88**
Bit     Function
15      Reserved
14      1: Ultra DMA mode 6 is selected
        0: Ultra DMA mode 6 is not selected
13      1: Ultra DMA mode 5 is selected
        0: Ultra DMA mode 5 is not selected
12      1: Ultra DMA mode 4 is selected
        0: Ultra DMA mode 4 is not selected
11      1: Ultra DMA mode 3 is selected
        0: Ultra DMA mode 3 is not selected
10      1: Ultra DMA mode 2 is selected
        0: Ultra DMA mode 2 is not selected
9       1: Ultra DMA mode 1 is selected
        0: Ultra DMA mode 1 is not selected
8       1: Ultra DMA mode 0 is selected
        0: Ultra DMA mode 0 is not selected
7       Reserved
6       1: Ultra DMA mode 6 and below supported
5       1: Ultra DMA mode 5 and below supported
4       1: Ultra DMA mode 4 and below are supported
3       1: Ultra DMA mode 3 and below are supported
2       1: Ultra DMA mode 2 and below are supported
1       1: Ultra DMA mode 1 and below are supported
0       1: Ultra DMA mode 0 is supported

**Word 89: Time required for Security erase unit completion**
Word 89 specifies the time required for the Security Erase Unit command to complete.

| Value | Time |
|-------|------|
| 0 | Value not specified |
| 1-254 | (Value*2) minutes |
| 255 | >508 minutes |

**Word 90: Time required for Enhanced security erase unit completion**

Word 90 specifies the time required for the Enhanced Security Erase Unit command to complete.

| Value | Time |
|-------|------|
| 0 | Value not specified |
| 1-254 | (Value*2) minutes |
| 255 | >508 minutes |

**Word 93: Hardware reset result**

Bit      Function

The contents of bits [12:0] of this word will change only during the execution of the hardware reset.

15       Shall be cleared to zero

14       Shall be set to one

13       1: Device detected CBLID - above VIH
         0: Device detected CBLIP - below VIL

12-8     Device 1 hardware reset result. Device 0 shall clear these bits to zero. Device 1shall set these
         bits as follows:
         12      Reserved.
         11      0: Device 1 did not assert PDIAG-.
                 1: Device 1 asserted PDIAG-.
         10-9    These bits indicate how Device 1 determined the device number:
                 00:     Reserved.
                 01:     A jumper was used.
                 10:     The CSEL signal was used.
                 11:     Some other method was used or the method is unknown.
         8       Shall be set to one.

7-0      Device 0 hardware reset result. Device 1 shall clear these bits to zero. Device 0 shall set these
         bits as follows:
         7       Reserved.
         6       0: Device 0 does not respond when Device 1 is selected.
                 1: Device 0 responds when Device 1 is selected.
         5       0: Device 0 did not detect the assertion of DASP-.
                 1: Device 0 detected the assertion of DASP-.
         4       0: Device 0 did not detect the assertion of PDIAG-.
                 1: Device 0 detected the assertion of PDIAG-.
         3       0: Device 0 failed diagnostics.
                 1: Device 0 passed diagnostics.
         2-1     These bits indicate how Device 0 determined the device number:
                 00: Reserved.
                 01: A jumper was used.
                 10: The CSEL signal was used.
                 11: Some other method was used or the method is unknown.
         0 Shall be set to one.

**Word 128: Security Status**

| Bit | Function |
|-----|----------|
| 8 | Security Level |
| | 1: Security mode is enabled and the security level is maximum |
| | 0: and security mode is enabled, indicates that the security level is high |
| 5 | Enhanced security erase unit feature supported |
| | 1: Enhanced security erase unit feature set is supported |
| 4 | Expire |
| | 1: Security count has expired and Security Unlock and Security Erase Unit are command aborted until a Power-on reset or hard reset |
| 3 | Freeze |
| | 1: Security is frozen |
| 2 | Lock |
| | 1: Security is locked |
| 1 | Enable/Disable |
| | 1: Security is enabled |
| | 0: Security is disabled |
| 0 | Capability |
| | 1: microSSD supports security mode feature set |
| | 0: microSSD does not support security mode feature set |

**Word 217: Nominal Media Rotation Rate**
Word 217 indicates the nominal media rotation rate of the device. For microSSD, the value is always 0001H for this field to indicate non-rotating media.

**Word 255: Integrity Word**
Word 255 is optional. When bits [7:0] of this word contain the signature A5h, bits [15:8] contain the data-structure checksum. The data-structure checksum value is the two's complement of the sum of all bytes in words [254:0] and the byte consisting of bits [7:0] in word 255. Add each byte with unsigned arithmetic, and ignore overflow. When the checksum is correct, the sum of all 512 bytes is zero.

**Set-Features - EFH**

| Bit -> | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|---|---|---|---|---|---|---|---|
| **Command (7)** | EFH | | | | | | | |
| **C/D/H (6)** | | X | | Drive | | X | | |
| **Cyl High (5)** | X | | | | | | | |
| **Cyl Low (4)** | X | | | | | | | |
| **Sec Num (3)** | X | | | | | | | |
| **Sec Cnt (2)** | Config | | | | | | | |
| **Feature (1)** | Feature | | | | | | | |

This command is used by the host to establish or select certain features. Table 9 defines all features that are supported.

## Table 9:Features Supported

| Feature | Operation |
|---|---|
| 01H | Enable 8-bit data transfers. |
| 02H | Enable Write cache |
| 03H | Set transfer mode based on value in Sector Count register. Table 10 defines the values. |
| 05H | Enable Advanced Power Management |
| 09H | Enable Extended Power Operations |
| 55H | Disable Read Look Ahead. |
| 66H | Disable Power-on Reset (POR) establishment of defaults at software reset. |
| 69H | NOP - Accepted for backward compatibility. |
| 81H | Disable 8-bit data transfer. |
| 82H | Disable Write Cache |
| 85H | Disable Advanced Power Management |
| 89H | Disable Extended Power operations |
| 96H | NOP - Accepted for backward compatibility. |
| 97H | Accepted for backward compatibility. Use of this Feature is not recommended. |
| AAH | Enable Read-Look-Ahead |
| CCH | Enable Power-on Reset (POR) establishment of defaults at software reset. |

Features 01H and 81H are used to enable and clear 8-bit data transfer mode. If the 01H feature command is issued all data transfers will occur on the low order D7-D0 data bus and the IOCS16# signal will not be asserted for data register accesses.

Features 02H and 82H allow the host to enable or disable write cache in the microSSD that implement write cache. When the subcommand Disable-Write-Cache is issued, the microSSD should initiate the sequence to flush cache to non-volatile memory before command completion.

Feature 03H allows the host to select the transfer mode by specifying a value in the Sector Count register. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value. One PIO mode is selected at all times. The host may change the selected modes by the Set-Features command.

Feature 55H is the default feature for the microSSD. Therefore, the host does not have to issue Set-Features command with this feature unless it is necessary for compatibility reasons.

Features 66H and CCH can be used to enable and disable whether the Power-on Reset (POR) Defaults will be set when a software reset occurs.

## Table 10:Transfer Mode Values

| Mode | Bits [7:3] | Bits [2:0] |
|------|------------|------------|
| PIO default mode | 00000b | 000b |
| PIO default mode, disable IORDY | 00000b | 001b |
| PIO flow control transfer mode | 00001b | mode[1] |
| Multi-word DMA mode | 00100b | mode[1] |
| Ultra-DMA mode | 01000b | mode[1] |
| Reserved | Other | N/A |

1.Mode = transfer mode number, all other values are not valid

### Idle - 97H or E3H

| Bit -> | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|---|---|---|---|---|---|---|---|
| Command (7) | 97H or E3H | | | | | | | |
| C/D/H (6) | X | | | Drive | X | | | |
| Cyl High (5) | X | | | | | | | |
| Cyl Low (4) | X | | | | | | | |
| Sec Num (3) | X | | | | | | | |
| Sec Cnt (2) | Time Count (5msec increments) | | | | | | | |
| Feature (1) | X | | | | | | | |

This command causes the microSSD to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5 milliseconds and the automatic Power-down mode is enabled. If the sector count is zero, the automatic Power-down mode is also enabled, the timer count is set to 3, with each count being 5 ms. Note that this time base (5 msec) is different from the ATA specification.

### Set-Sleep-Mode - 99H or E6H

| Bit -> | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|---|---|---|---|---|---|---|---|
| Command (7) | 99H or E6H | | | | | | | |
| C/D/H (6) | X | | | Drive | X | | | |
| Cyl High (5) | X | | | | | | | |
| Cyl Low (4) | X | | | | | | | |
| Sec Num (3) | X | | | | | | | |
| Sec Cnt (2) | X | | | | | | | |
| Feature (1) | X | | | | | | | |

This command causes the microSSD to set BSY, enter the Sleep mode, clear BSY and generate an interrupt. Recovery from sleep mode is accomplished by simply issuing another command (a reset is permitted but not required). Sleep mode is also entered when internal timers expire so the host does not need to issue this command except when it wishes to enter Sleep mode immediately. The default value for the timer is 15 milliseconds.

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**PRELIMINARY**

### Set-WP#/PD#-Mode - 8BH

| Bit -> | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Command (7) | 8BH | | | | | | | |
| C/D/H (6) | | X | | Drive | | X | | |
| Cyl High (5) | 6EH | | | | | | | |
| Cyl Low (4) | 44H | | | | | | | |
| Sec Num (3) | 72H | | | | | | | |
| Sec Cnt (2) | 50H | | | | | | | |
| Feature (1) | 55H or AAH | | | | | | | |

This command configures the WP#/PD# pin for either the Write Protect mode or the Power-down mode. When the host sends this command to the device with the value AAH in the feature register, the WP#/PD# pin is configured for the Write Protect mode. The Write Protect mode is the factory default setting. When the host sends this command to the device with the value 55H in the feature register, WP#/PD# is configured for the Power-down mode. (WP# / PD#, as well as all other pin descriptions with a # suffix, are active low.)

All values in the C/D/H register, the Cylinder Low register, the Cylinder High register, the Sector Number register, the Sector Count register, and the Feature register need to match the values shown above, otherwise, the command will be treated as an invalid command.

Once the mode is set with this command, the device will stay in the configured mode until the next time this command is issued. Power-off or reset will not change the configured mode.

## Error Posting

The following table summarizes the valid status and error values for the microSSD command set.

### Table 11:Error and Status Register[1] (1 of 2)

| Command | Error Register | | | | | Status Register | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | ICRC/BK | UNC | IDNF | ABRT | AMNF | RDY | DWF | DSC | CORR | ERR |
| Check-Power-Mode | | | | V | | V | V | V | | V |
| Execute-Drive-Diagnostic[2] | | | | | | V | | V | | V |
| Flush-Cache | | | | V | | V | V | V | | V |
| Flush-Cache-EXT | | | | V | | V | V | V | | V |
| Identify-Drive | | | | V | | V | V | V | | V |
| Idle | | | | V | | V | V | V | | V |
| Idle-Immediate | | | | V | | V | V | V | | V |
| Initialize-Drive-Parameters | | | | | | V | | V | | V |
| NOP | | | | V | | V | V | | | V |
| Read-Buffer | | | | V | | V | V | V | | V |
| Read-DMA | V | V | V | V | V | V | V | V | V | V |
| Read-DMA-EXT | V | V | V | V | V | V | V | V | V | V |

## Table 11:Error and Status Register[1] (2 of 2)

| Command | Error Register | | | | | Status Register | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | ICRC/BBK | UNC | IDNF | ABRT | AMNF | RDY | DWF | DSC | CORR | ERR |
| Read-Multiple | V | V | V | V | V | V | V | V | V | V |
| Read-Multiple-EXT | V | V | V | V | V | V | V | V | V | V |
| Read-Sector(s) | V | V | V | V | V | V | V | V | V | V |
| Read-Sector(s)-EXT | V | V | V | V | V | V | V | V | V | V |
| Read-Verify-Sector(s) | V | V | V | V | V | V | V | V | V | V |
| Read-Verify-Sector(s)-EXT | V | V | V | V | V | V | V | V | V | V |
| Recalibrate | | | | V | | V | V | V | | V |
| Security-Disable-Password | | | | V | | V | V | V | | V |
| Security-Erase-Prepare | | | | V | | V | V | V | | V |
| Security-Erase-Unit | | | | V | | V | V | V | | V |
| Security-Freeze-Lock | | | | V | | V | V | V | | V |
| Security-Set-Password | | | | V | | V | V | V | | V |
| Security-Unlock | | | | V | | V | V | V | | V |
| Seek | | | V | V | | V | V | V | | V |
| Set-Features | | | | V | | V | V | V | | V |
| Set-Multiple-Mode | | | | V | | V | V | V | | V |
| Set-Sleep-Mode | | | | V | | V | V | V | | V |
| Set-WP#/PD#-Mode | | | | V | | V | | V | | V |
| SMART | | | | V | | V | | V | | V |
| Standby | | | | V | | V | V | V | | V |
| Standby-Immediate | | | | V | | V | V | V | | V |
| Write-Buffer | | | | V | | V | V | V | | V |
| Write-DMA | V | | V | V | V | V | V | V | | V |
| Write-DMA-EXT | V | | V | V | V | V | V | V | | V |
| Write-Multiple | V | | V | V | V | V | V | V | | V |
| Write-Multiple-EXT | V | | V | V | V | V | V | V | | V |
| Write-Sector(s) | V | | V | V | V | V | V | V | | V |
| Write-Sector(s)-EXT | V | | V | V | V | V | V | V | | V |
| Write-Verify | V | | V | V | V | V | V | V | | V |
| Invalid-Command-Code | | | | V | | V | V | V | | V |

1.The host is required to reissue any media access command (such as Read-Sector and Write Sector) that ends with an error condition.

2.See Table 8, V = valid on this command.

**PRELIMINARY**

## Electrical Specifications

**Absolute Maximum Stress Ratings** (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Storage Temperature . . . . . . . . . . . . . . . . . . . . . . . ...... . . . . . . . . . . . .... . . . . . . . -55°C to +125°C
D.C. Voltage on Pins[1] I1, I2, O2, O3, and O4 to Ground Potential. . .. . . . . . . . .. . . . .-0.5V to $V_{DD}$+0.5V
Transient Voltage (<20 ns) on Pins[1] I1, I2, O2, O3, and O4 to Ground Potential.. . . -2.0V to $V_{DD}$+2.0V
Package Power Dissipation Capability (TA = 25°C). . . . . . . . . . . . . . . . ... . . . . . . . . . . . . . . . ...1.0W
Surface Mount Solder Reflow Temperature. . . . . . . . . . . . . . . . . . . . . . . . . . .260°C for 10 seconds
Output Short Circuit Current[2] . . . . . . . . . . . . . . .. . . . . . . . . . . . . . . . . . . . . . . . . .60 mA

1.Refer to Table 1 for pin assignment information.
2.Outputs shorted for no more than one second. No more than one output shorted at a time.

## Table 12: Absolute Maximum Power Pin Stress Ratings

| Parameter | Symbol | Conditions |
|---|---|---|
| Input Power | $V_{DD}$ | -0.3V min to 4.0V max |
| Voltage on all other pins with respect to $V_{SS}$ | | -0.5V min to VDD + 0.5V max |

## Table 13: Operating Range

| | | $V_{DD}$ | |
|---|---|---|---|
| | | **3.3V** | |
| **Range** | **Ambient Temperature** | **Min.** | **Max.** |
| Extended | -20°C to +85°C | 3.135V | 3.465V |

## Table 14: AC Conditions of Test[1]

| Input Rise / Fall Time | Output Load |
|---|---|
| 5ns | $C_L$ = 100pF |

1.See Figure 4

## Table 15: Recommended System Power-on Timing

| Symbol | Parameter | Typical | Maximum | Units |
|---|---|---|---|---|
| $T_{PU-INITIAL}$ | Drive Initialization to Ready | 7 | 50 | sec |
| $T_{PU-READY1}$[1] | Host Power-on/Reset to Ready Operation | 700 | 2000 | ms |
| $T_{PU-WRITE1}$[1] | Host Power-on/Reset to Write Operation | 700 | 2000 | ms |

1.This parameter is measured only for initial qualification and after a design or process change that could affect this

parameter.

**PRELIMINARY**

## Table 16:Capacitance (Ta = 25°C, f=1 MHz, other pins open)

| Parameter | Description | Test Condition | Maximum |
|---|---|---|---|
| $C_{I/O}$[1] | I/O Pin Capacitance | $V_{I/O}$ = 0V | 15 pF |
| $C_{IN}$[1] | Input Capacitance | $V_{IN}$ = 0V | 9 pF |

1.This parameter is measured only for initial qualification and after a design or process
   change that could affect this parameter.

## Table 17:Reliability Characteristics

| Symbol | Parameter | Minimum Specification | Units | Test Method |
|---|---|---|---|---|
| $I_{LTH}$[1] | Latch Up | $100 + I_{DD}$ | mA | JEDEC Standard 78 |

1.This parameter is measured only for initial qualification and after a design or process
   change that could affect this parameter.

## DC Characteristics

## Table 18:DC Characteristics for Host Interface

| Symbol | Type | Parameter | Min | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{IH1}$ | I1 | Input Voltage | 2 | | V | $V_{DD} = V_{DD}$ Max |
| $V_{IL1}$ | | | | 0.8 | V | $V_{DD} = V_{DD}$ Min |
| $I_{IL1}$ | I1Z | Input Leakage Current | -10 | 10 | µA | $V_I = V_{DD}$ Max or 0V |
| $I_{D1}$ | I1D | Input Pull-Down Current | 20 | 120 | µA | $V_{DD} = V_{DD}$ Max, $V_{IN} = V_{DD}$ Min |
| $I_{U1}$ | I1U | Input Pull-Up Current | -120 | -20 | µA | $V_{DD} = V_{DD}$ Max , $V_{IN}$ = GND |
| $V_{T+}$ | I2 | Input Voltage Schmitt Trigger | | 1.75 | V | $V_{DD} = V_{DD}$ Max |
| $V_{T-}$ | | | 1.09 | | V | $V_{DD} = V_{DD}$ Min |
| $I_{IL2}$ | I2Z | Input Leakage Current | -10 | 10 | µA | $V_I = V_{DD}$ Max or 0V |
| $I_{U2}$ | I2U | Input Pull-Up Current | -120 | -20 | µA | $V_{DD} = V_{DD}$ Max, $V_{IN}$ = GND |
| $V_{OH2}$ | O2 | Output Voltage | 2.4 | | V | $I_{OH2}=I_{OH2}$ Min |
| $V_{OL2}$ | | | | 0.4 | V | $I_{OL2}=I_{OL2}$ Max |
| $I_{OH2}$ | | Output Current | -4 | | mA | $V_{DD} = V_{DD}$ Min |
| $I_{OL2}$ | | | | 4 | mA | $V_{DD} = V_{DD}$ Min |
| $V_{OH3}$ | O3 | Output Voltage | 2.4 | | V | $I_{OH3}=I_{OH3}$ Min |
| $V_{OL3}$ | | | | 0.4 | V | $I_{OL3}=I_{OL3}$ Max |
| $I_{OH3}$ | | Output Current | -8 | | mA | $V_{DD} = V_{DD}$ Min |
| $I_{OL3}$ | | | | 8 | mA | $V_{DD} = V_{DD}$ Min |
| $V_{OH4}$ | O4 | Output Voltage | 2.4 | | V | $I_{OH4}=I_{OH4}$ Min |
| $V_{OL4}$ | | | | 0.4 | V | $I_{OL4}=I_{OL4}$ Max |
| $I_{OH4}$ | | Output Current | -12 | | mA | $V_{DD} = V_{DD}$ Min |
| $I_{OL4}$ | | | | 8 | mA | $V_{DD} = V_{DD}$ Min |

## Table 19: Power Consumption

| Symbol | Type | Device | Parameter | Min | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| $I_{DD}{}^{1,2}$ | PWR | AS3uSSD4GB28MPBG | Power supply current ($T_A$ = -20°C to +85°C) | | 225 | mA | $V_{DD}$=$V_{DD}$ Max |
| $I_{SP}$ | PWR | AS3uSSD4GB28MPBG | Sleep/Standby/Idle current ($T_A$ = -20°C to +85°C) | | 6.0 | mA | $V_{DD}$=$V_{DD}$ Max |

1. Sequential data transfer from host interface and write data to media.

2. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
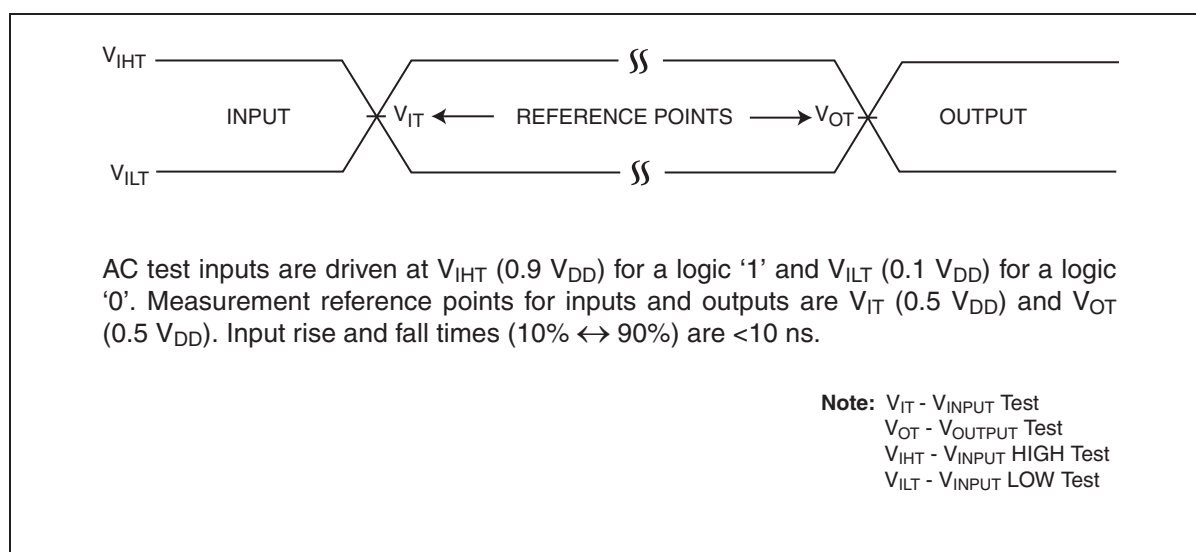
## AC Characteristics



AC test inputs are driven at $V_{IHT}$ (0.9 $V_{DD}$) for a logic '1' and $V_{ILT}$ (0.1 $V_{DD}$) for a logic '0'. Measurement reference points for inputs and outputs are $V_{IT}$ (0.5 $V_{DD}$) and $V_{OT}$ (0.5 $V_{DD}$). Input rise and fall times (10% ↔ 90%) are <10 ns.

**Note:** $V_{IT}$ - $V_{INPUT}$ Test
$V_{OT}$ - $V_{OUTPUT}$ Test
$V_{IHT}$ - $V_{INPUT}$ HIGH Test
$V_{ILT}$ - $V_{INPUT}$ LOW Test

**Figure 4:** AC Input/Output Reference Waveforms

## Appendix

### Differences Between the Micross microSSD and ATA Specifications

### Idle Timer
The Idle timer uses an incremental value of 5 ms, rather than the 5 sec minimum increment value specified in ATA specifications.

### Recovery from Sleep Mode
For microSSD devices, recovery from sleep mode is accomplished by simply issuing another command to the device. A hardware or software reset is not required.
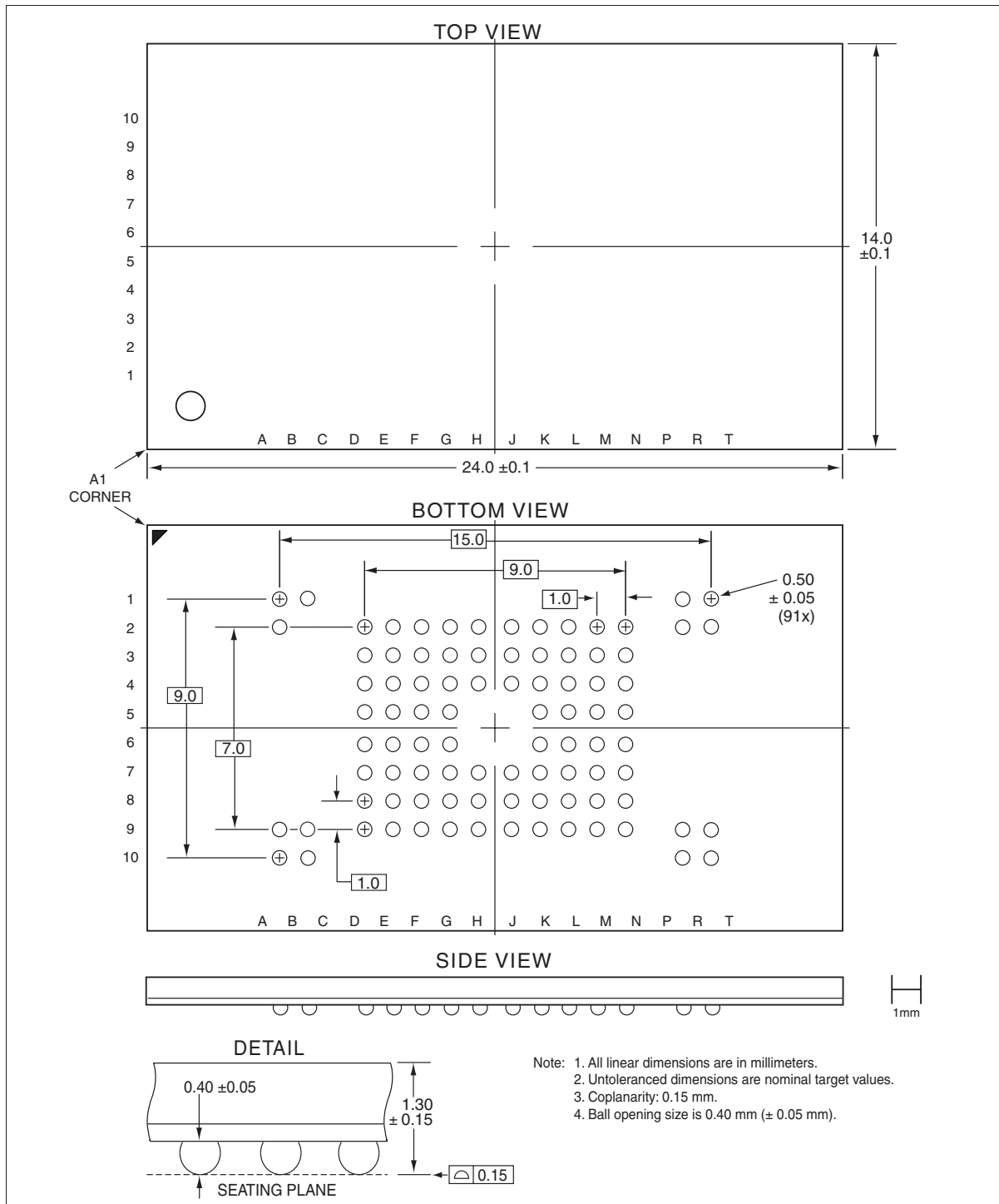
**PRELIMINARY**

## Packaging Diagram



**Figure 5:    microSSD** 91-Ball, Plastic Ball Grid Array (PBGA)
Micross Package Code: PBG

## PRELIMINARY

## Order Chart

| Part Number | Storage Density | Sustained Transfer Rate (Read) | Sustained Transfer Rate (Write) | Processing |
|---|---|---|---|---|
| AS3uSSD4GB28MPBGR | 4GB* | 28MByte/s | 7MByte/s | Extended (RoHS) |
| AS3uSSD4GB28MPBG | 4GB* | 28MByte/s | 7MByte/s | Extended |

\* Raw storage capacity, actual usable capacity may be less.

R = RoHS Compliant / Lead Free

Blank = Sn / Pb Ball Option

**\*AVAILABLE PROCESSES**
Blank = Extended Temperature Range
/IT = Industrial Temperature Range

**Temperature**
-20°C to +85°C
-40°C to +85°C (contact factory / refer to AS3uSSD4GB50S and AS3uSSD8GB50S datasheets)

## PRELIMINARY

**DOCUMENT TITLE**

4GB microSSD™ Solid State Disk

**REVISION HISTORY**

| Rev # | History | Release Date | Status |
|---|---|---|---|
| 0.0 | Initial Release | April 2010 | Preliminary |
| 0.1 | Changed part number to AS3uSSD4GB28MPBG, Change temp range to -20C to +85C, changed temp from enhanced to extended | June 2010 | Preliminary |
| 0.2 | Updated Set-WP#/PD# Mode paragraph pg 26, updated order chart pg 32, moved credits to page 33 | August 2010 | Preliminary |
| 0.3 | Updated features, write performance to 7MBytes / sec, page 1. Minor rev. to General Description, Embedded Flash File System, page 3. Updated pin assignments, pin E2 & M9 is VDD, page 5. Updated Tables: 1, 3, 5, 8, 9, 12, 13, 18, 19, Figure 3, 5 & Order chart, page 32. Updated Absolute Maximum Stress Ratings, page 28. Omitted Temp. Under Bias, VDDQ and Through hole soldering temp. Increased storage temp to -55°C to +125°C | September 2010 | Preliminary |
| 0.4 | Updated order chart on page 32 | November 2011 | Preliminary |

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