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MITEL®

CMOS **MD4330B/MD4332B** 30/32 Segment LCD Driver

FEB. 1985

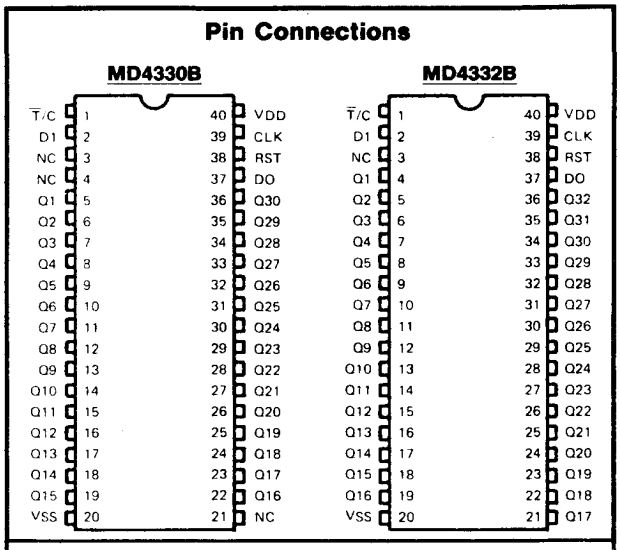
Features

- CMOS Low power
- 3 to 18 volt operation
- On-chip wave-shaping
- High-speed (typ. 3 MHz) shift register
- Std. 40-pin Dual-In-Line packages

Pin Names

- DI – Serial Data Input
- DO – Serial Data Output
- CLK – Clock (positive transition) Input
- RST – Master Reset (active HIGH) Input
- $\overline{T}/C$ – True/Complement (active LOW) Input
- Q1 thru Q32 – True/Complement Outputs

Pin Connections



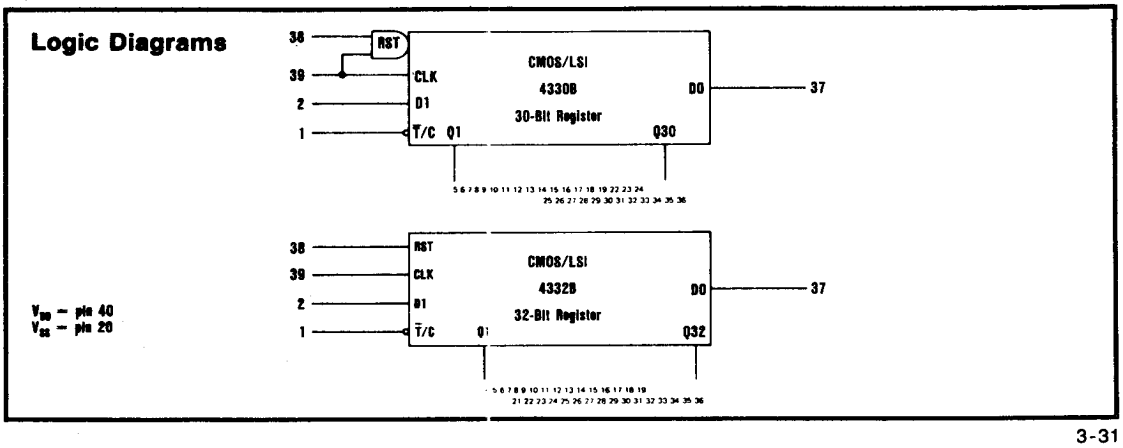
Ordering Information

MD4330BC	40-Pin Ceramic DIP
MD4330BE	40-Pin Epoxy DIP
MD4332BC	40-Pin Ceramic DIP
MD4332BE	40-Pin Epoxy DIP

Description

The MD4330B and 4332B are CMOS 30- and 32-bit static shift registers incorporating selectable true/complement outputs for each bit. These devices are well suited to drive LCD readouts directly since the AC signals required for the display may be generated simply by applying a low frequency signal directly to the True-Complement input pin and to the backplane of the display. One of these devices can drive four 7-segment displays or two 14-segment alphanumeric displays plus decimal points or two 16-segment alphanumeric displays directly.

Logic Diagrams



Absolute Maximum Rating (Referenced to VSS)

Item	Symbol	Limits	Unit
DC Supply Voltage	V_{DD}	−0.5 to 18	Vdc
Input Voltage	V_{IN}	−0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Ranges	TA	−40 to 85	°C
Storage Temperature Range	T_{STG}	−65 to 125	°C

Functional Description

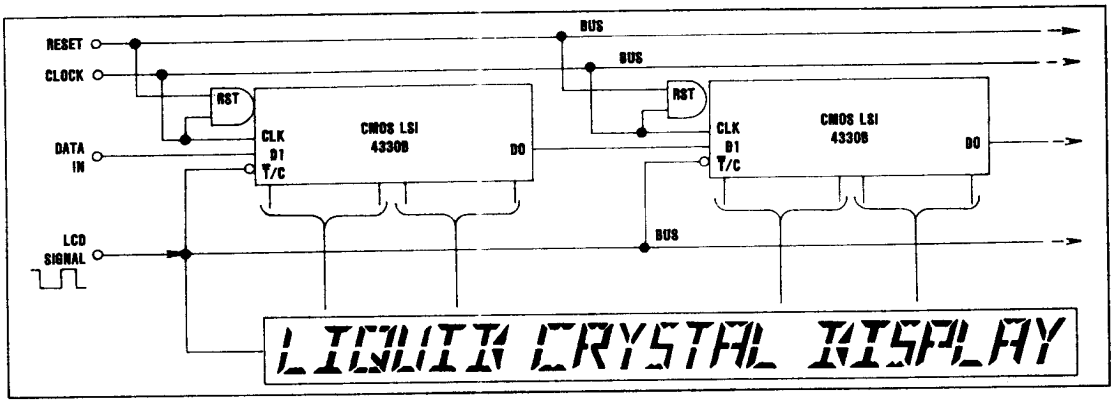
The 4330B and 4332B are CMOS/LSI static shift registers designed to drive all types of LCD readouts directly or as serial-to-parallel converters where both the true and complementary parallel outputs are available.

The circuits accept a serial input DI which is shifted into the register on the positive transition of the clock (CLK) input. A feature of these circuits is that the clock input and the true/complement control (T/C) input have wave-shaping circuits to ensure fast edges on-chip regardless of the shape of the incoming signals.

The 4330B type also has the reset (RST) input gated with the clock input for synchronous reset on the positive transition of the clock. The 4332B has asynchronous reset (RST) inputs which are active logic-level HIGH.

The parallel outputs of the shift registers are available in either true or complementary form dependent on the state of the true/complement control input. When input is logic-level LOW, the true form is available at all parallel outputs and when the input goes HIGH, the parallel outputs immediately revert to the complementary form of the data stored in each register. This action is independent of the clock input condition. A serial data (D_o) output is provided for applications using longer shift registers, etc. This output is the true form of the last stage of the register.

Application



D.C. Electrical Characteristics at $T_A = 25°C$

Characteristic		Symbol	Test Conditions	V_O Volts	V_{DD} Volts	Limits Min.	Limits Typ.	Limits Max.	Units
Quiescent Device Current		I_L			5	–	0.5	50	μA
					10	–	1	100	
Output Voltage	Low-Level	V_{OL}			5	–	0	0.01	V
					10	–	0	0.01	
	High-Level	V_{OH}			5	4.99	5	–	
					10	9.99	10	–	
Noise Immunity (Any Input)		V_{NL}		0.8	5	1.5	2.25	–	V
				1.0	10	3	4.5	–	
		V_{NH}		4.2	5	1.5	2.25	–	
				9.0	10	3	4.5	–	
Output Drive Current	D OUT	I_DN	N-Channel	0.5	5	0.8	1.7	–	mA
				0.5	10	1.0	3.0	–	
		I_DP	P-Channel	4.5	5	0.35	−0.9	–	
				9.5	10	−0.8	−1.9	–	
	Q OUT	I_DN	N-Channel	0.5	10	50	250	–	μA
		I_DN	P-Channel	9.5	10	−50	−250	–	
Input Current		I_I				–	10	–	pA

A.C. Electrical Characteristics at $T_A = 25°C$, $C_L = 50$ pF

Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C. All input rise and fall times = 20 ns.

Characteristic	Symbol	Test Conditions	V_{DD} Volts	Limits Min.	Limits Typ.	Limits Max.	Units
Propagation Delay Time	t_{PHL} t_{PLH}		10	–	300	–	ns
Transition Time	t_{THL}	D OUT (CL = 50 pF)	10	–	70	130	ns
	t_{TLH}	Q OUT (CL = 15 pF)	10	–	300	–	ns
Maximum Clock Frequency	f_{CL}		10	1.0	3.0	–	MHz
Minimum Clock Pulse Width	t_{WL} t_{WH}		10	–	200	–	ns
Minimum Reset Pulse Width	$t_{WH(R)}$		10	–	200	–	ns
Input Capacitance	C_I	Any Input		–	5	–	pF