ANALOG DEVICES

Preliminary Data Sheet

ADAQ7767-1

Flexible Resistive Input, 24-Bit, 1MSPS, Alias-Free μModule® DAQ Solution

FEATURES

- Highly integrated data acquisition solution
- Wide Input Common Mode Range of -16V to +12V
- Maximum input range of ±28V differential
- 3 Pin-Selectable Gain Options
  - G = 1, 0.364, 0.143 V/V
- 4th order AAF with maximum flatness and linear phase
  - Full aliasing protection with 80 dB typ rejection
- Excellent device to device phase matching and drift
- Combined precision ac and dc performance
  - Total system dynamic range up to 124 dB
  - -115 dB typical THD at ±28V input range (IN3)
  - 79 dB DC CMRR at ±28V input range (IN3)
  - ±3 ppm typ INL
  - 5 ppm/°C max gain drift
  - ± 0.2° maximum device phase matching at 20 kHz
- Programmable output data rate, filter type, and latency
  - Linear phase digital filter options:
    - Wideband low ripple FIR filter (256 kSPS, 110 kHz max input BW)
    - Sinc5 Filter (1.024 MSPS, 208.9 kHz max input BW, 4 uS max group delay)
    - Sinc3 Filter (50/60Hz rejection)
- Integrated LDO
- Built-in supply decoupling capacitors
- Configuration through pin strapping or SPI interface
- Digital interface optimized for isolated applications
- Suite of diagnostic check mechanisms
- Operating temperature range: −40°C to +105°C
- Packaging: 12 mm × 6 mm × 1.6 mm 84-ball BGA with 0.8mm ball-pitch
  - 8x footprint reduction versus discrete solution

APPLICATIONS

- Universal input measurement platform
- Electrical Test & Measurement
- Sound & Vibration, Acoustic & Material Science R&D
- Control & Hardware in Loop Verification
- Condition monitoring for predictive maintenance
- Audio Test

Protected by U.S. Patent 10,680,633 B1

Protected by U.S. Patent 10,979,062 B2

FUNCTIONAL BLOCK DIAGRAM

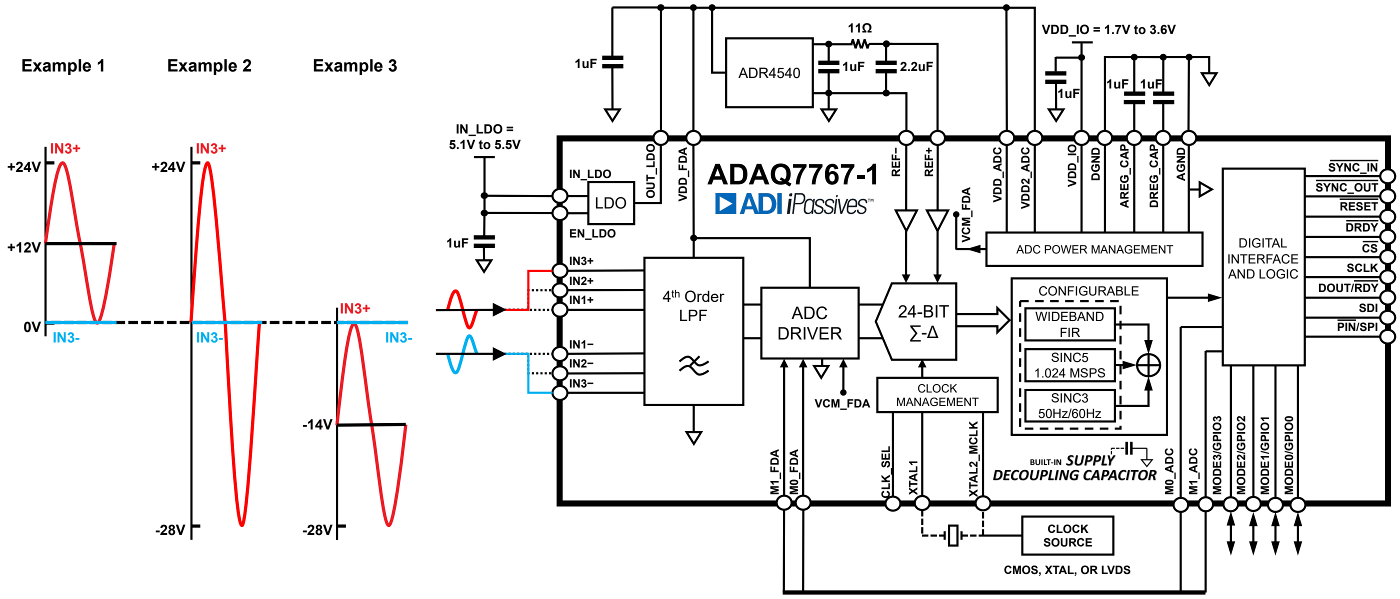

Figure 1. Block Diagram

Rev. PrE

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

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GENERAL DESCRIPTION

The ADAQ7767-1 is a 24-bit precision data acquisition (DAQ) μModule® system that encapsulates signal conditioning, conversion, and processing blocks into one system in package (SiP) design that enables rapid development of highly compact, high performance precision DAQ systems.

The ADAQ7767-1 consists of:

- A fourth order, low noise, linear phase anti-aliasing filter (AAF)
- A low noise, low distortion, high bandwidth, gain-selectable ADC driver plus an optional linearity boost buffer
- A high-performance medium bandwidth 24-bit sigma delta ADC with programmable digital filter
- A low noise, low dropout linear regulator
- Reference buffers
- Critical passive components required for the signal chain

The ADAQ7767-1 supports a wide variety of input types, which include unipolar and bipolar single-ended, pseudo-differential and differential signals, with a maximum differential range of ±28V and a common mode voltage range of −16V to +12V using IN3. With the precision of Analog Devices's iPASSIVES™ technology, ADAQ7767-1 performs with excellent common mode rejection ratio (CMRR). The three pairs of pin-selectable gain settings offer additional system dynamic range and improved signal chain noise performance with input signals of lower amplitude. In applications requiring high input impedance, ADAQ7767-1 allows the customer to choose their preferred input amplifier.

A 4th order low-pass analog filter combined with the user programmable digital filter ensures the signal chain is fully protected against the high frequency noise and out of band tones presented at the input node from aliasing back into the band of interest. The analog low pass filter is carefully designed to achieve high phase linearity and maximum in-band magnitude response flatness. Constructed with iPASSIVES™ technology, the resistor network used within the analog low-pass filter possess superior resistance matching in both absolute values and over temperature. As a result, the signal chain performance is maintained with minimum drift over temperature and the ADAQ7767-1 has an excellent device to device phase matching performance.

A high-performance ADC driver amplifier ensures the full settling of the ADC input at the maximum sampling rate. The driver circuit is designed to have minimum additive noise, error, and distortion while maintaining stability. The fully differential architecture helps maximizing the signal chain dynamic range.

The analog to digital converter (ADC) inside the ADAQ7767-1 is a high performance, 24-bit precision, single channel Sigma-Delta converter with excellent AC performance and DC precision and a throughput rate of 256 kSPS from a 16.384 MHz MCLK. It includes an optional linearity boost buffer that can further improve the signal chain linearity.

The ADAQ7767-1 is specified with the input reference voltage of 4.096V, but the device can support reference voltages ranging from VDD_ADC down to 1V.

The ADAQ7767-1 has two types of reference buffers. A precharge reference buffer to ease the reference input driving requirement or a full reference buffer to provide high impedance reference input. Both buffers are optional and can be turned off through register configuration.

ADAQ7767-1 supports three clock input types: crystal, CMOS or LVDS.

Three types of digital low pass filters are available on the ADAQ7767-1. The wideband low ripple FIR filter has a filter profile similar to an ideal brick wall filter, making it a great fit for doing frequency analysis. The Sinc5 filter has a low latency path with a smooth step response while maintaining a good level of aliasing rejection. It supports an output data rate up to 1.024 MSPS from a 16.384 MHz MCLK, making the Sinc5 filter ideal for low latency data capturing and time domain analysis. The Sinc3 filter supports a wide decimation ratio and can produce output data rate down to 50 SPS from a 16.384 MHz MCLK. This combined with the simultaneous 50/60Hz rejection post filter makes Sinc3 filter especially useful for precision DC measurement. All the three digital filters on the ADAQ7767-1 are FIR filters with linear phase response. The bandwidth of the filters, which directly corresponds to the bandwidth of the DAQ signal chain are fully programable through register configuration.

The ADAQ7767-1 supports two device configuration methods. The user has the option to choose to configure the device via register write through its SPI interface, or through a simple hardware pin strapping method to configure the device to operate under a number of pre-defined modes.

A single SPI interface supports both the register access and the sample data readback functions. The ADAQ7767-1 always acts as a SPI slave. Multiple interface modes are supported with a minimum of three IO channels required to communicate with the device.

ADAQ7767-1 features a suite of internal diagnostic functions that can detect a broad range of errors during operation to help improving the system reliability.

The ADAQ7767-1 supply connections can be greatly simplified by using its internal LDO. 0.1 uF decoupling capacitors are also integrated to further reduce the number of discrete components.

On power standby, each functional block of the device can be put into standby mode. This enables the device to have a total power consumption less than TBD mW.

The ADAQ7767-1 device has an operating temperature range of −40°C to +105°C and is available in a 12mm x 6mm, 84-ball BGA package with 0.8mm ball pitch, making it suitable for multiple-channel applications. The footprint of the device is eight times smaller

GENERAL DESCRIPTION

compared to the footprint of the same solution using discrete components.

SPECIFICATIONS

AGND = DGND = 0 V, Input common mode voltage = 0 V, IN_LDO = EN_LDO = 5.1 V to 5.5 V, OUT_LDO = VDD_FDA = VDD_ADC, VDD2_ADC = 2 V to 5.5 V, VDD_IO = 1.7 V to 3.6 V, REF+ = 4.096 V, REF−= 0 V, MCLK = SCLK = 16.384 MHz 50:50 duty cycle, f_{MOD} = MCLK/2, Filter = Wideband Low Ripple, Decimation = 32, ODR = 256 kSPS, linearity boost buffer on, reference precharge buffers on, FDA = Full Power Mode, T_A = -40°C to 105°C, unless otherwise noted. Typical values are at T_A = 25°C.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ANALOG INPUT CHARACTERISTICS					
Full-Scale Input Range (FSR)	Differential IN+ to IN-				
	FSR = ±V_{REF} / AFE_GAIN				
	Differential IN1+/-		±4.096		V
	Differential IN2+/-		±11.264		V
	Differential IN3+/-		±28.672		V
Input Common Mode Range	IN1+/-	-2.1		4.5	V
	IN2+/-	-6.1		6.2	V
	IN3+/-	-16		12	V
Analog Front-End Gain (AFE_GAIN)	IN1+/-, G = 1		1		V/V
	IN2+/-, G = 0.364		4/11		V/V
	IN3+/-, G = 0.143		1/7		V/V
Common-Mode Rejection DC	DC to 60Hz, RTI				
	IN1+/-		81.8		dB
	IN2+/-		78.5		dB
	IN3+/-		78.8		dB
Common-Mode Rejection AC	f = 10 kHz, RTI				
	IN1+/-		TBD		dB
	IN2+/-		TBD		dB
	IN3+/-		TBD		dB
Input Resistance, R_{IN}	Fully Differential Configuration				
	IN1+/-		4		kΩ
	IN2+/-		11		kΩ
	IN3+/-		28		kΩ
	Single-Ended to Differential Configuration				
	IN1+ = Input, IN1− = GND		2.67		kΩ
	IN2+ = Input, IN2− = GND		6.35		kΩ
	IN3+ = Input, IN3− = GND		14.93		kΩ
OVERALL SYSTEM DC ACCURACY					
Gain Error	RTI				
	IN1+/-		±0.02	±TBD	%
	IN2+/-		±0.01	±TBD	%
	IN3+/-		±0.02	±TBD	%
Gain Error Drift	RTI, Endpoint Method				
	IN1+/-	TBD	-1	TBD	ppm/°C
	IN2+/-	TBD	-1	TBD	ppm/°C
	IN3+/-	TBD	-1	TBD	ppm/°C
Offset Error	RTI				
	IN1+/-		TBD	TBD	mV
	IN2+/-		TBD	TBD	mV
	IN3+/-		TBD	TBD	mV
Offset Error Drift	RTI, Endpoint Method				
	IN1+/-	TBD	TBD	TBD	uV/°C
	IN2+/-	TBD	TBD	TBD	uV/°C

SPECIFICATIONS

Table 1. (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	IN3+/-	TBD	TBD	TBD	uV/°C
Integral Nonlinearity (INL)	Endpoint method				
	IN1+/-, Differential Input, −40°C < T_A < +105°C		±3	±TBD	ppm of FSR
	IN2+/-, Differential Input, −40°C < T_A < +105°C		±3	±TBD	ppm of FSR
	IN3+/-, Differential Input, −40°C < T_A < +105°C		±3	±TBD	ppm of FSR
Low Frequency Noise	Sinc3 filter, ODR= 50 SPS, BW = 15 Hz, shorted input, RTI				
	IN1+/-		0.51		uV rms
	IN2+/-		1.48		uV rms
	IN3+/-		3.23		uV rms
Peak-to-Peak Resolution[1]	Sinc3 filter, ODR= 50 SPS, BW = 15 Hz, shorted input, RTI				
	IN1+/-		21.2		bits
	IN2+/-		21.1		bits
	IN3+/-		21.3		bits
OVERALL SYSTEM AC PERFORMANCE	Wideband Low Ripple FIR Filter, ODR = 256 kSPS, DEC_RATE = 32, BW = 110.8 kHz				
Dynamic Range[2]	Shorted input				
	IN1+/-, Differential Input Range	TBD	107.1		dB
	IN2+/-, Differential Input Range	TBD	107.4		dB
	IN3+/-, Differential Input Range	TBD	107.4		dB
	Total System, Differential Input	TBD	124		dB
Noise Spectral Density	RTI, shorted input, at 1 kHz				
	IN1+/-		39		nV/√Hz
	IN2+/-		102		nV/√Hz
	IN3+/-		257		nV/√Hz
Total RMS Noise	RTI, shorted input				
	IN1+/-		12.8		uV rms
	IN2+/-		34.0		uV rms
	IN3+/-		85.9		uV rms
Signal-to-Noise Ratio (SNR)	-0.5 dBFS, sine input, 1 kHz tone				
	IN1+/-, -0.5 dBFS (3.87 Vp)	TBD	106.2		dB
	IN2+/-, -0.5 dBFS (10.63 Vp)	TBD	106.4		dB
	IN3+/-, -2.0 dBFS (22.67 Vp)	TBD	104.8		dB
Total Harmonic Distortion (THD)	sine input, 1 kHz tone				
	IN1+/-, -0.5 dBFS (3.87 Vp)		-119		dB
	IN2+/-, -0.5 dBFS (10.63 Vp)		-119		dB
	IN3+/-, -2.0 dBFS (22.67 Vp)		-119		dB
Signal-to-Noise and Distortion Ratio (SINAD)	sine input, 1 kHz tone				
	IN1+/-, -0.5 dBFS (3.87 Vp)	TBD	106.0		dB
	IN2+/-, -0.5 dBFS (10.63 Vp)	TBD	106.2		dB
	IN3+/-, -2.0 dBFS (22.67 Vp)	TBD	104.6		dB
Spurious-Free Dynamic Range (SFDR)	-0.5 dBFS, sine input, 1 kHz tone				
	IN1+/-		TBD		dBc
	IN2+/-		TBD		dBc
	IN3+/-		TBD		dBc

SPECIFICATIONS

Table 1. (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Intermodulation Distortion (IMD)	f_{IN_A} = 9kHz, f_{IN_B} = 10kHz				
	IN1+/-, second order		TBD		dBc
	IN1+/-, third order		TBD		dBc
	IN2+/-, second order		TBD		dBc
	IN2+/-, third order		TBD		dBc
	IN3+/-, second order		TBD		dBc
	IN3+/-, third order		TBD		dBc
ANALOG FRONT-END MAGNITUDE AND PHASE PERFORMANCE[3]					
Anti-Aliasing Filter Bandwidth	−3 dB relative to signal amplitude at DC				
	IN1+/-		365		kHz
	IN2+/-		304		kHz
	IN3+/-		283		kHz
Analog Group Delay	f_{IN} = 20 kHz				
	IN1+/-		0.81		us
	IN2+/-		1.02		us
	IN3+/-		1.13		us
Phase Angle Drift	f_{IN} = 20 kHz				
	IN1+/-	TBD	0.70	TBD	m°/°C
	IN2+/-	TBD	0.76	TBD	m°/°C
	IN3+/-	TBD	0.60	TBD	m°/°C
Device-to-Device Phase Angle Mismatch	f_{IN} = 20 kHz, Typ = ±1 σ, T_A= 25°C				
	IN1+/-	TBD	±0.012	TBD	Degrees
	IN2+/-	TBD	±0.014	TBD	Degrees
	IN3+/-	TBD	±0.015	TBD	Degrees
Device-to-Device Phase Angle Mismatch Drift	f_{IN} = 20 kHz, Typ = change in |1σ| per °C				
	IN1+/-		TBD	TBD	m°/°C
	IN2+/-		TBD	TBD	m°/°C
	IN3+/-		TBD	TBD	m°/°C
Magnitude Flatness	f_{IN} = 20 kHz, IN1+/-		0.005		dB
	f_{IN} = 100 kHz, IN1+/-		-0.050		dB
	f_{IN} = 20 kHz, IN2+/-		0.005		dB
	f_{IN} = 100 kHz, IN2+/-		-0.200		dB
	f_{IN} = 20 kHz, IN3+/-		0.005		dB
	f_{IN} = 100 kHz, IN3+/-		-0.100		dB
Alias Rejection	-20 dBFS input signal				
	IN1+/-, at MCLK = 16.384 MHz		88		dB
	IN1+/-, at MCLK = 13.107 MHz		88		dB
	IN2+/-, at MCLK = 16.384 MHz		86		dB
	IN2+/-, at MCLK = 13.107 MHz		86		dB
	IN3+/-, at MCLK = 16.384 MHz		80		dB
	IN3+/-, at MCLK = 13.107 MHz		80		dB
ADC SPEED AND PERFORMANCE					
Output Data Rate (ODR)[4]					
	Wideband Low Ripple FIR	8		256	kSPS
	Sinc5	8		1024	kSPS
	Sinc3	0.05		256	kSPS
No Missing Codes	Wideband Low Ripple FIR, Decimation ratio ≥ 32	24			Bits
	Sinc5 Filter, Decimation ratio ≥ 32	24			Bits

SPECIFICATIONS

Table 1. (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	Sinc3 Filter, Decimation ratio ≥ 64	24			Bits
Data Output Coding		2s complement, MSB first			
REFERENCE INPUT CHARACTERISTICS					
REFIN Voltage	REFIN = (REF+) - (REF−)	1		VDD_ADC-AGND	V
Absolute REFIN Voltage Limit	Reference unbuffered	AGND - 0.05		VDD_ADC+ 0.05	V
	Reference buffer on	AGND		VDD_ADC	V
	Reference precharge buffer on	AGND		VDD_ADC	V
Average REFIN Current	Reference unbuffered		±80		uA/V
	Reference precharge buffer on		±20		uA
	Reference buffer on		±300		nA
Average REFIN Current Drift	Reference unbuffered		±1.7		nA/V/°C
	Reference precharge buffer on		125		nA/°C
	Reference buffer on		4		nA/°C
Common Mode Rejection	Up to 10 MHz		100		dB
DIGITAL FILTER RESPONSE					
Wideband Low Ripple FIR Filter					
Decimation Rate	Six selectable decimation rates	32		1024	
Output Data Rate				256	kSPS
Group Delay	Latency		34/ODR		Sec
Settling Time	Complete settling		68/ODR		Sec
Passband Ripple				±0.005	dB
Passband	-0.005dB		0.4 × ODR		Hz
	-0.1dB pass band		0.409 × ODR		
	-3dB Bandwidth		0.433 × ODR		Hz
Stopband Frequency	Attenuation >105dB		0.499 × ODR		Hz
Stopband Attenuation		105			dB
Sinc5 Filter					
Decimation Rate	Eight selectable decimation rates	8		1024	
Output Data Rate				1.024	MSPS
Group Delay	Latency		< 3/ODR		Sec
Settling Time	Complete settling		< 6/ODR		Sec
Passband	-0.1dB Bandwidth		0.0376 × ODR		Hz
	-3dB Bandwidth		0.204 × ODR		Hz
Sinc3 Filter					
Decimation Rate	1024 decimation rates	32		185,280	
Output Data Rate				256	kSPS
Group Delay	Latency		2/ODR		Sec
Settling Time	Complete settling to reject 50Hz		60		ms
Passband	-0.1dB Bandwidth		0.0483 × ODR		Hz
	-3dB Bandwidth		0.2617 × ODR		Hz
CLOCK					
External Clock MCLK		0.6	16.384	17	MHz
Internal Clock MCLK			16.384		MHz
Input High Voltage	See to logic input parameter				
Duty Cycle	16.384MHz MCLK	25:75	50:50	25:75	%
MCLK Logic Low Pulse Width		16			ns
MCLK Logic High Pulse Width		16			ns
Crystal Frequency		8	16	17	MHz

SPECIFICATIONS

Table 1. (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Crystal Start-Up Time	Clock output valid		2		ms
ADC RESET					
ADC Start-Up Time after Reset	Reset rising edge to first $\overline{\text{DRDY}}$, $\overline{\text{PIN}}$ mode, decimate by 8		100		µs
Minimum $\overline{\text{RESET}}$ Low Pulse Width		0.0001		100	ms
LOGIC INPUTS	Applies to all logic inputs unless specified otherwise, voltage referenced to AGND.				
Input High Voltage, V_{INH}	1.7 V ≤ VDD_IO ≤ 1.9 V	0.65 × VDD_IO			V
	2.22 V ≤ VDD_IO ≤ 3.6 V	0.65 × VDD_IO			V
Input Low Voltage, V_{INL}	1.7 V ≤ VDD_IO ≤ 1.9 V			0.35 × VDD_IO	V
	2.22 V ≤ VDD_IO ≤ 3.6 V			0.7	V
Hysteresis	2.22 V ≤ VDD_IO ≤ 3.6 V	0.08		0.25	V
	1.7 V ≤ VDD_IO ≤ 1.9 V	0.04		0.2	V
Leakage Current	Excluding $\overline{\text{RESET}}$ pin	−10	0.05	+10	µA
	$\overline{\text{RESET}}$ pin pull-up resistor		1		kΩ
M0_FDA, M1_FDA	Voltage referenced to AGND				
Input High Voltage		TBD			V
Input Low Voltage				TBD	V
Input Current	TBD		TBD		nA
EN_LDO	Voltage referenced to AGND				
Input High Voltage	5.1 V ≤ IN_LDO≤ 5.5 V	1.2			V
Input Low Voltage	5.1 V ≤ IN_LDO ≤ 5.5 V			0.4	V
Input Current	EN_LDO = IN_LDO or GND		0.1		µA
LOGIC OUTPUTS					
Output High Voltage	2.2 V ≤ VDD_IO < 3.6 V, I_{SOURCE} = 500 µA, LV_BOOST_off	0.8 × VDD_IO			V
	1.7 V ≤ VDD_IO ≤ 1.9 V, I_{SOURCE} = 200 µA, LV_BOOST_on	0.8 × VDD_IO			V
Output Low Voltage	2.2 V ≤ VDD_IO < 3.6 V, I_{SINK} = 1 mA, LV_BOOST_off			0.4	V
	1.7 V ≤ VDD_IO ≤ 1.9 V, I_{SINK} = 400 µA, LV_BOOST_on			0.4	V
Leakage Current	Floating state	−10		+10	µA
Output Capacitance	Floating state		10		pF
LDO CHARACTERISTIC					
Input Voltage Range		5.1		5.5	V
IN_LDO Supply Current	OUT_LDO load current = 20mA		80		µA
OUT_LDO Voltage		4.80	4.90	5.03	V
Load Regulation	IOUT = 1 mA to 20 mA		0.0005		%/mA
Dropout Voltage[5]	IOUT = 20 mA		3		mV
Start-Up Time[6]			350		µs
Current Limit Threshold			500		mA
Thermal Shutdown Threshold			150		°C
Thermal Shutdown Hysteresis			15		°C
POWER REQUIREMENTS					
VDD_FDA	Referenced to AGND	4.75	5	5.5	V
VDD_ADC	Referenced to AGND	4.75	5	5.5	V
VDD2_ADC	Referenced to AGND	2	2.5	5.5	V
VDD_IO	Referenced to AGND	1.7	1.8	3.6	V

SPECIFICATIONS

Table 1. (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY REJECTION	Referred to output (RTO), DC to 100Hz				
VDD_FDA	V_{STEP}=0.1Vp-p		80		dB
VDD_ADC	V_{STEP}=0.1Vp-p		90		dB
VDD2_ADC	V_{STEP}=0.1Vp-p		100		dB
VDD_IO	V_{STEP}=0.1Vp-p		75		dB
LDO	V_{STEP}=0.1Vp-p		124		dB
POWER SUPPLY CURRENT					
VDD_FDA	Full scale 1 kHz sine input with common mode = AGND				
	IN1+/-		TBD		mA rms
	IN2+/-		TBD		mA rms
	IN3+/-		TBD		mA rms
	Full scale DC input with common mode = AGND				
	IN1+/-, 4Vdc		5.4		mA
	IN2+/-, 11Vdc		5.1		mA
	IN3+/-, 28Vdc		4.7		mA
	INx+ = INx- = AGND				
	IN1+ = IN1- = AGND		4.8		mA
	IN2+ = IN2- = AGND		4.4		mA
	IN3+ = IN3- = AGND		4.2		mA
	Standby		70		µA
VDD_ADC	Linearity boost buffer on, reference precharge buffer on		6.3		mA
	Linearity boost buffer off, reference precharge buffers off		2.4		mA
	Standby		205		µA
VDD2_ADC			4.7		mA
	Standby		30		µA
VDD_IO					
Sinc3 Filter			3.7		mA
Sinc5 Filter			3.7		mA
Wideband Low Ripple FIR Filter			9.5		mA
Standby			380		µA
POWER DISSIPATION	External CMOS MCLK, VDD2_ADC = VDD_IO = 3.3 V				
Full Operating Mode					
Sinc3 Filter	INx+ = INx- = AGND		82		mW
Sinc5 Filter	INx+ = INx- = AGND		82		mW
Wideband Low Ripple FIR Filter	INx+ = INx- = AGND		100	TBD	mW
	Full scale 1 kHz sine input with common mode = AGND			TBD	mW
Standby Mode			TBD	TBD	mW

---

[1] See Terminology for Peak-to-Peak Resolution. Noise used in calculation is listed under the "Low Frequency Noise" specification.

[2] See the Noise Performance section for further information on dynamic range and noise across different gain and filter configurations.

[3] See the Calculations on AFE Phase Performancesection for AFE performance, terminology, and calculation.

[4] Output data rate (ODR) ranges refer to the programmable decimation rates available on the ADAQ7767-1 for a fixed MCLK of 16.384MHz across varying MCLK_DIV and decimation rates. See the ADC Speed and Performance section for suggestion on the ODR speed to achieve optimum performance

SPECIFICATIONS

[5] Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage. This applies only for output voltages greater than 2.3 V.

[6] Start-up time is defined as the time between the rising edge of EN to VOUT being at 90% of its nominal value.

TIMING SPECIFICATIONS

VDD_ADC = 4.5 V to 5.5 V, VDD2_ADC = 2.0 V to 5.5 V, VDD_IO = 2.2 V to 3.6 V, AGND = DGND = 0 V, Input Logic 0 = 0 V, Input Logic 1 = VDD_IO, and load capacitance (C_{LOAD}) = 20 pF, LV_BOOST bit (Bit 7, INTERFACE_FORMAT register, Register 0x14) disabled, unless otherwise noted.

These specifications were sample tested during the initial release to ensure compliance. All input signals are specified with $t_R = t_F = 5$ ns (10% to 90% of VDD_IO and timed from a voltage level of VDD_IO/2). See Figure 2 to Figure 8 for the timing diagrams.

These specifications are not production tested, but are supported by characterization data at initial product release.

Table 2.

Parameter	Description	Test Conditions/Comments	Min	Typ	Max	Unit
MCLK	Master Clock Frequency			16.384	17	MHz
t_{MCLK_HIGH}	MCLK high time		16			ns
t_{MCLK_LOW}	MCLK low time		16			ns
f_{MOD}	Modulator frequency	MCLK_DIV[1:0]=11		MCLK/2		Hz
		MCLK_DIV[1:0]=10		MCLK/4		Hz
		MCLK_DIV[1:0]=01		MCLK/8		Hz
		MCLK_DIV[1:0]=00		MCLK/16		Hz
$t_{\overline{DRDY}}$	Conversion period	Rising DRDY edge to next rising DRDY edge, continuous conversion mode		f_{MOD}/DEC_RATE		Hz
$t_{\overline{DRDY}\_HIGH}$	DRDY high time	t_{MCLK} = 1/MCLK	t_{MCLK} − 5	1 × t_{MCLK}		ns
$t_{MCLK\_\overline{DRDY}}$	MCLK to DRDY	Rising MCLK edge to DRDY rising edge	10	13	18	ns
$t_{MCLK\_\overline{RDY}}$	MCLK to RDY indicator on the DOUT/RDY pin	Rising MCLK edge to RDY falling edge	10	13	18	ns
t_{UPDATE}	ADC data update	Time prior to DRDY rising edge where the ADC conversion register updates, single conversion read		1 × t_{MCLK}		ns
$t_{\overline{START}}$	START pulse width		1.5 × t_{MCLK}			ns
$t_{MCLK\_\overline{SYNC\_OUT}}$	MCLK to SYNC_OUT	Falling MCLK to falling SYNC_OUT			t_{MCLK} + 16	ns
t_{SCLK}	SCLK period		50			ns
t_1	CS falling to SCLK falling		0			ns
t_2	CS falling to data output enable				6	ns
t_3	SCLK falling edge to data output valid			10	15	ns
t_4	Data output hold time after SCLK falling edge		4			ns
t_5	SDI setup time before SCLK rising edge		3			ns
t_6	SDI hold time after SCLK rising edge		8			ns
t_7	CS high time	4-wire interface	10			ns
t_8	SCLK high time		20			ns
t_9	SCLK low time		20			ns
t_{10}	SCLK rising edge to DRDY high	Single conversion read only; time from last SCLK rising edge to DRDY high	1 × t_{MCLK}			ns
t_{11}	SCLK rising edge to CS rising edge		6			ns
t_{12}	CS rising edge to DOUT/RDY output disable		4		7	ns
t_{13}	DOUT/RDY indicator pulse width	In continuous read mode with RDY on, DOUT enabled, with SCLK idling high		1 × t_{MCLK}		ns

SPECIFICATIONS

Table 2. (Continued)

Parameter	Description	Test Conditions/Comments	Min	Typ	Max	Unit
t_{14}	$\overline{\text{CS}}$ falling edge to SCLK rising edge		2			ns
t_{15}	$\overline{\text{SYNC\_IN}}$ setup time before MCLK rising edge		2			ns
t_{16}	$\overline{\text{SYNC\_IN}}$ pulse width		1.5 × t_{MCLK}			ns
t_{17}	SCLK rising edge to $\overline{\text{RDY}}$ indicator rising edge	In continuous read mode with $\overline{\text{RDY}}$ enabled on DOUT	1			ns
t_{18}	$\overline{\text{DRDY}}$ rising edge to SCLK falling edge	In continuous read mode with $\overline{\text{RDY}}$ enabled on DOUT	8			ns

1.8 V TIMING SPECIFICATIONS

VDD_ADC = 4.5 V to 5.5 V, VDD2_ADC = 2 V to 5.5 V, VDD_IO = 1.7 V to 1.9 V, AGND = DGND = AGND2_ADC = 0 V, Input Logic 0 = 0 V, Input Logic 1 = VDD_IO, and C_{LOAD} = 20 pF, LV_BOOST bit (Bit 7, INTERFACE_FORMAT register, Register 0x14) enabled, unless otherwise noted.

These specifications were sample tested during the initial release to ensure compliance. All input signals are specified with $t_R = t_F = 5$ ns (10% to 90% of VDD_IO and timed from a voltage level of VDD_IO/2. See Figure 2 to Figure 8 for the timing diagrams.

These specifications are not production tested but are supported by characterization data at initial product release.

Table 3.

Parameter	Description	Test Conditions/Comments	Min	Typ	Max	Unit
MCLK	Frequency			16.384	17	MHz
t_{MCLK_HIGH}	MCLK high time		16			ns
t_{MCLK_LOW}	MCLK low time		16			ns
f_{MOD}	Modulator frequency	MCLK_DIV[1:0]=11		MCLK/2		Hz
		MCLK_DIV[1:0]=10		MCLK/4		Hz
		MCLK_DIV[1:0]=01		MCLK/8		Hz
		MCLK_DIV[1:0]=00		MCLK/16		Hz
$t\overline{\text{DRDY}}$	Conversion period	Rising $\overline{\text{DRDY}}$ edge to next rising $\overline{\text{DRDY}}$ edge, continuous conversion mode		f_{MOD}/DEC_RATE		Hz
$t\overline{\text{DRDY}}_{\text{\_HIGH}}$	$\overline{\text{DRDY}}$ high time	t_{MCLK} = 1/MCLK	t_{MCLK} − 5	1 × t_{MCLK}		ns
$t_{MCLK\_}\overline{\text{DRDY}}$	MCLK to $\overline{\text{DRDY}}$	Rising MCLK edge to $\overline{\text{DRDY}}$ rising edge	13	19	25	ns
$t_{MCLK\_}\overline{\text{RDY}}$	MCLK to $\overline{\text{RDY}}$ indicator on the DOUT/$\overline{\text{RDY}}$ pin	Rising MCLK edge to $\overline{\text{RDY}}$ falling edge	13	19	25	ns
t_{UPDATE}	ADC data update	Time prior to $\overline{\text{DRDY}}$ rising edge where the ADC conversion register updates		1 × t_{MCLK}		ns
$t\overline{\text{START}}$	$\overline{\text{START}}$ pulse width		1.5 × t_{MCLK}			ns
$t_{MCLK\_\overline{SYNC\_OUT}}$	MCLK to $\overline{\text{SYNC\_OUT}}$	Falling MCLK to falling $\overline{\text{SYNC\_OUT}}$, see the Synchronization of Multiple ADAQ7767-1 Devices section			t_{MCLK} + 31	ns
t_{SCLK}	SCLK period		50			ns
t_1	$\overline{\text{CS}}$ falling to SCLK falling		0			ns
t_2	$\overline{\text{CS}}$ falling to data output enable				11	ns
t_3	SCLK falling edge to data output valid			14	19	ns
t_4	Data output hold time after SCLK falling edge		7			ns
t_5	SDI setup time before SCLK rising edge		3			ns
t_6	SDI hold time after SCLK rising edge		8			ns
t_7	$\overline{\text{CS}}$ high time	4-wire interface	10			ns
t_8	SCLK high time		23			ns
t_9	SCLK low time		23			ns

SPECIFICATIONS

Table 3. (Continued)

Parameter	Description	Test Conditions/Comments	Min	Typ	Max	Unit
t_{10}	SCLK rising edge to $\overline{\text{DRDY}}$ high	Time from last SCLK rising edge to DRDY high; if this is exceeded, conversion N + 1 is missed; single conversion read	$1 \times t_{MCLK}$			ns
t_{11}	SCLK rising edge to $\overline{\text{CS}}$ rising edge		6			ns
t_{12}	$\overline{\text{CS}}$ rising edge to DOUT/$\overline{\text{RDY}}$ output disable		7.5		13	ns
t_{13}	DOUT/$\overline{\text{RDY}}$ indicator pulse width	In continuous read mode with $\overline{\text{RDY}}$ on, DOUT enabled, with SCLK idling high		$1 \times t_{MCLK}$		ns
t_{14}	$\overline{\text{CS}}$ falling edge to SCLK rising edge		2.5			ns
t_{15}	$\overline{\text{SYNC\_IN}}$ setup time before MCLK rising edge		2			ns
t_{16}	$\overline{\text{SYNC\_IN}}$ pulse width		$1.5 \times t_{MCLK}$			ns
t_{17}	SCLK rising edge to $\overline{\text{RDY}}$ indicator rising edge	In continuous read mode with $\overline{\text{RDY}}$ on, DOUT enabled	5.5			ns
t_{18}	$\overline{\text{DRDY}}$ rising edge to SCLK falling edge	In continuous read mode with $\overline{\text{RDY}}$ on, DOUT enabled	15			ns

Timing Diagrams

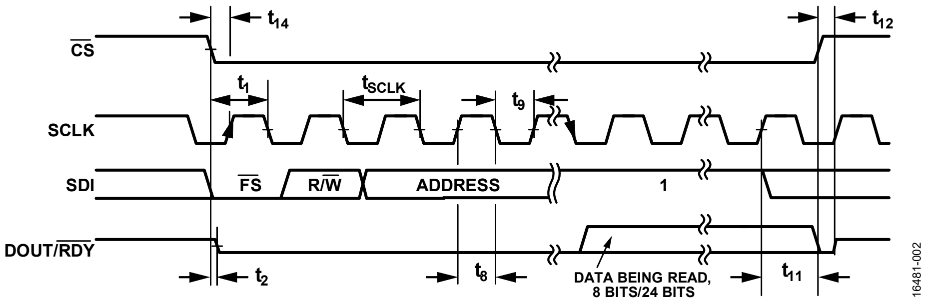


Figure 2. SPI Read Timing Diagram

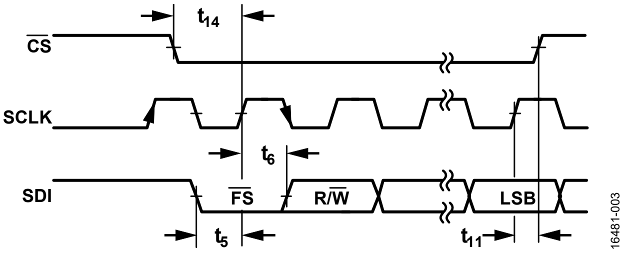


Figure 3. SPI Write Timing Diagram

SPECIFICATIONS

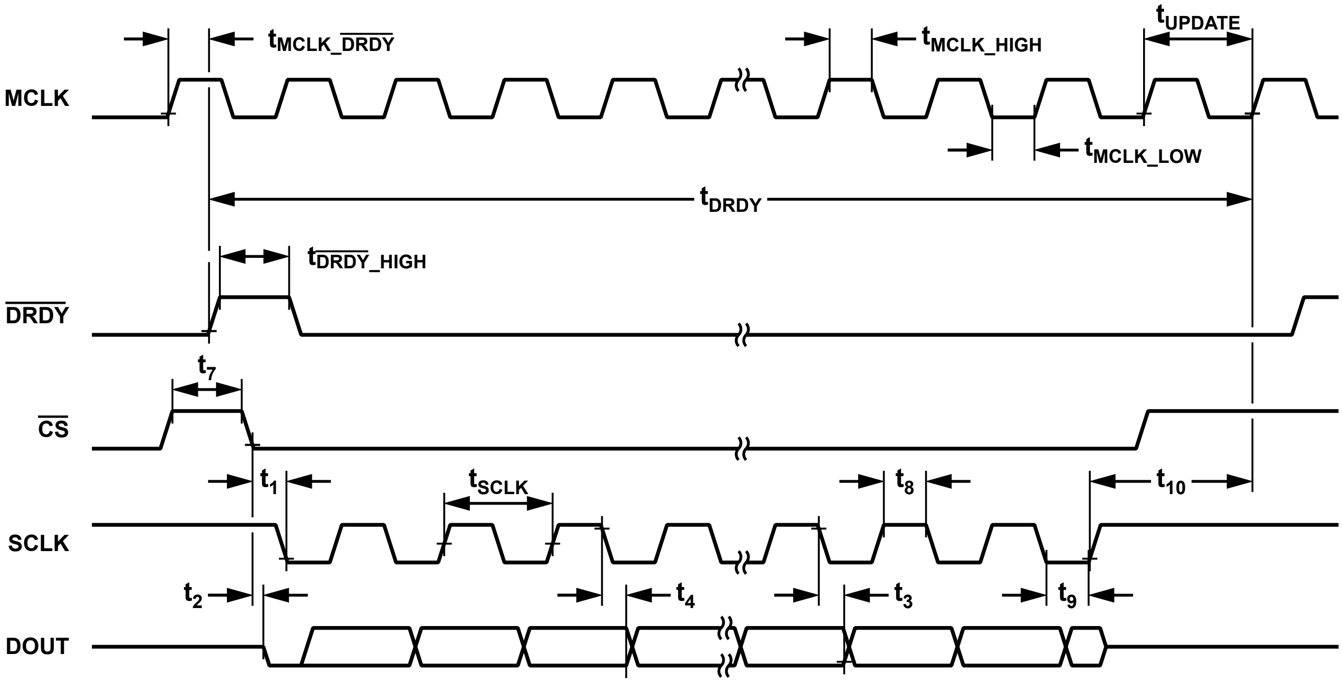


Figure 4. Reading Conversion Result in Continuous Conversion Mode ($\overline{CS}$ Toggling)

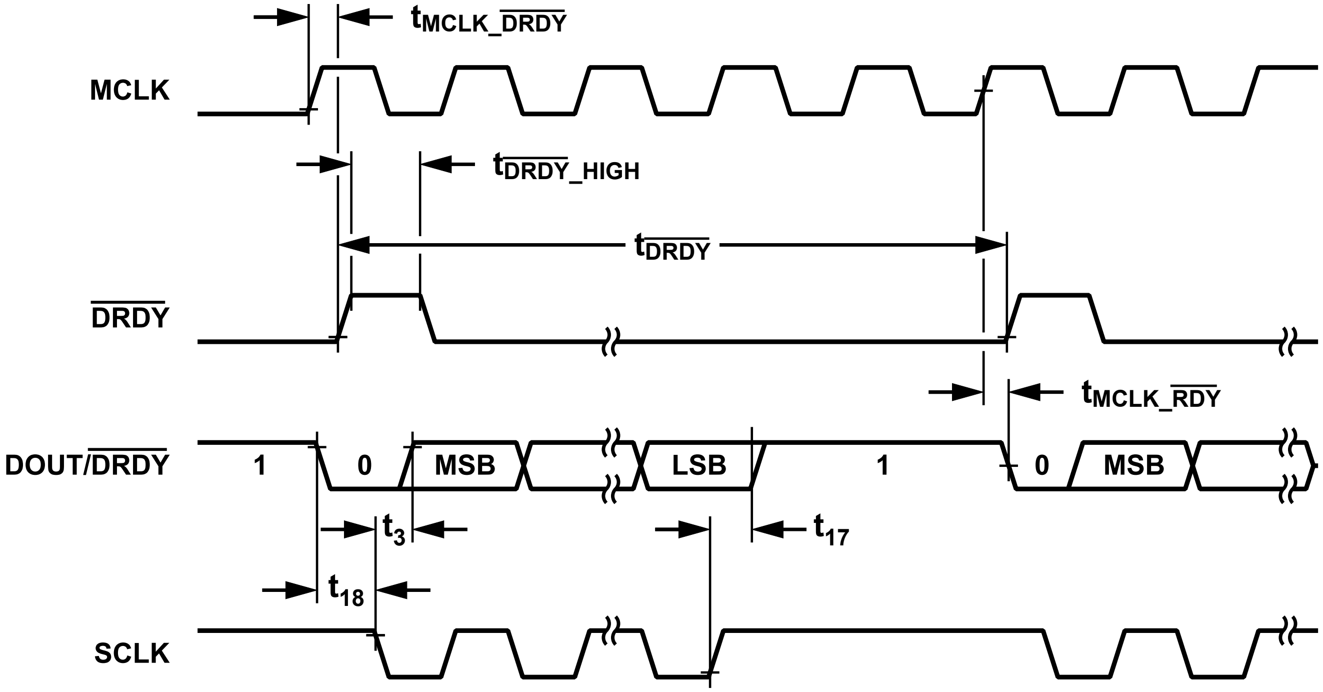


Figure 5. Reading Conversion Result in Continuous Conversion Mode, Continuous Read Mode with $\overline{RDY}$ Enabled ($\overline{CS}$ Held Low)

SPECIFICATIONS

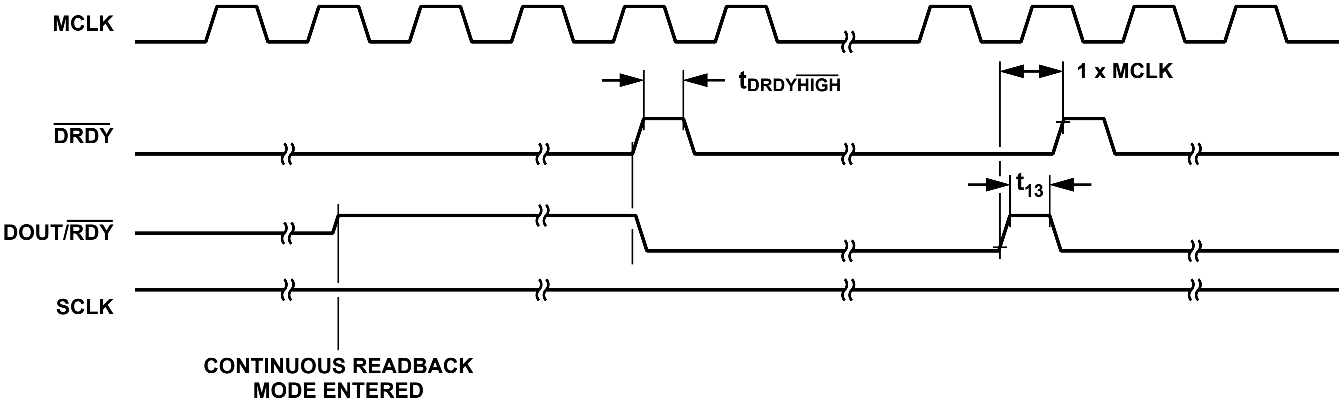


Figure 6. DOUT/$\overline{\text{RDY}}$ Behavior Without SCLK Applied

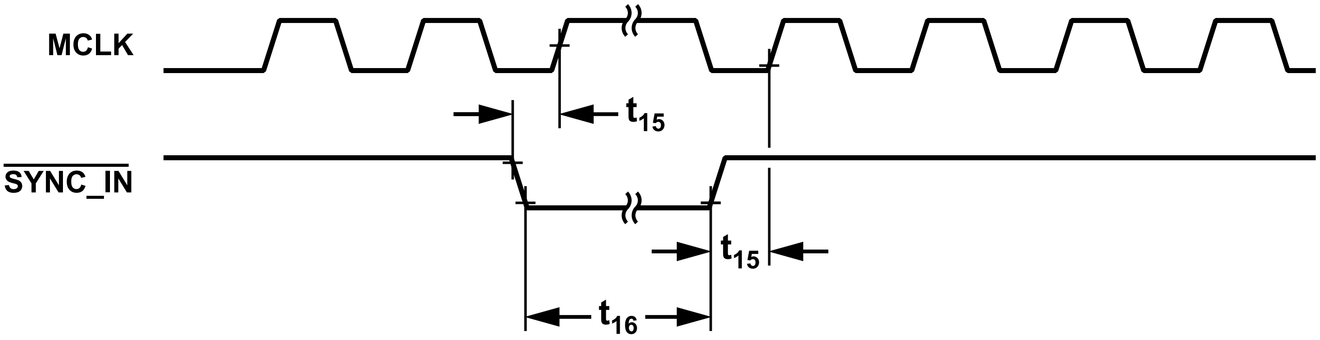


Figure 7. Synchronous $\overline{\text{SYNC\_IN}}$ Pulse

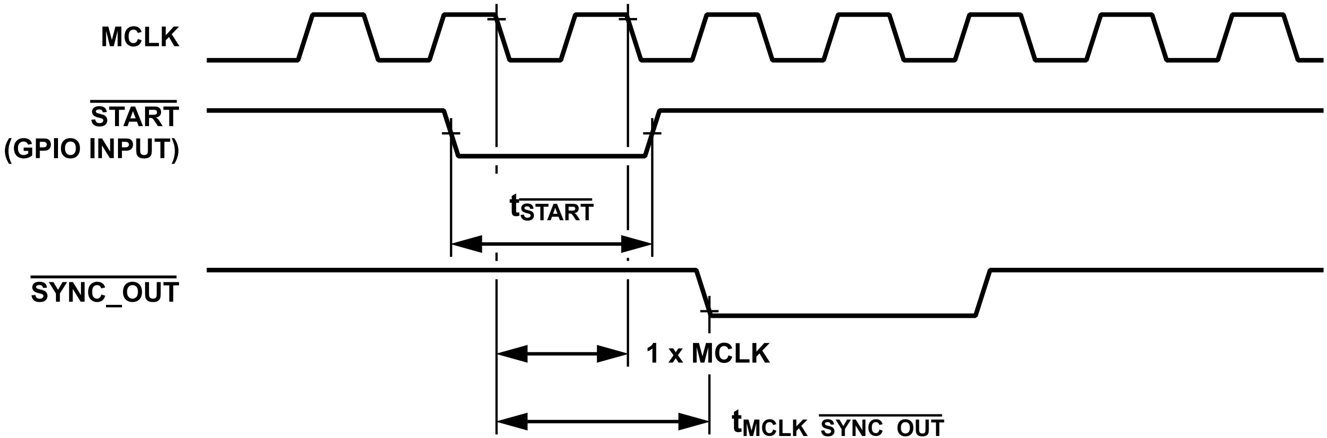


Figure 8. Asynchronous $\overline{\text{START}}$ and $\overline{\text{SYNC\_OUT}}$

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
IN1+, IN1− to AGND	±15 V
IN2+, IN2− to AGND	±15 V
IN3+, IN3− to AGND	±36 V
VDD_FDA to VDD_ADC	−0.3 V to +0.3 V
VDD_FDA to AGND	−0.3 V to +6.5 V
M0_FDA, M1_FDA to AGND	TBD
IN_LDO to AGND	−0.3 V to +6.5 V
EN_LDO to AGND	−0.3 V to +6.5 V
OUT_LDO to AGND	−0.3 V to IN_LDO
VDD_ADC to AGND	−0.3 V to +6.5 V
VDD2_ADC to AGND	−0.3 V to +6.5 V
VDD_IO to DGND	−0.3 V to +6.5 V
DGND to AGND	−0.3 V to +0.3 V
VDDIO, DREG_CAP to DGND (VDD_IO tied to DREG_CAP for 1.8 V Operation)	−0.3 V to +2.25 V
REF+, REF− to AGND	−0.3 V to VDD_ADC + 0.3 V
Digital Input Voltage to DGND	−0.3 V to VDD_IO + 0.3 V
Digital Output Voltage to DGND	−0.3 V to VDD_IO + 0.3 V
XTAL1 to DGND	−0.3 V to +2.1 V
Operating Temperature Range	-40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Pb-Free Temperature, Soldering Reflow (10 sec to 30 sec)	260°C
Maximum Package Classification Temperature	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 5. Thermal Resistance

Package Type[1]	θ_{JA}	θ_{JC_TOP}	θ_{JC_BOTTOM}	θ_{JB}	Ψ_{JT}	Ψ_{JB}	Unit
BC-84-4	29.3	14.7	18.1	21.8	2.4	22.2	°C/W

[1] Test Condition 1: Thermal impedance simulated values are based on the use of a 2S2P with vias JEDEC PCB excluding the θ_{JCtop} which uses 1S0P JEDEC PCB.

Thermal resistance values specified in Table 5 are simulated based on JEDEC specs (unless specified otherwise) and should be used in compliance with JESD51-12.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided to handle ESD-sensitive devices in an ESD protected area only.

- Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.
- Field-induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADAQ7767-1

Table 6. ADAQ7767-1, 84-Ball CSP_BGA

ESD Model	Withstand Voltage (V)	Class
HBM	±TBD	TBD
FICDM	±TBD	TBD

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TERMINOLOGY

AC Common-Mode Rejection Ratio (CMRR)

The ratio of the power in the ADC output at frequency, f, to the power of a sine-wave applied to the common-mode voltage of INx+ and INx- at frequency, f_S.

$$CMRR\ (dB) = 10\log\left(\frac{Pf}{Pf_S}\right) \quad (1)$$

where:

Pf is the power at frequency, f, in the ADC output.

Pf_S is the power at frequency, f_S, in the ADC output.

Least Significant Bit (LSB)

The smallest increment that can be represented by a converter. For a fully differential input ADC with N bits of resolution, the LSB expressed in volts is:

$$LSB\ (V) = \frac{V_{REF} \times 2}{2^N \times AFE\_GAIN} \quad (2)$$

Gain Error

The first transition (from 100 … 000 to 100 …001) occurs at a level ½ LSB above nominal negative full scale (−4.0955999756 V for the ±4.096 V range). The last transition (from 011 … 110 to 011 … 111) occurs for an analog voltage 1½ LSB below the nominal full scale (+4.095999268V for the ±4.096 V range). The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

Gain Error Drift

The ratio of the gain error change due to a temperature change of 1°C and the full-scale range (2^N). It is expressed in parts per million.

Offset Error

The difference between the ideal midscale input voltage (0 V) and actual voltage producing the midscale output code.

Offset Error Drift

The ratio of the offset error change due to a temperature change of 1°C and the full scale code range (2^N). It is expressed in parts per million.

Differential Nonlinearity (DNL) Error

In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value, often specified in terms of resolution for which no missing codes are guaranteed.

Integral Nonlinearity (INL) Error

The deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Dynamic Range

The ratio of the root mean-square (RMS) value of the full scale to the RMS noise measured when input pins are shorted together. The value is expressed in decibels.

Total System Dynamic Range

The ratio of the RMS value of the full scale using IN3+/- to the input referred RMS noise measured when IN1+/- pins are shorted together. The value is expressed in decibels.

Peak-to-Peak Resolution

The number of bits unaffected by peak-to-peak noise or flicker. It is also sometimes called 'flicker-free resolution' or 'noise-free code resolution'. It follows this formula:

$$\log_2\left(\frac{Full\ \ Scale\ \ Range}{6.6 \times RMS\,Noise}\right) \quad (3)$$

Signal-to-Noise Ratio (SNR)

The ratio of the RMS value of the actual input signal to the RMS sum of all other spectral components below the Nyquist frequency, excluding harmonics and DC. The value is expressed in decibels.

Total Harmonic Distortion (THD)

The ratio of the RMS sum of the harmonics to the fundamental. It is expressed in decibels. For the ADAQ7767-1, THD is defined as:

$$THD\ (dB) = 20\log\left(\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}\right) \quad (4)$$

where:

V_2, V_3, V_4, V_5, V_6 are the RMS amplitudes of the second to sixth harmonics.

V_1 is the RMS amplitude of the fundamental.

Signal-to-Noise and Distortion (SINAD) Ratio

The ratio of the RMS value of the actual input signal to the RMS sum of all other spectral components below the Nyquist frequency, including harmonics but excluding DC. The value is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)

The difference, in decibels, between the RMS amplitude of the input signal and peak spurious signal (including harmonics).

TERMINOLOGY

Intermodulation Distortion

With inputs consisting of sine-waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa and nfb, where m, n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n are equal to 0. For example, the second-order terms include (fa + fb) and (fa − fb), and the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

The calculation of the intermodulation distortion is per the THD specification, where it is the ratio of the RMS sum of the individual distortion products to the RMS amplitude of the sum of the fundamentals expressed in decibels.

Device-to-Device Phase Angle Mismatch

It measures the deviation of the phase delay of a single ADAQ7767-1 device relative to the average phase delay of a group of ADAQ7767-1 devices at a given input signal frequency. It shows how well the phase response of the data acquisition signal chain matches among channels. The typical specification is equal to ±1σ (standard deviation) of the distribution, while the maximum (or minimum) is six times this value.

Device-to-Device Phase Angle Mismatch Drift

It quantifies how much the device-to-device phase angle mismatch standard deviation (σ) widens/tightens across temperature at a given input signal frequency. A positive sign indicates a wider phase mismatch distribution as temperature increases, while a negative sign indicates a tighter phase mismatch distribution as temperature increases. This specification is calculated using the endpoint method over the full operating temperature range. The typical specification is the change in |1σ| per °C, while the maximum is six times this value, as shown in Figure 9.

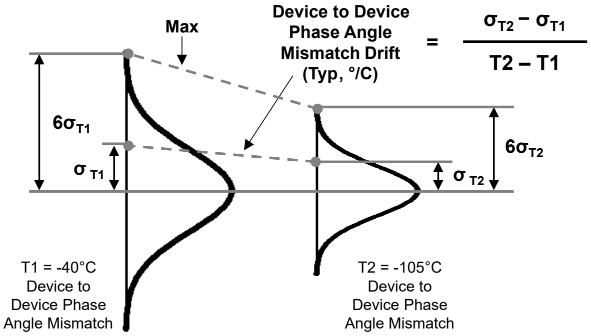


Figure 9. Device-to-Device Phase Angle Mismatch Drift Calculation

Power Supply Rejection Ratio PSRR

Variations in power supply affect the full-scale transition but not the linearity of the converter. PSRR is the maximum change in the full-scale transition point due to a change in power supply voltage from the nominal value.

QUICK START UP GUIDE

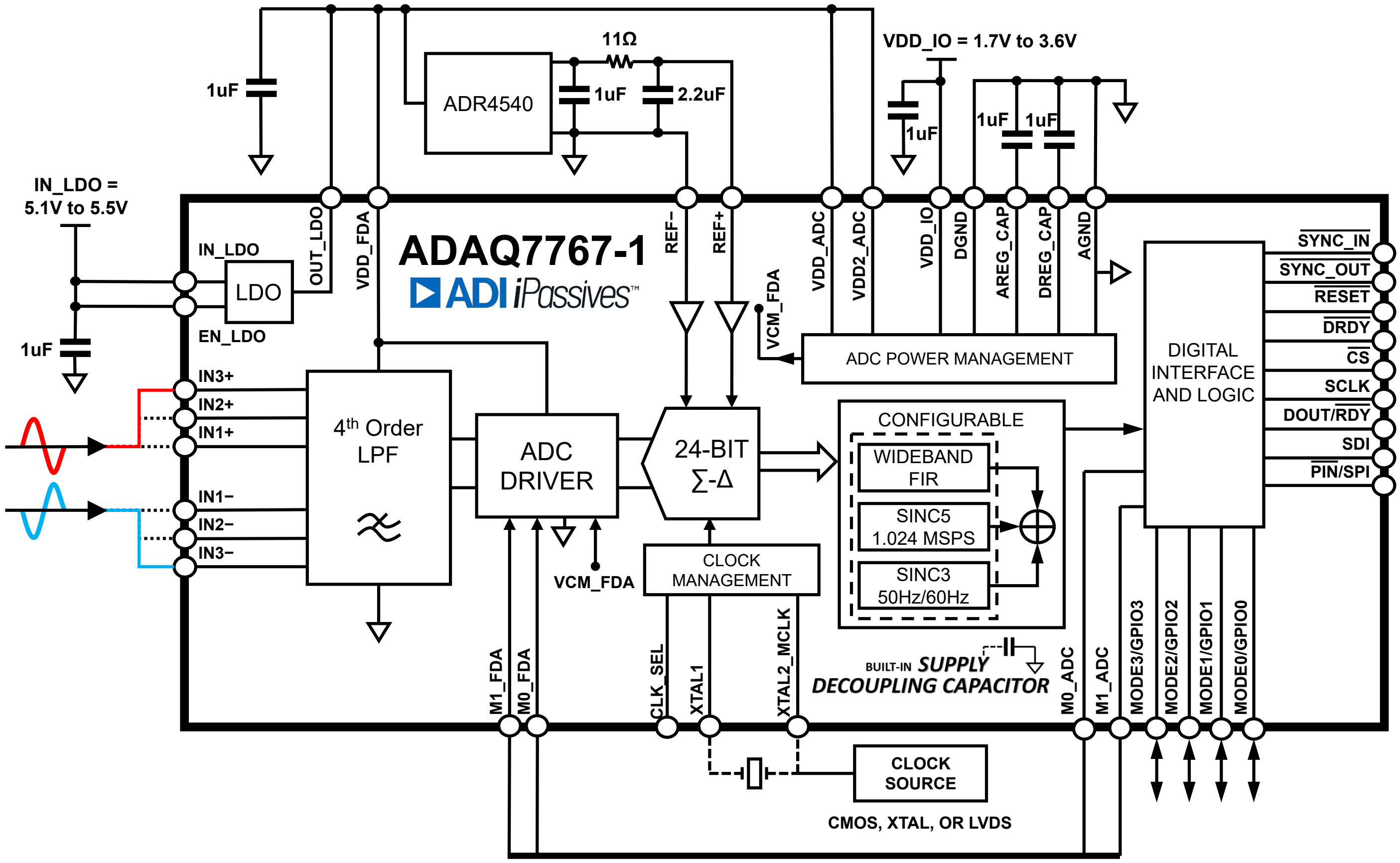


Figure 10. Typical Connection Diagram of ADAQ7767-1

POWER SUPPLY CONNECTION

The ADAQ7767-1 has several power supplies to power each block of the signal chain. To reduce the number of power supplies needed to power up the part, the ADAQ7767-1 has a built-in LDO to supply power to VDD_FDA, VDD_ADC, and VDD2_ADC. The LDO can also supply the power needed by suggested reference device ADR4540. The LDO can handle input voltage range of 5.1V to 5.5V. For proper operation it is recommended to use a 1µF capacitor at the input and output of the LDO. If the LDO is not used during normal operation, it is recommended to keep all the LDO pins floating.

The VDD_IO powers the internal regulator needed by the digital logic of the ADC, VDD_IO is referenced to DGND and can vary from 1.7V to 3.6V.

The ADAQ7767-1 has a built-in 0.1µF internal decoupling capacitor on each power supply. For detailed information regarding power supply connection and decoupling, see the Power Supplies and Power Supply Decoupling sections.

Table 7. Power Supply Voltage Requirements

	Supply Voltage (V)		
Supplies	**Min**	**Typical**	**Max**
IN_LDO	5.1	5.3	5.5
VDD_FDA	4.75	OUT_LDO (5V)	5.5
VDD_ADC	4.75	OUT_LDO (5V)	5.5
VDD2_ADC	2	OUT_LDO (5V) or 2.5	5.5
VDD_IO	1.7	1.8	3.6

DEVICE CONTROL MODE

The ADAQ7767-1 has two options to control device functionality. On power-up, the mode is determined by the state of the PIN/ SPI pin. The two modes of configuration are

- PIN/SPI = VDD_IO = SPI control mode: over a 3- or 4-wire SPI interface (complete configurability), suggested control mode.
- PIN/SPI = DGND = Pin control mode: pin strapped digital logic inputs (a subset of complete configurability, daisy-chain is available only at this mode)
- The first design decision is setting the ADC in either the SPI or PIN mode of configuration.

On power-up, apply a soft or hard reset to the device when using either control mode. A SYNC_IN pulse is also recommended after the reset or after any change to the device configuration. Choose between controlling and configuring over the SPI or through pin connections only.

The Device Configuration Method section provides a detailed discussion on the capability and limitations of the two control mode options.

INPUT RANGE SELECTION

The ADAQ7767-1 input is a low noise, low distortion, high bandwidth ADC driver with a fourth order anti-aliasing filter (AAF). It has three differential input pairs IN1, IN2, and IN3, from which the user selects from. Each input pair has a fixed gain, leading to full-scale ranges of ±4.096V, ±11.264V, and ±28.672V differential, respectively. Noise performance across various input ranges and ADC configurations are seen in the Noise Performance section.

GPIO Pins

A common use of the GPIO pins is to digitally control the gain settings of a programmable gain amplifier (PGA) used as a high impedance amplifier at the input of the ADAQ7767-1. The PGA gain pins can be connected to the GPIO pins of the ADAQ7767-1 to enable the user to control the PGA gain over SPI. When the GPIO pins are used to control the gain, the user must configure the GPIO port control Register (Register 0x1E) to enable the GPIO and set the necessary GPIO ports as outputs. To set the logic output level for the GPIO pins, configure the GPIO output control register (Register 0x1F).

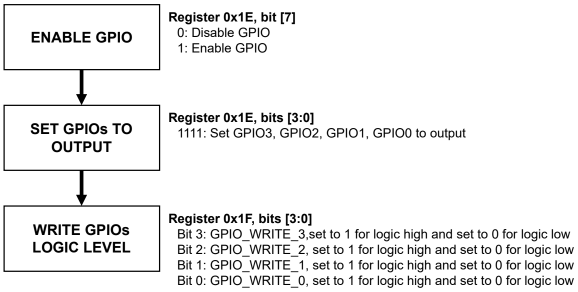


Figure 11. GPIO Gain Control Flow Chart

For example, if a connected PGA has GAIN0, GAIN1, and GAIN2 as gain control pins, they can be connected to ADAQ7767-1's GPIO0, GPIO1, and GPIO2 respectively. In SPI control mode, the user can enable the GPIO control port and set the necessary GPIO pins as outputs by writing 0x87 to the GPIO port control Register (Register 0x1E). By default, the GPIO output control register (Register 0x1F) has an output logic low to GPIO0, GPIO1, and GPIO2.

SELECTING THE MCLK DIVIDER AND SOURCE

MCLK Source Selection

The ADAQ7767-1 has an internal oscillator used for initial power-up of the device. After the ADAQ7767-1 completes the start-up routine, there is a clock handover to the external MCLK. Program the MCLK source using the two control mode options, pin and SPI control modes.

In the $\overline{\text{PIN}}$ control mode, the CLK_SEL pin sets the external MCLK source. Three clock options are available in the $\overline{\text{PIN}}$ control mode: an internal oscillator, an external CMOS, or a crystal oscillator.

- CLK_SEL = 0 in the $\overline{\text{PIN}}$ control mode, select the CMOS clock option and apply to the MCLK pin. In this case, tie the XTAL1 pin to DGND.
- CLK_SEL = 1 in the $\overline{\text{PIN}}$ control mode, select the crystal option is and connect between the XTAL1 and XTAL2 pins.
- On the condition that no external clock is detected, the ADAQ7767-1 uses its internal clock as a default clock source.

In the SPI control mode, the following options are available for the MCLK input source, and can be set from the Power and Clock Control Register (Register 0x15) CLOCK_SEL bits [7:6]:

- CLOCK_SEL bits = 00 → CMOS input MCLK
- CLOCK_SEL bits = 01 → External crystal
- CLOCK_SEL bits = 10 → LVDS (exclusive to the SPI control mode)
- CLOCK_SEL bits = 11 → Internal clock

When switching from one clock source to another, apply soft reset to the device.

For optimum AC performance, it is not recommended to use in the internal clock as MCLK source.

MCLK Divider

The MCLK signal received by the ADAQ7767-1 defines the core ADC's sigma-delta modulator clock rate (f_{MOD}) and, in turn, the sampling frequency of the modulator of 2 × f_{MOD}. For optimum performance it is recommended to use MCLK = 16.384 MHz and MCLK_DIV = 2. This sets the f_{MOD} = 8.192 MHz, keeping the f_{MOD} frequency high and maximizing the out-of-band tone rejection from the frontend anti-aliasing filter.

$$f_{MOD} = \frac{MCLK}{MCLK\_DIV}$$

The default controller clock divider setting for ADAQ7767-1 is MCLK divider = 16. To configure the MCLK divider to MCLK = 2, write 11 to MCLK_DIV bits [5:4] of Power and Clock Control Register (Register 0x15) after power up.

Control of the settings for the modulator frequency differ in $\overline{\text{PIN}}$ control mode vs. SPI control mode. Refer to Table 25 for $\overline{\text{PIN}}$ control and refer to Power and Clock Control Register for SPI control.

MCLK and SCLK Alignment

The ADAQ7767-1 interface is flexible to allow the multiple modes of operation and various data output formats to work across different digital signal processors (DSPs) and microcontroller units (MCUs).

QUICK START UP GUIDE

To achieve maximum performance, it is recommended to have a synchronous SCLK and MCLK from the same clock source. It is also possible to set SCLK to be a divided down version of MCLK. The Recommended Interface section provides a detailed discussion about digital interface.

DIGITAL FILTER SETTING

The ADAQ7767-1 offers three types of digital filters. The digital filters available on the ADAQ7767-1 are

- Wideband Low Ripple FIR filter, −3 dB at 0.433 × ODR (6 rates)
- Sinc5 low latency filter, −3 dB at 0.204 × ODR (8 rates)
- Sinc3 low latency filter, –3 dB at 0.2617 × ODR, widely programmable data rate

- Details on the digital filter setting can be found in the Digital Filtering section.

Decimation Rate and Output Data Rate

The ADAQ7767-1 has programmable decimation rates for the Wideband Low Ripple FIR, Sinc5, and Sinc3 digital filters. The decimation rates allow to band limit the measurement, which reduces the speed and input bandwidth, but increases the resolution because there is further averaging in the digital filter. Filter selection and decimation rate setting when using the $\overline{\text{PIN}}$ control mode are listed in Table 25, while the SPI control mode requires a register write to the Digital Filter and Decimation Control Register (Register 0x19). Another register (SINC3 Decimation Rate (LSB) Register) is needed when setting the decimation rate for Sinc3 using SPI.

Calculate the ODR of the ADAQ7767-1 using the formula:

$$ODR = \frac{f_{MOD}}{DEC\_RATE} \quad (5)$$

ADC POWER MODE

Th ADC core power mode must match the MCLK_DIV setting. The default power setting of the ADAQ7767-1 is set to low power mode. For optimum performance, change the ADC_MODE to fast power mode by writing 11 to the ADC_MODE bits [1:0] of Power and Clock Control Register (Register 0x15), with MCLK_DIV = 2.

BASIC REGISTER SETUP

Figure 12 shows the basic flow of register writes for ADAQ7767-1 upon power up.

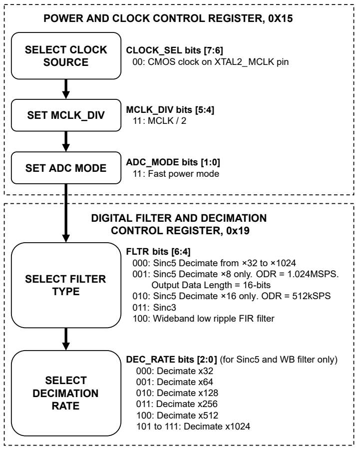


Figure 12. Basic Register Setup for ADAQ7767-1

QUICK START EXAMPLES

Wideband Low Ripple FIR Filter

For example, to operate the ADAQ7767-1 under the following conditions:

- MCLK sourced from CMOS clock
- Set the MCLK divider to 2 (recommended)
- Set the ADC power mode to fast power mode (recommended)
- Wideband low ripple FIR filter
- Decimation rate to 32

Equivalent consecutive SPI writes are:

- Data 0x33 to Power and Clock Control Register (Register 0x15)
- Data 0x40 to Digital Filter and Decimation Control Register (Register 0x19)

ODR = 1.024 MSPS

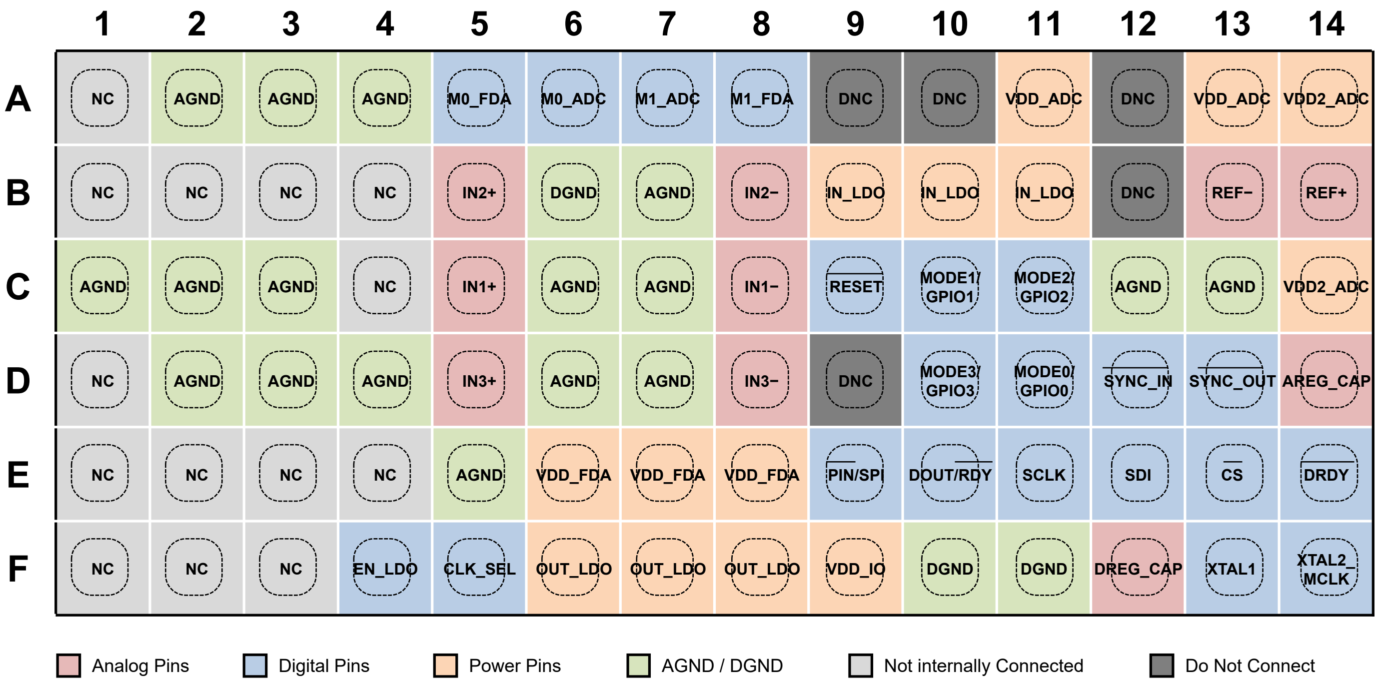
If the application has an ODR = 1.024 MSPS, it requires the following:

- 16.384 MHz MCLK
- The MCLK divider should be set to 2
- ADC Power mode should be set to Fast mode
- Sinc5 Filter
- Decimation rate to 8 (16-bit output data length)

Note that the ADAQ7767-1 automatically changes the output data length to 16-bit instead of 24-bit when using a Sinc5 filter specifically with the decimation rate of 8 because this particular use case is quantization noise limited. Assuming a CMOS MCLK source, equivalent consecutive SPI writes are:

- Data 0x33 to Power and Clock Control Register (Register 0x15)
- Data 0x10 to Digital Filter and Decimation Control Register (Register 0x19)

PIN CONFIGURATION AND FUNCTION DESCRIPTION



	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	NC	AGND	AGND	AGND	M0_FDA	M0_ADC	M1_ADC	M1_FDA	DNC	DNC	VDD_ADC	DNC	VDD_ADC	VDD2_ADC
B	NC	NC	NC	NC	IN2+	DGND	AGND	IN2−	IN_LDO	IN_LDO	IN_LDO	DNC	REF−	REF+
C	AGND	AGND	AGND	NC	IN1+	AGND	AGND	IN1−	$\overline{\text{RESET}}$	MODE1/ GPIO1	MODE2/ GPIO2	AGND	AGND	VDD2_ADC
D	NC	AGND	AGND	AGND	IN3+	AGND	AGND	IN3−	DNC	MODE3/ GPIO3	MODE0/ GPIO0	$\overline{\text{SYNC\_IN}}$	$\overline{\text{SYNC\_OUT}}$	AREG_CAP
E	NC	NC	NC	NC	AGND	VDD_FDA	VDD_FDA	VDD_FDA	$\overline{\text{PIN}}$/SPI	DOUT/$\overline{\text{RDY}}$	SCLK	SDI	$\overline{\text{CS}}$	$\overline{\text{DRDY}}$
F	NC	NC	NC	EN_LDO	CLK_SEL	OUT_LDO	OUT_LDO	OUT_LDO	VDD_IO	DGND	DGND	DREG_CAP	XTAL1	XTAL2_ MCLK

Figure 13. Pin Configuration

Table 8. ADAQ7767-1 Pin Function Descriptions

Pin No.	Name	Type[1]	Description
A1	NC		Not (internally) connected. Leave floating or connect to ground reference.
A2	AGND	P	Ground reference for VDD_FDA, IN_LDO, VDD_ADC and VDD2_ADC supplies. Connect to system ground for normal operation.
A3	AGND	P	Ground reference for VDD_FDA, IN_LDO, VDD_ADC and VDD2_ADC supplies. Connect to system ground for normal operation.
A4	AGND	P	Ground reference for VDD_FDA, IN_LDO, VDD_ADC and VDD2_ADC supplies. Connect to system ground for normal operation.
A5	M0_FDA	DI	FDA mode control input 0. Connect to M0_ADC for normal operation.
A6	M0_ADC	DO	FDA mode control output 0. Connect to M0_FDA for normal operation.
A7	M1_ADC	DO	FDA mode control output 1. Connect to M1_FDA for normal operation.
A8	M1_FDA	DI	FDA mode control input 1. Connect to M1_ADC for normal operation.
A9	DNC		Do not connect. Leave the node floating for normal operation.
A10	DNC		Do not connect. Leave the node floating for normal operation.
A11	VDD_ADC	P	ADC analog supply voltage. Referenced to AGND. Connect to OUT_LDO if using on-device LDO, else connect it to a single power source that also supplies the VDD_FDA pin.
A12	DNC		Do not connect. Leave the node floating for normal operation.
A13	VDD_ADC	P	ADC analog supply voltage. Referenced to AGND. Connect to OUT_LDO if using on-device LDO, else connect it to a single power source that also supplies the VDD_FDA pin.
A14	VDD2_ADC	P	ADC secondary analog supply voltage. Referenced to AGND.
B1	NC		Not (internally) connected. Leave floating or connect to ground reference.
B2	NC		Not (internally) connected. Leave floating or connect to ground reference.
B3	NC		Not (internally) connected. Leave floating or connect to ground reference.
B4	NC		Not (internally) connected. Leave floating or connect to ground reference.
B5	IN2+	AI	Signal input, non-inverting, gain of 0.364. Maximum differential input of 22Vpp.
B6	DGND	P	Ground reference for VDD_IO supplies. Connect to system ground for normal operation.

PIN CONFIGURATION AND FUNCTION DESCRIPTION

Table 8. ADAQ7767-1 Pin Function Descriptions (Continued)

Pin No.	Name	Type[1]	Description
B7	AGND	P	Ground reference for VDD_FDA, IN_LDO, VDD_ADC and VDD2_ADC supplies. Connect to system ground for normal operation.
B8	IN2−	AI	Signal input, inverting, gain of 0.364. Maximum differential input of 22Vpp.
B9	IN_LDO	P	On-device LDO supply input. Bypass IN_LDO to AGND with a capacitor of at least 1 μF.
B10	IN_LDO	P	On-device LDO supply input. Bypass IN_LDO to AGND with a capacitor of at least 1 μF.
B11	IN_LDO	P	On-device LDO supply input. Bypass IN_LDO to AGND with a capacitor of at least 1 μF.
B12	DNC		Do not connect. Leave the node floating for normal operation.
B13	REF−	AI	ADC reference input negative node. Connect to AGND for normal operation.
B14	REF+	AI	ADC reference input positive node. Apply an external reference between REF+ and REF− with voltage level ranging from VDD_ADC to AGND +1 V.
C1	AGND	P	Ground reference for VDD_FDA, IN_LDO, VDD_ADC and VDD2_ADC supplies. Connect to system ground for normal operation.
C2	AGND	P	Ground reference for VDD_FDA, IN_LDO, VDD_ADC and VDD2_ADC supplies. Connect to system ground for normal operation.
C3	AGND	P	Ground reference for VDD_FDA, IN_LDO, VDD_ADC and VDD2_ADC supplies. Connect to system ground for normal operation.
C4	NC		Not (internally) connected. Leave floating or connect to ground reference.
C5	IN1+	AI	Signal input, non-inverting, gain of 1. Maximum differential input of 8Vpp.
C6	AGND	P	Ground reference for VDD_FDA, IN_LDO, VDD_ADC and VDD2_ADC supplies. Connect to system ground for normal operation.
C7	AGND	P	Ground reference for VDD_FDA, IN_LDO, VDD_ADC and VDD2_ADC supplies. Connect to system ground for normal operation.
C8	IN1−	AI	Signal input, inverting, gain of 1. Maximum differential input of 8Vpp.
C9	$\overline{\text{RESET}}$	DI	ADC hardware asynchronous reset input. After the device is fully powered up it is recommended to do a hardware or software reset.
C10	MODE1/GPIO1	DI/O	Multi-function pin. ▸ In the pin control mode: Pin control operating profile selection input 1. ▸ In the SPI control mode: General purpose I/O pin, with logic level referenced to VDD_IO and DGND pins.
C11	MODE2/GPIO2	DI/O	Multi-function pin. ▸ In pin control mode: Pin control operating profile selection input 2. ▸ In SPI control mode: General purpose I/O pin, with logic level referenced to VDD_IO and DGND pins.
C12	AGND	P	Ground reference for VDD_FDA, IN_LDO, VDD_ADC and VDD2_ADC supplies. Connect to system ground for normal operation.
C13	AGND	P	Ground reference for VDD_FDA, IN_LDO, VDD_ADC and VDD2_ADC supplies. Connect to system ground for normal operation.
C14	VDD2_ADC	P	ADC secondary analog supply voltage. Referenced to AGND.
D1	NC		Not (internally) connected. Leave floating or connect to ground reference.
D2	AGND	P	Ground reference for VDD_FDA, IN_LDO, VDD_ADC and VDD2_ADC supplies. Connect to system ground for normal operation.
D3	AGND	P	Ground reference for VDD_FDA, IN_LDO, VDD_ADC and VDD2_ADC supplies. Connect to system ground for normal operation.
D4	AGND	P	Ground reference for VDD_FDA, IN_LDO, VDD_ADC and VDD2_ADC supplies. Connect to system ground for normal operation.
D5	IN3+	AI	Signal input, non-inverting, gain of 0.143. Maximum differential input of 57Vpp.
D6	AGND	P	Ground reference for VDD_FDA, IN_LDO, VDD_ADC and VDD2_ADC supplies. Connect to system ground for normal operation.
D7	AGND	P	Ground reference for VDD_FDA, IN_LDO, VDD_ADC and VDD2_ADC supplies. Connect to system ground for normal operation.
D8	IN3−	AI	Signal input, inverting, gain of 0.143. Maximum differential input of 57Vpp.
D9	DNC		Do not connect. Leave the node floating for normal operation.

PIN CONFIGURATION AND FUNCTION DESCRIPTION

Table 8. ADAQ7767-1 Pin Function Descriptions (Continued)

Pin No.	Name	Type[1]	Description
D10	MODE3/GPIO3	DI/O	Multi-function pin. ▶ In the pin control mode: Pin control operating profile selection input 3. ▶ In the SPI control mode: General purpose I/O pin, with logic level referenced to VDD_IO and DGND pins.
D11	MODE0/GPIO0	DI/O	Multi-function pin. ▶ In the pin control mode: Pin control operating profile selection input 0. ▶ In the SPI control mode: General purpose I/O pin, with logic level referenced to VDD_IO and DGND pins.
D12	$\overline{\text{SYNC\_IN}}$	DI	$\overline{\text{SYNC\_IN}}$ receives the synchronization signal from $\overline{\text{SYNC\_OUT}}$ pin or from the main controller. The synchronization signal needs to be synchronous to MCLK. $\overline{\text{SYNC\_IN}}$ enables synchronization and simultaneous sampling of multiple ADAQ7767-1 devices.
D13	$\overline{\text{SYNC\_OUT}}$	DO	Synchronization pulse output synchronous to MCLK. This pin allows one or multiple ADAQ7767-1 devices to be synchronized through SPI. Send a SYNC command over the SPI to initiate a $\overline{\text{SYNC\_OUT}}$ output. If used, route $\overline{\text{SYNC\_OUT}}$ signal back to the $\overline{\text{SYNC\_IN}}$ pin of the same device and the $\overline{\text{SYNC\_IN}}$ pins of other ADAQ7767-1 devices for simultaneous sampling.
D14	AREG_CAP	AO	ADC's internal analog LDO regulator output. Decouple this pin to AGND with a 1 μF capacitor. Do not use the voltage output from AREG_CAP in circuits external to the ADAQ7767-1.
E1	NC		Not (internally) connected. Leave floating or connect to ground reference.
E2	NC		Not (internally) connected. Leave floating or connect to ground reference.
E3	NC		Not (internally) connected. Leave floating or connect to ground reference.
E4	NC		Not (internally) connected. Leave floating or connect to ground reference.
E5	AGND	P	Ground reference for VDD_FDA, IN_LDO, VDD_ADC and VDD2_ADC supplies. Connect to system ground for normal operation.
E6	VDD_FDA	P	ADC driver amplifier positive supply. Referenced to AGND. Connect to OUT_LDO if using on-device LDO, else connect it to a single power source that also supplies the VDD_ADC pin.
E7	VDD_FDA	P	ADC driver amplifier positive supply. Referenced to AGND. Connect to OUT_LDO if using on-device LDO, else connect it to a single power source that also supplies the VDD_ADC pin.
E8	VDD_FDA	P	ADC driver amplifier positive supply. Referenced to AGND. Connect to OUT_LDO if using on-device LDO, else connect it to a single power source that also supplies the VDD_ADC pin.
E9	$\overline{\text{PIN}}$/SPI	DI	Device mode selection input. ▶ 0: Pin mode operation. Control and configure device operation through configuration pin logic. ▶ 1: Control and configure through register over SPI.
E10	DOUT/$\overline{\text{RDY}}$	DO	Serial interface data output & data ready signal combined. Configure this output data pin as either a DOUT pin only, or through the SPI control mode, and include the ready signal ($\overline{\text{RDY}}$). The ability to program the device to provide a combined DOUT/$\overline{\text{RDY}}$ signal can reduce the number of required interface IO lines.
E11	SCLK	DI	Serial interface clock.
E12	SDI	DI	Serial interface data input.
E13	$\overline{\text{CS}}$	DI	Serial interface chip-select input. Active low.
E14	$\overline{\text{DRDY}}$	DO	ADC conversion data ready output. Periodic signal output to signify conversion results are available.
F1	NC		Not (internally) connected. Leave floating or connect to ground reference.
F2	NC		Not (internally) connected. Leave floating or connect to ground reference.
F3	NC		Not (internally) connected. Leave floating or connect to ground reference.
F4	EN_LDO	DI	On-device LDO enable input. Active high.

F5	CLK_SEL	DI	ADC clock source selection input.
			▶ In pin control mode:
			  ▶ 0: CMOS clock option. Apply external CMOS clock signal to XTAL2_MCLK pin, tie XTAL1 pin to DGND.
			  ▶ 1: Crystal Option. Connect external crystal across the XTAL1 and XTAL2_MCLK pins.
			▶ In the SPI control mode: Tie CLK_SEL pin to DGND. Select the clock source through register access. The LVDS clock option is available only in the SPI control mode.

F6	OUT_LDO	P	On-device LDO output. Bypass OUT_LDO to AGND with a capacitor of at least 1 μF.

PIN CONFIGURATION AND FUNCTION DESCRIPTION

Table 8. ADAQ7767-1 Pin Function Descriptions (Continued)

Pin No.	Name	Type[1]	Description
F7	OUT_LDO	P	On-device LDO output. Bypass OUT_LDO to AGND with a capacitor of at least 1 µF.
F8	OUT_LDO	P	On-device LDO output. Bypass OUT_LDO to AGND with a capacitor of at least 1 µF.
F9	VDD_IO	P	Digital Supply. The VDD_IO pin sets the logic levels for all interface pins. This pin powers the digital processing through the internal digital LDO. Referenced to DGND. Bypass VDD_IO to DGND with a capacitor of at least 1 µF.
F10	DGND	P	Ground reference for VDD_IO supplies. Connect to system ground for normal operation.
F11	DGND	P	Ground reference for VDD_IO supplies. Connect to system ground for normal operation.
F12	DREG_CAP	AO	ADC's internal digital LDO regulator output. Decouple this pin to DGND with a 1 µF capacitor. For VDD_IO ≤ 1.8 V, use a 10 µF capacitor. Do not use the voltage output from AREG_CAP in circuits external to the ADAQ7767-1.
F13	XTAL1	DI	ADC clock input 1. ▶ External Crystal: Connect to one node of the external crystal. ▶ LVDS: Connect to one node of the LVDS clock source. ▶ CMOS clock: Connect to DGND.
F14	XTAL2_MCLK	DI	ADC clock input 2. ▶ External Crystal: Connect to the second node of the external crystal. ▶ LVDS: Connect to the second node of the LVDS clock source. ▶ CMOS clock: Connect to the CMOS clock source. Logic level referenced to VDD_IO and DGND.

[1] AI is analog input; AO is analog output; DI is digital input; DO is digital output; DI/O is bidirectional digital; P is power or ground.

TYPICAL PERFORMANCE CHARACTERISTICS

AGND = DGND = 0 V, Input common mode voltage = 0 V, IN_LDO = EN_LDO = 5.1 V to 5.5 V, OUT_LDO = VDD_FDA = VDD_ADC, VDD2_ADC = 2 V to 5.5 V, VDD_IO = 1.7 V to 3.6 V, REF+ = 4.096 V, REF−= 0 V, MCLK = SCLK = 16.384 MHz 50:50 duty cycle, f_{MOD} = MCLK/2, Filter = Wideband Low Ripple, Decimation = 32, ODR = 256 kSPS, linearity boost buffer on, reference precharge buffers on, FDA = Full Power Mode, T_A = -40°C to 105°C, unless otherwise noted. Typical values are at T_A = 25°C.

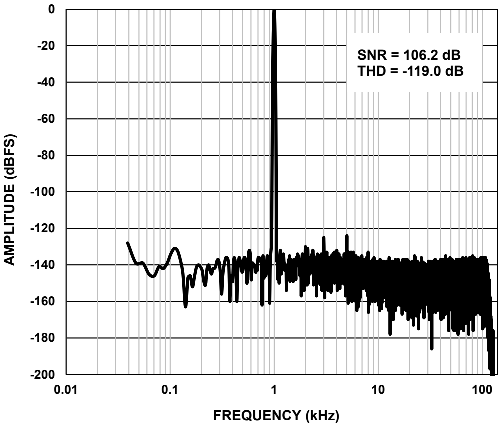


Figure 14. Wideband Low Ripple FIR Filter, Differential Input, IN1, -0.5 dBFS (3.9 Vp)

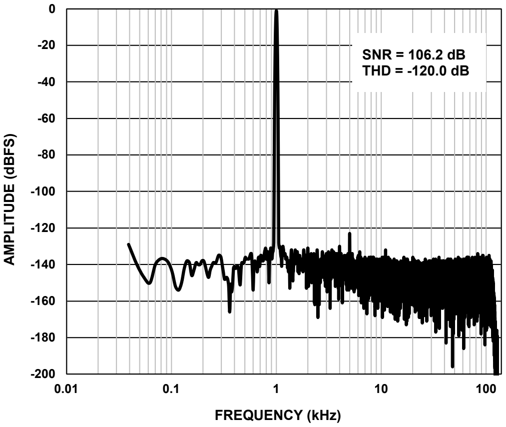


Figure 15. Wideband Low Ripple FIR Filter, Differential Input, IN2, -0.5dBFS (10.6Vp)

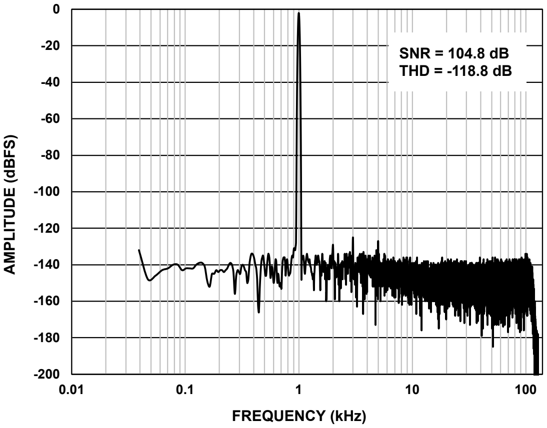


Figure 16. Wideband Low Ripple FIR Filter, Differential Input, IN3, -2.0dBFS (22.67Vp)

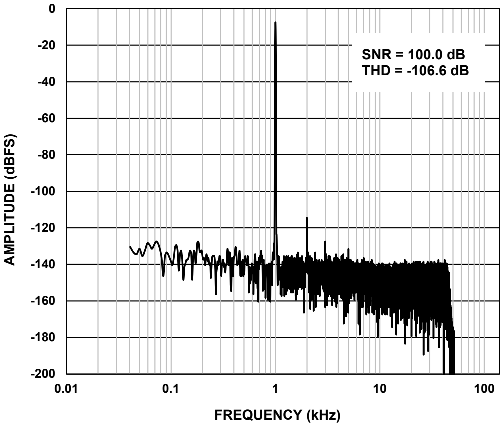


Figure 17. Wideband Low Ripple FIR Filter, MCLK = 13.107 MHz, ODR = 102.4kSPS, Single-Ended Input, IN3, -12VDC + 10Vp [-2V to -22V]

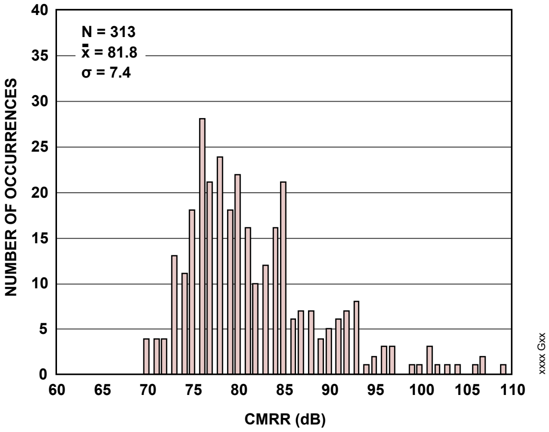


Figure 18. IN1 DC CMRR Distribution

TYPICAL PERFORMANCE CHARACTERISTICS

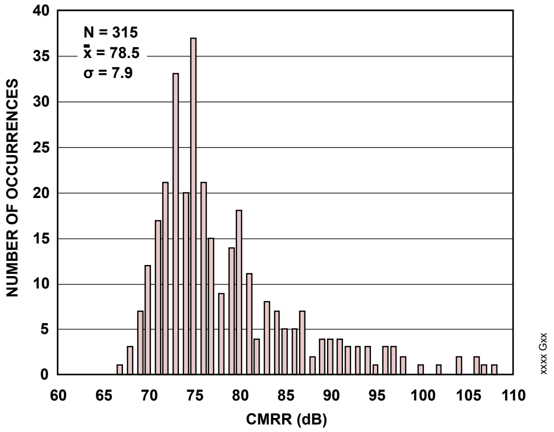


Figure 19. IN2 DC CMRR Distribution

TBD

Figure 20. IN3 DC CMRR Distribution

TBD

Figure 21. Differential RTI Offset Voltage vs. Input Common-Mode Voltage

TBD

Figure 22. ADAQ7767-1 AC CMRR vs. Input Frequency

TBD

Figure 23. Gain Error Distribution

TBD

Figure 24. Gain Error Drift Distribution

TYPICAL PERFORMANCE CHARACTERISTICS

TBD

Figure 25. Offset Error Distribution

TBD

Figure 26. Offset Error Drift Distribution

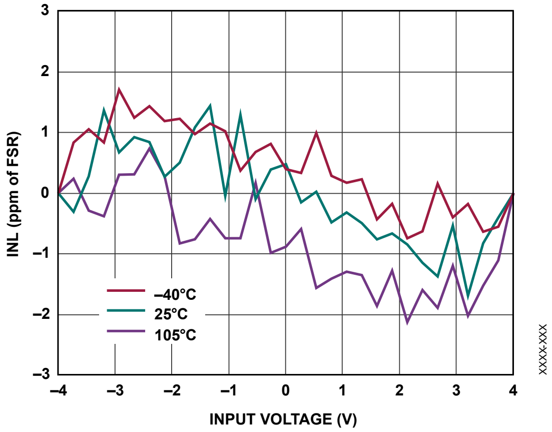


Figure 27. INL Error vs. Input Voltage over Temperature, IN1, Differential Input

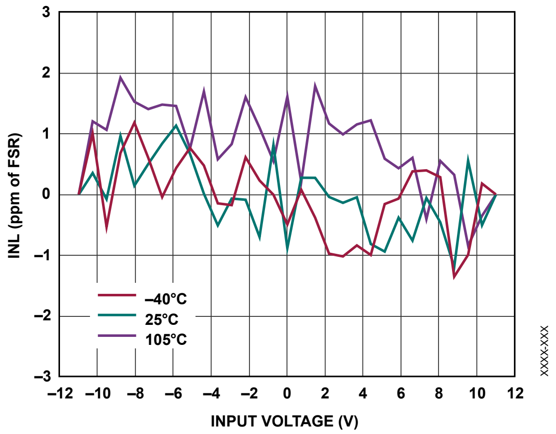


Figure 28. INL Error vs. Input Voltage over Temperature, IN2, Differential Input

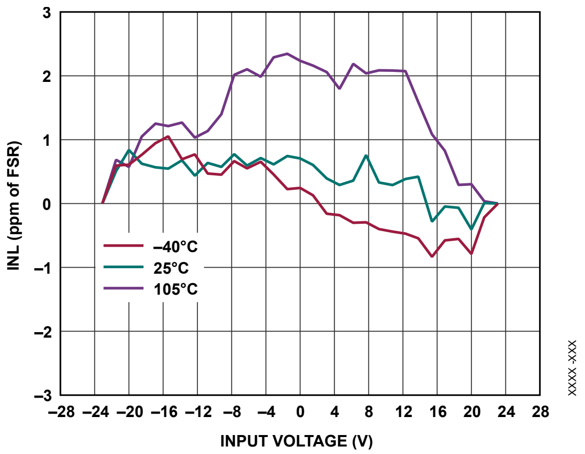


Figure 29. INL Error vs. Input Voltage over Temperature, IN3, Differential Input

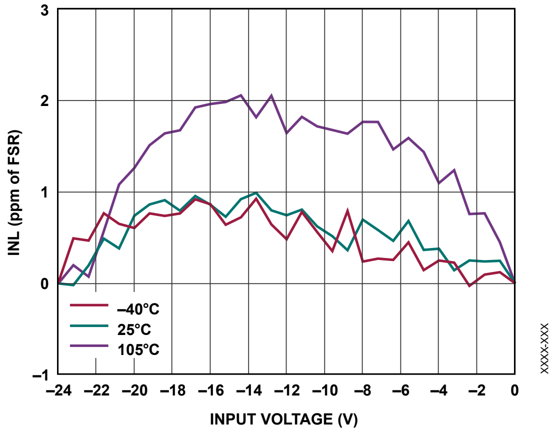


Figure 30. INL Error vs. Input Voltage over Temperature, IN3, Single-ended Input, 0 to -24V (unipolar) input sweep

TYPICAL PERFORMANCE CHARACTERISTICS

TBD

Figure 31. Dynamic Range vs. Decimation Rate, Wideband Low Ripple Filter, Shorted Inputs

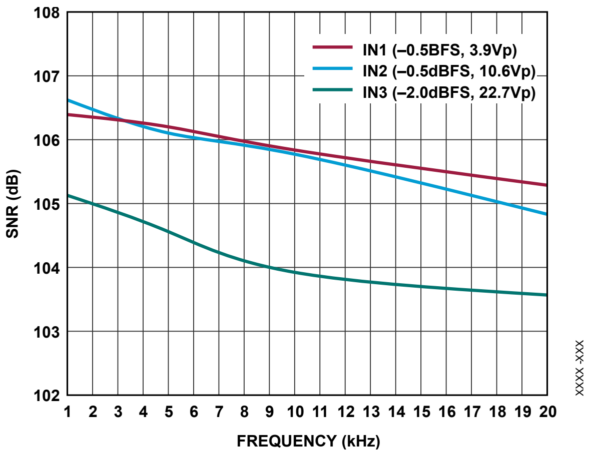


Figure 32. SNR vs. Input Frequency at 25°C, Differential Input, FDA = Full Power

TBD

Figure 33. SNR vs. Decimation Rate, Wideband Low Ripple Filter, -0.5 dBFS, 1 kHz

TBD

Figure 34. THD Distribution, -0.5 dBFS, 1kHz

TBD

Figure 35. THD vs. Temperature, -0.5 dBFS, 1 kHz

TBD

Figure 36. THD vs. Input Amplitude Across All Input Ranges, 1 kHz

TYPICAL PERFORMANCE CHARACTERISTICS

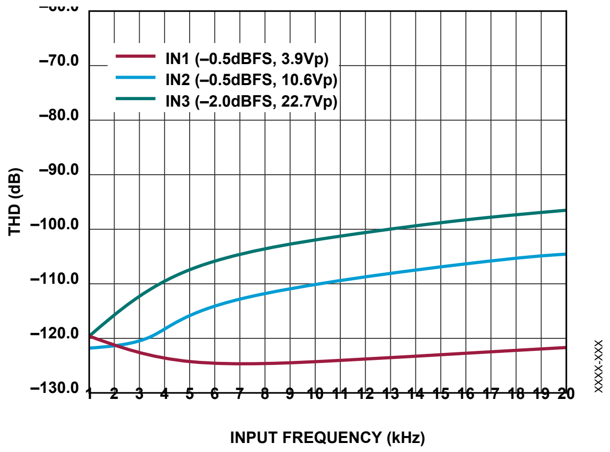


Figure 37. THD vs. Input Frequency Across FDA Power Modes, at 25°C, Differential Input

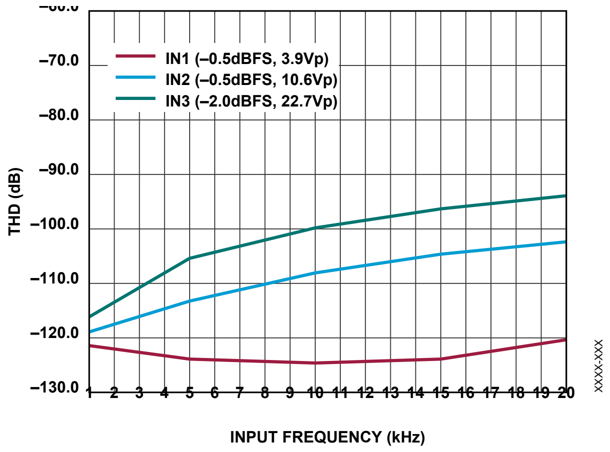


Figure 38. THD vs. Input Frequency Across FDA Power Modes, at 105°C, Differential Input

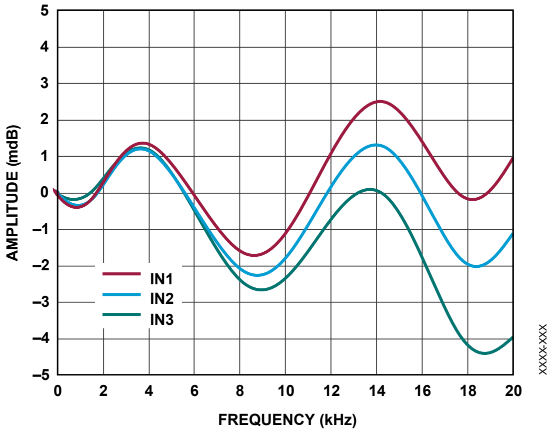


Figure 39. Wideband Low Ripple FIR Filter Passband Ripple, ODR = 256 kSPS

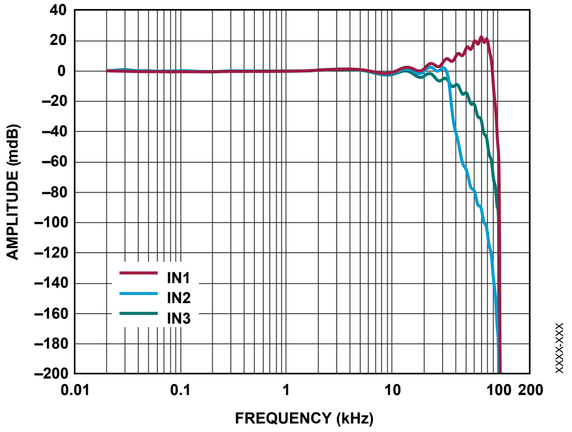


Figure 40. Wideband Low Ripple FIR Filter Magnitude Flatness, ODR = 256 kSPS

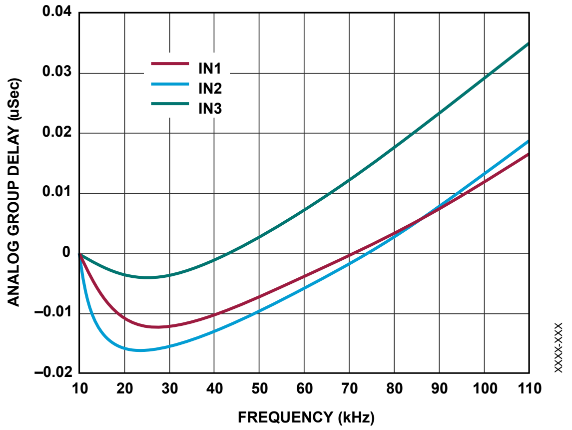


Figure 41. Analog Front-End (AFE) Passband Analog Group Delay vs. Frequency at 25°C, Normalized to Delay at 10 kHz

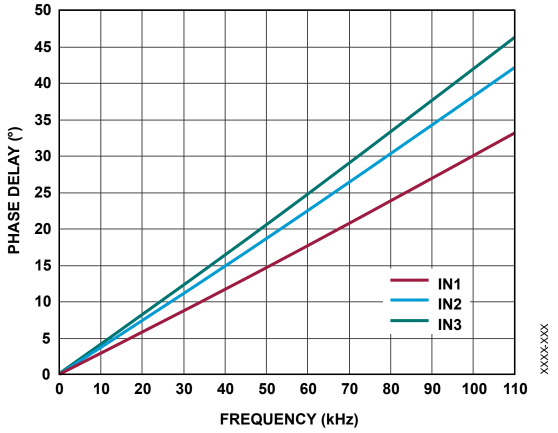


Figure 42. Analog Front-End (AFE) Passband Phase Response

TYPICAL PERFORMANCE CHARACTERISTICS

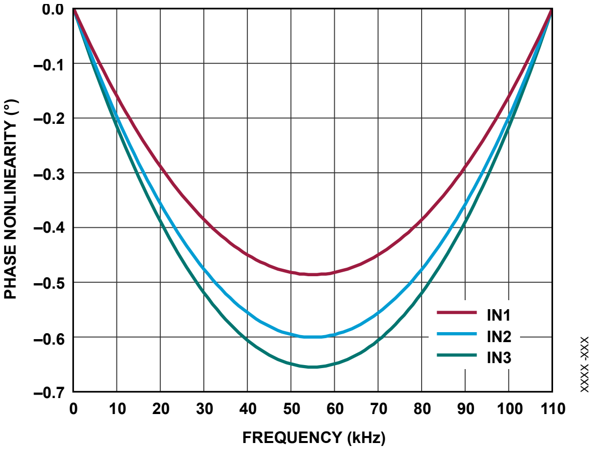


Figure 43. Analog Front-End (AFE) Phase Nonlinearity vs. Passband Frequency, Endpoint Method (100 Hz to 110kHz)

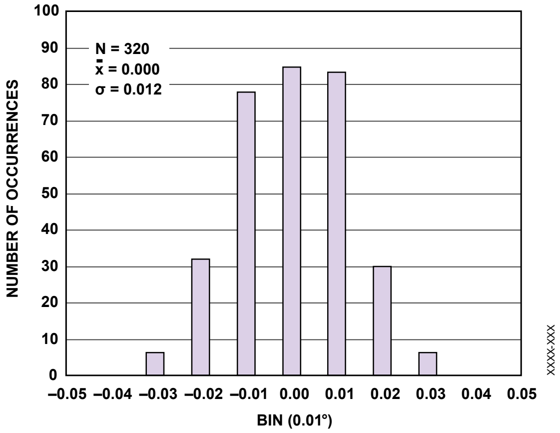


Figure 44. Device-to-Device Phase Angle Mismatch, 20 kHz, 25°C, IN1, Normalized to the Mean Value

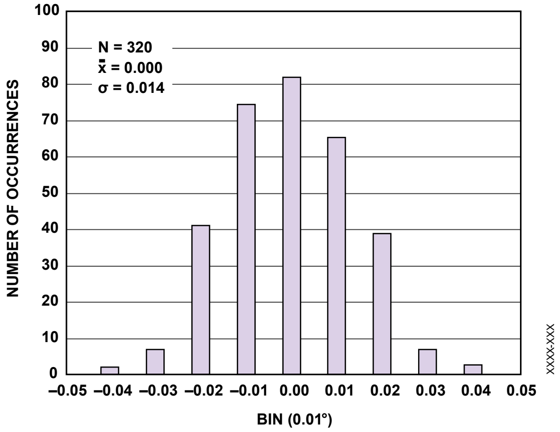


Figure 45. Device-to-Device Phase Angle Mismatch, 20 kHz, 25°C, IN2, Normalized to the Mean Value

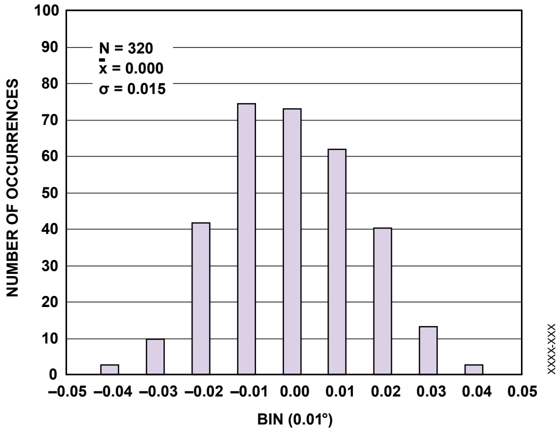


Figure 46. Device-to-Device Phase Angle Mismatch, 20 kHz, 25°C, IN3, Normalized to the Mean Value

TBD

Figure 47. LDO AC PSRR, Connected to VDD_FDA, VDD_ADC, VDD2_ADC with 1µF External Supply Decoupling Capacitor at OUT_LDO

TBD

Figure 48. VDD_IO AC PSRR Using Built-In Supply Decoupling vs. Additional External Capacitor

TYPICAL PERFORMANCE CHARACTERISTICS

TBD

Figure 49. LDO Supply Current vs. Temperature, DC Input, FDA = Full Power, OUT_LDO Connected to VDD_FDA, VDD_ADC, VDD2_ADC

TBD

Figure 50. LDO Supply Current vs. Temperature, DC Input, FDA = Low Power, OUT_LDO Connected to VDD_FDA, VDD_ADC, VDD2_ADC

TBD

Figure 51. LDO Supply Current vs. Temperature, AC Input, FDA = Full Power, OUT_LDO Connected to VDD_FDA, VDD_ADC, VDD2_ADC

TBD

Figure 52. LDO Supply Current vs. Temperature, AC Input, FDA = Low Power, OUT_LDO Connected to VDD_FDA, VDD_ADC, VDD2_ADC

TBD

Figure 53. VDD_IO Supply Current vs. Temperature, DC Input

TBD

Figure 54. VDD_IO Supply Current vs. Temperature at Various Gain Modes, AC Input

NOISE PERFORMANCE

The noise performance of the signal chain is highly dependent on the application's input range and the desired output data rate (ODR) of the ADAQ7767-1. While the input range is varied by simply selecting from the pairs of input pins, the ODR of the device is dependent on the MCLK and the configured decimation rate. The ODR, for any digital filter, can be calculated by:

$$f_{MOD} = \frac{MCLK}{MCLK\_DIV} \tag{6}$$

$$ODR = \frac{f_{MOD}}{DEC\_RATE} \tag{7}$$

where f_{MOD} is the ADC modulator frequency, DEC_RATE is the decimation rate, MCLK is the master clock frequency, and MCLK_DIV is the ratio between the MCLK applied at the input to the ADAQ7767-1 and the clock used by the ADC modulator.

Noise performance also depends on the type of digital filter used; each having different -3 dB bandwidths. The digital filters available on the ADAQ7767-1 are

- Wideband low ripple FIR filter, −3 dB at 0.433 × ODR
- Sinc5 low latency filter, −3 dB at 0.204 × ODR
- Sinc3 low latency filter, –3 dB at 0.2617 × ODR

The DEC_RATE, MCLK, MCLK_DIV, and type of digital filter can be varied by the user, and the manner of configuration varies between the PIN and SPI Modes (see Device Configuration Method).

Table 9, Table 10, and Table 11 show the noise performance for the different digital filters of the ADAQ7767-1 for various ODR values. The specified noise values and dynamic ranges are typical with an external 4.096 V reference (VREF). The rms noise is measured with shorted analog inputs to ground reference. The dynamic range (DR) is the ratio of the rms value of the full scale to the rms noise measured when input pins are shorted together. The full-scale value depends on the input range, determined by the input pins used, and the input configuration. In decibels, the DR is given by:

$$DR = 20log\left(\frac{Input\ \ Range\ \ (Vpp)}{2\sqrt{2} \times RMS\ \ Noise}\right) \tag{8}$$

Table 9. Wideband Low Ripple FIR Filter Noise Performance vs. ODR (V_{REF} = 4.096 V, f_{MOD}=MCLK/2)

MCLK (MHz)	DEC_RATE	ODR (kSPS)	−3 dB Bandwidth (kHz)	Gain	Input Range (V)	Input Configuration	Shorted Input Dynamic Range (dB)	RTI Noise Spectral Density (nV/√Hz)	RTI RMS Noise (µVrms)
16.384	32	256	110.8	1	±4.096	Differential	107.1	39	12.8
16.384	32	256	110.8	0.36	±11.264	Differential	107.4	102	34.0
16.384	32	256	110.8	0.14	±28.672	Differential	107.4	257	85.9
16.384	32	256	110.8	1	IN1+ = 0 to +/-4.096V, IN1− = GND	Unipolar Single-Ended	101.1	39	12.8
16.384	32	256	110.8	0.36	IN2+ = 0 to +/-11.264V, IN2− = GND	Unipolar Single-Ended	101.4	102	34.0
16.384	32	256	110.8	0.14	IN3+ = 0 to +/-24V, IN3− = GND	Unipolar Single-Ended	99.9	257	85.9
16.384	64	128	55.4	1	±4.096	Differential			
16.384	64	128	55.4	0.36	±11.264	Differential			
16.384	64	128	55.4	0.14	±28.672	Differential			
16.384	64	128	55.4	1	IN1+ = 0 to +/-4.096V, IN1− = GND	Unipolar Single-Ended			
16.384	64	128	55.4	0.36	IN2+ = 0 to +/-11.264V, IN2− = GND	Unipolar Single-Ended			
16.384	64	128	55.4	0.14	IN3+ = 0 to +/-24V, IN3− = GND	Unipolar Single-Ended			
16.384	128	64	27.7	1	±4.096	Differential			
16.384	128	64	27.7	0.36	±11.264	Differential			
16.384	128	64	27.7	0.14	±28.672	Differential			
16.384	128	64	27.7	1	IN1+ = 0 to +/-4.096V, IN1− = GND	Unipolar Single-Ended			
16.384	128	64	27.7	0.36	IN2+ = 0 to +/-11.264V, IN2− = GND	Unipolar Single-Ended			
16.384	128	64	27.7	0.14	IN3+ = 0 to +/-24V, IN3− = GND	Unipolar Single-Ended			
13.107	64	102.4	44.3	1	±4.096	Differential	110.3	42	8.9
13.107	64	102.4	44.3	0.36	±11.264	Differential	110.6	113	23.7

NOISE PERFORMANCE

Table 9. Wideband Low Ripple FIR Filter Noise Performance vs. ODR (V_{REF} = 4.096 V, f_{MOD}=MCLK/2) (Continued)

MCLK (MHz)	DEC_RATE	ODR (kSPS)	−3 dB Bandwidth (kHz)	Gain	Input Range (V)	Input Configuration	Shorted Input Dynamic Range (dB)	RTI Noise Spectral Density (nV/√Hz)	RTI RMS Noise (µVrms)
13.107	64	102.4	44.3	0.14	±28.672	Differential	110.5	284	59.8
13.107	64	102.4	44.3	1	IN1+ = 0 to +/-4.096V, IN1− = GND	Unipolar Single-Ended	104.2	42	8.9
13.107	64	102.4	44.3	0.36	IN2+ = 0 to +/-11.264V, IN2− = GND	Unipolar Single-Ended	104.5	113	23.7
13.107	64	102.4	44.3	0.14	IN3+ = 0 to +/-24V, IN3− = GND	Unipolar Single-Ended	103.1	284	59.8

Table 10. Sinc5 Filter Noise Performance vs. ODR (V_{REF} = 4.096 V, f_{MOD}=MCLK/2)

MCLK (MHz)	DEC_RATE	ODR (kSPS)	−3 dB Bandwidth (kHz)	Gain	Input Range (V)	Input Configuration	Shorted Input Dynamic Range (dB)	RTI Noise Spectral Density (nV/√Hz)	RTI RMS Noise (µVrms)
16.384	8	1024(16-bit)	208.9	1	±4.096	Differential	92.8	144	65.8
16.384	8	1024(16-bit)	208.9	0.36	±11.264	Differential	92.8	395	180.5
16.384	8	1024(16-bit)	208.9	0.14	±28.672	Differential	92.9	1004	458.9
16.384	8	1024(16-bit)	208.9	1	IN1+ = 0 to +/-4.096V, IN1− = GND	Unipolar Single-Ended	86.8	144	65.8
16.384	8	1024(16-bit)	208.9	0.36	IN2+ = 0 to +/-11.264V, IN2− = GND	Unipolar Single-Ended	86.8	395	180.5
16.384	8	1024(16-bit)	208.9	0.14	IN3+ = 0 to +/-24V, IN3− = GND	Unipolar Single-Ended	85.3	1004	458.9
16.384	16	512	104.4						
16.384	32	256	52.2						
16.384	64	128	26.1						
16.384	128	64	13.1						
16.384	256	32	6.5						
13.107	32	204.8	41.8						
13.107	64	102.4	20.9						
13.107	128	51.2	10.4						
13.107	256	25.6	5.2						

Table 11. Sinc3 Filter Noise Performance vs. ODR (V_{REF} = 4.096 V, f_{MOD}=MCLK/2)

MCLK (MHz)	DEC_RATE	ODR (kSPS)	−3 dB Bandwidth (kHz)	Gain	Input Range (V)	Input Configuration	Shorted Input Dynamic Range (dB)	RTI Noise Spectral Density (nV/√Hz)	RTI RMS Noise (µVrms)
16.384	32	256	67						
16.384	128	64	16.7						
16.384	512	16	4.2						
16.384	2048	4	1.05						
16.384	8192	1	0.26						
16.384	163840	0.05	0.013						

THEORY OF OPERATION

ANALOG INPUT

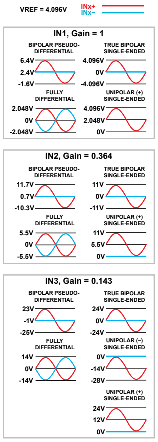


Figure 55. Examples of Different Input Signals

The wide common mode input range and high CMRR of the ADAQ7767-1 allow each pair of its input pins to swing with an arbitrary relationship to each other, allowing the device to accept a wide variety of signal swings, including unipolar and bipolar single-ended, pseudodifferential and fully differential signals, as shown in Figure 55. Emphasis is given on IN3's positive single-ended range, where the single-ended signal is limited to +24V (-1.55 dBFS) due to IN3's common mode limit.

Arbitrary Input

The two-tone test shown in Figure TBA demonstrates the arbitrary input drive capability of the ADAQ7767-1. This test simultaneously drives INx+ with a −6dBFS 19.5kHz single-ended sine wave and INx− with a −6dBFS 20.5kHz single-ended sine wave. Together, these signals sweep the analog inputs across a wide range of common mode and differential mode voltage combinations. They also have a simple spectral representation. An ideal differential converter with no common-mode sensitivity will digitize this signal as two −6dBFS spectral tones, one at each sine wave frequency. The FFT plot in Figure TBA demonstrates the ADAQ7767-1 response approaches this ideal, with TBA dB of SFDR limited by the converter's second harmonic distortion response to the 20.5kHz sine wave on INx–.

TBD

Figure 56. Two-Tone input, IN1+ = -6dBFS 19.5kHz Sine, IN1– = -6dBFS 20.5kHz Sine, 32k Point FFT, ODR= 256 kSPS, VREF=4.096V, G=1

TBD

Figure 57. Two-Tone input, IN2+ = -6dBFS 19.5kHz Sine, IN2– = -6dBFS 20.5kHz Sine, 32k Point FFT, ODR= 256 kSPS, VREF=4.096V, G=0.36

TBD

Figure 58. Two-Tone input, IN3+ = -6dBFS 19.5kHz Sine, IN3– = -6dBFS 20.5kHz Sine, 32k Point FFT, ODR= 256 kSPS, VREF=4.096V, G=0.14

THEORY OF OPERATION

Absolute Input Range

The absolute voltage that the device accepts varies between the input pairs. For IN1+/− and IN2+/−, the absolute maximum input is at ±15V. For IN3+/−, the absolute maximum is at ±36V.

Differential Input Range

The differential signal amplitude depends on the frontend signal gain and the reference voltage level. The maximum differential input voltage can be calculated by:

$$V_{INx+} - V_{INx-} = \pm V_{REF} \ /AFE\_GAIN \tag{9}$$

Common Mode Input Range

The common mode input signal (VICM) is the average of the absolute voltage across a particular pair of differential inputs, given by the formula:

$$V_{ICM} = \frac{V_{INx+} + V_{INx-}}{2} \tag{10}$$

The input signal common mode range depends on the driver amplifier supply voltage (VDD_FDA) and the selected pair of input pins. The diagram in Figure 59 show the operating region where a valid output is produced for each input pair of the ADAQ7767-1. To simplify selection of input pins, Table 12 lists maximum differential input range and common mode input range for each of the input pins.

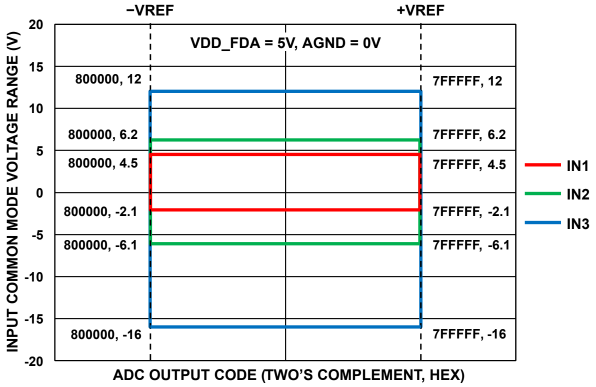


Figure 59. Common Mode Input Range vs. ADC Output Code

Table 12. Input Selection Table

Input Pin	Gain (V/V)	Differential Input Range with V_{REF} = 4.096V (V)	Common Mode Input Range with Full-scale Input Signal V_{REF} = 4.096V	
			Min (V)	Max (V)
IN1+/−	1	±4.096	−2.1	+4.5
IN2+/−	0.364	±11.264	−6.1	+6.2
IN3+/−	0.143	±28.672	−16	+12

IN3 Single-Ended Input Range

For IN3+/−, emphasis is given to its single-ended input configuration, where IN3+ = Vin, and IN3− = AGND, because it limited by IN3's input common mode range, unlike IN1 and IN2. In this configuration, the single-ended signal positive amplitude is linear only up to +24V, which corresponds to 83.7% of the Full-Scale Input (or -1.55 dBFS). This range captures the intended application of single-ended IEPE sensors.

On the negative side, a single-ended signal at IN3 is not limited, and it can swing as low as −28.672V.

Figure 60 show the relative scaling between the differential voltages applied to the input pins and the respective 24-bit, twos complement digital outputs, expressed as hexadecimal codes, while Figure 61 shows the special case of a single-ended input at IN3. ADAQ7767-1 is typically characterized with differential inputs at -0.5 dBFS of each input pair.

THEORY OF OPERATION

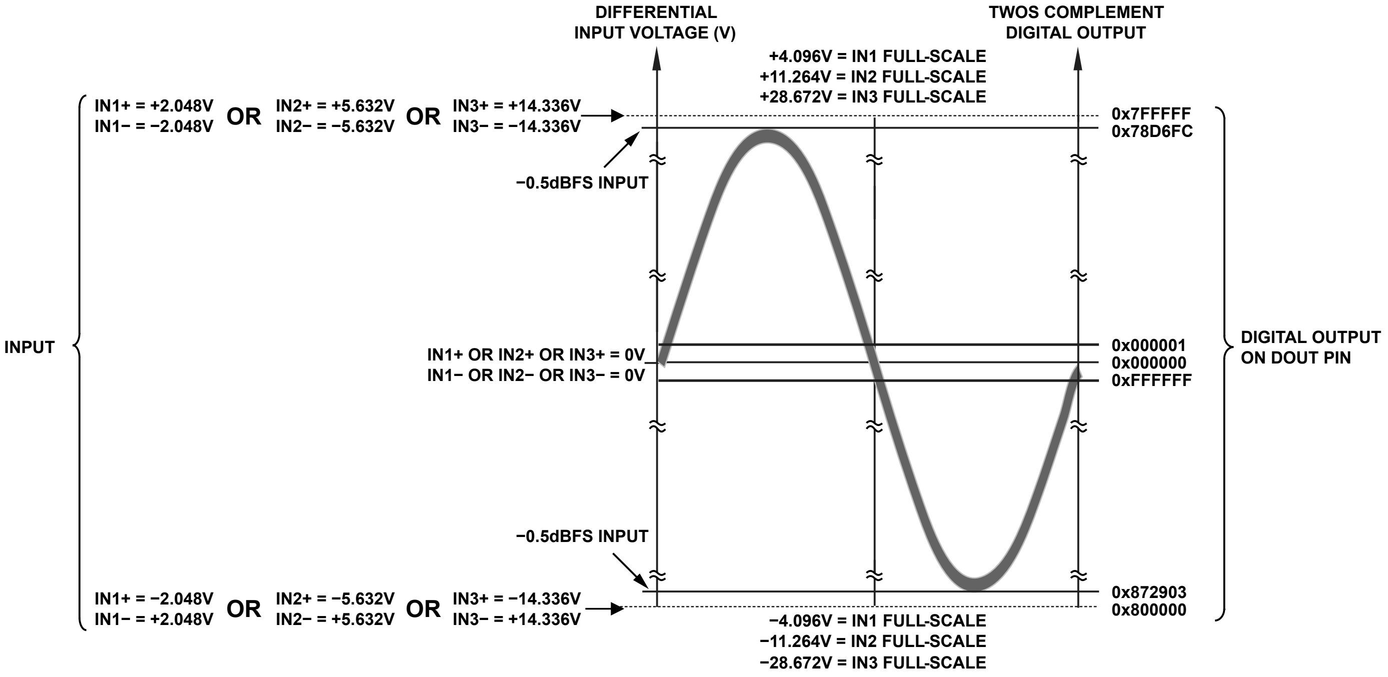


Figure 60. Differential Input Voltage vs. ADC Output Code

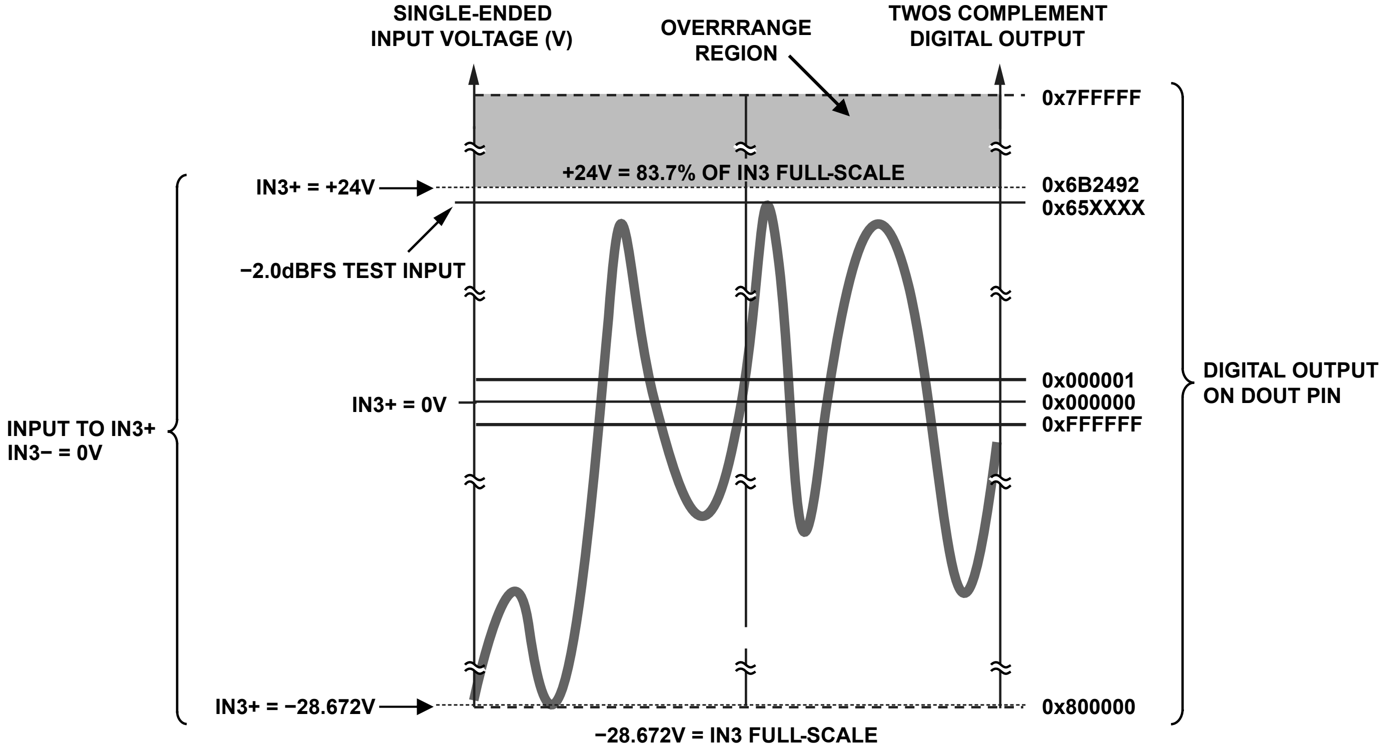


Figure 61. IN3 Single-Ended Input Voltage vs. ADC Output Code

THEORY OF OPERATION

ANTI-ALIASING FILTER

The input signal bandwidth of the ADAQ7767-1 is dominated by its digital filter. The user can program the decimation ratio to adjust the digital filter bandwidth. The filter bandwidth can also be fine-tuned through the change of MCLK frequency. For example, with the wideband digital filter option and an ODR = 256 kSPS, the -3dB bandwidth of the overall signal chain is equal to the digital filter bandwidth of 0.433 × ODR = 110.85 kHz. The same filter has a stop band of 0.499 × ODR and a minimum stop band attenuation of -105dB. As with any sampled system, the ADAQ7767-1's digital filter does not offer rejection to signals around the signal sampling frequency Fs. As shown in Figure 62, an additional analog anti-aliasing filter is required to reject signals around Fs to prevent out-of-band signals from folding back to the band of interest.

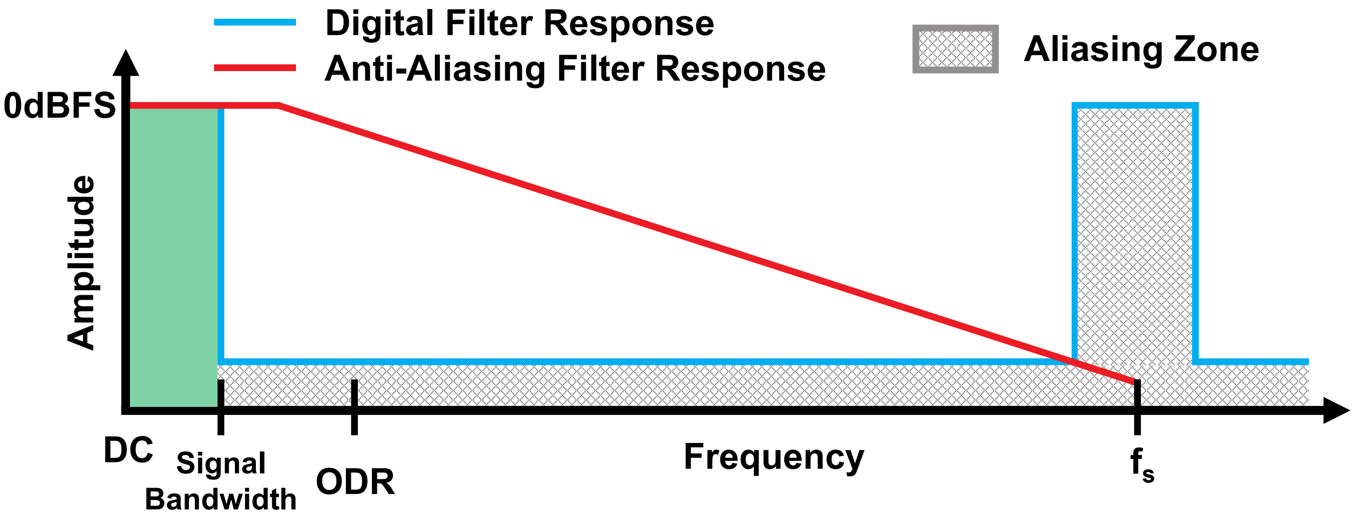


Figure 62. Simplified illustration of the overall frequency response

The digital filter has no rejection to signals within frequency range of Fs +/- F_{3dB}. The ADAQ7767-1's core ADC samples at a frequency of 2 × f_{MOD}. In normal operating mode with f_{MOD} = MCLK/2, the ADC's sampling frequency Fs is equal to MCLK.

The ADAQ7767-1 features a fourth order analog anti-aliasing filter that is designed to achieve greater than 80dB of rejection at 16.384 MHz for all input pairs, as listed in Table 13. Combining its analog anti-aliasing filter with its Wideband Low Ripple FIR Filter, the ADAQ7767-1 is able to reject all of the out-of-band signals by a minimum of 105dB.

Magnitude and Phase Response

The anti-aliasing filter is designed to achieve optimal aliasing rejection level with minimum magnitude and phase distortion to the in-band signal. With the help of ADI's iPASSIVES™ technology, the filter has highly stable -3dB corners and minimal passband droop from DC-100 kHz for each of the three input pairs, as listed in Table 13. The filter's passband phase response is also highly linear. And the tightly controlled -3dB point of the filter gives the ADAQ7767-1 a superior device to device phase matching performance, as shown in Figure 67 to Figure 69.

THEORY OF OPERATION

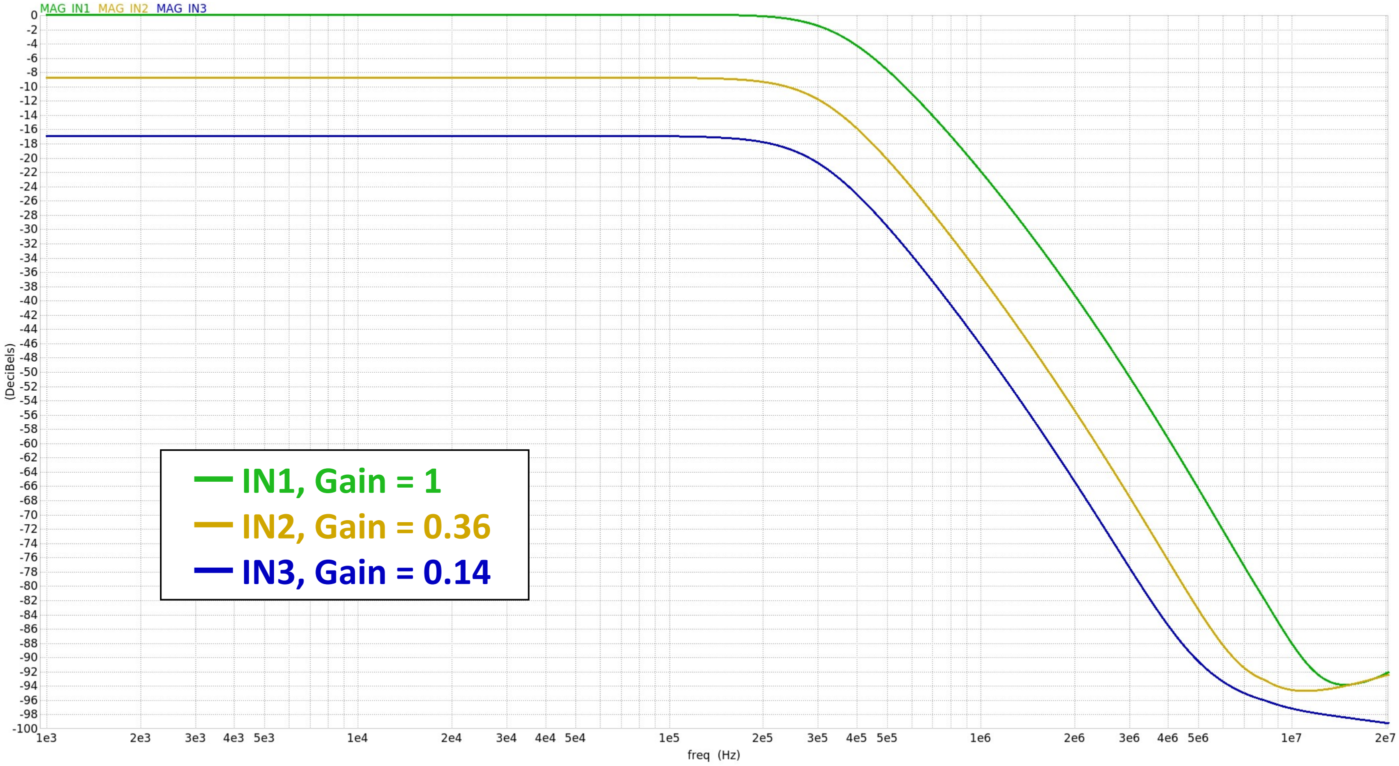


Figure 63. Anti-Aliasing Filter Magnitude Response

Table 13. Anti-Aliasing Filter Profile

Input Pin	Gain	-3dB Bandwidth (kHz)	Relative to DC Attenuation at MCLK=16.384 MHz (dB)	DC-100 kHz Passband Droop (mdB)	Change in Group Delay from DC to 100 kHz (nseconds)
IN1+/−	1	365	88	-50	17
IN2+/−	0.36	304	86	-200	19
IN3+/−	0.14	283	80	-100	35

TBD

Figure 64. AAF frequency response.

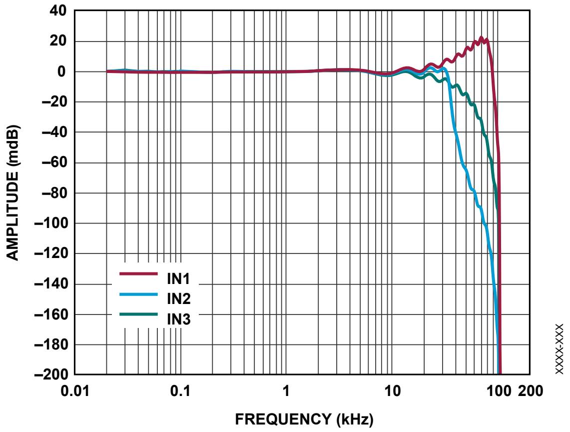


Figure 65. AAF Passband Droop for Various Input Ranges

THEORY OF OPERATION

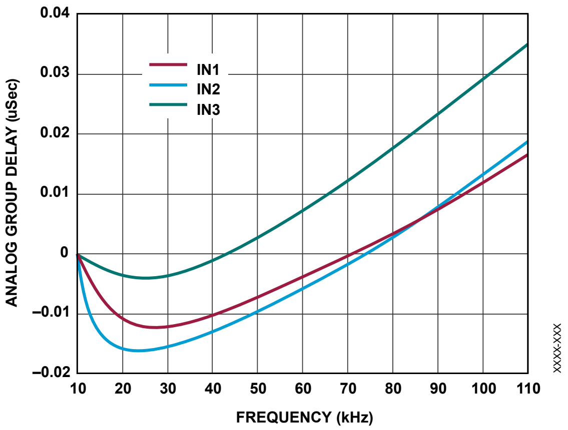


Figure 66. AAF Passband Analog Group Delay vs. Frequency for Various Input Ranges at 25°C, Normalized to Delay at 10kHz

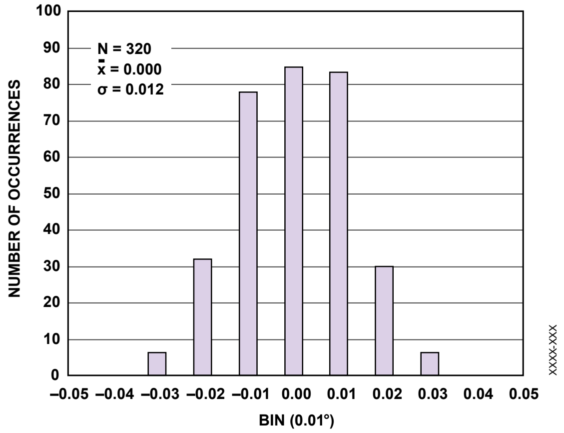


Figure 67. Device to Device Phase Matching, 20 kHz, 25°C, IN1, Normalized to the Mean Value

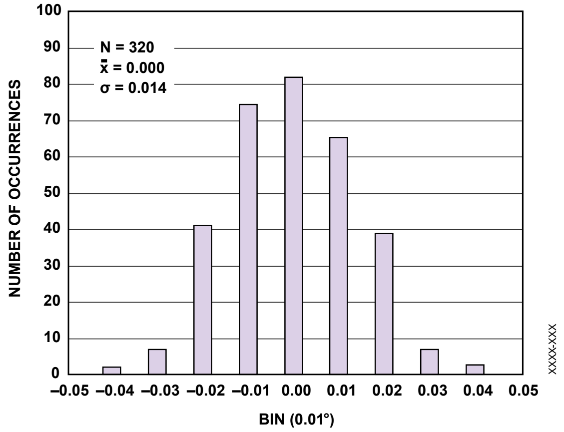


Figure 68. Device to Device Phase Matching, 20 kHz, 25°C, IN2, Normalized to the Mean Value

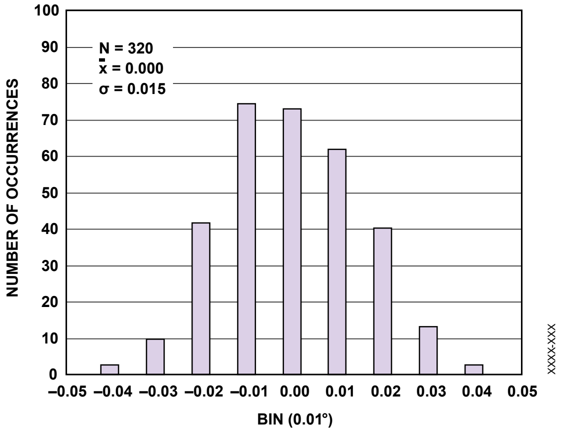


Figure 69. Device to Device Phase Matching, 20 kHz, 25°C, IN3, Normalized to the Mean Value

Calculations on AFE Phase Performance

All mismatches on the phase angle across gain or temperature, or from device to device are due to the analog front-end and its filters, as the group delay of the digital filter is constant.

Phase Angle Over Frequency

The ADAQ7767-1 has a linear phase response. To interpolate the phase delay from one frequency to another, the ideal formula is:

$$\frac{\theta_1}{f_{IN\_1}} = \frac{\theta_2}{f_{IN\_2}} \qquad (11)$$

where:

θ_x is the phase delay of the AFE using an input frequency of f_{IN_x}.

However, due to small nonlinearities, calibrate the formula in terms of its slope and intercept.

$$\theta = m * f_{IN} + b + nonlinearity \qquad (12)$$

where:

m is the slope and *b* is the y-intercept of the linear equation of the phase delay with respect to the input frequency over the span of the passband frequency using endpoint method, as shown in Figure 70.

Using the phase delay at 100 Hz to 110 kHz as endpoints, a typical device has a worst nonlinearity of approximately -0.3° to -0.7°, depending on the input range, as shown in Figure 71.

THEORY OF OPERATION

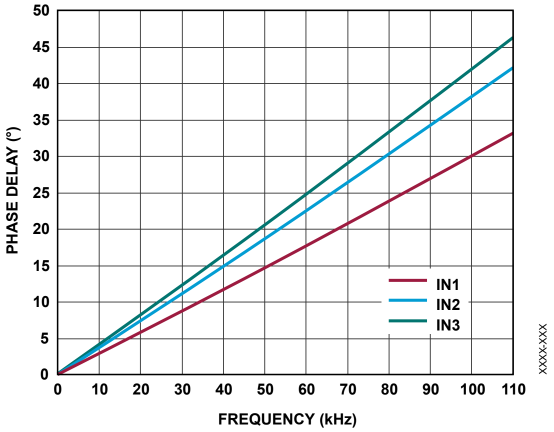


Figure 70. Analog Front-End (AFE) Phase Response Across All Input Ranges

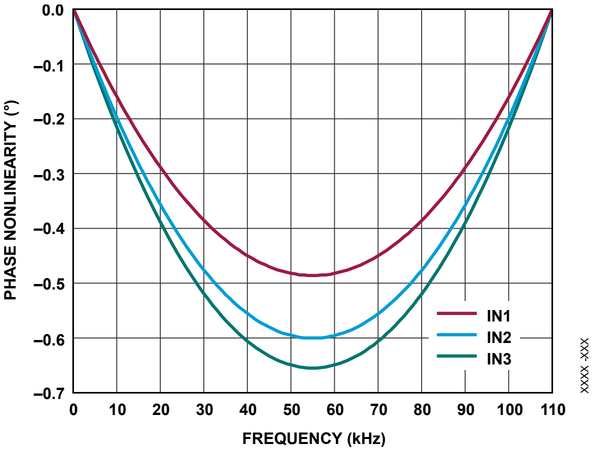


Figure 71. Analog Front-End (AFE) Phase Nonlinearity vs. Passband Frequency, Endpoint Method (100 Hz to 110 kHz)

Phase Angle Drift

Phase Angle Drift defines the rate of change of the phase delay over temperature of a single device at a given input signal frequency. The drift in degrees/°C is calculated using the endpoint method over the full operating temperature range of -40°C and 105°C. The typical specification is the average phase angle drift across a large number of devices, while the maximum (or minimum) specification is six standard deviations (σ) away from the typical value.

For example, Typical Device A has a 5.8° phase delay from input to output at 20 kHz at T_A = 25°C using IN1. At T_A = 105°C, the same Device A typically has:

5.8° + 0.00070°/°C (typical spec) * (105°C – 25°C) = 5.856° phase delay.

If a Device B is operating on the maximum phase angle drift specifications, then the same Device B typically has:

5.8° + TBD°/°C (max spec) * (105°C – 25°C) = TBD° phase delay.

Device-to-Device Phase Angle Mismatch

Device-to-device phase angle mismatch measures the deviation of the phase delay of a single ADAQ7767-1 device relative to the average phase delay of a group of ADAQ7767-1 devices at a given input signal frequency. It shows how well the phase response of the data acquisition signal chain matches between channels. The typical specification is equal to ±1σ (standard deviation) of the distribution, while the maximum (or minimum) is six times this value.

For example, measuring the phase delay of a large number of devices with 20 kHz input using IN1, Device C has a phase delay on the minimum side of the distribution, which is (-) TBD° earlier than the average. Again, Device D has a phase delay on the maximum side of the distribution, which is (+) TBD° later than the average. The phase angle mismatch between Device C and Device D is:

+TBD° (max) – (-) TBD° (min) = TBD°

This is the worst-case phase angle mismatch between any two ADAQ7767-1 devices (using IN1, T_A = 25°C, 20 kHz input).

Device-to-Device Phase Angle Mismatch Drift

Device-to-device phase angle mismatch drift quantifies how much the device-to-device phase angle mismatch standard deviation (σ) widens/tightens across temperature at a given input signal frequency. A positive sign indicates a wider phase mismatch distribution as temperature increases, while a negative sign indicates a tighter phase mismatch distribution as temperature increases. This specification is calculated using the endpoint method over the full operating temperature range of -40°C and 105°C. The typical specification is the change in 1σ per °C, while the maximum is six times this value, as shown in Figure 72.

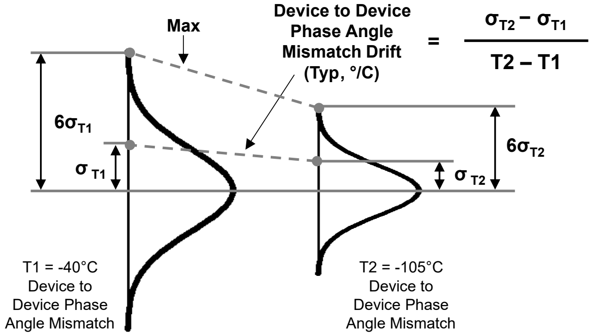


Figure 72. Device-to-Device Phase Angle Mismatch Drift Calculation

Measuring the device-to-device phase angle mismatch standard deviation (σ) of a large number of devices at 25°C with 20 kHz input using IN1, it is observed that the σ of the distribution is TBD°. To interpolate the standard deviation at another temperature:

$\sigma_{T2} = \sigma_{T1}$ + Device-to-Device Phase Angle Mismatch Drift * (T_2 – T_1)

Example. $\sigma_{-40°C}$ = TBD° + (TBD µ°/°C) * (-40°C – 25°C) = TBD°

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FDA POWER MODE

The ADAQ7767-1 Fully Differential Amplifier (FDA) is a low noise, low distortion amplifier that can drive high resolution and high performance ∑ - ∆ analog-to-digital converters (ADC).

The FDA two selectable power modes are Low Power Mode and Full Power Mode. The FDA Low Power Mode is ideal for DC input applications due to its low 1/f noise. The Full Power Mode offers better linearity performance at a higher current consumption.

Figure 73 shows the connection between M0_FDA, M1_FDA, and M0_ADC, M1_ADC. The connection sets the FDA to Full Power Mode. To set the FDA to Low Power Mode, the M0_FDA needs to be pulled to ground, while keeping the M1_FDA and M1_ADC connected as shown on Figure 74.

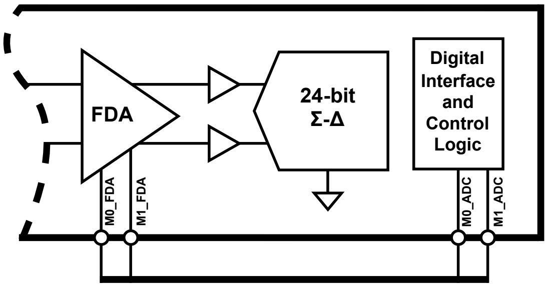

Figure 73. FDA Full Power Mode Connection

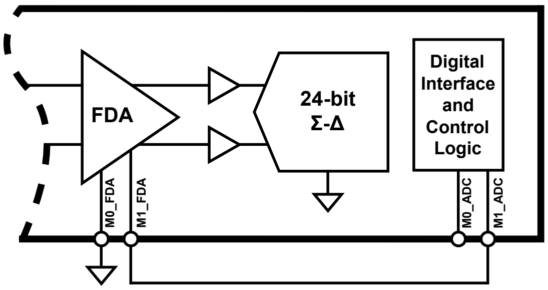

Figure 74. FDA Low Power Mode Connection

LINEARITY BOOST BUFFER

The ADAQ7767-1 has a pair of linearity boost buffers placed between the driver amplifier and core ADC. There is the option to turn them on to boost the linearity performance of the device. The linearity boost buffers add no noise to the signal chain performance and consume additional 2 mA typical current (as a pair) on the VDD_ADC supply.

The linearity boost buffers are enabled by default. Turn them off in the SPI control mode by setting the LINEARITY_BOOST_A_OFF and LINEARITY_BOOST_B_OFF Bits[1:0] in Analog Buffer Control Register (Register 0x16) to zero. The linearity buffers are always enabled in the $\overline{\text{PIN}}$ control mode.

REFERENCE INPUT AND BUFFERING

The ADAQ7767-1 has differential reference inputs, REF+ and REF−. The absolute input reference voltage range is from 1 V to VDD_ADC − AGND.

The reference inputs can be configured for a fully buffered input on each of the REF+ and REF− pins, a precharge buffered input, or to bypass both buffers.

Use of either the full buffers or the precharge buffers reduce the burden on the external reference when driving large loads or multiple devices. The fully buffered input to the reference pins provides a high-impedance input node and enables the use of the ADAQ7767-1 in ratiometric applications, where the ultra-low source impedance of a traditional external reference is not available.

In the $\overline{\text{PIN}}$ control mode, the reference precharge buffers are on by default. In the SPI mode, choose fully buffered or precharge buffers.

The reference input current scales linearly with the modulator clock rate.

For MCLK = 16.384 MHz in the fast mode, the reference input current is ~80 μA/V unbuffered and ~20 μA with the precharge buffers enabled.

With the precharge buffers off, REF+ = 5 V and REF− = 0 V.

REF± = 5 V × 80 μA/V = + 400 μA

With the precharge buffers on, REF+ = 5 V, and REF− = 0 V.

REF± = approximately 20 μA

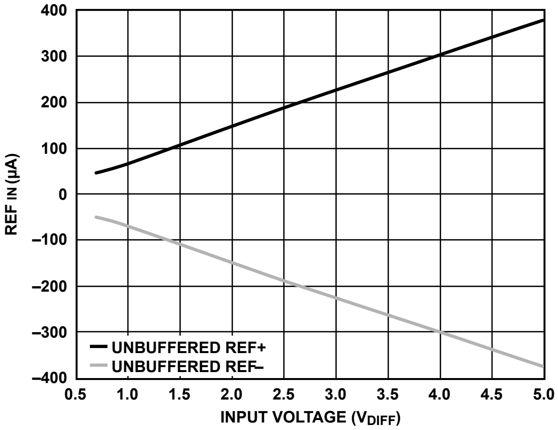

Figure 75. Reference Input Current (REF_{IN}) vs. Input Voltage, Unbuffered REF+ and REF−

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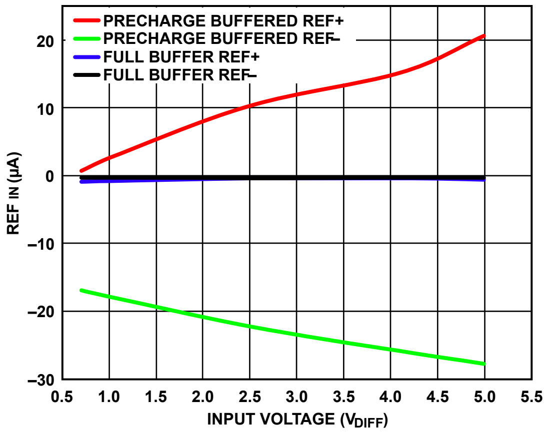

Figure 76. Reference Input Current (REF_{IN}) vs. Input Voltage, Precharge Buffered REF+ and REF− and Full Buffer REF+ and REF−

For the best performance and headroom, use a 4.096 V reference, such as the ADR444 or ADR4540, that can both be supplied by a 5 V rail and shared to the VDD_ADC supply.

A reference detect function is available in the SPI control mode. See the SPI Mode Diagnostic Features section for details.

CORE CONVERTER

The ADAQ7767-1 can use up to a 5 V reference and convert the differential voltage between any input pair to a digital output. The 24-bit conversion result is in MSB first, 2s complement format. Figure 77 shows the ideal transfer function, while Table 14 lists down some common input levels and their output code.

Use the following equation to convert from codes to volts, assuming the codes are first converted from 2s complement to straight binary:

$$Voltage = \frac{(Code - Midscale\ \ Code) \times 2 \times V_{REF}}{2^{24} \times AFE\_GAIN} \qquad (13)$$

where:

The Midscale Code is 0x800000 in straight binary, and 0x7FFFFF in Table 14 is converted to 0xFFFFFF in straight binary. Use the previous equation to calculate a voltage in the V_{REF} / AFE_GAIN range.

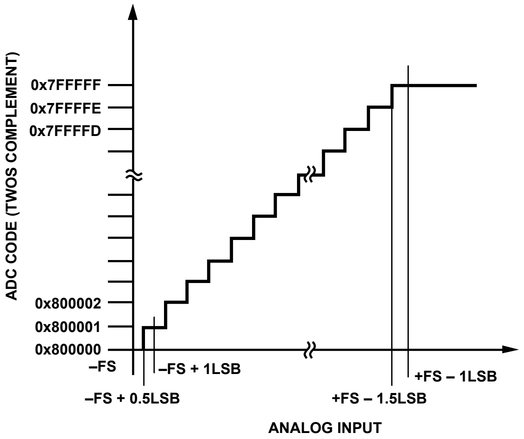

Figure 77. Ideal Transfer Function (FS is Full-Scale)

Table 14. Output Codes and Ideal Input Voltages

Description	Analog Input (V) IN1 AFE_GAIN = 1 IN2 AFE_GAIN = 4/11 IN3 AFE_GAIN = 1/7	Digital Output Code, 2s Complement (Hexadecimal)
FS − 1 LSB	$+V_{REF}$/AFE_GAIN*(1-1/2^{23})	0x7FFFFF
Midscale + 1 LSB	+VREF/AFE_GAIN/2^{23}	0x000001
Midscale	0	0x000000
Midscale − 1 LSB	-VREF/AFE_GAIN /2^{23}	0xFFFFFF
−FS + 1 LSB	-VREF/AFE_GAIN *(1-1/2^{23})	0x800001
−FS	-VREF/AFE_GAIN	0x800000

POWER SUPPLIES

ADAQ7767-1 has several power supply pins to power the ADC driver and ADC.

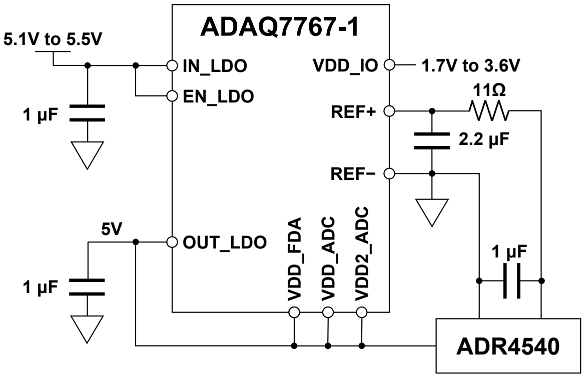

Figure 78. ADAQ7767-1 Power Supply Connection Using Internal LDO

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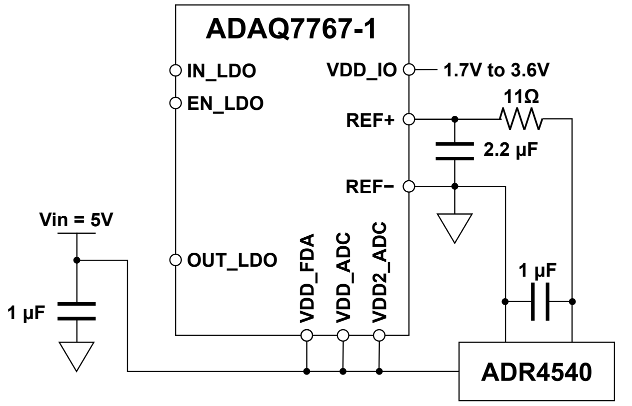

Figure 79. ADAQ7767-1 Power Supply Connection Using External 5V Supply

To simplify the connection, the internal LDO may be used with an input ranging from 5.1 V to 5.5 V to regulate an output of 5 V for the use of pins VDD_FDA, VDD_ADC, VDD2_ADC and the external reference like ADR4540, as shown in Figure 78. For proper operation, it is recommended to use a 1µF capacitor at the input and output of the LDO.Figure 79 illustrates the use of an external power supply for VDD_FDA, VDD_ADC, VDD2_ADC and the reference if the internal LDO is not preferred. In applications requiring less power consumption, VDD2_ADC can be separately supplied with a well-regulated power supply from 2 V to 5.5 V (2.5 V typical). With a typical current consumption of 4.7 mA, using a 2.5 V external LDO for VDD2_ADC typically conserves 11.75 mW compared to using the 5 V from the internal LDO or an external 5 V power supply.

The VDD_FDA supply powers the ADC driver.

The VDD_ADC supply powers the linearity boost buffer, core ADC front-end, and reference input.

The VDD2_ADC supply connects to an internal 1.8V analog LDO regulator. This regulator powers the ADC core. VDD2_ADC − AGND can range from 5.5 V (maximum) to 2.0 V (minimum).

VDD_IO powers the internal 1.8 V digital LDO regulator. This regulator powers the digital logic of the ADC. VDD_IO sets the voltage levels for the SPI interface of the ADC. VDD_IO is referenced to DGND, and VDD_IO − DGND can vary from 3.6 V (maximum) to 1.7 V (minimum).

POWER SUPPLY DECOUPLING

The ADAQ7767-1 has built-in 0.1uF supply decoupling capacitors on the VDD_FDA, VDD_ADC, VDD_ADC2, and VDD_IO supply pins. Externally, the ADC's own analog and digital LDOs should be decoupled to the ground with a 1uF capacitor through pins AREG_CAP and DREG_CAP.

Figure 80 shows the AC PSRR of the internal 5V LDO while it is connected to VDD_FDA, VDD_ADC, and VDD_ADC2 with their internal 0.1uF supply decoupling capacitors and the recommended 1uF external decoupling capacitor at the OUT_LDO pin, as shown in Figure 78. Figure 81 shows the AC PSRR of VDD_IO using its internal 0.1uF supply decoupling capacitor compared to having an additional 1uF external supply decoupling capacitor.

TBD

Figure 80. LDO AC PSRR, using internal decoupling capacitor of VDD_FDA, VDD_ADC, and VDD2_ADC

TBD

Figure 81. VDD_IO AC PSRR using internal decoupling capacitor and additional 1uF supply decoupling capacitor

POWER STANDBY

Each functional block of the ADAQ7767-1 can be put into standby mode. The device can achieve TBD W of total power consumption while all functional blocks are put into standby mode.

CLOCKING AND SAMPLING TREE

The ADAQ7767-1 core ADC receives a master clock signal (MCLK). The MCLK signal can be sourced from one of four options: a CMOS clock, a crystal connected between the XTAL1 and XTAL2 pins, an LVDS signal, and the internal clock. The MCLK signal received by the ADAQ7767-1 defines the core ADC's sigma delta

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modulator clock rate (f_{MOD}) and, in turn, the sampling frequency of the modulator of 2 × f_{MOD}.

$$f_{MOD} = \frac{MCLK}{MCLK\_DIV} \quad (14)$$

To determine f_{MOD}, select and set one of four clock divider settings: MCLK/2, MCLK/4, MCLK/8, or MCLK/16 from the MCLK_DIV bits[5:4] of the Power and Clock Control Register. For example, to maximize the ODR or input bandwidth, an MCLK rate of 16.384 MHz is required. Select an MCLK divider (MCLK_DIV) equal to 2 for a modulator frequency of 8.192 MHz.

Control of the settings for the modulator frequency differ in $\overline{\text{PIN}}$ control mode vs. SPI control mode.

In SPI control mode, the user can program the power mode and MCLK_DIV independently. Independent selection of the power mode and MCLK_DIV allows full freedom in the MCLK speed selection to achieve a target modulator frequency, which can also result in a small power saving. For example, if the power mode is low power, it is more power efficient to use MCLK = 2.048 MHz with MCLK_DIV = 2 than MCLK = 16.384 MHz with MCLK_DIV = 16. Both options are valid selections and result in an f_{MOD} frequency of 1.024 MHz. Table 15 gives a recommendation on setting the ADC power mode with respect to the f_{MOD} frequency.

Table 15. Recommended f_{MOD} Range for Each ADC Power Mode

Power Mode	Recommended f_{MOD} Range (MHz)
Low	0.038 to 1.024
Median	1.024 to 4.096
Fast	4.096 to 8.192

In $\overline{\text{PIN}}$ control mode, the MODEx pins determine the modulator frequency (see Table 25). The MODEx pins are also used to select the filter type and decimation rate.

It is recommended to keep the f_{MOD} frequency high to maximize the out of band tone rejection from the frontend anti-aliasing filter. Increase the decimation rate if low input bandwidth is required.

Power vs. Noise Performance Optimization

Depending on the bandwidth of interest for the measurement, the user can choose a strategy of either lowest current consumption or highest resolution. This choice is due to an overlap in the coverage of each power mode. There are different ways to achieve the same ODR. Using a lower MCLK frequency in tandem with a lower decimation rate allows the user to achieve the same data rate as using a higher MCLK frequency with a higher decimation. Lower power can be achieved by using lower modulator clock frequencies. Conversely, to achieve the highest resolution, use higher modulator clock frequencies and maximize the amount of oversampling.

CLOCKING AND CLOCK SELECTION

The ADAQ7767-1 has an internal oscillator that is used for initial power-up of the device. After the ADAQ7767-1 completes the start-up routine, a clock handover occurs to the external MCLK. The ADAQ7767-1 counts the falling edges of the external MCLK over a given number of internal clock cycles to determine if the clock is valid and of a frequency of at least 600 kHz. If there is a fault with the external MCLK, the handover does not occur, the ADAQ7767-1 clock error bit is set, and the ADAQ7767-1 continues to operate from the internal clock.

In SPI control mode, use the clock source bits in Register 0x15 to set the external MCLK source. Four clock options are available: internal oscillator, external CMOS, crystal oscillator, or LVDS. If selecting the LVDS clock option, the clock source must be selected using the CLOCK_SEL bits [7:6] in Power and Clock Control Register.

In $\overline{\text{PIN}}$ control mode, the CLK_SEL pin sets the external MCLK source. Three clock options are available in $\overline{\text{PIN}}$ control mode: an internal oscillator, an external CMOS, or a crystal oscillator. The CLK_SEL pin is sampled on power-up.

For both $\overline{\text{PIN}}$ and SPI mode, it is suggested to reset the device whenever the clock source is changed.

Set the EN_ERR_EXT_CLK_QUAL bit (Bit 0 in SPI Mode Diagnostic Features) to turn off the clock qualification. Turning off the clock qualification allows the use of slower external MCLK rates outside the recommended MCLK frequency.

CLK_SEL Pin

If CLK_SEL = 0 in $\overline{\text{PIN}}$ control mode, the CMOS clock option is selected and must be applied to the MCLK pin. In this case, tie the XTAL1 pin to DGND. The connection is illustrated in Figure 82.

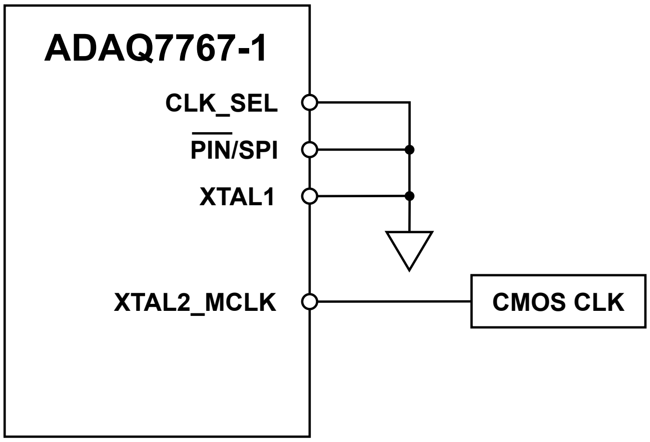

Figure 82. PIN Mode using external CMOS Clock as MCLK

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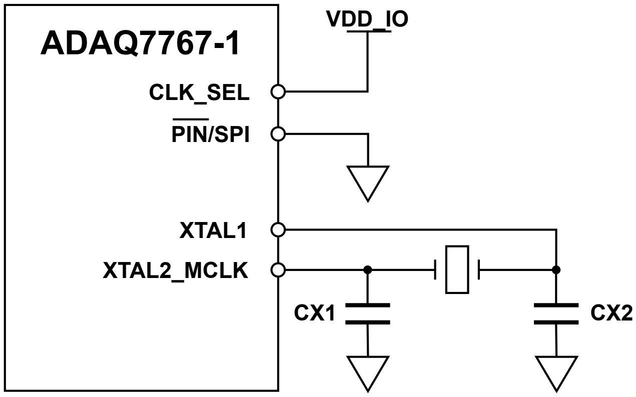

Figure 83. PIN Mode using external crystal as MCLK

If CLK_SEL = 1 in PIN control mode, the crystal option is selected and must be connected between the XTAL1 and XTAL2 pins, as shown in Figure 83. CX1 and CX2 are capacitors connected from each terminal of the crystal to DGND for circuit tuning. The values for these capacitors depend on the length and capacitance of the trace connections between the crystal and the XTAL1 and XTAL2_MCLK pins.

In SPI control mode, the CLK_SEL pin does not determine the MCLK source used and CLK_SEL must be tied to DGND.

Using the Internal Oscillator

In some cases, conversion using an internal clock oscillator may be preferred, such as in isolated applications where dc input voltages must be measured. Converting ac signals with the internal clock is not recommended because using the internal clock can result in degradation of SNR due to jitter.

DIGITAL FILTERING

The ADAQ7767-1 offers three types of digital filters. The digital filters available on the ADAQ7767-1 are

- Wideband low ripple FIR filter, −3 dB at 0.433 × ODR (6 rates in SPI Control Mode)
- Sinc5 low latency filter, −3 dB at 0.204 × ODR (8 rates in SPI Control Mode)
- Sinc3 low latency filter, –3 dB at 0.2617 × ODR, widely programmable data rate in SPI Control Mode

Decimation Rate Control

The ADAQ7767-1 has programmable decimation rates for the sinc and wideband low ripple FIR digital filters, as shown in Table 16. The decimation rates allow the user to band limit the measurement, which reduces the speed and input bandwidth, but increases the resolution because there is further averaging in the digital filter. Control of the decimation rate on the ADAQ7767-1 when using the SPI control is set in the Digital Filter and Decimation Control Register for the sinc5 and wideband low ripple FIR filters.

The decimation rate of the sinc3 filter is controlled using the SINC3 Decimation Rate (LSB) Register and the SINC3 Decimation Rate (MSB) Register. These registers combine to provide 13 bits of programmability. The decimation rate is set by incrementing the value in these registers by one and multiplying the value by 32. For example, setting a value of 0x5 in the SINC3 Decimation Rate (LSB) Register results in a decimation rate of 192 for the sinc3 filter.

In PIN control mode, the MODE0 pin controls the decimation ratio. Only decimation rates of ×32 and ×64 are available for use with the sinc5 and wideband filter options. See Table 25 for the full list of options available in PIN control mode.

Table 16. Decimation Rate Options

	Available Decimation Rates	
Filter Option	**SPI Control Mode**	**Pin Control Mode**
Wideband Low Ripple FIR	×32, ×64, ×128, ×256, ×512, ×1024	×32, ×64
Sinc5	×8, ×16, ×32, ×64, ×128, ×256, ×512, ×1024	×8, ×32, ×64
Sinc3	Programmable decimation rate	50 Hz and 60 Hz output only, based on a 16.384 MHz MCLK

Wideband Low Ripple FIR Filter

The FIR filter is a low ripple, input passband up to 0.433 × ODR. The wideband low ripple FIR filter has almost full attenuation of 105 dB at 0.5 × ODR (Nyquist), maximizing anti-alias protection. The frequency response of the wideband low ripple FIR filter is shown in Figure 84. The wideband low ripple FIR filter has a pass-band ripple of ±0.005 dB, shown in Figure 85, and a stop band attenuation of 105 dB. The wideband low ripple FIR filter is a 64-order digital filter. The group delay of the filter is 34/ODR. After a sync pulse, there is an additional delay from the SYNC_IN rising edge to fully settled data. The time from a SYNC_IN pulse to both the first DRDY and to fully settled data for various ODR values is shown in Table 17.

The wideband low ripple FIR filter can be selected in one of six different decimation rates, allowing the user to choose the optimal input bandwidth and speed of the conversion vs. the desired resolution.

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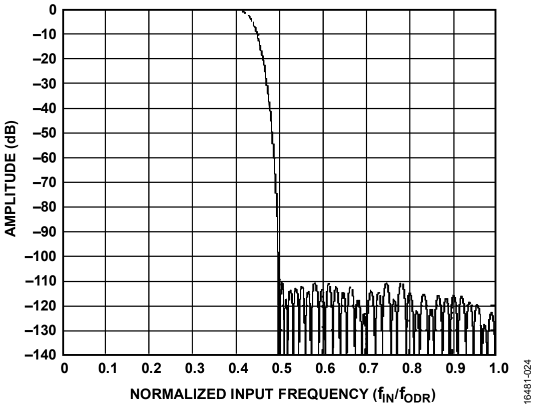

Figure 84. Wideband Low Ripple FIR Filter Frequency Response

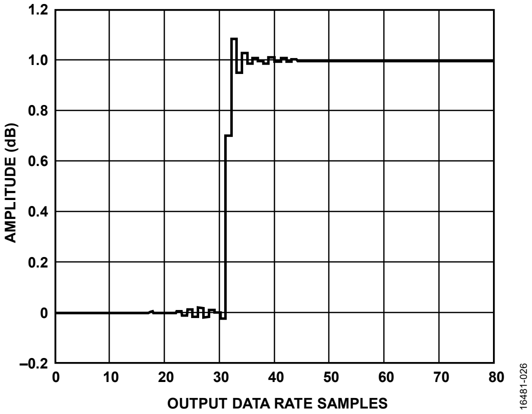

Figure 86. Wideband Low Ripple FIR Filter Step Response

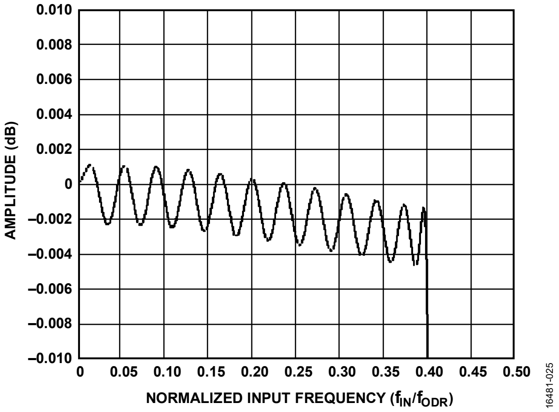

Figure 85. Wideband Low Ripple FIR Filter Pass-Band Ripple

Table 17. Wideband Low Ripple FIR Filter $\overline{\text{SYNC\_IN}}$ to Settled Data

		ODR (kSPS)		MCLK Periods	
MCLK Divide Setting	Decimation Rate	MCLK = 16.384MHz	MCLK = 13.107MHz	Delay from First MCLK Rise After $\overline{\text{SYNC\_IN}}$ Rise to First $\overline{\text{DRDY}}$ Rise	Delay from First MCLK Rise After $\overline{\text{SYNC\_IN}}$ Rise to Earliest Settled $\overline{\text{DRDY}}$ Rise
MCLK/2	32	256	204.8	284	4,252
	64	128	102.4	413	8,349
	128	64	51.2	797	16,669
	256	32	25.6	1,565	33,309
	512	16	12.8	3,101	66,589
	1024	8	6.4	6,157	133,133
MCLK/4	32	128	102.4	428	8,364
	64	64	51.2	812	16,684
	128	32	25.6	1,580	33,324
	256	16	12.8	3,116	66,604
	512	8	6.4	6,188	133,164
	1024	4	3.2	12,300	266,252
MCLK/16	32	32	25.6	1,674	33,418
	64	16	12.8	3,202	66,690
	128	8	6.4	6,274	133,250

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Table 17. Wideband Low Ripple FIR Filter SYNC_IN to Settled Data (Continued)

		ODR (kSPS)		MCLK Periods	
MCLK Divide Setting	**Decimation Rate**	**MCLK = 16.384MHz**	**MCLK = 13.107MHz**	**Delay from First MCLK Rise After SYNC_IN Rise to First DRDY Rise**	**Delay from First MCLK Rise After SYNC_IN Rise to Earliest Settled DRDY Rise**
	256	4	3.2	12,418	266,370
	512	2	1.6	24,706	532,610
	1024	1	0.8	49,154	1,064,962

Sinc5 Filter

The sinc5 filter offered in the ADAQ7767-1 enables a low latency signal path useful for dc inputs on control loops, or for where user specific post processing is required. The sinc5 filter has a −3 dB bandwidth of 0.204 × ODR.

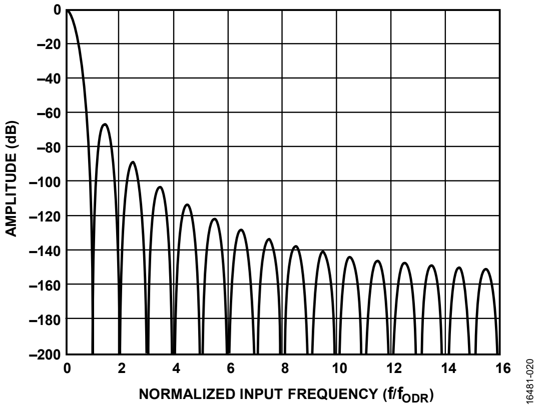

Figure 87. Sinc5 Filter Frequency Response

The impulse response of the filter is five times 1/ODR. For 250 kSPS ODR, the time to settle data fully is 20 µs. For the 1.024 MSPS ODR, the time to settle data fully is 5 µs.

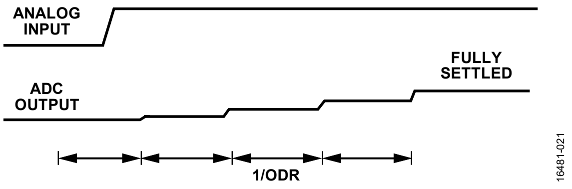

Figure 88. Sinc5 Filter Step Response

The time from a SYNC_IN pulse to both the first DRDY and to fully settled data for various ODR values for the sinc5 filter is shown in Table 18.

Table 18. Sinc5 Filter, SYNC_IN to Settled Data

		ODR (kSPS)		MCLK Periods	
MCLK Divide Setting	**Decimation Rate**	**MCLK = 16.384MHz**	**MCLK = 13.107MHz**	**Delay from First MCLK Rise After SYNC_IN Rise to First DRDY Rise**	**Delay from First MCLK Rise After SYNC_IN Rise to Earliest Settled DRDY Rise**
MCLK/2	8	1024	819.2	46	110
	16	512	409.6	62	190
	32	256	204.8	94	350
	64	128	102.4	162	674
	128	64	51.2	295	1,319
	256	32	25.6	561	2,609
	512	16	12.8	1,093	5,189
	1024	8	6.4	2,173	10,365
MCLK/4	8	512	409.6	79	207
	16	256	204.8	111	367
	32	128	102.4	175	687
	64	64	51.2	310	1,334
	128	32	25.6	576	2,624
	256	16	12.8	1,108	5,204
	512	8	6.4	2,172	10,364
	1024	4	3.2	4,332	20,716

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Table 18. Sinc5 Filter, SYNC_IN to Settled Data (Continued)

		ODR (kSPS)		MCLK Periods	
MCLK Divide Setting	**Decimation Rate**	**MCLK = 16.384MHz**	**MCLK = 13.107MHz**	**Delay from First MCLK Rise After SYNC_IN Rise to First DRDY Rise**	**Delay from First MCLK Rise After SYNC_IN Rise to Earliest Settled DRDY Rise**
MCLK/16	8	128	102.4	278	790
	16	64	51.2	406	1,430
	32	32	25.6	662	2,710
	64	16	12.8	1,194	5,290
	128	8	6.4	2,258	10,450
	256	4	3.2	4,386	20,770
	512	2	1.6	8,642	41,410
	1024	1	0.8	17,282	82,818

Programming for 1.024MSPS Output Data Rate

A 1.024MSPS sinc5 filter path exists for users seeking an even higher ODR than is achievable using the Wideband Low Ripple FIR filter. This path is quantization noise limited. Therefore, it is best suited for customers requiring minimum latency for control loops or implementing custom digital filtering on an external field programmable gate array (FPGA) or digital signal processor (DSP).

To configure the Sinc5 FIR filter for 1.024MSPS output data rate, write 001 to FILTER bits [6:4] of Digital Filter and Decimation Control Register. The ADAQ7767-1 automatically changes the decimation rate to 8 and output data length is reduced to 16 bits from 24 bits due to the maximum speed limitation of digital serial interface.

For example, to program the ADAQ7767-1 to 1.024MSPS output data rate from power up using 16.384MHz MCLK, while using the CMOS_MCLK as the clock source, the subsequent SPI writes below can be used.

- Data 0x33 to Register 0x15
- Data 0x10 to Register 0x19

Sinc3 Filter

The sinc3 filter offered in the ADAQ7767-1 enables a low latency signal path useful for dc inputs on control loops, or for eliminating unwanted known interferers at specific frequencies. The sinc3 filter path incorporates a programmable decimation rate to achieve rejection of known interferers. Decimation rates from 32 to 185,280 are achievable using the sinc3 filter. The sinc3 filter has a −3 dB bandwidth of 0.2617 × ODR.

For example, to calculate for a 16.384 MHz MCLK to achieve an ODR of 50 SPS using the sinc3 filter, use the following equation:

$$ODR = \frac{MCLK}{MCLK\_DIV \times DEC\_RATE} \tag{15}$$

Assuming the ADAQ7767-1 is using, MCLK_DIV = 2,

$$DEC\_RATE = \frac{MCLK}{MCLK\_DIV \times ODR} \tag{16}$$

Decimation Rate = 163,840

The SINC3_DECIMATION_RATE registers (Register 0x1A and Register 0x1B) increments the value in the registers by one and then multiplies it by 32 to give the actual decimation rate. To set the decimation rate to 163,840, simply follow the equation:

$$Value = \frac{DEC\_RATE}{32} - 1 \tag{17}$$

The value to be written to the sinc3 decimation registers is 5119.

Table 19 and Table 20 lists the values to be written to the sinc3 decimation registers to achieve an ODR of 50 SPS and 60 SPS, respectively, for various MCLK and MCLK_DIV.

Table 19. Sinc3 Decimation Register Values for 50 SPS ODR Using Various MCLK and MCLK_DIV

MCLK(MHz)	MCLK_DIV	Decimation Rate	Value in DEC_RATE register
16.384	2	163840	5119
	4	81920	2559
	8	40960	1279
	16	20480	639
13.1072	2	131072	4095
	4	65536	2047
	8	32768	1023
	16	16384	511

Table 20. Sinc3 Decimation Register Values for 60 SPS ODR Using Various MCLK and MCLK_DIV

MCLK (MHz)	MCLK_DIV	Decimation Rate	Value in DEC_RATE register
16.384	2	136533	4266
	4	68267	2132
	8	34133	1066
	16	17067	532
13.1072	2	109227	3412
	4	54613	1706
	8	27307	852
	16	13653	426

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Programming for 50 Hz, 60 Hz, and 50 Hz and 60 Hz Rejection

To reject 50 Hz tones, program the ODR of the sinc3 filter to 50 Hz (see Figure 89). It is also possible to achieve simultaneous rejection of both 50 Hz and 60 Hz by setting Bit 7 in the Digital Filter and Decimation Control Register. Rejection of both 50 Hz and 60 Hz line frequencies is possible in this configuration. Table 21 and Table 22 show the minimum rejection measured at the frequencies of interest with a 50 SPS ODR.

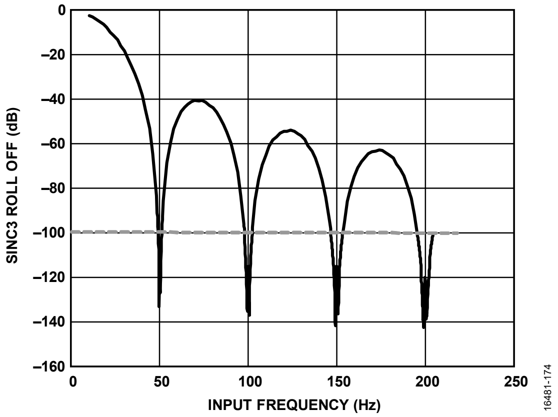

Figure 89. Sinc3 Filter Frequency Response Showing 50 Hz Rejection, 50 Hz ODR, ×163,840 Decimation

Table 21. Sinc3 Filter 50 Hz Rejection, 50 Hz ODR and Decimate by 163,840

Frequency Band (Hz)	Minimum Measured Rejection (dB)
50 ± 1	101
100 ± 2	102
150 ± 3	102
200 ± 4	102

Table 22. Sinc3 Filter 50 Hz and 60 Hz Rejection, 50 Hz ODR and Decimate by 163,840

Frequency Band (Hz)	Minimum Measured Rejection (dB)
50 ± 1	81
60 ± 1	67
100 ± 2	83
120 ± 2	72
150 ± 3	86
180 ± 3	78
200 ± 4	90
240 ± 4	87

The impulse response of the filter is three times 1/ODR. For 250 kSPS ODR, the time to settle data fully is 12 µs.

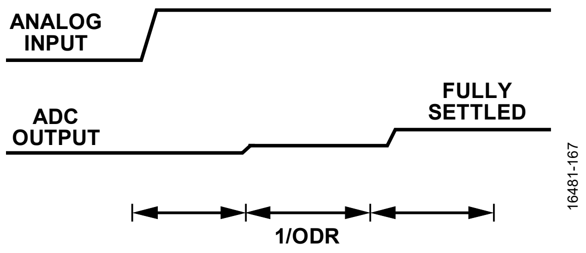

Figure 90. Sinc3 Filter Step Response

Table 23. Sinc3 Filter, $\overline{\text{SYNC\_IN}}$ to Settled Data

			ODR (kSPS)		MCLK Periods	
MCLK Divide Setting	Decimation Rate	Value in DEC_RATE register	MCLK = 16.384MHz	MCLK = 13.107MHz	Delay from First MCLK Rise After $\overline{\text{SYNC\_IN}}$ Rise to First $\overline{\text{DRDY}}$ Rise	Delay from First MCLK Rise After $\overline{\text{SYNC\_IN}}$ Rise to Earliest Settled $\overline{\text{DRDY}}$ Rise
MCLK/2	32	0	256	204.8	127	255
	64	1	128	102.4	191	447
	128	3	64	51.2	319	831
	256	7	32	25.6	575	1,599
	512	15	16	12.8	1,087	3,135
	1024	31	8	6.4	2,111	6,207
	163,840	5119	0.05	0.04	327,743	983,103
MCLK/4	32	0	128	102.4	241	497
	64	1	64	51.2	369	881
	128	3	32	25.6	625	1,649
	256	7	16	12.8	1,137	3,185
	512	15	8	6.4	2,161	6,257
	1024	31	4	3.2	4,209	12,401
	81,920	2559	0.05	0.04	327,793	983,153
MCLK/16	32	0	32	25.6	926	1,950
	64	1	16	12.8	1,438	3,486

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Table 23. Sinc3 Filter, SYNC_IN to Settled Data (Continued)

			ODR (kSPS)		MCLK Periods	
MCLK Divide Setting	Decimation Rate	Value in DEC_RATE register	MCLK = 16.384MHz	MCLK = 13.107MHz	Delay from First MCLK Rise After SYNC_IN Rise to First DRDY Rise	Delay from First MCLK Rise After SYNC_IN Rise to Earliest Settled DRDY Rise
	128	3	8	6.4	2,462	6,558
	256	7	4	3.2	4,510	12,702
	512	15	2	1.6	8,606	24,990
	1024	31	1	0.8	16,798	49,566
	20,480	639	0.05	0.04	328,094	983,454

ADC SPEED AND PERFORMANCE

The ADAQ7767-1 offers a wide selection of ODR depending on the digital filter used. The ADAQ7767-1 can have an ODR as low as 1 kSPS using the wideband low ripple FIR filter and Sinc5 filter, and 0.0125 kSPS using the Sinc3 filter. This can be achieved using a high decimation ratio and operating the modulator at the lowest possible sampling rate. For example, with the wideband low ripple FIR filter option, 1 kSPS ODR can be achieved using MCLK = 16.384 MHz, decimation rate = 1024, and f_{MOD} = MCLK / 16.

Note that the ADAQ7767-1 modulator samples on the rising and falling edge of the f_{MOD} and outputs data to the digital filter at a rate of f_{MOD}. There is a zero in the frequency response profile of the modulator centered at the odd multiples of f_{MOD}, which means there is no foldback from frequencies at the f_{MOD} rate and at odd multiple rates. However, the modulator is open to noise for even multiples of f_{MOD}. There is no attenuation at these zones.

For optimum performance, it is recommended to use MCLK = 16.384 MHz and MCLK_DIV = 2. This sets the f_{MOD} = 8.192 MHz, and by keeping the f_{MOD} frequency high, it maximizes the out-of-band tone rejection from the front-end anti-aliasing filter.

The default controller clock divider setting for the ADAQ7767-1 is MCLK_DIV = 16. To configure the MCLK divider to MCLK = 2, write 11 to MCLK_DIV bits [5:4] of the Power and Clock Control Register (Register 0x15) after power up.

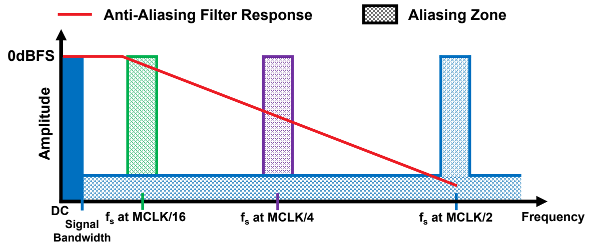

Figure 91. Anti-Alias Filter Response versus MCLK Divider

Figure 91 shows the AAF rejection relative to the sampling frequency. Using higher MCLK divider results in lower sampling frequency with reduced rejection from the anti-alias filter.

DEVICE CONFIGURATION METHOD

The ADAQ7767-1 has two options for controlling device functionality. On power-up, the mode is determined by the state of the PIN/SPI pin. The two modes of configuration are

- SPI: over a 3- or 4-wire SPI interface (complete configurability)
- PIN: pin strapped digital logic inputs (a subset of complete configurability)

On power-up, the user must apply a soft or hard reset to the device when using either control mode. A SYNC_IN pulse is also recommended after the reset or after any change to the device configuration. Choose between controlling and configuring over the SPI or via pin connections only.

The first design decision is setting the ADC in either the SPI or PIN mode of configuration. In either mode, the digital host reads the ADC data over the SPI port lines.

PIN Control Mode

An overview of the PIN control mode features is as follows:

- No SPI write access to the device.
- Pins control all functions.
- ADC results read back over the SPI pins.
- ADC result includes an 8-bit status header output after each conversion result.
- SDI pin can be used to create a daisy chain of multiple devices operating in PIN mode.

SPI Control Mode

An overview of the SPI control mode features is as follows:

- Standard SPI Mode 3 interface for register access, where the ADC always behaves as an SPI slave.
- Indication of a new conversion via the DRDY pin output.

  A second method allows the user to merge the ready signal within the DOUT output stream, which allows a reduction in the number of lines across an isolation barrier.
- Reading back conversions can be performed by writing 8 bits to address the ADC register and reading back the result from the register.

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- Continuous readback mode, which is enabled via an SPI write. There is no need to supply the 8 bits to address the Conversion result Register (ADC_DATA, Register 0x2C). Data readback occurs on the application of SCLK. The DRDY pin indicates that a conversion result is complete and can be used to trigger a readback of the conversion result.
- In continuous read back mode, there is the option to append either the 8-bit status header or an 8-bit CRC check, or both.

PIN CONTROL MODE OVERVIEW

PIN control mode eliminates the need for SPI communication to set the required mode of operation. It is best used for situations where the user requires a single, known configuration, to reduce routing signals to the digital host. PIN control mode is useful in digitally isolated applications where minimal configuration is needed. PIN control mode offers a subset of the core functionality and ensures a known state of operation after power-up, reset, or a fault condition on the power supply. In PIN control mode, the linearity boost buffers and the reference input precharge buffers are enabled by default for best performance.

An automatic sync pulse drives out on the SYNC_OUT pin in PIN control mode when the device is either initially powered up or after a reset. A SYNC_OUT pulse also occurs when a GPIOx pin toggles, meaning after a change to the PIN control mode settings of the device, the synchronization is automatically performed. For this synchronization to work, tie SYNC_OUT to SYNC_IN, eliminating the need to provide a synchronous SYNC_IN pulse. The SYNC_OUT of one device can also be tied to the SYNC_IN of many devices when the synchronization of multiple devices is required. If synchronization of multiple devices is required, all devices must share a common MCLK.

Data Output Format

PIN control mode has a set output format for conversion data. The rising DRDY edge indicates that a new conversion is ready. The next 24 serial clock falling edges clock out the 24-bit ADC result. The following eight serial clocks output the status bits of the ADAQ7767-1. The ADC data is output MSB first in twos complement format. If further SCLK falling edges are applied to the ADC after clocking out the status bits, the logic level applied to SDI is clocked out, similar to a daisy-chain scenario. In Figure 92, an extra serial clock edge (33rd falling edge) is shown. If an extra serial clock edge occurs, the logic level of the SDI pin clocks out.

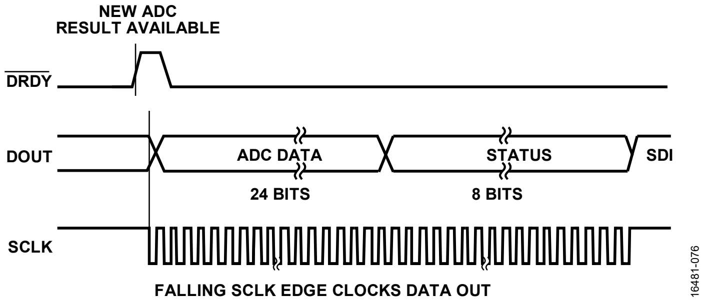

Figure 92. PIN Mode Data Output Format (This Figure Does Not Show the CS Signal)

Table 24. Differences in Control and Interface Pin Functions in PIN Control Mode and SPI Control Mode

	Pin Function	
Mnemonic	**PIN Control Mode**	**SPI Control Mode**
MODE0/GPIO0	MODE0 configuration pin	GPIO0 pin
MODE1/GPIO1	MODE1 configuration pin	GPIO1 pin
MODE2/GPIO2	MODE2 configuration pin	GPIO2 pin
MODE3/GPIO3	MODE3 configuration pin	GPIO3 pin
CS	SPI pin for readback of ADC conversion results	SPI interface for full configuration of the ADAQ7767-1 via a register read/write and readback of the ADC conversion results
SCLK	SPI pin for readback of ADC conversion results	SPI interface for full configuration of the ADAQ7767-1 via a register read/write and readback of the ADC conversion results
SDI	SPI pin for readback of ADC conversion results	SPI interface for full configuration of the ADAQ7767-1 via a register read/write and readback of the ADC conversion results
DOUT/RDY	SPI pin for readback of ADC conversion results	SPI interface for full configuration of the ADAQ7767-1 via a register read/write and readback of the ADC conversion results

Diagnostics and Status Bits

PIN control mode offers a subset of diagnostics features. Internal errors are reported in the status header output with the data conversion results for each channel.

The status header reports the internal CRC errors, memory map flipped bits, and the undetected external clock, indicating a reset is required. The status header also reports filter settled and filter saturated signals. Users can determine when to ignore data by monitoring these error flags.

If a significant error shows in the status bits, a reset of the ADC using RESET pin is recommended because, in PIN mode, there is no way to interrogate further for specific errors.

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Daisy-Chaining—PIN Control Mode Only

Daisy-chaining devices allows multiple devices to use the same data interface lines by cascading the outputs of multiple ADCs from separate ADAQ7767-1 devices. Daisy-chaining devices is only possible in PIN control mode.

When configured for daisy-chaining, only one ADAQ7767-1 device has its data interface in direct connection with the digital host. For the ADAQ7767-1 cascading the DOUT/RDY pin of the upstream ADAQ7767-1 device to the SDI pin of the next downstream ADAQ7767-1 device in the chain implements this daisy-chaining. The ability to daisy-chain devices and the limit on the number of devices that can be handled by the chain is dependent on the serial clock frequency used and the time available to clock through multiple 32-bit conversion outputs (24-bit conversion + 8-bit status) before the next conversion is complete.

The daisy-chaining feature is useful to reduce component count and to wire connections to the controller.

Figure 93 shows an example of daisy-chaining multiple ADAQ7767-1 devices.

The daisy-chain scheme depends on all devices receiving the same MCLK and SCLK, being synchronized, and being configured with the same decimation rate. The chip select signal (CS) gates each conversion chain of data, its rising edge resetting the SPI to a known state after each conversion ripples through. The ADAQ7767-1 device that is furthest from the controller must have its SDI pin tied to VDD_IO, logic high.

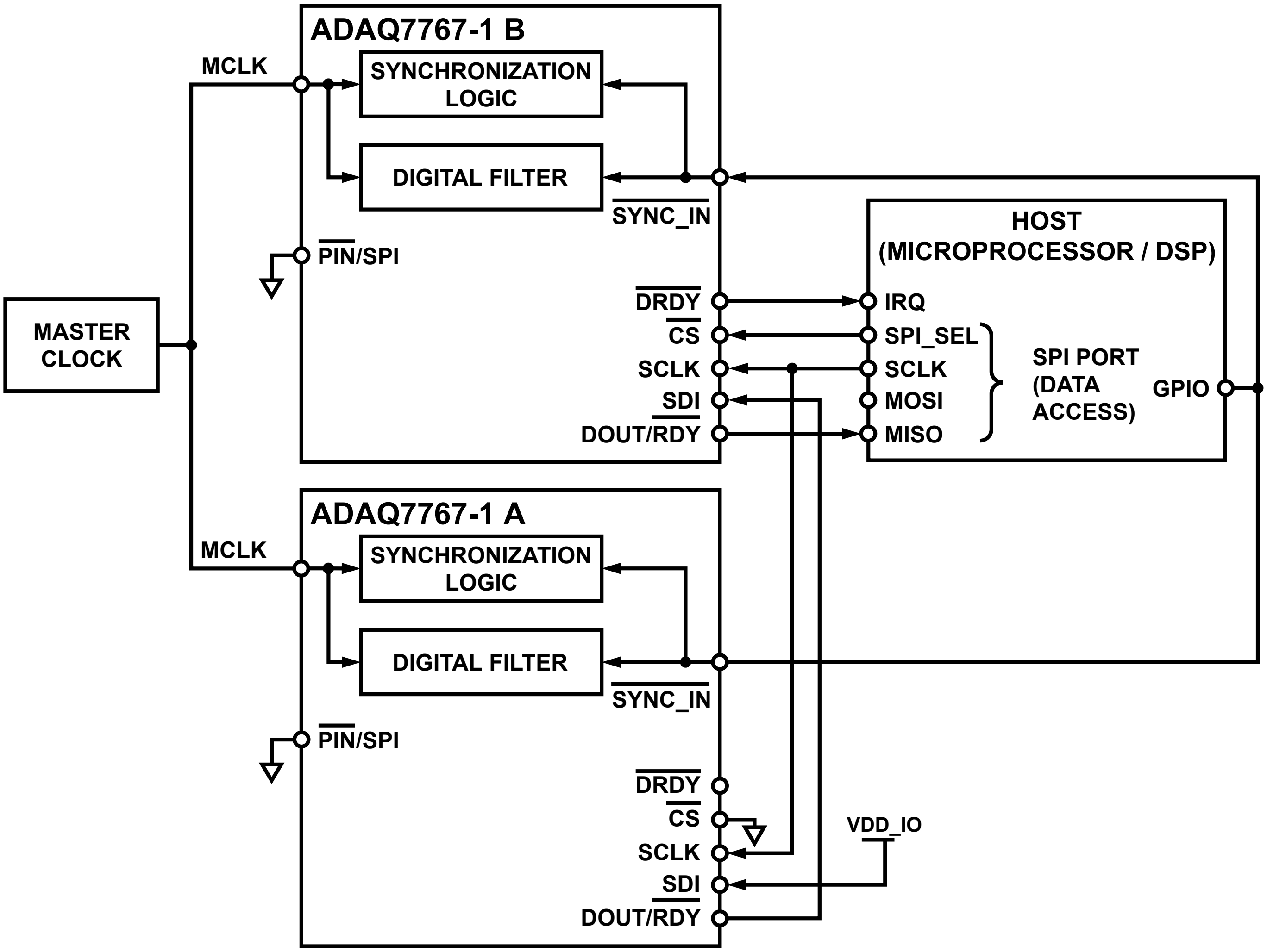

Figure 93. Daisy-Chaining Multiple ADAQ7767-1 Devices

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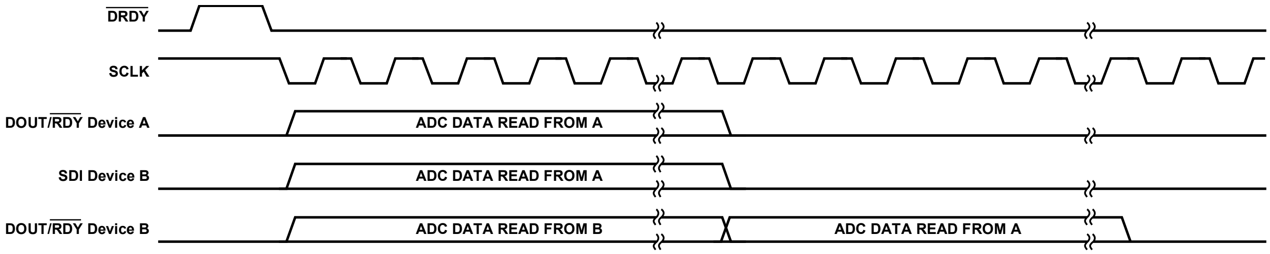

Figure 94. Data Output Format When Devices Daisy-Chained (PIN Control Mode Only)

Table 25. PIN Control Settings for MODEx Pins

MODEx Pin Settings					ADC Configuration			MCLK = 16.384 MHz
MODEx (Hex)	**MODE3/ GPIO3**	**MODE2/ GPIO2**	**MODE1/ GPIO1**	**MODE0/ GPIO0**	**f_{MOD} Frequency**	**Filter**	**Decimation**	**ODR**
0	0	0	0	0	MCLK/2	Wideband low ripple FIR	×32	256 kHz
1	0	0	0	1	MCLK/2	Wideband low ripple FIR	×64	128 kHz
2	0	0	1	0	MCLK/2	Sinc5	×32	256 kHz
3	0	0	1	1	MCLK/2	Sinc5	×64	128 kHz
4	0	1	0	0	MCLK/4	Wideband low ripple FIR	×32	128 kHz
5	0	1	0	1	MCLK/4	Wideband low ripple FIR	×64	64 kHz
6	0	1	1	0	MCLK/4	Sinc5	×32	128 kHz
7	0	1	1	1	MCLK/4	Sinc5	×64	64 kHz
8	1	0	0	0	MCLK/16	Wideband low ripple FIR	×32	32 kHz
9	1	0	0	1	MCLK/16	Wideband low ripple FIR	×64	16 kHz
A	1	0	1	0	MCLK/16	Sinc5	×32	32 kHz
B	1	0	1	1	MCLK/16	Sinc5	×64	16 kHz
C	1	1	0	0	MCLK/2	Sinc5	×8	1 MHz
D	1	1	0	1	MCLK/2	Sinc3 50 Hz and 60 Hz rejection[1]	×163,840	50 Hz
E	1	1	1	0	MCLK/16	Sinc3 50 Hz and 60 Hz rejection[1]	×20,480	50 Hz
F	1	1	1	1	ADC Standby			

[1] Sinc3 filter, rejection of 50 Hz and 60 Hz. Rejection of 50 Hz and 60 Hz is possible only if the MCLK applied in control mode is equal to 16.384 MHz. The decimation rate is tuned internally for these pin mode settings so that the sinc filter notches fall at 50 Hz and 60 Hz.

SPI CONTROL OVERVIEW

SPI control offers a superset of flexibility and diagnostics to the user. The categories described in Table 26 define the major controls, conversion modes, and diagnostic monitoring abilities enabled in SPI control mode.

Table 26. SPI Control Capabilities

SPI Control	Capabilities	Meaning for the User
MCLK Division	MCLK/2 to MCLK/16	The ability to customize clock frequency relating to the bandwidth of interest.
MCLK Source	CMOS, crystal, LVDS, and internal clock	Allows the user a distributed or local clock capability.
Digital Filter Style	Wideband Low Ripple FIR, Sinc5, Sinc3 (programmable)	The ability to customize the latency and frequency response to the measurement target of the user and its bandwidth.
Interface Format	Bit length	The ability to change between a 24-bit and a 16-bit conversion length in continuous read mode.
	Status bits	The ability to view output device status bits with the ADC conversion results.
	CRC	The ability to implement error checking when transmitting data.

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Table 26. SPI Control Capabilities (Continued)

SPI Control	Capabilities	Meaning for the User
	Data streaming	The ability to stream conversion data, eliminating interface write overhead.
Analog Buffers	Linearity boost buffer	Boost the linearity performance.
	Reference input precharge	Reduces reference input current, making it easier to filter the reference.
	Reference input full buffer	This full high impedance buffer enables filtering of reference source and enables high impedance sources, that is, reference resistors.
Conversion Modes	Single conversion	The ability to return to standby after one conversion.
	One shot	The ability to perform a conversion similar to a timed successive approximation register (SAR) conversion, in which the ADAQ7767-1 converts on a timed pulse.
	Continuous conversion	Normal operation keeps the modulator continually converting, offering the fastest response to a change on the input.
	Duty-cycled conversion	The ability to save more power for point conversions. Times the rate of conversion and sets the time for the ADC to remain in standby after the conversion completes.
	Calibration	The ability to run a calibration of the system and to save gain calibration or offset calibration results to the system settings of the user by reading back from the gain/offset registers.
Conversion Targets	ADC inputs	The ability to measure the input signal applied at the ADC input.
	Temperature sensor	The ability to measure local temperatures with an on-chip temperature sensor. Used for relative temperature measurement.
	Diagnostic sources	The ability to measure reference inputs and internal voltages for periodic functional safety checking.
GPIO Control	Up to four GPIOx pins	The ability to control other local hardware (such as gain stages), to power down other blocks in the signal chain, or read local status signals over the SPI interface of the ADAQ7767-1.
System Offset and Gain Correction	System calibration routines	The ability to correct offset and/or gain by writing to registers when the environment changes (that is, the temperature increases). Requires characterization of system errors to feed these registers.
Diagnostics	Internal checks and flags	Users can have the highest confidence in the conversion results.

SPI CONTROL MODE

MCLK Source and MCLK Division

MCLK division bits control the divided ratio between the MCLK applied at the input to the ADAQ7767-1 and the clock used by the ADC modulator. Select the division ratio best for configuration of the clocks.

The following options are available as the MCLK input source in SPI mode:

- LVDS
- External crystal
- CMOS input MCLK

From the Power and Clock Control Register, Register 0x15, pulling the CLOCK_SEL bits [7:6] low configures the ADAQ7767-1 for a CMOS clock. Pulling the CLOCK_SEL bits high enables the use of an external crystal. Setting Bits[7:6] to 10 enables the application of the LVDS clock to the MCLK pin. LVDS clocking is exclusive to SPI mode and requires the register selection for operation.

ADC Power-Down Mode

All blocks on the core ADC are turned off. A specific code is required to wake the ADC up. All register contents are lost when entering power-down mode. Ensure the FDA is powered down before entering the ADC into power-down mode.

Standby Mode

Core ADC's Analog clocking and power functions are powered down. The digital LDO and register settings are retained when in standby mode. This mode is best used in scenarios where the ADC is not in use, briefly, and the user wants to save power.

SPI Synchronization

The ADAQ7767-1 can be synchronized over the SPI. The final SCLK rising edge of the command is the instance of synchronization. This command initiates the SYNC_OUT pin to pulse active low and then back active high again. SYNC_OUT is a signal synchronized internally to the MCLK of the ADC. By connecting the output of SYNC_OUT to the SYNC_IN input, synchronize that individual ADC. Routing SYNC_OUT to other ADAQ7767-1 devices also ensures the devices are synchronized, as long as the devices share a common MCLK source, as shown in Figure 95.

It is recommended to perform synchronization functions directly after the DRDY pulse. If the ADAQ7767-1 SYNC_IN pulse occurs too close to the upcoming DRDY pulse edge, the upcoming DRDY pulse may still be output because the SYNC_IN pulse has not yet propagated through the device.

When using the SYNC_OUT function with an VDD_IO voltage of 1.8 V, it is recommended to set the SYNC_OUT_POS_EDGE bit to a one (Synchronization Modes and Reset Triggering Register 0x1D, Bit 6).

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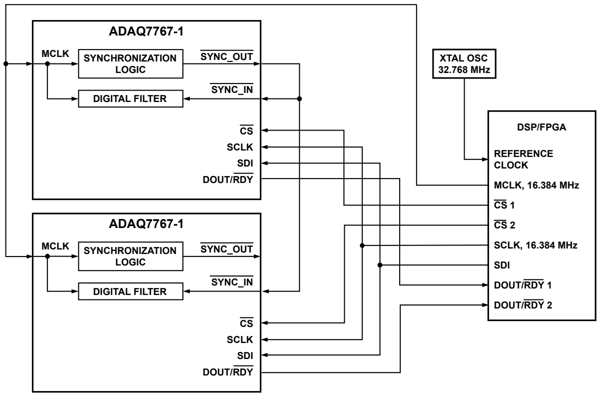

Figure 95. Basic SPI Synchronization Diagram

Offset Calibration

In the SPI control mode, the ADAQ7767-1 has the ability to calibrate the offset and gain. There are the options to alter the gain and offset of the ADAQ7767-1 and its subsystem. These options are available in the SPI control mode only.

The offset correction registers provide 24-bit, signed, 2s complement registers for channel offset adjustment. If the channel gain setting is at the ideal nominal value of 0x555555, an LSB of offset register adjustment changes the digital output by −4/3 LSBs. For example, changing the offset register from 0 to 100 changes the digital output by −133 LSBs. As offset calibration occurs before gain calibration, and the LSB ratio of −4/3 changes linearly with gain adjustment through the gain correction registers.

The Offset Calibration Registers section provides further register information and calibration instructions.

Gain Calibration

In the SPI control mode, alter the gain and offset of the ADAQ7767-1 and its subsystem. These options are available in the SPI control mode only.

The ADC has an associated gain coefficient stored for each ADC after factory programming. Nominally, this gain is approximately the 0x555555 value (for an ADC channel). Overwrite the gain register setting. However, after a reset or power cycle, the gain register values revert to the hard-coded, programmed factory setting.

$$ADC\_DATA = \left[\frac{3 \times V_{IN} \times AFE\_GAIN}{V_{REF}} \times 2^{21} - \left(OffsetCal\right)\right] \times \frac{GainCal}{4} \times \frac{4,194,300}{2^{42}} \quad (18)$$

where:

ADC_DATA is in the 2s complement format.

OffsetCal is the decimal value from the Offset Calibration Registers.

GainCal is the decimal value from the Gain Calibration Registers.

The Gain Calibration Registers section provides further register information and calibration instructions.

Reset over SPI Control Interface

Issue a reset command to the ADAQ7767-1 by writing to the SPI_RESET bits [1:0] in the Synchronization Modes and Reset Triggering Register(Register 0x16). Two successive writes to these bits are required to initiate the device reset.

Resume from Shutdown

Shutdown mode features the lowest possible current consumption with all blocks on the device turned off, including the standard SPI interface. Therefore, to wake the ADC up from this mode, either a hardware reset on the $\overline{\text{RESET}}$ pin, or a specific code on the SPI SDI input, is required. The specific sequence required on SDI consists of a 1 followed by 63 zeros, clocked in by SCLK while $\overline{\text{CS}}$ is low, which allows the system to wake up the ADAQ7767-1 from shutdown without using the $\overline{\text{RESET}}$ pin. This reset function is useful in isolated applications where the number of pins brought across the isolation barrier must be minimized.

GPIO and $\overline{\text{START}}$ Functions

When operating in SPI mode, the ADAQ7767-1 has additional GPIO functionality. This fully configurable mode allows the device to operate four GPIOs. These pins can be configured as read or write in any order.

GPIO read is a useful feature because it allows a peripheral device to send information to the input GPIO. Then, this information can be read from the SPI interface of the ADAQ7767-1.

The GPIOx pins can be set as inputs or outputs on a per pin basis, and there is an option to configure outputs as open-drain.

In SPI control mode, one of the GPIOx pins can be assigned the function of the $\overline{\text{START}}$ input. The $\overline{\text{START}}$ function allows a signal asynchronous to MCLK to be used to generate the $\overline{\text{SYNC\_OUT}}$ signal to reset the digital filter path of the ADAQ7767-1. The $\overline{\text{START}}$ pin function can be enabled on GPIO3.

SPI Mode Diagnostic Features

The ADAQ7767-1 includes diagnostic coverage across the internal blocks within the core ADC. The diagnostics in the following list allow the user to monitor the ADC and to increase confidence in the fidelity of the data acquired:

- Reference detection
- Clock qualification
- CRC on SPI transaction
- Flags for detection of an illegal register write
- CRC checks
- POR monitor

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- MCLK counter

In addition, these diagnostics are useful in situations where instruments require remote checking of power supplies and references during initialization stages.

The diagnostics are selectable by the user via enable registers. The flags for power-on reset (POR) and the clock qualification are on by default. The flags are readable via registers, but also ripple through to the top-level status bits that can be output with each ADC conversion, if desired.

Reference Detection

Write 1 to Bit 3 of the ADC diagnostic feature control Register (Register 0x29) to enable the reference detection block in SPI control mode. When enabled, the error flags in the ADC diagnostics output Register (Register 0x2F). Any error flags then propagate through to the Device error flags master Register (Register 0x2D). The reference error flags when the reference applied on the REF+ pin is below 1/3 of (VDD_ADC − AGND).

Clock Qualification

The clock qualification check attempts to detect when a valid MCLK is detected. When the MCLK applied is greater than 600 kHz, the clock qualification passes. The error flags in both the ADC diagnostics output Register (Register 0x2F) and the Device error flags master Register (Register 0x2D). If the clock detected is below the 600 kHz frequency threshold, or if an external MCLK is not detected, the clock qualification error bit is set to 1. To disable the clock qualification check, write 0 to Bit 0 of the ADC diagnostic feature control Register (Register 0x29).

CRC on SPI Transaction

See the CRC Check on Serial Interface section for more details.

Flags for Detection of Illegal Register Write

See the SPI Control Interface Error Handling section for more details.

CRC Checks

Enable CRC checks in the Digital diagnostic feature control Register (Register 0x2A) to check the state of the memory map of the ADAQ7767-1 and the internal random-access memory (RAM) and fuse settings. If any of these errors flag on the device, perform a reset to return the device to a valid state.

POR Monitor

The POR monitor flag appears in both the register and the status bits when output. The POR flag indicates that a reset or a temporary supply brown out occurred.

MCLK Counter

The MCLK Diagnostic output Register (Register 0x31) updates every 64 MCLKs. The MCLK counter register verifies that the ADAQ7767-1 is still receiving a valid MCLK. Read the MCLK counter register according to the specific MCLK to SCLK ratio to ensure that a valid read occurs. The SCLK applied to read the MCLK_COUNTER register must not be less than 2.1 × MCLK or greater than 4.6 × MCLK. For example, if MCLK = 2 MHz, the SCLK applied cannot be in the 4.2 MHz to 9.2 MHz range. If the MCLK to SCLK ratio is not adhered to, the read may corrupt because the MCLK may update during the read of the register, causing an error.

Product Identification (ID) Number

The ADAQ7767-1 contains ID registers that allow software interrogation of the silicon. The class of the product (precision ADC), product ID, device revision, and grade of device can all be read from the registry over the SPI. The vendor ID for Analog Devices, Inc., is also included in the registry for readback. These registers, in addition to a scratch pad that allows free reads from and writes to a specific register address, are methods of verifying the correct operation of the serial control interface.

Table 27. Product Identification Registers

Register Address (Hex)	Name	Bit Fields	
0x03	Chip type	Reserved	Class
0x04	Product ID [7:0]	PRODUCT_ID[7:0]	
0x05	Product ID [15:8]	PRODUCT_ID[15:8]	
0x06	Grade and revision	Grade	DEVICE_REVISION
0x0A	Scratch pad	Value	
0x0C	Vendor ID	VID[7:0]	
0x0D		VID[15:8]	

DIGITAL INTERFACE

The ADAQ7767-1 has a 4-wire SPI interface. The interface operates in SPI Mode 3. In SPI Mode 3, SCLK idles high, the first data is clocked out on the first falling or drive edge of SCLK, and data is clocked in on the rising or sample edge. Figure 96 shows SPI Mode 3 operation where the falling edge of SCLK is driving out the data and the rising edge of SCLK is when the data is sampled.

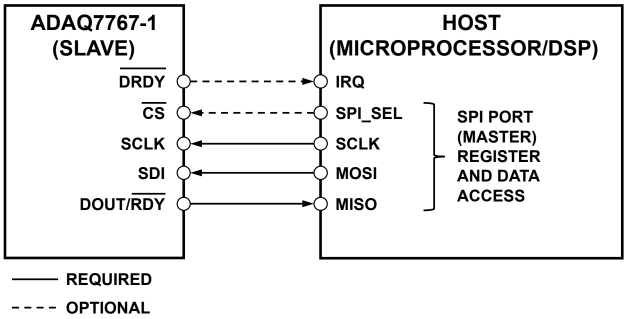

Figure 96. Basic Serial Port Connection Diagram

Figure 97. SPI Mode 3

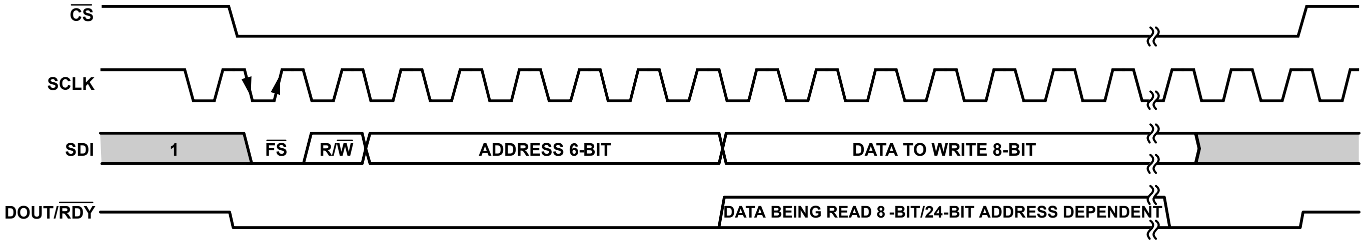

Figure 98. SPI Basic Read/Write Frame

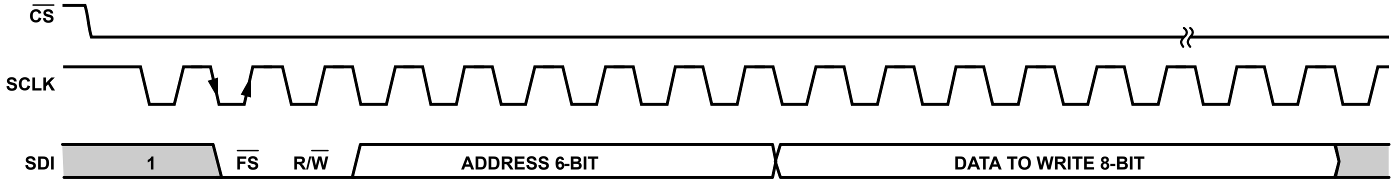

Figure 99. 3-Wire SPI Write Frame ($\overline{\text{CS}}$ = 0)

SPI READING AND WRITING

To use SPI control mode, set the $\overline{\text{PIN}}$/SPI pin high. The SPI control operates as a 4-wire interface allowing read and write access. In systems where $\overline{\text{CS}}$ can be tied low, such as those requiring isolation, the ADAQ7767-1 can operate in a 3-wire configuration. Figure 96 shows a typical connection between the ADAQ7767-1 and the digital host. The corresponding 3-wire interface involves tying the $\overline{\text{CS}}$ pin low and using SCLK, SDI, and DOUT/$\overline{\text{RDY}}$.

The format of the SPI read or write is shown in Figure 98. The MSB is the first bit in both read and write operations. An active low frame start signal ($\overline{\text{FS}}$) begins the transaction, followed by the R/W bit that determines if the transaction being carried out is to a read (1) or a write (0). The next six bits are used for the address, and the eight bits of data to be written follow. All registers in the ADAQ7767-1 are 8 bits in width, except for the ADC_DATA register (Register 0x2C), which is 24 bits in width. In the case where $\overline{\text{CS}}$ is tied low, the last SCLK rising edge completes the SPI transaction and resets the interface. When reading back data with $\overline{\text{CS}}$ held low, it is recommended that SDI idle high to prevent an accidental reset of the device where SCLK is free running (see the Reset section).

DIGITAL INTERFACE

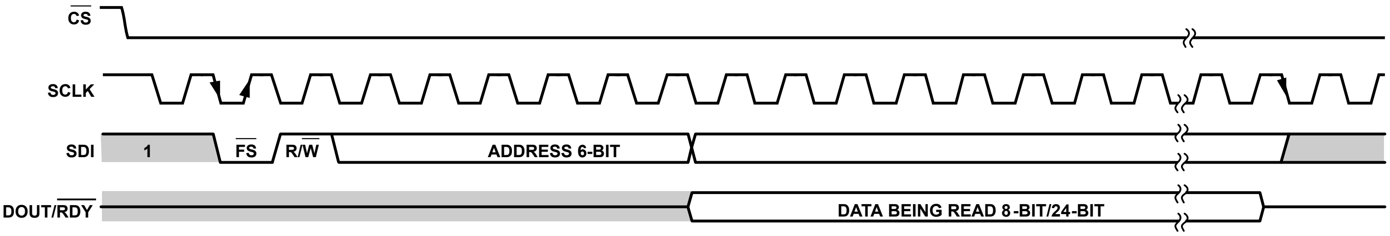

Figure 100. 3-Wire SPI Read Frame (CS = 0)

SPI CONTROL INTERFACE ERROR HANDLING

The ADAQ7767-1 SPI control interface detects if an illegal command is received. An illegal command is a write to a read only register, a write to a register address that does not exist, or a read from a register address that does not exist. If any of these illegal commands are received by the ADAQ7767-1, error bits are set in the SPI_DIAG_STATUS register (Register 0x2E).

Five sources of SPI error can be detected. These detectable error sources must be enabled in the SPI_DIAG_ENABLE register (Register 0x28). Only the EN_ERR_SPI_IGNORE (Bit 4) error is enabled on startup.

The five detectable sources of SPI error are as follows:

- SPI CRC error. This error occurs when the received CRC/XOR does not match the calculated CRC/XOR.
- SPI read error. This error occurs when an incorrect read address is detected (for example, when the user attempts to access a register that does not exist).
- SPI write error. This error occurs when a write to an incorrect address is detected (for example, when the user attempts to write to a register that does not exist).
- SPI clock count error. When the SPI transaction is controlled by CS, this error flags when the SPI clock count during the frame is not equal to 8, 16, 24, 32, or 40. This error can be detected in both continuous read mode and normal SPI mode.
- SPI ignore error. This error flags when an SPI transaction is attempted before initial power-up completes.

All SPI errors are sticky, meaning they can only be cleared if the user writes a 1 to the corresponding error location.

CRC CHECK ON SERIAL INTERFACE

The ADAQ7767-1 can deliver up to 40 bits with each conversion result, consisting of 24 bits of data and eight status bits, with the option to add eight further CRC/XOR check bits in the SPI mode only.

The status bits default per the description in the Status Header section. The CRC functionality is available only when operating in the SPI control mode. When the CRC functionality is in use, the CRC message is calculated internally by the ADAQ7767-1. The CRC is then appended to the conversion data and optional status bits.

The ADAQ7767-1 uses a CRC polynomial to calculate the CRC message. The 8-bit CRC polynomial used is $x^8 + x^2 + x + 1$.

To generate the checksum, shift the data by eight bits to create a number ending in eight Logic 0s.

The polynomial is aligned such that the MSB is adjacent to the leftmost Logic 1 of the "command bits and register data". For example, when reading the ADC_DATA register containing 0xABCDEF:

Initial Value = Frame Start bit + R/W bit + ADDR[5:0] + ADC_DATA[23:0]

Initial Value = 0x6CABCDEF

Apply an exclusive OR (XOR) function to the data to produce a new, shorter number. The polynomial is again aligned such that the MSB is adjacent to the leftmost Logic 1 of the new result, and the procedure is repeated. This process repeats until the original data is reduced to a value less than the polynomial, which is the 8-bit checksum. In the example above, the CRC checksum = 0x9E.

If enabled, the SPI writes always use CRC, regardless of whether the XOR option is selected in the INTERFACE_FORMAT register (Register 0x14). The initial CRC checksum for SPI transactions is 0x00, unless reading back data in the continuous read mode, in which case the initial CRC is 0x03.

If using the XOR option in the continuous read mode, the initial value is set to 0x6C. The XOR option is only available for SPI reads.

DIGITAL INTERFACE

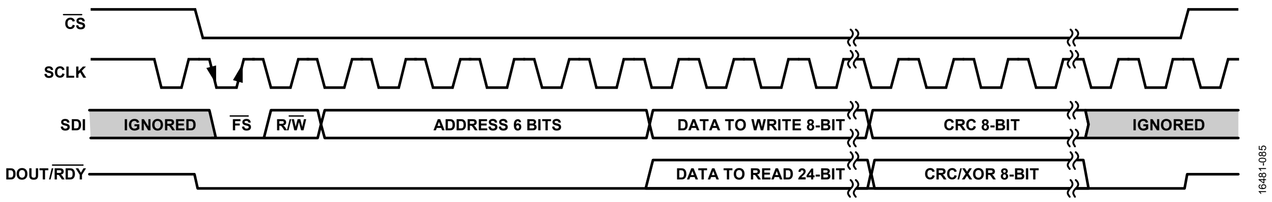

Figure 101. Data Output Format When Using CRC

DIGITAL INTERFACE

Example of a Polynomial CRC Calculation—(24-Bit Word: 0x654321 (Eight Command Bits and 16-Bit Data))

An example to generate the 8-bit checksum using the polynomial-based checksum is as follows:

```
011001010100001100100001          = Initial Value
01100101010000110010000100000000  left shifted eight bits
 100000111                        = x^8 + x^2 + x + 1 polynomial value
  100100100000110010000100000000  XOR result
  100000111                       polynomial value
     100011000110010000100000000  XOR result
     100000111                    polynomial value
         11111110010000100000000  XOR result
         100000111                polynomial value
          1111101110000100000000  XOR result
          100000111               polynomial value
           111100000000100000000  XOR result
           100000111              polynomial value
            11100111000100000000  XOR result
            100000111             polynomial value
             1100100100100000000  XOR result
             100000111            polynomial value
              100101010100000000  XOR result
              100000111           polynomial value
                 101101100000000  XOR result
                 100000111        polynomial value
                   1101011000000  XOR result
                   100000111      polynomial value
                    101010110000  XOR result
                    100000111     polynomial value
                      1010001000  XOR result
                      100000111   polynomial value
                        10000110  XOR result; checksum = 0x86
```

Example of an XOR Calculation— (24-Bit Word: 0x654321 (Eight Command Bits and 16-Bit Data))

Using the previous example, divide into three bytes (0x65, 0x43, and 0x21) as follows:

```
01100101 0x65
01000011 0x43
00100110 XOR result
00100001 0x21
00000111 XOR result; checksum = 0x07
```

CONVERSION READ MODES

The digital interface of the ADAQ7767-1 is a 4-wire SPI implementation operating in Mode 3 SPI. An 8-bit write instruction is needed to access the memory map address space. All registers are eight bits wide, with the exception of the ADC data register. The ADAQ7767-1 operates in a continuously converting mode by default. The user must decide whether to read the data. Two read modes are available to access the ADC conversion results: single-conversion read mode and continuous read mode.

Single-conversion read mode is a basic SPI read cycle where the user must write an 8-bit instruction to read the ADC data register. The status register must be read separately, if needed.

Write a 1 to the LSB of the Interface Format Control Register (Register 0x14) to enter continuous read mode. Subsequent data reads do not require an initial 8-bit write to query the ADC_DATA register. Simply provide the required number of SCLKs for continuous readback of the data. Figure 102 shows an SPI read in continuous read mode.

Key considerations for users on the interface are as follows:

- Conversion data is available for readback after the rising edge of $\overline{\text{DRDY}}$. In continuous read mode, the $\overline{\text{RDY}}$ function can be enabled, and the $\overline{\text{DRDY}}$ function can be ignored. Data is available for readback on the falling edge of $\overline{\text{RDY}}$.
- The ADC conversion data register is updated internally 1 MCLK period prior to the rising $\overline{\text{DRDY}}$ edge.
- MCLK has a maximum frequency of 16.384 MHz.
- SCLK has a maximum frequency of 20 MHz.
- The $\overline{\text{DRDY}}$ high time is 1 × t_{MCLK}
- In fast power mode, decimate by 32, the $\overline{\text{DRDY}}$ period is ~4 μs, the fastest conversion can have a $\overline{\text{DRDY}}$ period of 1 μs.
- The $\overline{\text{CS}}$ rising edge resets the serial data interface. If $\overline{\text{CS}}$ is tied low, the final rising SCLK edge of the SPI transaction resets the serial interface. The point at which the interface is reset corresponds to 16 × SCLKs for a normal read operation and up to 40 SCLKs when reading back ADC conversion data, plus the status and CRC headers.

Single-Conversion Read Mode

When using single-conversion read mode, the ADC_DATA register can be accessed in the same way as a normal SPI read transaction. The ADC_DATA register (Register 0x2C), is 24 bits wide. Therefore, 32 SCLKs are required to read a conversion result.

DIGITAL INTERFACE

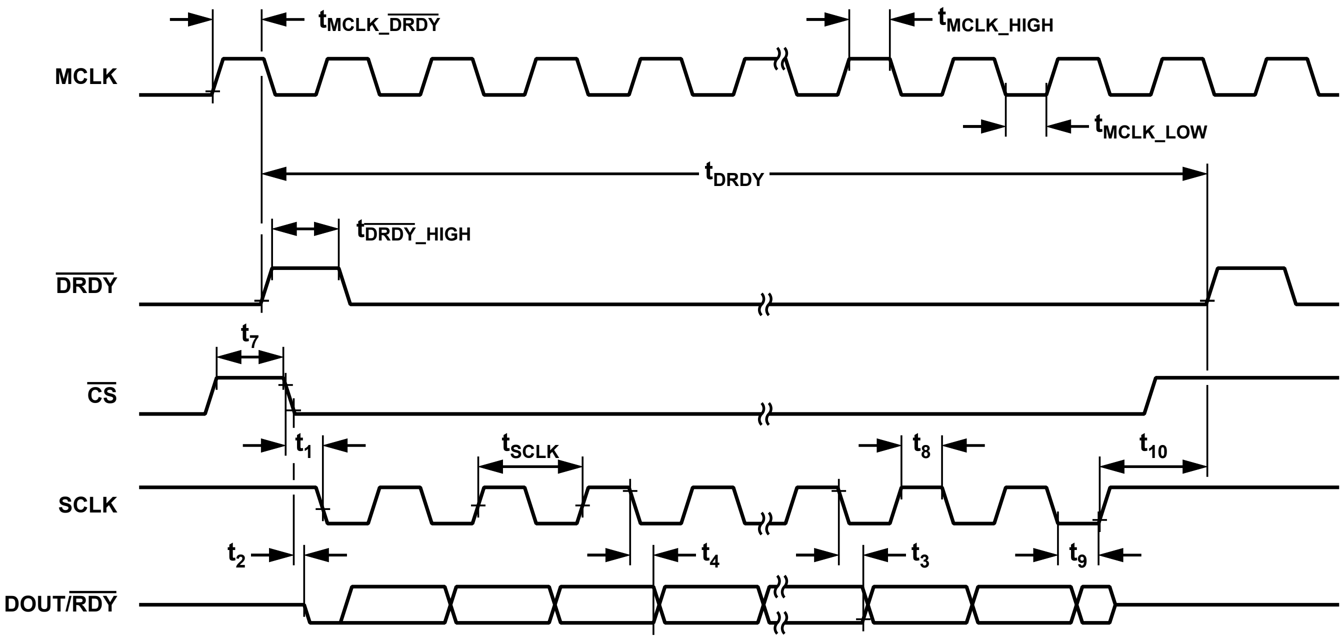

Figure 102. Serial Interface Timing Diagram, Example Reflects Reading an ADC Conversion in Continuous Read Mode

Continuous Read Mode

To eliminate the overhead of needing to write a command to read the ADC data register each time, the user can place the ADC in continuous read mode so that the ADC register can be read directly after the data ready signal is pulsed. In continuous read mode, data is output on the falling edge of the first SCLK received. Therefore, only 24 SCLKs are required to read a conversion. In this continuous read mode, it is also possible to append one or both of the status or CRC headers (eight bits each) to the conversion result. If both the status and CRC headers are enabled, the data format is ADC data + status bits + CRC.

When the $\overline{RDY}$ function is not used, the ADC conversion result can be read multiple times in the $\overline{DRDY}$ period, as is shown in Figure 103. When the $\overline{RDY}$ function is enabled, the DOUT/$\overline{RDY}$ pin goes high after reading the ADAQ7767-1 conversion result and, therefore, the data cannot be read more than once (see Figure 104). The $\overline{RDY}$ function can be enabled by setting a logic low to bit[2] of the Interface Format Control Register (Register 0x14).

Continuous readback is the readback mode used in $\overline{PIN}$ control mode. However, in this mode, the data output format is fixed. There is no option for $\overline{RDY}$ on the DOUT pin. See the Pin Control Mode Overview section for more details.

When using continuous read mode with the LV_BOOST bit enabled (Bit 7 in the Interface Format Control Register, Register 0x14), it is necessary to re-enable LV_BOOST each time continuous read mode is exited.

Exiting Continuous Read Mode

To exit continuous read mode, write a key of 0x6C on the SDI, which allows access to the register map one more time and allows further configuration of the device. To comply with a normal SPI write, use the $\overline{CS}$ signal to reset the SPI interface after this key is entered. If $\overline{CS}$ cannot be controlled and is permanently held low, 16 SCLKs are needed to complete the transaction so that the SPI interface remains synchronized. For example, when $\overline{CS}$ is permanently tied low, write 0x006C to exit continuous read mode when using the 3-wire version of the interface. The exit command must be written between $\overline{DRDY}$ pulses to ensure that the device exits correctly.

A software reset can also be written in this mode in the same way as the exit command, but by writing 0xAD instead of 0x6C.

DIGITAL INTERFACE

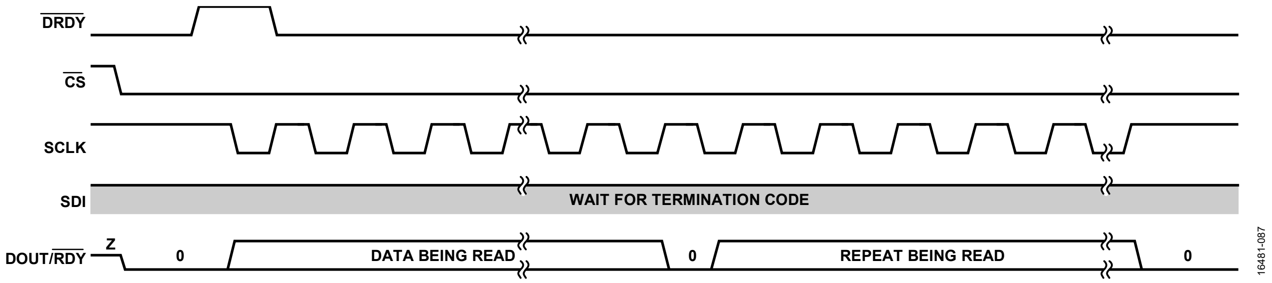

Figure 103. Continuous ADC Read Data Format with $\overline{RDY}$ Function Disabled

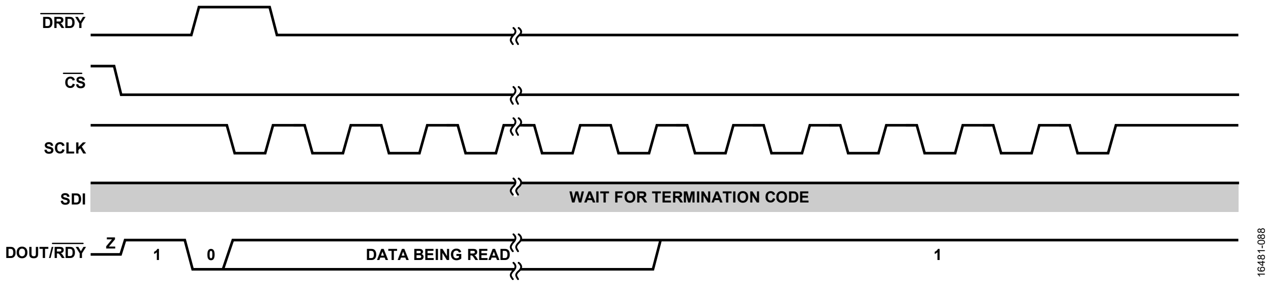

Figure 104. Continuous ADC Read Data Format with $\overline{RDY}$ Function Enabled on the DOUT/$\overline{RDY}$ Pin

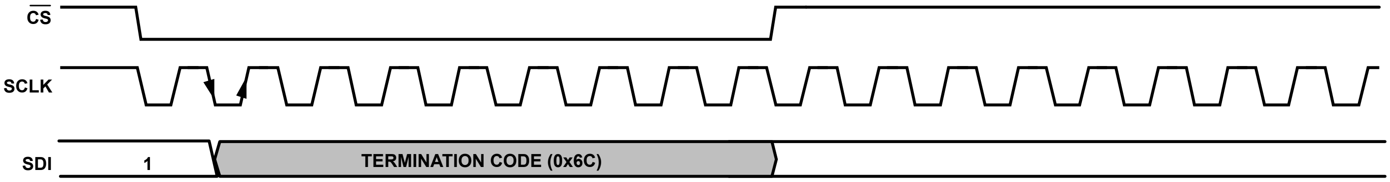

Figure 105. Exiting Continuous Read Mode ($\overline{CS}$ Toggling)

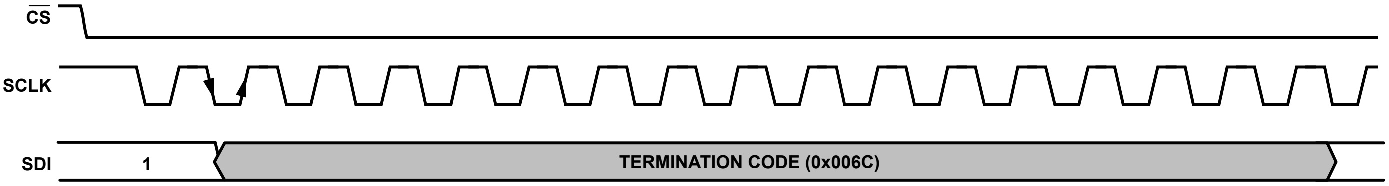

Figure 106. Exiting Continuous Read Mode ($\overline{CS}$=0)

DATA CONVERSION MODES

The four data conversion modes available in SPI control mode are as follows:

- Continuous conversion
- One shot conversion
- Single conversion
- Duty cycled conversion

The default conversion mode is continuous conversion. Write to bits[2:0] of the Conversion Source Select and Mode Control Register (Register 0x2E) to change the conversion mode. A SYNC_IN pulse must be provided to the ADAQ7767-1 after any change to the configuration of the device, including changing filter settings and data conversion modes.

CONTINUOUS CONVERSION MODE

In continuous conversion mode, the ADC continuously converts and a new ADC result is ready at an interval determined by the ODR, which is the default conversion operation in SPI control mode. This is the only data conversion mode in which the wideband low ripple FIR filter is available. Two methods of data readback are available to the user in SPI control mode and are described in the Conversion Read Modes section.

ONE SHOT CONVERSION MODE

shows the device operating in one shot conversion mode. In this mode, conversions occur on request by the master device, for example, the DSP or FPGA. The SYNC_IN pin receives the command initiating the data output.

In one shot conversion mode, the ADC runs continuously. However, the SYNC_IN pin rising controls the point in time from which data is output.

To receive data, the master device must pulse the SYNC_IN pin, which resets the filter and forces DRDY low. DRDY subsequently goes high to indicate to the master device that the device has valid settled data available.

When the master asserts SYNC_IN and the ADAQ7767-1 receives the rising edge of this signal, the digital filter is reset, the full settling time of the filter elapses before the data is settled, and the output is available. The duration of the settling time depends on the filter path and decimation rate. One shot conversion mode is only available for use with the sinc5 or sinc3 filters because these filters feature a minimal settling time. One shot conversion mode is not available as an option for use with the wideband low ripple FIR filter.

When settled data is available, the DRDY signal pulses. The time from the SYNC_IN signal until the ADC path settles data (t_{SETTLE}) is shown in Figure 107. After settled data is available, DRDY is asserted high, and the user can read the conversion result. The device then waits for another SYNC_IN signal before outputting more data.

The settling time is calculated relative to the settling time of the filter used, with some added latency for starting the one shot conversion. This settling time limits the overall throughput achievable in one shot conversion mode.

Because the ADC is sampling continuously, one shot conversion mode affects the sampling theory of the ADAQ7767-1. Periodically sending a SYNC_IN pulse to the device is a form of subsampling of the ADC output. The bandwidth around this subsampling rate can now alias down to the baseband. Consider keeping the SYNC_IN pulse synchronous with the master clock to ensure coherent sampling and to reduce the effects of jitter on the frequency response, which otherwise heavily distort the output.

Any SPI configuration of the ADAQ7767-1 required is performed in continuous conversion mode before switching back to one shot conversion mode.

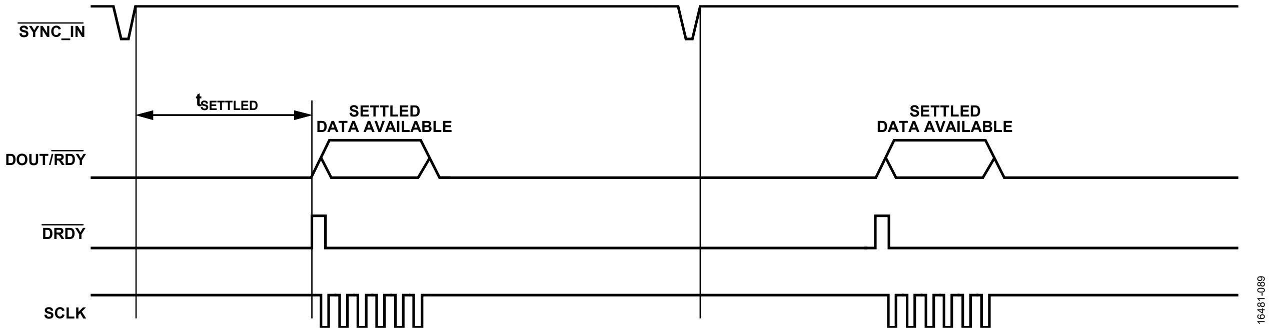

Figure 107. One Shot Conversion Mode, SYNC_IN Pin Driven with an External Source

DATA CONVERSION MODES

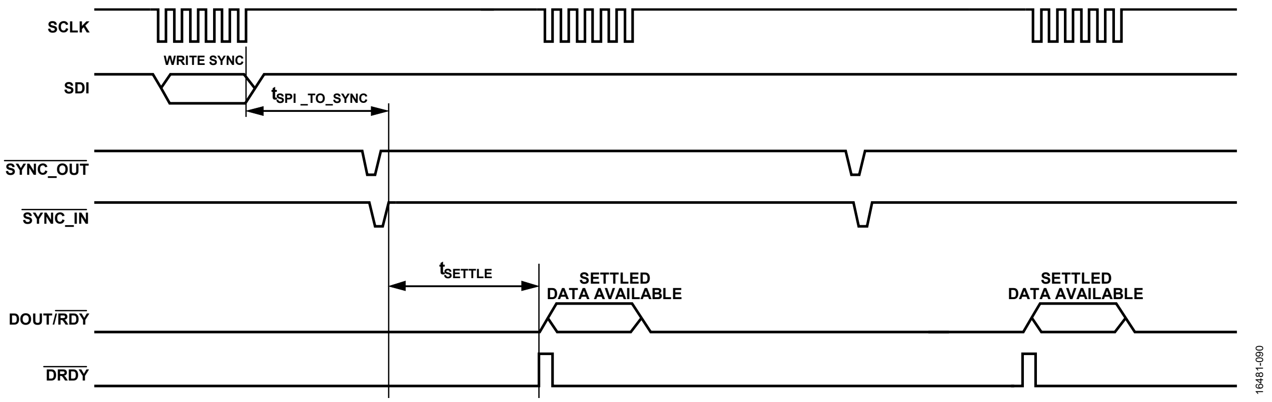

Figure 108. One Shot Conversion Mode, $\overline{\text{SYNC\_IN}}$ Pulse Initiated by a Register Write

SINGLE-CONVERSION MODE

In single-conversion mode, the ADC wakes up from standby, performs a conversion, and then returns to standby. Only use single-conversion mode when operating in low power and median power modes. The user must send a command to initiate the read and subsequently read back the ADC conversion result. Use a toggle of the $\overline{\text{SYNC\_IN}}$ pin to exit the device from standby and to start a new conversion.

Any SPI configuration of the ADAQ7767-1 required must be performed in continuous conversion mode before then switching back to single-conversion mode.

DUTY CYCLED CONVERSION MODE

In duty cycled conversion mode, the ADC wakes up from standby, performs a conversion, and then returns to standby. The user can set the period between each conversion, and the ADC automatically performs the single conversion before returning to standby, repeating the single conversion performed by the ADC at a period specified by the user. Only use duty cycled conversion mode when operating in low power and median power modes. Duty cycled conversion mode allows a method to reduce the power consumption for dc point conversions, and to eliminate any overhead in timing and initiating the conversion.

Use a toggle of the $\overline{\text{SYNC\_IN}}$ pin to begin the duty cycled conversion mode sequence. $\overline{\text{DRDY}}$ toggles once when a settled result is reached. Then, the device enters standby one more time. The Periodic Conversion Rate Control Register controls the determined idle time.

Any SPI configuration of the ADAQ7767-1 required must be performed in continuous conversion mode before switching back to duty cycled conversion mode.

SYNCHRONIZATION OF MULTIPLE ADAQ7767-1 DEVICES

Synchronization is an important consideration when using multiple ADAQ7767-1 devices in a system. The basic provision for synchronizing multiple devices is that each device is clocked with the same base MCLK signal. Provide a SYNC_IN pulse to the ADAQ7767-1 both after power-up and after any change to the configuration of the device. This pulse flushes out the digital filters and ensures that the device is in a known configuration, as well as synchronizing multiple devices in a system.

The ADAQ7767-1 has three options to ease system synchronization. Choosing among the options depends on the system. However, the most basic consideration is whether the user can supply a synchronization pulse that is truly synchronous with the base MCLK signal.

If a signal that is synchronous to the base MCLK signal cannot be provided, use one of the following methods:

- Configure the GPIOx pin of one of the ADAQ7767-1 devices in the system to be a START input. Apply a START pulse to the configured GPIOx pin. Route the SYNC_OUT pin output to the SYNC_IN input of that same device and all other devices to be synchronized.
- The ADAQ7767-1 samples the asynchronous START pulse and generates a SYNC_OUT pulse related to the base MCLK signal for local distribution.
- Use synchronization over SPI (only available in the SPI control mode). Write a synchronization command to one predetermined ADC device. Connect the SYNC_OUT pin of this device to its own SYNC_IN pin and to the SYNC_IN pin of any other device locally. Similar to the START pin method, the SPI synchronization is received by one device and, subsequently, the SYNC_OUT signal is routed to local devices to allow synchronization.

If a SYNC_IN signal synchronous to the base MCLK can be provided, apply the SYNC_IN synchronous signal to the SYNC_IN pin from a star point and connect directly to the pin of each ADAQ7767-1 device. The SYNC_IN signal is sampled on the rising MCLK edge and, therefore, setup and hold times are associated with the SYNC_IN input relative to the ADAQ7767-1 MCLK rising edge (see Figure 7).

In this case, SYNC_OUT is redundant and can remain open-circuit or tied to VDD_IO. GPIOx can be used for a different purpose because it is not required for the START function. Figure 109 shows synchronization in channel-to-channel isolated systems.

It is recommended to perform synchronization functions directly after the DRDY pulse. If the ADAQ7767-1 SYNC_IN pulse occurs too close to the upcoming DRDY pulse edge, the upcoming DRDY pulse may still be output because the SYNC_IN pulse has not yet propagated through the device.

When using the SYNC_OUT function with a VDD_IO voltage of 1.8 V, it is recommended to set the SYNC_OUT_POS_EDGE bit (Synchronization Modes and Reset Triggering Register 0x1D, Bit 6) to 1.

SYNCHRONIZATION OF MULTIPLE ADAQ7767-1 DEVICES

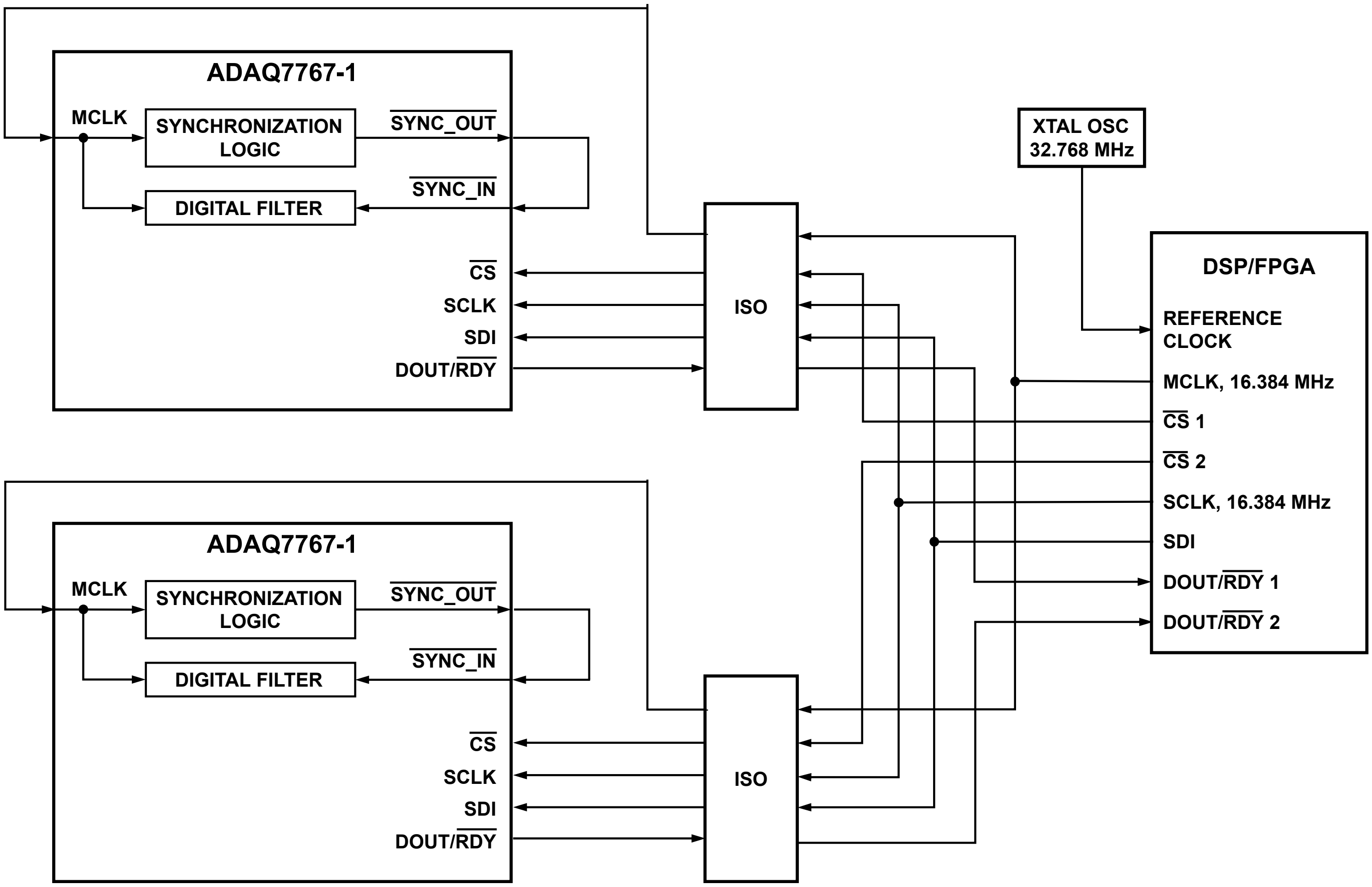

Figure 109. Synchronization in Channel to Channel Isolated Systems

ADDITIONAL FUNCTIONALITY OF THE ADAQ7767-1

RESET

After powering up the device, it is recommended to perform a full reset. There are multiple options available on the ADAQ7767-1 to perform a reset, including

- Using the dedicated $\overline{\text{RESET}}$ pin. See the Pin Configuration and Function Description section.
- When in continuous read mode, the ADAQ7767-1 monitors for the exit command or a reset command of 0xAD. See the Exiting Continuous Read Mode section for more details.
- A software reset can be performed by two consecutive writes to the Synchronization Modes and Reset Triggering Register (Register 0x1D).
- When $\overline{\text{CS}}$ is held low, it is possible to provide a reset by clocking in a 1 followed by 63 zeros on SDI, which is the SPI resume command reset function used to exit power-down mode.

The time taken from $\overline{\text{RESET}}$ to an SPI write must be at least 200 µs.

STATUS HEADER

In SPI control mode, the status header can be output after the conversion result when operating the ADAQ7767-1 in continuous read back mode. The status header mirrors the MASTER_ STATUS register (Register 0x2D).

In $\overline{\text{PIN}}$ control mode, the status header is output by default after the conversion result. The status header contains the following bits and functions:

- The MASTER_ERROR bit is an OR of all other errors present and can be monitored to provide a quick indication of a problem having occurred.
- The ADC_ERROR bit sets to 1 if any error is present in the ADC_DIAG_STATUS register (Register 0x2F). It is an OR of the error bits in the ADC_DIAG_STATUS register.
- The DIG_ERROR bit sets to 1 if any error is present in the DIG_DIAG_STATUS register (Register 0x30). It is an OR of the error bits in the DIG_DIAG_STATUS register.
- The ADC_ERR_EXT_CLK_QUAL bit sets if a valid clock is not detected (see the Clock Qualification section).
- The ADC_FILT_SATURATED bit sets to 1 if the digital filter is clipped on either positive or negative full scale. The clipping can be caused by the analog input exceeding the analog input range, or by a large step input to the device that causes a large overshoot in the digital filter. In addition, the filter may saturate if the ADC gain registers are incorrectly set. The combination of a full-scale signal and a large gain saturates the digital filter.
- The ADC_FILT_NOT_SETTLED bit is set to 1 if the output of the digital filter is not settled. The digital filters are cleared following a $\overline{\text{RESET}}$ pulse, or after a $\overline{\text{SYNC\_IN}}$ command is received. Table 17, Table 18, and Table 23 list the time for $\overline{\text{SYNC\_IN}}$ to settled data for each filter type. When using the Wideband Low Ripple FIR filter, the filter not settled bit takes longer to update and propagate through the device than to read the status header. The filter not settled bit appears set when in fact the data output is settled. The worst-case update delay is 128 MCLK cycles for the Wideband Low Ripple FIR filter, decimate by 1024 setting. In this case, if the readback is delayed by 128 MCLK cycles, the filter not settled bit has time to update, and the time to settled data is equal to the data shown in Table 17, Table 18, and Table 23.
- The SPI_ERROR bit sets to 1 if any error is present in the SPI_DIAG_STATUS register (Register 0x2E). The bit is an OR of the error bits in the SPI_DIAG_STATUS register.
- The POR_FLAG bit detects if a reset or a temporary supply brown out occurred. In $\overline{\text{PIN}}$ control mode, instead of being the POR flag, this bit is always set to 1 and then detects if that the interface is operating correctly.

DIAGNOSTICS

Internal diagnostics are available on the ADAQ7767-1 that allow the user to check both the functionality of the ADC and the environment in which the ADC is operating. The internal diagnostics are enabled in the conversion register (Register 0x18). To use the diagnostics, the device must be configured to eco mode, MCLK_DIV = MCLK/16, and the linearity boost buffers must be enabled. The diagnostics available are as follows:

- The temperature sensor is an on-chip temperature sensor that determines the approximate temperature. Temperature changes measured give approximately a 0.6 mV/°C change in the dc converted voltage. For example, at ambient temperature, the conversion result is approximately 180 mV. A 50°C increase in temperature reads back as approximately 210 mV, signaling, for example, a potential fault or the need to calibrate the system.
- The analog input short disconnects the core ADC's input pins from the external input and creates an internal short across the analog input pins that can detect a fault.
- The voltage converted is V_{REF+} for positive full scale, if selected.
- The voltage converted is V_{REF-} for negative full scale, if selected.

APPLICATIONS INFORMATION

IEPE SENSOR APPLICATION

A common application of the ADAQ7767-1 is condition-based monitoring (CbM) using integrated electronics piezo-electric (IEPE) sensors. In the application shown in Figure 110 and Figure 111, the IEPE sensor can be interfaced with the ADAQ7767-1 with the use of ADG5421F as a fault protection switch, LT3092 as a current source to bias the sensor, and ADA4610-1 as a high impedance buffer. Whenever a voltage source is used to test the signal chain, the current source should be disconnected through the switch. This application solution is designed to convert a unipolar input from either +2.5V to +21.5V or −21.5V to −2.5V by using ADAQ7767-1's IN3 inputs and by simply changing the power supply levels of the switch, current source, and buffer. The ±2.5V headroom of the ADA4610-1 from both power rails causes the input range to be narrower, but nevertheless captures the operational range of IEPE sensors in the market. The ADAQ7767-1's excellent DC performance allows the IEPE sensor to be DC-coupled to the system and convert the signals with precision in the sub-Hz frequencies.

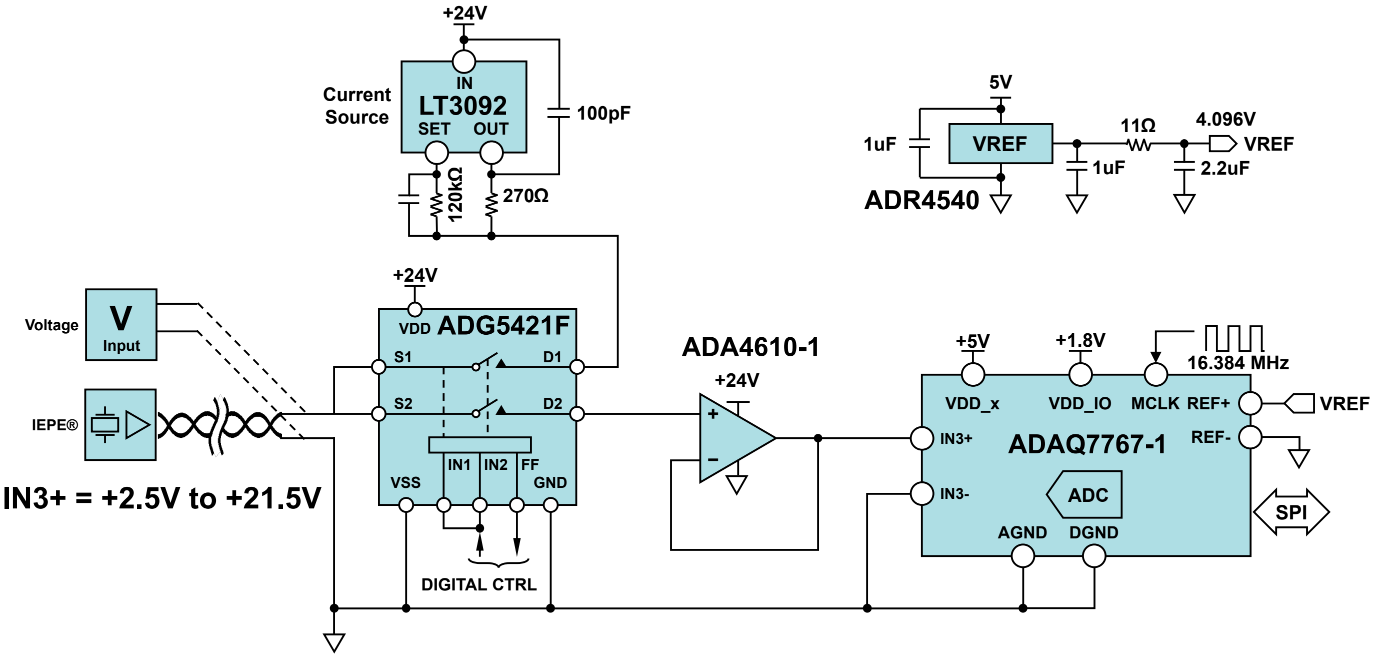

Figure 110. DC-coupled IEPE Sensor Application, IN3+ = +2.5V to +21.5V

APPLICATIONS INFORMATION

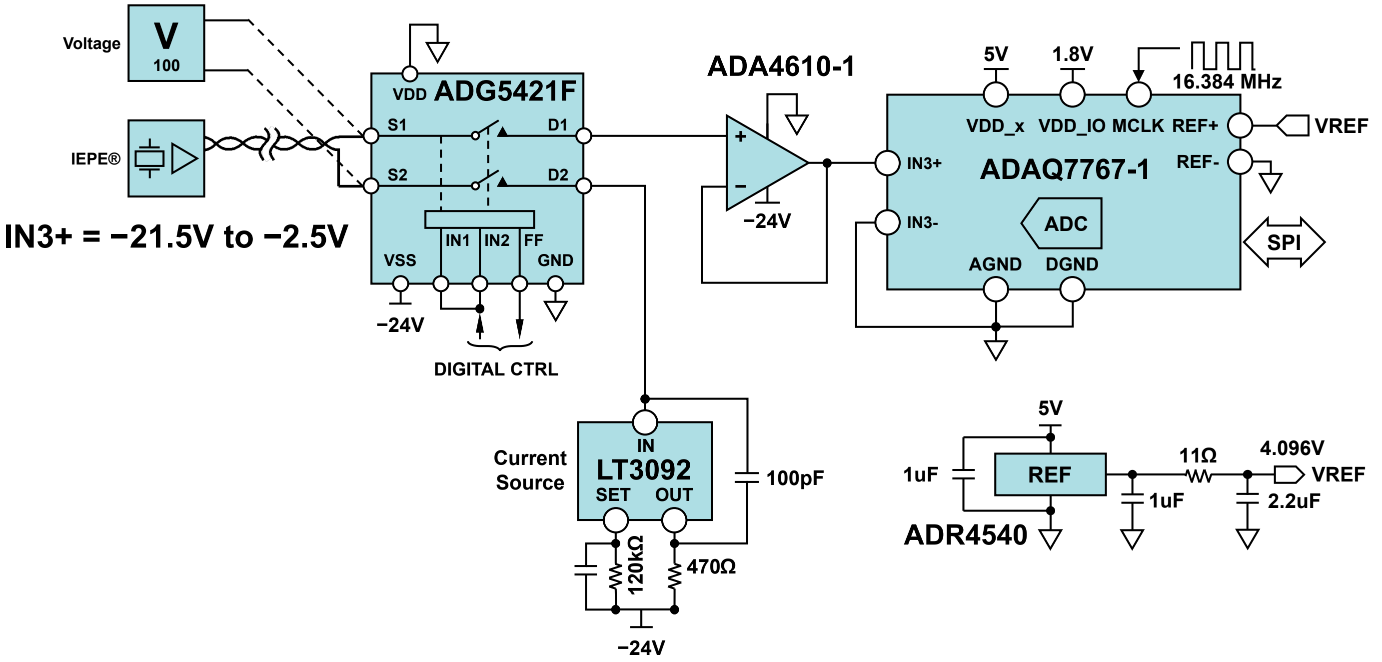

Figure 111. DC-Coupled IEPE Sensor Application, IN3+ = −21.5V to −2.5V

ANALOG INPUTS

Differential Inputs

Figure 112, Figure 113, and Figure 114 show the typical application examples of differential signals with varying common-mode voltages applied to IN1+/-, IN2+/-, or IN3+/- of the ADAQ7767-1 for gains of 1, 0.36, and 0.14, respectively, assuming V_{REF} = 4.096 V.

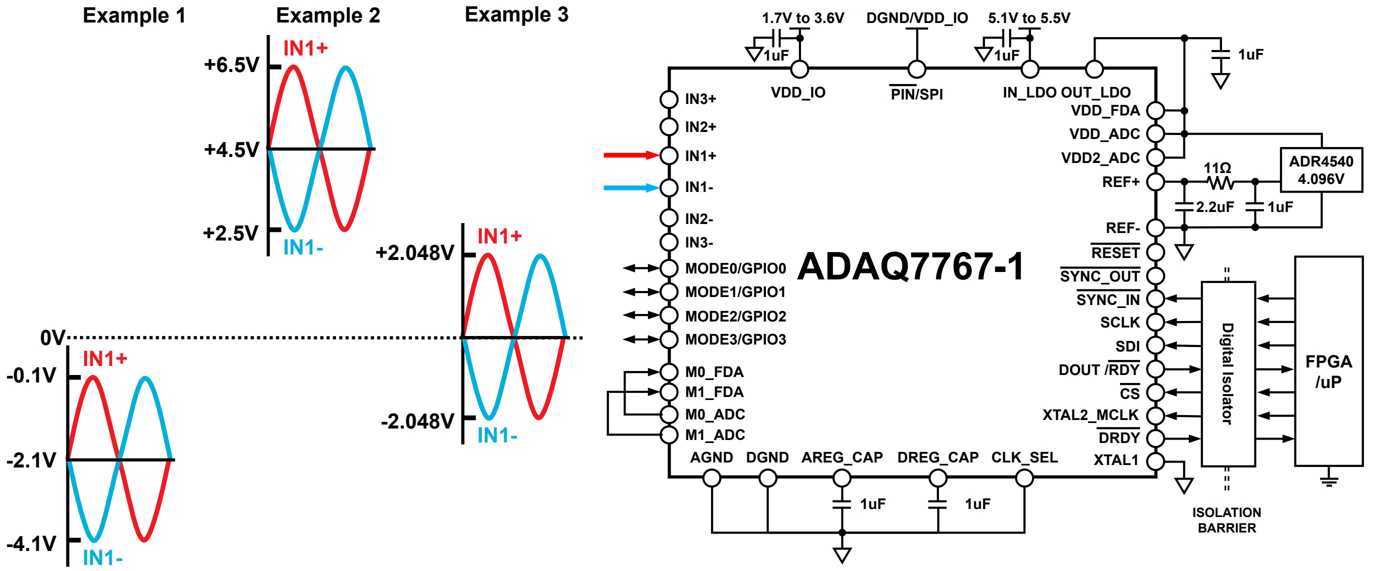

Figure 112. ADAQ7767-1 differential input configuration to IN1+/− (AFE_GAIN = 1 V/V)

APPLICATIONS INFORMATION

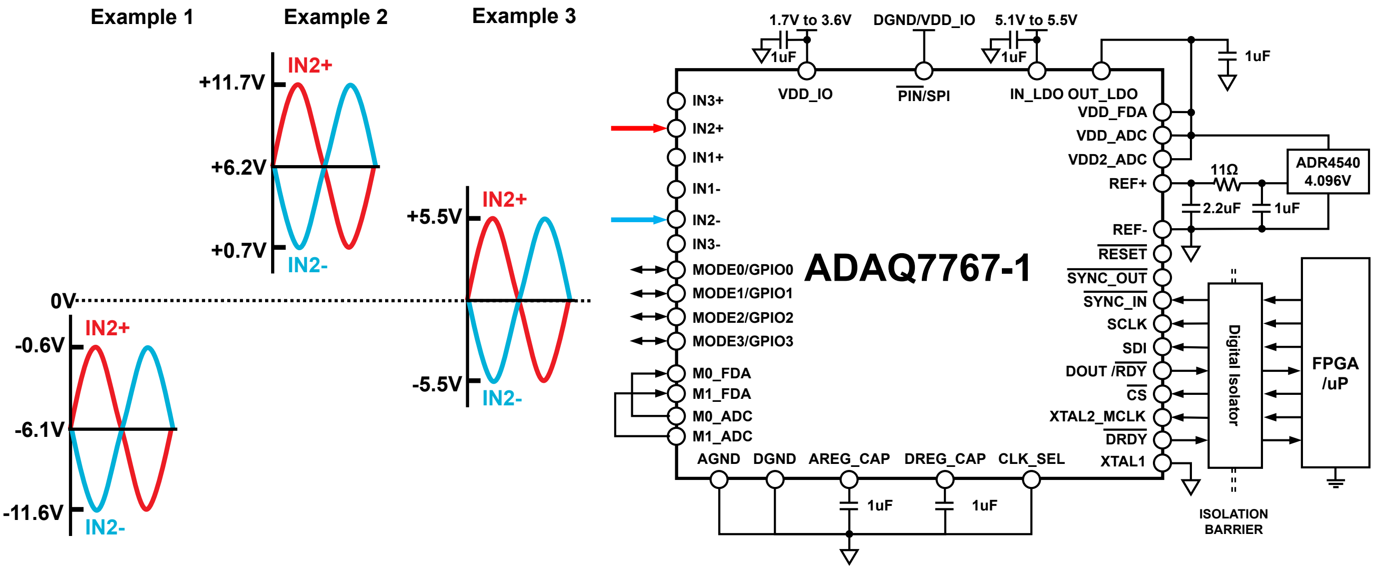

Figure 113. ADAQ7767-1 differential input configuration to IN2+/− (AFE_GAIN = 0.36 V/V)

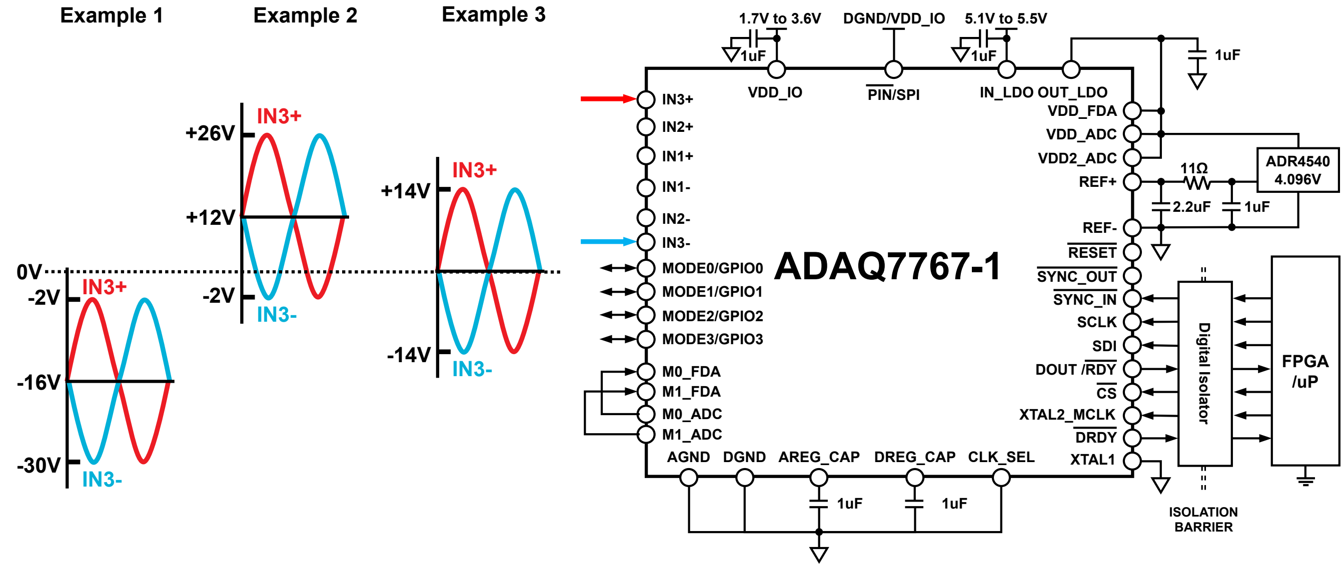

Figure 114. ADAQ7767-1 differential input configuration to IN3+/− (AFE_GAIN = 0.14 V/V)

Single-Ended Inputs

Figure 115, Figure 116, and Figure 117 show the typical application examples of single-ended signals applied to IN1+/-, IN2+/-, or IN3+/- of the ADAQ7767-1 for gains of 1, 0.36, and 0.14, respectively, assuming V_{REF} = 4.096 V.

APPLICATIONS INFORMATION

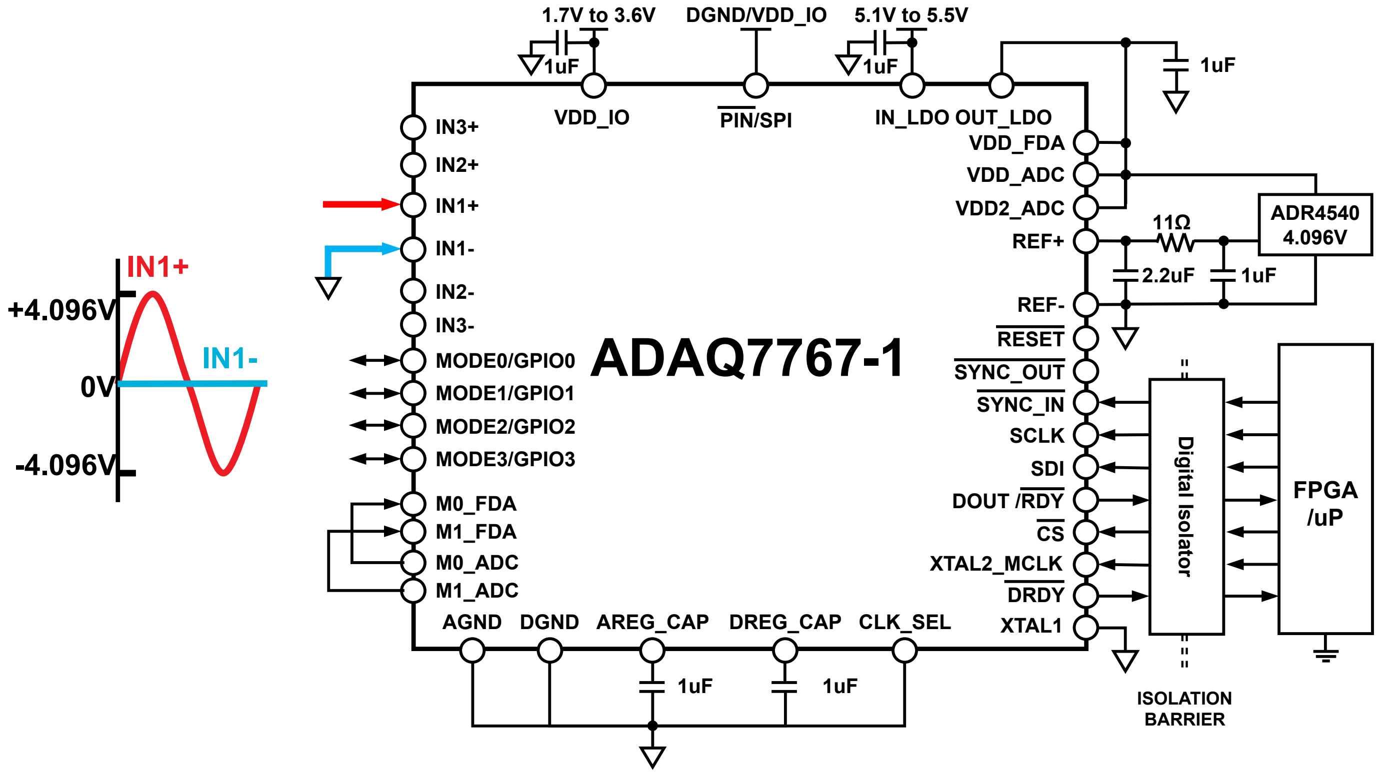

Figure 115. ADAQ7767-1 single-ended input configuration to IN1+/− (AFE_GAIN = 1 V/V)

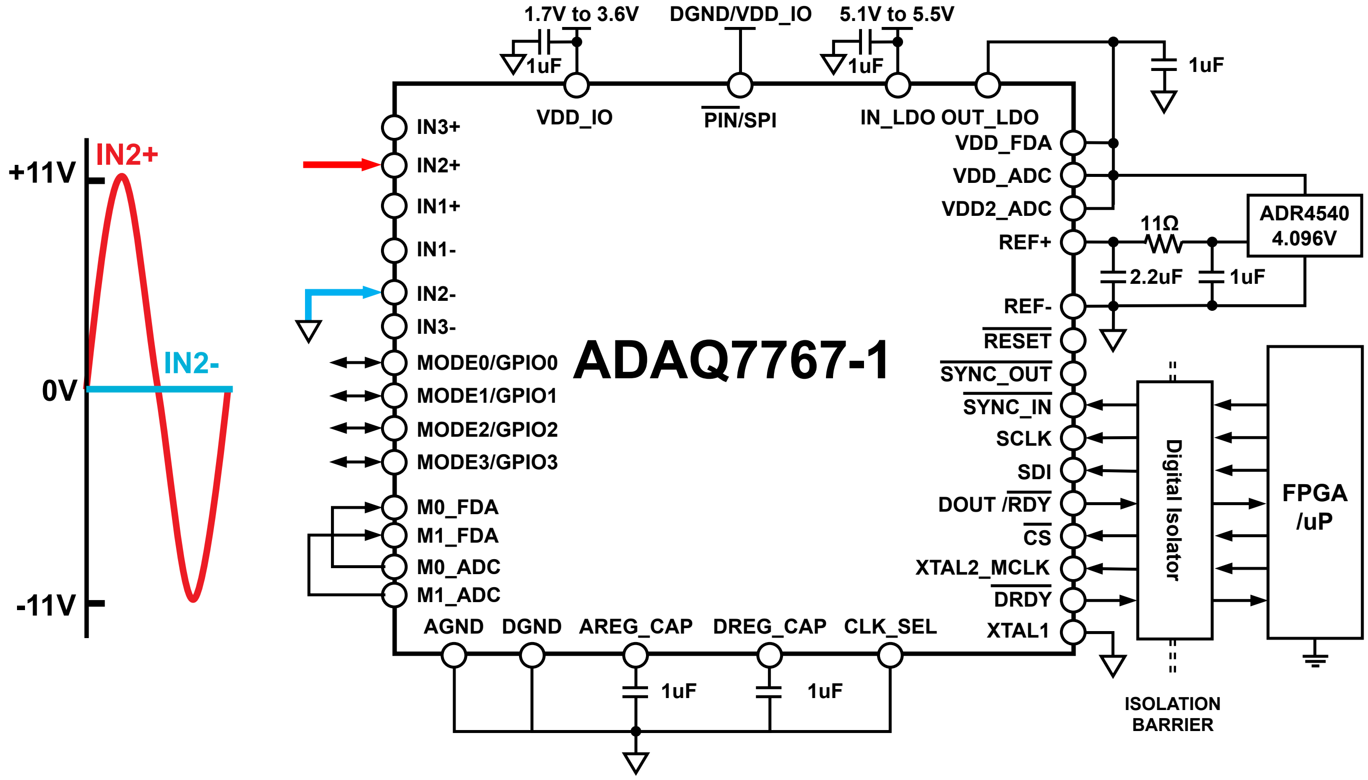

Figure 116. ADAQ7767-1 single-ended input configuration to IN2+/− (AFE_GAIN = 0.36 V/V)

APPLICATIONS INFORMATION

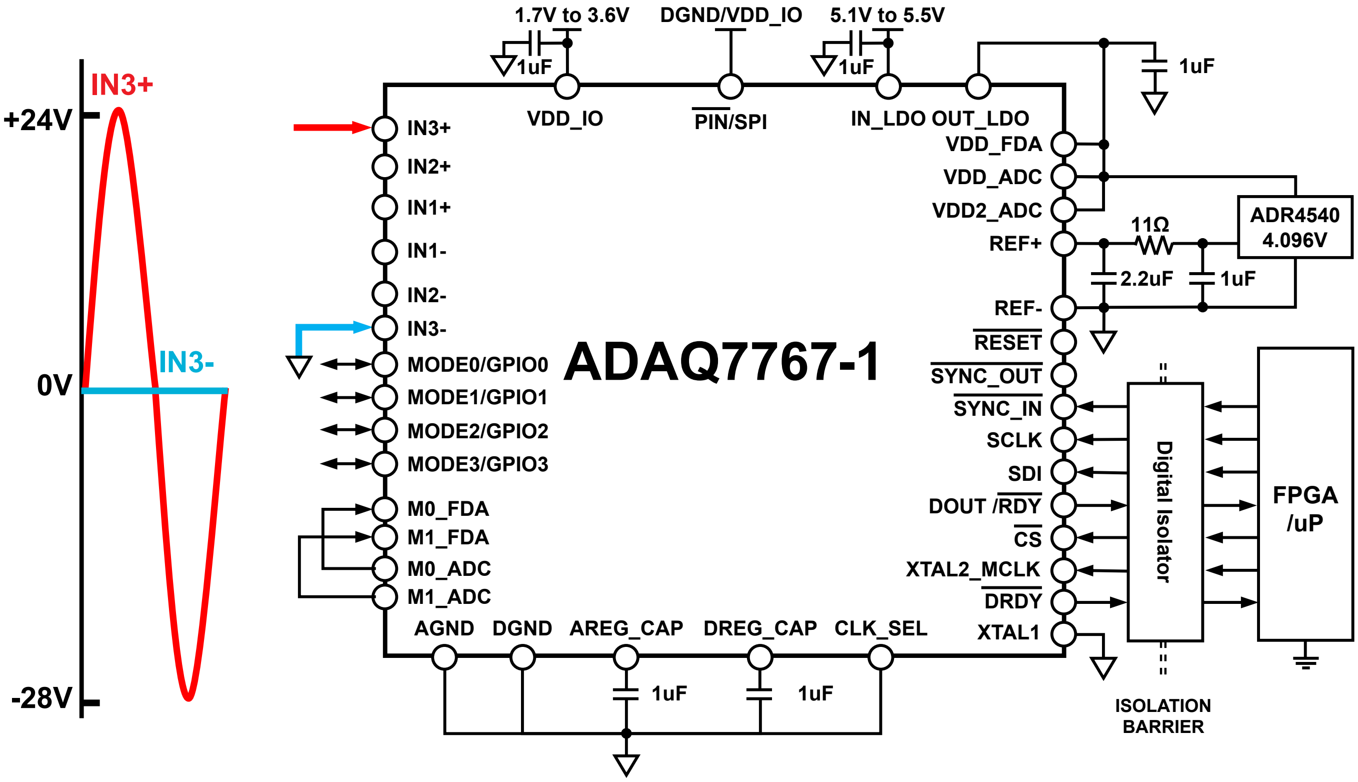

Figure 117. ADAQ7767-1 single-ended input configuration to IN3+/− (AFE_GAIN = 0.14 V/V)

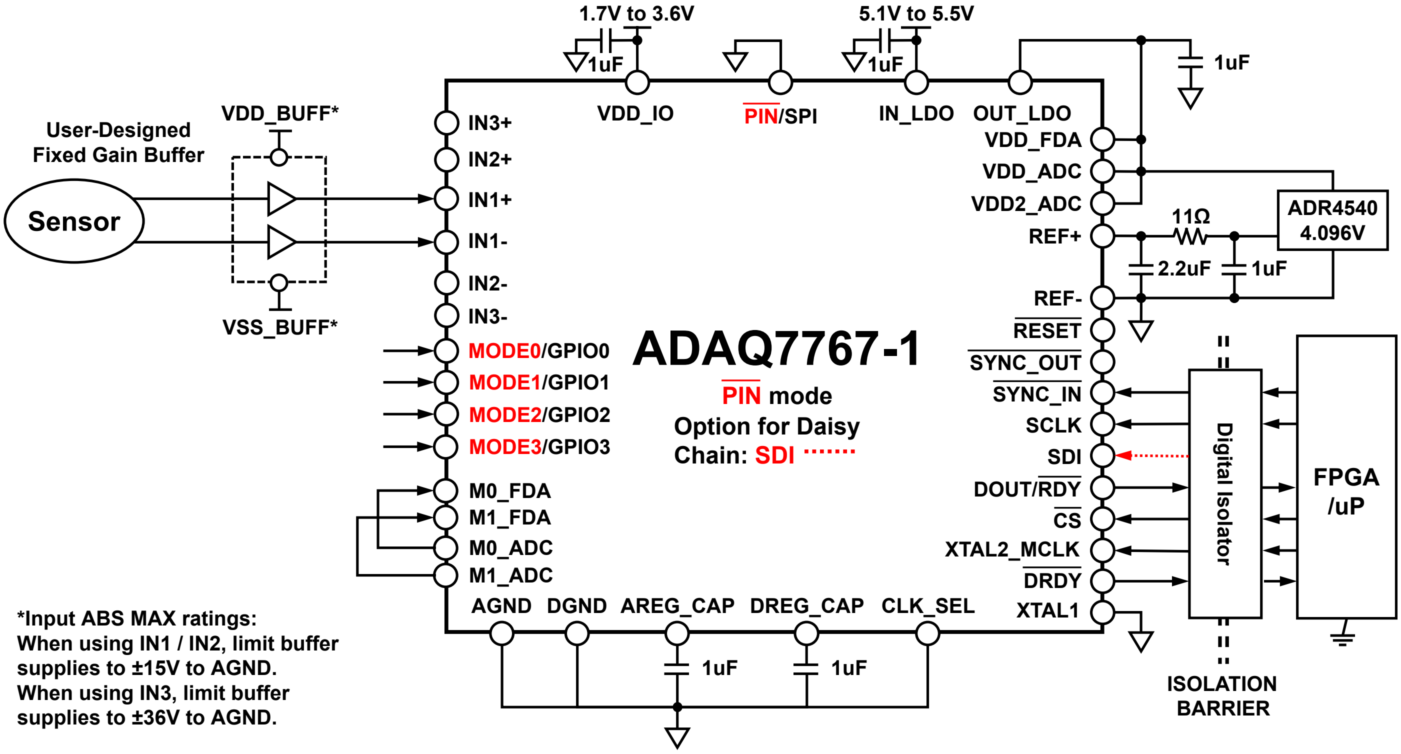

Figure 118. Typical applications diagram of DAQ system involving one sensor input and $\overline{\text{PIN}}$ mode

APPLICATIONS INFORMATION

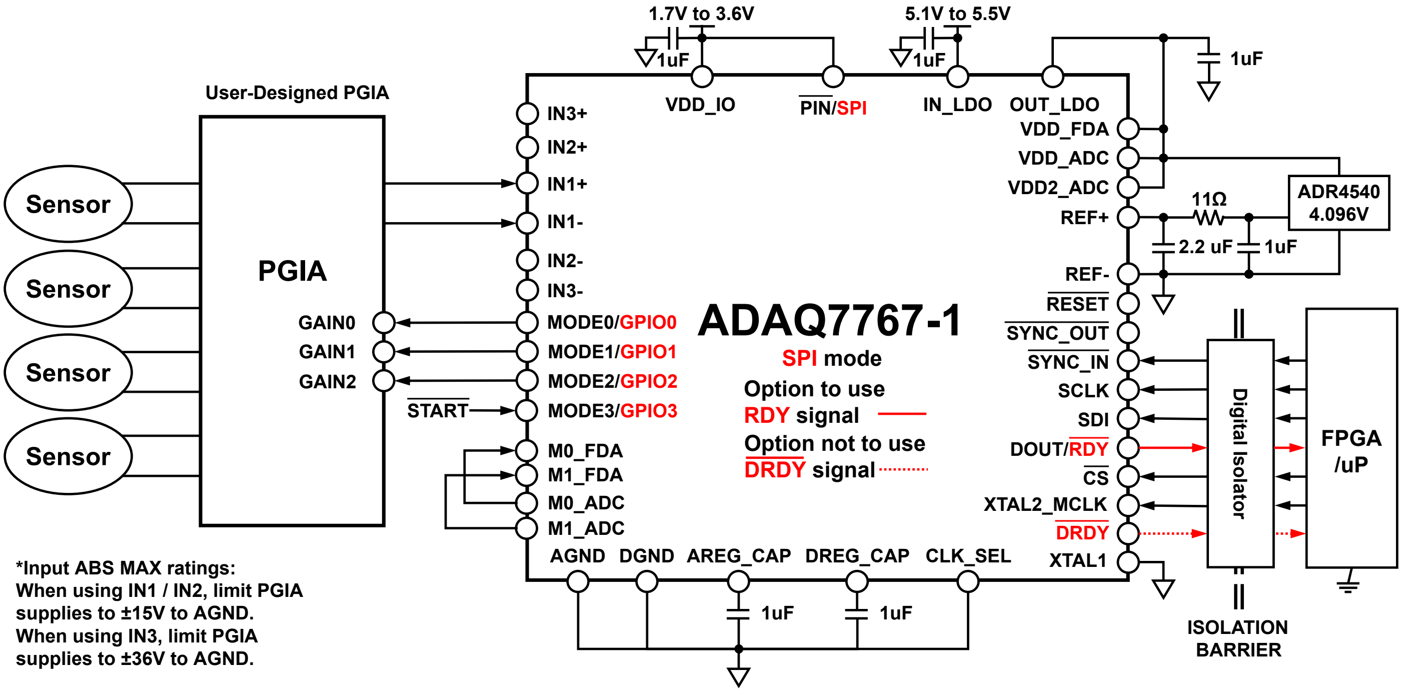

Figure 119. Typical applications diagram of DAQ system involving multiple sensor inputs and SPI Mode

SENSOR INTERFACING

The applications diagram in Figure 118 illustrates how the ADAQ7767-1 is typically used with a single sensor. In the application, an external fixed gain signal conditioning circuit designed by the user buffers between the sensor and ADAQ7767-1.

Figure 119 illustrates how the user may also use the ADAQ7767-1 using multiple sensors. In this case, an external PGIA designed by the user multiplexes and buffers multiple sensor inputs. The ADAQ7767-1 features GPIO pins which can be configured to set the gain for each channel of the user-designed PGIA.

PIN/SPI CONTROL MODE

PINControl Mode

The ADAQ7767-1 can be configured in either PIN/SPI Mode, whose distinct advantages are presented in Device Configuration Method. One of the advantages of PIN Mode is illustrated in Figure 118, wherein the MODEx pins are used to set the ADC configurations such as f_{MOD} frequency, type of digital filter, and decimation rate from a list of predetermined modes as shown in Table 25. This allows the user to make an easier choice of ADC configuration and eliminates the need to write to the ADC registers that control these configurations. Since a write is not allowed, the SDI pin can be used for daisy-chaining, which is only available in PIN control mode. To use the PIN control mode, the PIN/SPI pin should be grounded on startup.

SPI Control Mode

Figure 119 illustrates an application in SPI control mode, wherein the user utilizes the GPIOs, in this case, to control the gain of a PGIA. This can be done by configuring the GPIO port control Register (Register 0x1E) and GPIO output control register (Register 0x1F). The SPI mode also allows the complete flexibility in ADC configurations, conversion read modes, and data conversion modes. The SPI control mode in continuous read mode may use the RDY signal, which can be enabled through the Interface Format Control Register (Register 0x14), to merge the indication of new ADC data with the DOUT output stream, eliminating the need for a digital line for DRDY. To use SPI control mode, the PIN/SPI pin should be connected to high (or VDD_IO) on startup.

POWER SUPPLIES

The power supplies illustrated in Figure 118 and Figure 119 are recommended in using ADAQ7767-1 for its typical applications. Instead of using an external LDO to supply 5V to VDD_FDA, VDD_ADC, VDD2_ADC, and the external 4.096V reference, an internal LDO that accepts a voltage of 5.1V to 5.5V is included in ADAQ7767-1 to conveniently output a well-regulated 5V supply. VDD_IO is supplied with a minimum of 1.7V to power the digital logic of the ADC driver, and the GPIO and SPI of the ADC.

The ADAQ7767-1 has built-in 0.1uF supply decoupling capacitors on the VDD_FDA, VDD_ADC, VDD_ADC2, and VDD_IO supply pins. When the LDO is in use, it should be decoupled with a 1uF capacitor at IN_LDO and OUT_LDO. Additionally, the ADC's own analog and digital LDOs are also decoupled to the ground with a 1uF capacitor through pins AREG_CAP and DREG_CAP.

APPLICATIONS INFORMATION

REFERENCE AND BUFFER

While the ADC reference may range from VDD_ADC down to 1V, the typical application and specification of the ADAQ7767-1 is set with an input reference at 4.096V. This can be implemented by applying the output of the LDO to an ADR4540 to output a voltage reference of 4.096V. In PIN mode, the reference voltage is input to the ADC's internal precharge buffer by default for enhanced performance.

RECOMMENDED INTERFACE

The ADAQ7767-1 interface is flexible to allow the many modes of operation and for data output formats to work across different DSPs and microcontroller units (MCUs). To achieve maximum performance, the recommended interface configuration for reading conversion results is shown in Figure 120. This recommended implementation uses a synchronous SCLK to MCLK relationship.

Configure the interface as follows to achieve the recommended operation:

1. Tie the CS signal low during the conversion readback.
2. Enter continuous readback mode to avoid needing to provide the address bits for the ADC_DATA register. Continuous readback mode is the default readback mode in PIN mode.
3. 32 bits of data are clocked out, consisting of the 24-bit conversion result plus eight bits that can be selected to be either the status or CRC bits. In PIN mode, this is always the conversion result plus the eight status bits.
4. Provide an SCLK that is phase-coherent to MCLK. SCLK could be identical to MCLK (SCLK=MCLK), or a divided down version of MCLK (SCLK=MCLK/N). For example, SCLK = MCLK/2 in a case where decimate by 32 is selected.
5. Clocking 32 bits ensures that the data readback operation fills the entire DRDY period when SCLK = MCLK/2. SCLK runs continuously. The readback spans the full DRDY period, thus spreading the noise coupling due to the current on VDD_IO across the full ODR period.
6. The DRDY signal can synchronize the data being read into the host controller.

Figure 120 shows how the recommended interface operates. The data read back spans the entire length of the DRDY period and the LSB remains until DRDY goes high for the next conversion.

Initializing the Recommended Interface

To configure the recommended interface, take the following steps:

1. Configure the device settings, such as power mode, decimation ratio, filter type, and so on.
2. Enter continuous readback mode.
3. Issue a synchronization pulse to apply the changes to the digital domain and to reset the digital filter. Issue the pulse immediately after DRDY goes high.

Recommended Interface for Reading Data

The recommended interface for reading data is as follows:

1. Synchronize the host controller with the DRDY or RDY pulse. See Figure 6 for details on the RDY behavior before data is clocked out.
2. Generate SCLK based on the DRDY or RDY timing. SCLK is high when the DRDY signal goes high and transitions on the MCLK falling edges (see Figure 120) to ensure that the LSB can be read correctly as the DOUT/RDY output is reset on the DRDY rising edge. However, SCLK rising occurs before this transition.
3. The MSB is clocked out on the next falling edge of SCLK.
4. In PIN control mode, the LSB of the conversion output is the last bit of the status output. In PIN control mode, this bit is always 1 and, therefore, does not need to be read.

Resynchronization of the Recommended Interface

Because the full ODR period is for clocking data, the RDY signal no longer flags after each LSB outputs. This signal only flags if the ADAQ7767-1 is in continuous readback mode, or if the ADAQ7767-1 does not count 32 SCLKs within 1 × t_{MCLK} before DRDY, as is shown in Figure 120.

The RDY function is only available in continuous readback mode. In normal readback, where the ADC_DATA register must be addressed each time, the DOUT line is reset 1 × t_{MCLK} before DRDY, as per t_{10} in the Timing Specifications section. If DRDY is used, the device operates as normal, and conversion readback is timed from the DRDY pulse. In the case where RDY detects the beginning of each sample, and where the data readback loses synchronization, the SCLK timing can be recovered by one of the following two methods:

- Using CS to reset the interface and to observe the RDY transition.
- Stopping SCLK toggling until the RDY transition is detected one more time.

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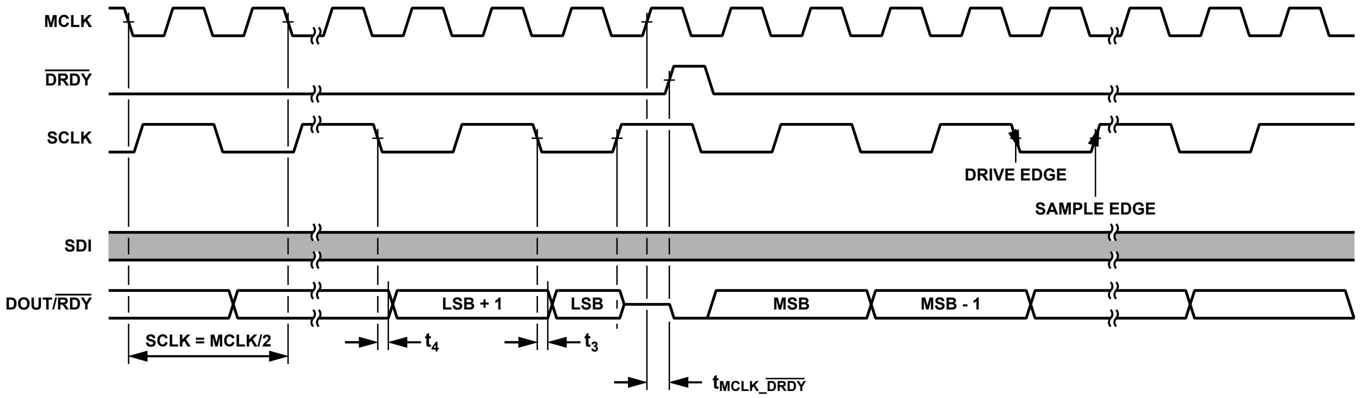

Figure 120. Recommended Interface for Reading Conversions, SPI Control, Continuous Readback Mode

PROGRAMMABLE DIGITAL FILTER

If there are additional filter requirements outside of the digital filters offered by default on the ADAQ7767-1, there is the added option of designing and uploading a custom digital filter to memory. This upload overwrites the default low ripple FIR filter coefficients to be replaced by a set of user defined coefficients.

The ADAQ7767-1 filter path has three separate stages:

- Initial sinc filter
- Sinc compensation filter
- Low ripple FIR filter

The user cannot change the first two stages. The only programmable stage is the third stage, where the default low ripple FIR filter coefficients can be replaced by a set of user-defined coefficients.

The data rate into the third stage is double the final ODR due to a fixed decimation by two that occurs after the final stage of filtering. Therefore, the programmable FIR stage receives data at a rate that is decimated from f_{MOD} by rates of 16, 32, 64, 128, 256, and 512.

After the final decimation by 2, the overall decimation values are given and are in the range of decimate by 32 to decimate by 1024. The data rates into the final FIR stage are listed in Table 28. Table 28 describes the data rate into the final filter stage for each power mode, assuming the correct MCLK_DIV setting is selected for the corresponding power mode. For example, when median power mode is selected, MCLK_DIV must be MCLK/4.

Filter Coefficients

The ADAQ7767-1 low ripple FIR filter uses a set of 112 coefficients. By writing the appropriate key to the ADAQ7767-1, these coefficients can be overwritten. Then, the customized filter coefficients can upload and lock into memory. If the ADAQ7767-1 is reset, these coefficients must be rewritten.

The coefficients uploaded are subject to the following required conditions:

- The number of coefficients in a full set is 112, which is made up of 56 coefficients that are mirrored to make the total coefficients sum 112. Therefore, only 56 coefficients are written to during any one filter upload.
- Coefficients written must be in integer form. The format used is twos complement.
- The coefficient data register to be written is 24 bits wide, which is the only 24-bit register write used on the ADAQ7767-1. Only 23 bits are used for the coefficients. The remaining MSB is a control bit, detailed in the Register 0x33.
- Filter coefficients are scaled such that the 56 coefficients must sum to 2^{22}. The total (112) coefficients, therefore, sum to 2^{23}.

For example, if the filter coefficient to be written to is −0.0123, this value is scaled to $-0.0123 \times 2^{22} = -51{,}590$. In twos complement format, this value is represented by 0x7F367A.

Each filter coefficient is written by first selecting the coefficient address. Then, a separate write of the data occurs, which is repeated for all 56 coefficients from Address 0 to Address 55.

Because the FIR size cannot be changed, the filter group delay remains fixed at 34/ODR when using the programmable filter option. If a shorter number of coefficients are required, padding before the coefficients with zeros can achieved this requirement. The group delay of the uploaded filter must always be equal to the group delay of the default ADAQ7767-1 FIR filter that equals approximately 34/ODR.

Each time either the coefficient address register or the coefficient data register (COEFF_CONTROL or COEFF_DATA) are accessed, the user must wait a period before performing another read or write. The following equation determines the wait time:

$$t_{WAIT} = 512/MCLK$$

This wait time allows time for the register contents to update. Then, the coefficients are written to memory.

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Table 28. Data Rates into the Final FIR Input Stage

	Input to Third Stage, Programmable FIR (MCLK = 16.384 MHz)								
Power Mode	512 kHz	256 kHz	128 kHz	64 kHz	32 kHz	16 kHz	8 kHz	4 kHz	2 kHz
Fast	Yes	Yes	Yes	Yes	Yes	Yes		Not applicable	Not applicable
Median	Not applicable	Yes	Yes	Yes	Yes	Yes	Yes	Not applicable	Not applicable
Low Power	Not applicable	Not applicable	Not applicable	Yes	Yes	Yes	Yes	Yes	Yes

Upload Sequence

To program a user defined set of filter coefficients, perform the following sequence:

1. Write 0x4 to the filter bits in the DIGITAL_FILTER register (Register 0x19, Bits[6:4]).
2. The following key must be written to access the filter upload. First, write 0xAC to the ACCESS_KEY register (Register 0x34). Second, write 0x45 to the ACCESS_KEY register. Bit 0 (the key bit) of the ACCESS_KEY register can be read back to check if the key is entered correctly.
3. Write 0xC0 to the COEFF_CONTROL register (Register 0x32). Wait for t_{WAIT} sec to perform the following actions:
    a. Set the coefficient address to Address 0.
    b. Enable the access to memory (COEFFACCESSEN = 1).
    c. Allow a write to the coefficient memory (COEFFWRITEEN = 1).
4. The address of the first coefficient is selected. Write the required coefficient to the COEFF_DATA register (Register 0x33), and then wait for t_{WAIT} sec. Always wait t_{WAIT} sec between writes to Register 0x32 and Register 0x33.
5. Repeat Step 4 and Step 5 for each of the 56 coefficients. For example, write 0xC1 to COEFF_CONTROL to select coefficient Address 1. After waiting t_{WAIT} sec, enter the coefficient data. Increment the data until Coefficient 55 is reached. (Coefficient 55 is a write of 0xF7 to COEFF_CONTROL.)
6. Disable writing to the coefficients by first writing 0x80 to COEFF_CONTROL. Then, wait t_{WAIT} sec. Then, write 0x00 to COEFF_CONTROL to disable coefficient access.
7. Set USERCOEFFEN = 1 by writing 0x800 to COEFF_DATA to allow the user to toggle the synchronization pulse and to begin reading data.
8. Exit the filter upload by writing 0x55 to the ACCESS_KEY register (Register 0x34).
9. Send a synchronization pulse to the ADAQ7767-1. One way of sending this pulse is by writing to the SYNC_RESET register (Register 0x1D). The filter upload is now complete.

The RAM CRC error check fails when the digital filter uploads. To disable this check, use the DIG_DIAG_ENABLE register (Register 0x2A).

Example Filter Upload

The following sequence programs a sinc1 filter. The coefficients in Address 0 to Address 23 = 0. The coefficients from Address 24 to Address 55 = 131,072 ($2^{22}/32$). When MCLK = 16.384 MHz and ODR = 256 kHz, the filter notch appears at 8 kHz and multiplies of 8 kHz. This filter provides low noise and is recognizable by the distinctive filter profile shown in Figure 121.

To program the filter, take the following steps:

1. Write 0x4 to the filter bits in the DIGITAL_FILTER register (Register 0x19, Bits[6:4]).
2. Enter the key by writing to the ACCESS_KEY register (Register 0x34).
3. Write 0xC0 to the COEFF_CONTROL register, Register 0x32, (COEFFADDR = 0, COEFFACCESSEN = 1, and COEFFWRITEEN = 1). Wait t_{WAIT} sec.
4. Write 0x000000 to COEFF_DATA (Register 0x33). Wait t_{WAIT} sec.
5. Write 0xC1 to the COEFF_CONTROL register (COEFFADDR = 1). Wait t_{WAIT} sec. In this case, the coefficient in Address 0 is equal to Address 1 and, therefore, the value in COEFF_DATA does not change.
6. Write 0xC2 to the COEFF_CONTROL register (COEFFADDR = 2). Wait t_{WAIT} sec.
7. Increment the address of the COEFF_CONTROL register (COEFFADDR = 23) until the write of 0xD7. Continue to wait t_{WAIT} sec.
8. Write 0xD8 to COEFF_CONTROL (COEFFADDR = 24).
9. Write 0x010000 to COEFF_DATA. Wait t_{WAIT} sec.
10. Write 0xD9 to COEFF_CONTROL (COEFFADDR = 25). Wait t_{WAIT} sec.
11. Write 0xDA to COEFF_CONTROL (COEFFADDR = 26) Wait t_{WAIT} sec.
12. Increment the address of the COEFF_CONTROL register (COEFFADDR = 55) until the write 0xF7. Wait t_{WAIT} sec.
13. Disable write and access by first writing 0x80 to the COEFF_CONTROL register. Wait t_{WAIT} sec. Then, write 0x00 to the COEFF_CONTROL register.
14. Set USERCOEFFEN = 1 to allow the user to toggle synchronization without reloading the default coefficients. (Write 0x800000 to COEFF_DATA.)
15. Exit the write by writing 0x55 to the ACCESS_KEY register.
16. Toggle synchronization.
17. Gather data. The resulting filter profile is shown in Figure 121.

APPLICATIONS INFORMATION

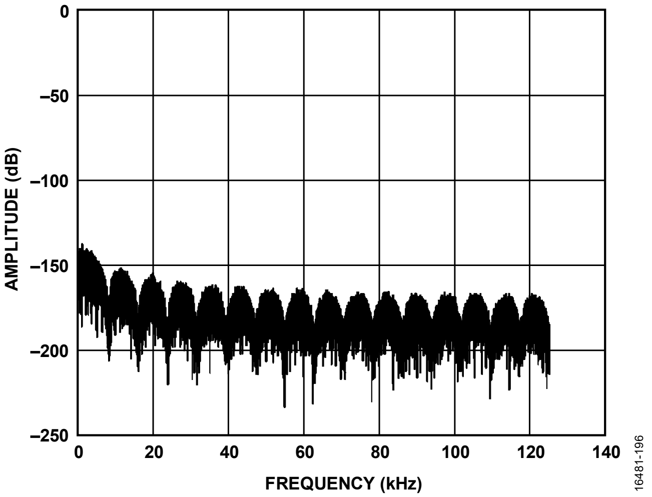

Figure 121. Example Filter Profile Upload

Filter Upload Verification

To check that the filter coefficients are uploaded correctly, it is possible to read back the values written to the COEFF_DATA register. This read can be performed after an upload by taking the following steps:

1. Enter the key by writing to the ACCESS_KEY register (Register 0x34). First, write 0xAC to the ACCESS_KEY register, and then write 0x45 to the ACCESS_KEY register.
2. Write 0x80 to the COEFF_CONTROL register, Register 0x32, (COEFFADDR = 0, COEFFACCESSEN = 1, COEFFWRITEEN = 0). Wait t_{WAIT} sec.
3. Read back the contents of the 24-bit COEFF_DATA register (Register 0x33). Check that the coefficient matches the uploaded value.
4. Write 0x81 to the COEFF_CONTROL register (COEFFADDR = 1). Wait t_{WAIT} sec.
5. Read the 24-bit COEFF_DATA register for Address 1. Increment and continue to read back the data. Continue to wait t_{WAIT} sec between updates to the COEFF_CONTROL register.
6. Disable the coefficient access by writing 0x00 to the COEFF_CONTROL register.
7. Exit the readback process by writing 0x55 to the ACCESS_KEY register.

LAYOUT GUIDELINES

The printed circuit board (PCB) that houses the ADAQ7767-1 should be designed so that the analog and digital sections are separated and confined to different areas of the board. The ADAQ7767-1 pins are laid out with analog and digital pin partitioning. It is suggested to route to the analog pins on the top layer, and to use symmetrical traces for the differential inputs. This layer should be followed by a ground plane, while the lower layers are used for the digital lines. Do not connect unused inputs (i.e. to a multiplexer), else it may degrade performance.

To minimize gain error and gain error drift, the differential inputs should have the following PCB trace resistances, measured from the signal source to the analog input pins:

Table 29. Trace Resistance for Optimal Gain Error and Gain Error Drift

Input	Trace Resistance (Ω)
IN1+ and IN1−	TBD
IN2+ and IN2−	TBD
IN3+ and IN3−	TBD

The trace resistance can be calculated by:

$$R_T = \frac{\rho * L}{W * T}$$

where *ρ* is trace material resistivity (Ω-m), *L* is trace length (m), *W* is the trace width (m), and *T* is board layer thickness (m). Copper has a resistivity of 1.7 x 10^{-8} Ω-m.

For the stack-up, at least one ground plane should be used. It can be common or split between the digital and analog sections. In the case of the split plane, the digital and analog ground planes should be joined in only one place, preferably as close as possible to the ADAQ7767-1.

If the ADAQ7767-1 are in a system where multiple devices require analog-to-digital ground connections, the connection should still be made at only one point: a star ground point that should be established as close as possible to the ADAQ7767-1. Good connections should be made to the ground plane. Avoid sharing one connection for multiple ground pins. Use individual vias or multiple vias to the ground plane for each ground pin.

Avoid running digital lines under the devices because doing so couples noise onto the die. The analog ground plane should be allowed to run under the ADAQ7767-1 to avoid noise coupling. Fast switching signals like MCLK should be shielded with digital ground to avoid radiating noise to other sections of the board, and they should never run near analog signal paths. Avoid crossover of digital and analog signals. Traces on layers in close proximity on the board should run at right angles to each other to reduce the effect of feedthrough through the board.

The power supply lines to the IN_LDO and VDD_IO pins on the ADAQ7767-1 should use as large trace as possible to provide low impedance paths and reduce the effect of glitches on the power supply lines. When possible, use of supply planes to make good connections between the ADAQ7767-1 supply pins and the power supplies on the board. Use a single via or multiple vias for each supply pin.

Decouple the REF, AREG_CAP, DREG_CAP pins with minimal parasitic inductances by placing the decoupling ceramic capacitor close to (ideally right up against) the REF, AREG_CAP, DREG_CAP, and GND pins, and connect them with wide, low impedance traces.

REGISTER SUMMARY

Table 30. ADAQ7767-1 Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x03	CHIP_TYPE	[7:0]	RESERVED				CLASS				0x07	R
0x04	PRODUCT_ID_L	[7:0]	PRODUCT_ID[7:0]								0x01	R
0x05	PRODUCT_ID_H	[7:0]	PRODUCT_ID[15:8]								0x00	R
0x06	CHIP_GRADE	[7:0]	GRADE				DEVICE_REVISION				0x00	R
0x0A	SCRATCH_PAD	[7:0]	VALUE								0x00	R/W
0x0C	VENDOR_L	[7:0]	VID[7:0]								0x56	R
0x0D	VENDOR_H	[7:0]	VID[15:8]								0x04	R
0x14	INTERFACE_FORMAT	[7:0]	LV_BOOST	EN_SPI_CRC	CRC_TYPE	STATUS_EN	CONVLEN	EN_RDY_DOUT	RESERVED	EN_CONT_READ	0x00	R/W
0x15	POWER_CLOCK	[7:0]	CLOCK_SEL		MCLK_DIV		ADC_POWER_DOWN	RESERVED	ADC_MODE		0x00	R/W
0x16	ANALOG	[7:0]	REF_BUF_POS		REF_BUF_NEG		RESERVED		LINEARITY_BOOST_A_OFF	LINEARITY_BOOST_B_OFF	0x00	R/W
0x18	CONVERSION	[7:0]	DIAG_MUX_SELECT				CONV_DIAG_SELECT	CONV_MODE			0x00	R/W
0x19	DIGITAL_FILTER	[7:0]	EN_60HZ_REJ	FILTER			RESERVED	DEC_RATE			0x00	R/W
0x1A	SINC3_DEC_RATE_MSB	[7:0]	RESERVED			SINC3_DEC[12:8]					0x00	R/W
0x1B	SINC3_DEC_RATE_LSB	[7:0]	SINC3_DEC[7:0]								0x00	R/W
0x1C	DUTY_CYCLE_RATIO	[7:0]	IDLE_TIME								0x00	R/W
0x1D	SYNC_$\overline{\text{RESET}}$	[7:0]	SPI_$\overline{\text{START}}$	$\overline{\text{SYNC_OUT}}$_POS_EDGE	RESERVED		EN_GPIO_$\overline{\text{START}}$	RESERVED	SPI_$\overline{\text{RESET}}$		0x80	R/W
0x1E	GPIO_CONTROL	[7:0]	UGPIO_EN	GPIO2_OPEN_DRAIN_EN	GPIO1_OPEN_DRAIN_EN	GPIO0_OPEN_DRAIN_EN	GPIO3_OP_EN	GPIO2_OP_EN	GPIO1_OP_EN	GPIO0_OP_EN	0x00	R/W
0x1F	GPIO_WRITE	[7:0]	RESERVED				GPIO_WRITE_3	GPIO_WRITE_2	GPIO_WRITE_1	GPIO_WRITE_0	0x00	R/W
0x20	GPIO_READ	[7:0]	RESERVED				GPIO_READ_3	GPIO_READ_2	GPIO_READ_1	GPIO_READ_0	0x00	R
0x21	OFFSET_HI	[7:0]	OFFSET[23:16]								0x00	R/W
0x22	OFFSET_MID	[7:0]	OFFSET[15:8]								0x00	R/W
0x23	OFFSET_LO	[7:0]	OFFSET[7:0]								0x00	R/W
0x24	GAIN_HI	[7:0]	GAIN[23:16]								0x00	R/W
0x25	GAIN_MID	[7:0]	GAIN[15:8]								0x00	R/W
0x26	GAIN_LO	[7:0]	GAIN[7:0]								0x00	R/W

REGISTER SUMMARY

Table 30. ADAQ7767-1 Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x28	SPI_DIAG_ENABLE	[7:0]	RESERVED			EN_ERR_SPI_IGNORE	EN_ERR_SPI_CLK_CNT	EN_ERR_SPI_RD	EN_ERR_SPI_WR	RESERVED	0x10	R/W
0x29	ADC_DIAG_ENABLE	[7:0]	RESERVED		EN_ERR_DLDO_PSM	EN_ERR_ALDO_PSM	EN_ERR_REF_DET	EN_ERR_FILTER_SATURATED	EN_ERR_FILTER_NOT_SETTLED	EN_ERR_EXT_CLK_QUAL0	0x07	R/W
0x2A	DIG_DIAG_ENABLE	[7:0]	RESERVED			EN_ERR_MEMMAP_CRC	EN_ERR_RAM_CRC	EN_ERR_FUSE_CRC	RESERVED	EN_FREQ_COUNT	0x0D	R/W
0x2C	ADC_DATA	[23:16]	ADC_READ_DATA[23:16]								0x000000	R
		[15:8]	ADC_READ_DATA[15:8]									
		[7:0]	ADC_READ_DATA[7:0]									
0x2D	MASTER_STATUS	[7:0]	MASTER_ERROR	ADC_ERROR	DIG_ERROR	ERR_EXT_CLK_QUAL	FILT_SATURATED	FILT_NOT_SETTLED	SPI_ERROR	POR_FLAG	0x00	R
0x2E	SPI_DIAG_STATUS	[7:0]	RESERVED			ERR_SPI_IGNORE	ERR_SPI_CLK_CNT	ERR_SPI_RD	ERR_SPI_WR	ERR_SPI_CRC	0x00	R/W
0x2F	ADC_DIAG_STATUS	[7:0]	RESERVED		ERR_DLDO_PSM	ERR_ALDO_PSM	ERR_REF_DET	FILT_SATURATED	FILT_NOT_SETTLED	ERR_EXT_CLK_QUAL	0x00	R
0x30	DIG_DIAG_STATUS	[7:0]	RESERVED			ERR_MEMMAP_CRC	ERR_RAM_CRC	ERR_FUSE_CRC	RESERVED		0x00	R
0x31	MCLK_COUNTER	[7:0]	MCLK_COUNTER								0x00	R
0x32	COEFF_CONTROL	[7:0]	COEFF_ACCESS_EN	COEFF_WRITE_EN	COEFF_ADDR						0x00	R/W
0x33	COEFF_DATA	[23:16]	USER_COEFF_EN	COEFF_DATA[22:16]							0x000000	R/W
		[15:8]	COEFF_DATA[15:8]									
		[7:0]	COEFF_DATA[7:0]									
0x34	ACCESS_KEY	[7:0]	RESERVED							KEY	0x00	R/W

REGISTER DETAILS

COMPONENT TYPE REGISTER

Register: 0x03, Reset: 0x07, Name: CHIP_TYPE

Table 31. Bit Descriptions for CHIP_TYPE

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	CLASS	Chip Type 111: Analog to digital converter.	0x7	R

UNIQUE PRODUCT ID REGISTER

Register: 0x04, Reset: 0x01, Name: PRODUCT_ID_L

Table 32. Bit Descriptions for PRODUCT_ID_L

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[7:0]	Product ID	0x1	R

Register: 0x05, Reset: 0x00, Name: PRODUCT_ID_H

Table 33. Bit Descriptions for PRODUCT_ID_H

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[15:8]	Product ID	0x0	R

DEVICE GRADE AND REVISION REGISTER

Register: 0x06, Reset: 0x00, Name: CHIP_GRADE

Table 34. Bit Descriptions for CHIP_GRADE

Bits	Bit Name	Description	Reset	Access
[7:4]	GRADE	Device Grade	0x0	R
[3:0]	DEVICE_REVISION	Device Revision ID	0x0	R

USER SCRATCHPAD REGISTER

Register: 0x0A, Reset: 0x00, Name: SCRATCH_PAD

Table 35. Bit Descriptions for SCRATCH_PAD

Bits	Bit Name	Description	Reset	Access
[7:0]	VALUE	Scratch PAD - Read/Write area communication/POR check	0x0	R/W

DEVICE VENDOR ID REGISTER

Register: 0x0C, Reset: 0x56, Name: VENDOR_L

Table 36. Bit Descriptions for VENDOR_L

Bits	Bit Name	Description	Reset	Access
[7:0]	VID[7:0]	Vendor ID	0x56	R

Register: 0x0D, Reset: 0x04, Name: VENDOR_H

REGISTER DETAILS

Table 37. Bit Descriptions for VENDOR_H

Bits	Bit Name	Description	Reset	Access
[7:0]	VID[15:8]	Vendor ID	0x4	R

INTERFACE FORMAT CONTROL REGISTER

Register: 0x14, Reset: 0x00, Name: INTERFACE_FORMAT

Table 38. Bit Descriptions for INTERFACE_FORMAT

Bits	Bit Name	Description	Reset	Access
7	LV_BOOST	Boosts drive strength of SPI output for use with IOVDD levels of 1.8 V, or when a high capacitive-load is present on the DOUT/RDY pin. The default state is LV_BOOST enabled when in the PIN control mode. 0: Disables LV_BOOST. 1: Enables LV_BOOST. Re-enable this bit following an exit from the continuous read mode, if applicable.	0x0	R/W
6	EN_SPI_CRC	Activates CRC on all SPI transactions 0: Disable CRC function on all SPI transfers. 1: Enable CRC function on all SPI transfers.	0x0	R/W
5	CRC_TYPE	Selects CRC method as XOR or 8-bit polynomial 1: XOR instead of CRC (applied to READ transactions only). 0: CRC bits are based on CRC-8 Polynomial.	0x0	R/W
4	STATUS_EN	Enables Status bits output. In the SPI control mode, the status bits can be output after the ADC conversion result by setting the bits in this bit field. In the PIN control mode, the status bits are output after the ADC conversion result. 0: Disable outputting STATUS bits after ADC result in the continuous read mode. 1: Output STATUS bits after ADC result in the continuous read mode.	0x0	R/W
3	CONVLEN	Conversion Result Output Length 0: Full 24 BIT. 1: Output only 16 MSB of the ADC result.	0x0	R/W
2	EN_RDY_DOUT	Enables RDY signal on DOUT/RDY pin. Enables RDY indicator on DOUT/RDY pin in the continuous read mode. By default, the DOUT/RDY pin does not signal when new ADC conversion data is ready. Setting this bit causes DOUT/RDY to signal the availability of ADC conversion data. 0: Disables RDY function on DOUT/RDY pin in the continuous read mode after result is clocked out. 1: Enables RDY function on DOUT/RDY pin in continuous read mode after result has been clocked out.	0x0	R/W
1	RESERVED	Reserved.	0x0	R
0	EN_CONT_READ	Continuous read enable bit 0: Disable Continuous Read Mode. 1: Enable Continuous Read Mode.	0x0	R/W

POWER AND CLOCK CONTROL REGISTER

Register: 0x15, Reset: 0x00, Name: POWER_CLOCK

Table 39. Bit Descriptions for POWER_CLOCK

Bits	Bit Name	Description	Reset	Access
[7:6]	CLOCK_SEL	Options for setting the clock used by the device 00: CMOS clock on XTAL2_MCLK. 01: Crystal oscillator. 10: LVDS input enable. 11: Internal coarse RC clock (diagnostics).	0x0	R/W
[5:4]	MCLK_DIV	Sets the division of the MCLK to create the ADC modulator frequency f_{MOD}. 00: Modulator CLK is equal to Master clock divided by 16. 01: Modulator CLK is equal to Master clock divided by 8.	0x0	R/W

REGISTER DETAILS

Table 39. Bit Descriptions for POWER_CLOCK (Continued)

Bits	Bit Name	Description	Reset	Access
		10: Modulator CLK is equal to Master clock divided by 4. 11: Modulator CLK is equal to Master clock divided by 2.		
3	ADC_POWER_DOWN	Places ADC into a power down state. All blocks including the SPI are powered down. The standard SPI is not active in this state. Power-down is the lowest power consumption mode. To enter power-down mode, write 0x08 to this register. If the user attempts to set Bit 3 while also setting other bits in this register, the SPI write command is ignored, the device does not enter power-down, and the other bits are not set. Power-down mode can be exited in three ways: by a reset using the $\overline{\text{RESET}}$ pin, by issuing the SPI resume command over SDI and SCLK, or by using the power cycle of the device.	0x0	R/W
2	RESERVED	Reserved.	0x0	R/W
[1:0]	ADC_MODE	Sets the operation mode of the ADC core. This setting in conjunction with MCLK_DIV create the conditions for the power scaling the ADC versus input bandwidth/throughput. 00: Low Power Mode. 01: Median Power Mode. 11: Fast Power Mode.	0x0	R/W

ANALOG BUFFER CONTROL REGISTER

Register: 0x16, Reset: 0x00, Name: ANALOG

Used to turn on or off front end buffering.

Table 40. Bit Descriptions for ANALOG

Bits	Bit Name	Description	Reset	Access
[7:6]	REF_BUF_POS	Buffering options for the reference positive input. 00: Precharge reference buffer on. 01: Unbuffered reference input. 10: Full reference buffer on.	0x0	R/W
[5:4]	REF_BUF_NEG	Buffering options for the reference negative input. 00: Precharge Reference buffer on. 01: Unbuffered input. 10: Full Reference buffer on.	0x0	R/W
[3:2]	RESERVED	Reserved.	0x0	R
1	LINEARITY_BOOST_A_OFF	Linearity boost buffer A disable control. Setting this bit will disable the linearity boost buffer A. Use in conjunction with LINEARITY_BOOST_B_OFF. 0: Linearity boost buffer A enable. 1: Linearity boost buffer A disable.	0x0	R/W
0	LINEARITY_BOOST_B_OFF	Linearity boost buffer B disable control. Setting this bit will disable the linearity boost buffer B. Use in conjunction with LINEARITY_BOOST_A_OFF. 0: Linearity boost buffer B enable. 1: Linearity boost buffer B disable.	0x0	R/W

CONVERSION SOURCE SELECT AND MODE CONTROL REGISTER

Register: 0x18, Reset: 0x00, Name: CONVERSION

Table 41. Bit Descriptions for CONVERSION

Bits	Bit Name	Description	Reset	Access
[7:4]	DIAG_MUX_SELECT	Selects which signal to route through diagnostic mux. Perform diagnostic checks in low-power mode only. 0000: Temperature sensor. 1000: ADC input short (zero check). 1001: Positive full scale.	0x0	R/W

REGISTER DETAILS

Table 41. Bit Descriptions for CONVERSION (Continued)

Bits	Bit Name	Description	Reset	Access
		1010: Negative full scale.		
3	CONV_DIAG_SELECT	Select the ADC's input for conversion as normal or diagnostic mux 0: Converting signal through the normal signal chain. 1: ADC converting (and turning on) diagnostic subblocks.	0x0	R/W
[2:0]	CONV_MODE	Sets the conversion mode of the ADC. 000: Continuous Conversion Mode. The modulator is converting continuously. Continuous DRDY pulse for every filter conversion. 001: Continuous One-Shot Mode. One shot is the method of using the SYNC_IN time to start a conversion. It is similar to a conversion start signal when using the one-shot mode. The ADC modulator is continuously running while waiting on a SYNC_IN rising edge. On release of a pulse (low to high transition) to the SYNC_IN pin, a new conversion begins, converting and integrating over the settling time of the filter selected. DRDY toggles when the conversion completes, indicating it is available for readback over the SPI. 010: Single-Conversion Standby Mode. In single-conversion standby mode, the ADC runs one conversion with the selected filter, sampling and integrating over the full settling time of the filter before providing a single conversion result. After the conversion is complete, the ADC goes into standby. Initiating another single conversion from standby means that there is a start-up time to come out of standby before the ADC begins converting to produce the single conversion. This mode is recommended for use in the low-power mode. 011: Duty Cycled Conversion Standby Mode. Low-power periodic conversion is a method of setting the single conversion to run in a timed loop. A separate register sets the ratio for the time spent in standby vs. converting. The ADC automatically comes out of standby periodically, performs a single conversion, and then returns to standby without the need to initiate the single conversion over the SPI. 100: Standby.	0x0	R/W

DIGITAL FILTER AND DECIMATION CONTROL REGISTER

Register: 0x19, Reset: 0x00, Name: DIGITAL_FILTER

Table 42. Bit Descriptions for DIGITAL_FILTER

Bits	Bit Name	Description	Reset	Access
7	EN_60HZ_REJ	For use with Sinc3 filter only. First, program the Sinc3 filter to output at 50Hz. Subsequently selecting the EN_60HZ_REJ bit allows one zero of the Sinc3 filter to fall at 60Hz. This bit will only enable rejection of both 50 and 60Hz if it is set in combination with programming Sinc3 filter for 50Hz ODR. 0: Sinc3 Filter optimized for single frequency rejection - 50Hz or 60Hz. 1: Filter operation is modified to allow both 50Hz and 60Hz Rejection.	0x0	R/W
[6:4]	FILTER	Selects the style of filter for use 000: Sinc5 filter. Decimate x32 to x1024. Use DEC_RATE bits to select one of six available decimation rates from x32 to x1024. 001: Sinc5 filter. Decimate x8 only. Enables a maximum data rate of 1MHz. This path allows viewing of wider bandwidth, however it is quantization noise limited so output data is reduced to 16-bits. 010: Sinc5 filter. Decimate x16 only. Enables a maximum data rate of 512 kHz. This path allows viewing of wider bandwidth. 011: Sinc3 filter. Programmable decimation rate. Decimation rate is selected via SINC3_DEC bits in Sinc3 decimation rate MSB and LSB registers. The Sinc3 filter can be tuned to reject 50 or 60Hz. With the EN_60HZ_REJ bit set, it can allow rejection of both 50 and 60Hz when used with a 16.384 MHz MCLK. 100: Wideband low ripple filter. FIR filter with low ripple passband and sharp transition band. Use DEC_RATE bits to select one of six available decimation rates from x32 to x1024.	0x0	R/W
3	RESERVED	Reserved.	0x0	R
[2:0]	DEC_RATE	Selects the Decimation rate for the Sinc5 filter and the Wideband Low Ripple FIR filter. 000: Decimate x32. 001: Decimate x64.	0x0	R/W

REGISTER DETAILS

Table 42. Bit Descriptions for DIGITAL_FILTER (Continued)

Bits	Bit Name	Description	Reset	Access
		010: Decimate x128. 011: Decimate x256. 100: Decimate x512. 101: Decimate x1024. 110: Decimate x1024. 111: Decimate x1024.		

SINC3 DECIMATION RATE (MSB) REGISTER

Register: 0x1A, Reset: 0x00, Name: SINC3_DEC_RATE_MSB

Table 43. Bit Descriptions for SINC3_DEC_RATE_MSB

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	SINC3_DEC[12:8]	Determines the decimation rate of used with the Sinc3 filter. Value entered is incremented by 1 and multiplied by 32 to give actual decimation rate	0x0	R/W

SINC3 DECIMATION RATE (LSB) REGISTER

Register: 0x1B, Reset: 0x00, Name: SINC3_DEC_RATE_LSB

Table 44. Bit Descriptions for SINC3_DEC_RATE_LSB

Bits	Bit Name	Description	Reset	Access
[7:0]	SINC3_DEC[7:0]	Determines the decimation rate of used with the Sinc3 filter. Value entered is incremented by 1 and multiplied by 32 to give actual decimation rate	0x0	R/W

PERIODIC CONVERSION RATE CONTROL REGISTER

Register: 0x1C, Reset: 0x00, Name: DUTY_CYCLE_RATIO

Table 45. Bit Descriptions for DUTY_CYCLE_RATIO

Bits	Bit Name	Description	Reset	Access
[7:0]	IDLE_TIME	Sets idle time for periodic conversion when in standby. 1 in this register corresponds to time for one output from filter selected. The value in this register is incremented by one and doubled.	0x0	R/W

SYNCHRONIZATION MODES AND RESET TRIGGERING REGISTER

Register: 0x1D, Reset: 0x80, Name: SYNC_RESET

Table 46. Bit Descriptions for SYNC_RESET

Bits	Bit Name	Description	Reset	Access
7	SPI_START	Trigger START signal. Initiates a SYNC_OUT pulse over SPI. Setting this bit low drives a low pulse through SYNC_OUT, which can be used as a SYNC_IN signal to the same device and other ADAQ7767-1 devices where synchronized sampling is required. This bit clears itself after use.	0x1	R
6	SYNC_OUT_POS_EDGE	SYNC_OUT drive edge select. Setting this bit causes SYNC_OUT to be driven low by the positive edge of MCLK. Device default is that SYNC_OUT is driven low on the negative edge of MCLK.	0x0	R/W
[5:4]	RESERVED	Reserved.	0x0	R
3	EN_GPIO_START	Enable START function on the GPIO input. Allows to use one of the GPIO pins as a START input pin. When enabled, a low pulse on the START input generates a low pulse through SYNC_OUT that can be used as a SYNC_IN signal to the same device and other ADAQ7767-1 devices where synchronized sampling is required. When enabled, GPIO3 becomes the START input. While the START function is enabled, the GPIOx pins cannot be used for general-purpose input/output reading and writing. The remaining GPIOs are set to outputs.	0x0	R/W

REGISTER DETAILS

Table 46. Bit Descriptions for SYNC_RESET (Continued)

Bits	Bit Name	Description	Reset	Access
		0: Disable. 1: Enable.		
2	RESERVED	Reserved.	0x0	R
[1:0]	SPI_$\overline{\text{RESET}}$	Enables device reset over SPI. Two writes to these bits are required to initiate the reset. First set the bits to 11, then set the bits to 10. Once this sequence is detected on these two bits, the reset occurs. It is not dependent on other bits in this register being set or cleared.	0x0	R/W

GPIO PORT CONTROL REGISTER

Register: 0x1E, Reset: 0x00, Name: GPIO_CONTROL

Table 47. Bit Descriptions for GPIO_CONTROL

Bits	Bit Name	Description	Reset	Access
7	UGPIO_EN	Universal enabling of GPIO pins. This bit must be set HI to change GPIO settings.	0x0	R/W
6	GPIO2_OPEN_DRAIN_EN	Change GPIO2 output from strong driver to open drain	0x0	R/W
5	GPIO1_OPEN_DRAIN_EN	Change GPIO1 output from strong driver to open drain	0x0	R/W
4	GPIO0_OPEN_DRAIN_EN	Change GPIO0 output from strong driver to open drain	0x0	R/W
3	GPIO3_OP_EN	Output Enable for GPIO pin. 0 -> input, 1-> output	0x0	R/W
2	GPIO2_OP_EN	Output Enable for GPIO pin. 0 -> input, 1-> output	0x0	R/W
1	GPIO1_OP_EN	Output Enable for GPIO pin. 0 -> input, 1-> output	0x0	R/W
0	GPIO0_OP_EN	Output Enable for GPIO pin. 0 -> input, 1-> output	0x0	R/W

GPIO OUTPUT CONTROL REGISTER

Register: 0x1F, Reset: 0x00, Name: GPIO_WRITE

Table 48. Bit Descriptions for GPIO_WRITE

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
3	GPIO_WRITE_3	Write to this bit to set GPIO[3] HI	0x0	R/W
2	GPIO_WRITE_2	Write to this bit to set GPIO[2] HI	0x0	R/W
1	GPIO_WRITE_1	Write to this bit to set GPIO[1] HI	0x0	R/W
0	GPIO_WRITE_0	Write to this bit to set GPIO[0] HI	0x0	R/W

GPIO INPUT READ REGISTER

Register: 0x20, Reset: 0x00, Name: GPIO_READ

Table 49. Bit Descriptions for GPIO_READ

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
3	GPIO_READ_3	Read the value from GPIO[3]	0x0	R
2	GPIO_READ_2	Read the value from GPIO[2]	0x0	R
1	GPIO_READ_1	Read the value from GPIO[1]	0x0	R
0	GPIO_READ_0	Read the value from GPIO[0]	0x0	R

OFFSET CALIBRATION MSB REGISTER

Register: 0x21, Reset: 0x00, Name: OFFSET_HI

REGISTER DETAILS

Table 50. Bit Descriptions for OFFSET_HI

Bits	Bit Name	Description	Reset	Access
[7:0]	OFFSET[23:16]	User offset calibration coefficient. The offset correction registers provide 24-bit, signed, twos-complement registers for channel offset adjustment. If the channel gain setting is at its ideal nominal value of 0x555555, an LSB of offset register adjustment changes the digital output by −4/3 LSBs. For example, changing the offset register from 0 to 100 changes the digital output by −133 LSBs. The user offset calibration coefficient correction is applied to the digital filter output data before the gain calibration correction, so the ratio above changes linearly with any gain adjustment applied via the gain calibration registers.	0x0	R/W

OFFSET CALIBRATION MID REGISTER

Register: 0x22, Reset: 0x00, Name: OFFSET_MID

Table 51. Bit Descriptions for OFFSET_MID

Bits	Bit Name	Description	Reset	Access
[7:0]	OFFSET[15:8]	User offset calibration coefficient. The offset correction registers provide 24-bit, signed, twos-complement registers for channel offset adjustment. If the channel gain setting is at its ideal nominal value of 0x555555, an LSB of offset register adjustment changes the digital output by −4/3 LSBs. For example, changing the offset register from 0 to 100 changes the digital output by −133 LSBs. The user offset calibration coefficient correction is applied to the digital filter output data before the gain calibration correction, so the ratio above changes linearly with any gain adjustment applied via the gain calibration registers.	0x0	R/W

OFFSET CALIBRATION LSB REGISTER

Register: 0x23, Reset: 0x00, Name: OFFSET_LO

Table 52. Bit Descriptions for OFFSET_LO

Bits	Bit Name	Description	Reset	Access
[7:0]	OFFSET[7:0]	User offset calibration coefficient. The offset correction registers provide 24-bit, signed, twos-complement registers for channel offset adjustment. If the channel gain setting is at its ideal nominal value of 0x555555, an LSB of offset register adjustment changes the digital output by −4/3 LSBs. For example, changing the offset register from 0 to 100 changes the digital output by −133 LSBs. The user offset calibration coefficient correction is applied to the digital filter output data before the gain calibration correction, so the ratio above changes linearly with any gain adjustment applied via the gain calibration registers.	0x0	R/W

GAIN CALIBRATION MSB REGISTER

Register: 0x24, Reset: 0x00, Name: GAIN_HI

Table 53. Bit Descriptions for GAIN_HI

Bits	Bit Name	Description	Reset	Access
[7:0]	GAIN[23:16]	User gain calibration coefficient. The ADC has an associated factory programmed gain calibration coefficient. The coefficient is stored in the ADC during factory programming and the nominal value is around 0x555555. The user can read back the factory programmed value, and may overwrite the gain register setting to apply their own calibration coefficient. The user offset calibration coefficient correction is applied to the digital filter output data before the gain calibration correction.	0x0	R/W

GAIN CALIBRATION MID REGISTER

Register: 0x25, Reset: 0x00, Name: GAIN_MID

Table 54. Bit Descriptions for GAIN_MID

Bits	Bit Name	Description	Reset	Access
[7:0]	GAIN[15:8]	User gain calibration coefficient. The ADC has an associated factory programmed gain calibration coefficient. The coefficient is stored in the ADC during factory programming and the nominal value is around 0x555555. The user can read back the factory programmed value, and may overwrite the gain register setting to apply their own calibration	0x0	R/W

REGISTER DETAILS

Table 54. Bit Descriptions for GAIN_MID (Continued)

Bits	Bit Name	Description	Reset	Access
		coefficient. The user offset calibration coefficient correction is applied to the digital filter output data before the gain calibration correction.		

GAIN CALIBRATION LSB REGISTER

Register: 0x26, Reset: 0x00, Name: GAIN_LO

Table 55. Bit Descriptions for GAIN_LO

Bits	Bit Name	Description	Reset	Access
[7:0]	GAIN[7:0]	User gain calibration coefficient. The ADC has an associated factory programmed gain calibration coefficient. The coefficient is stored in the ADC during factory programming and the nominal value is around 0x555555. The user can read back the factory programmed value, and may overwrite the gain register setting to apply their own calibration coefficient. The user offset calibration coefficient correction is applied to the digital filter output data before the gain calibration correction.	0x0	R/W

SPI INTERFACE DIAGNOSTIC CONTROL REGISTER

Register: 0x28, Reset: 0x10, Name: SPI_DIAG_ENABLE

Table 56. Bit Descriptions for SPI_DIAG_ENABLE

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
4	EN_ERR_SPI_IGNORE	SPI Ignore Error Enable	0x1	R/W
3	EN_ERR_SPI_CLK_CNT	SPI Clock Count Error Enable. The SPI clock count error is only valid for SPI transactions that use $\overline{\text{CS}}$.	0x0	R/W
2	EN_ERR_SPI_RD	SPI Read Error Enable	0x0	R/W
1	EN_ERR_SPI_WR	SPI Write Error Enable	0x0	R/W
0	RESERVED	Reserved.	0x0	R

ADC DIAGNOSTIC FEATURE CONTROL REGISTER

Register: 0x29, Reset: 0x07, Name: ADC_DIAG_ENABLE

Table 57. Bit Descriptions for ADC_DIAG_ENABLE

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	EN_ERR_DLDO_PSM	DLDO PSM Error Enable	0x0	R/W
4	EN_ERR_ALDO_PSM	ALDO PSM Error Enable	0x0	R/W
3	EN_ERR_REF_DET	REF DET Error Enable	0x0	R/W
2	EN_ERR_FILTER_SATURATED	Filter Saturated Error Enable	0x1	R/W
1	EN_ERR_FILTER_NOT_SETTLED	Filter Not Settled Error Enable	0x1	R/W
0	EN_ERR_EXT_CLK_QUAL	Enable qualification check on external clock	0x1	R/W

DIGITAL DIAGNOSTIC FEATURE CONTROL REGISTER

Register: 0x2A, Reset: 0x0D, Name: DIG_DIAG_ENABLE

Table 58. Bit Descriptions for DIG_DIAG_ENABLE

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
4	EN_ERR_MEMMAP_CRC	Memmap CRC Error Enable	0x0	R/W
3	EN_ERR_RAM_CRC	RAM CRC Error Enable	0x1	R/W

REGISTER DETAILS

Table 58. Bit Descriptions for DIG_DIAG_ENABLE (Continued)

Bits	Bit Name	Description	Reset	Access
2	EN_ERR_FUSE_CRC	Fuse CRC Error Enable	0x1	R/W
1	RESERVED	Reserved.	0x0	R/W
0	EN_FREQ_COUNT	Enable MCLK counter	0x1	R/W

CONVERSION RESULT REGISTER

Register: 0x2C, Reset: 0x00000000, Name: ADC_DATA

Table 59. Bit Descriptions for ADC_DATA

Bits	Bit Name	Description	Reset	Access
[23:0]	ADC_READ_DATA	ADC Read Data	0x0	R

DEVICE ERROR FLAGS MASTER REGISTER

Register: 0x2D, Reset: 0x00, Name: MASTER_STATUS

Table 60. Bit Descriptions for MASTER_STATUS

Bits	Bit Name	Description	Reset	Access
7	MASTER_ERROR	Master Error	0x0	R
6	ADC_ERROR	Any ADC Error (OR)	0x0	R
5	DIG_ERROR	Any Digital Error (OR)	0x0	R
4	ERR_EXT_CLK_QUAL	No Clock Error - Applied to Master Status Register Only	0x0	R
3	FILT_SATURATED	Filter Saturated	0x0	R
2	FILT_NOT_SETTLED	Filter Not Settled	0x0	R
1	SPI_ERROR	Any SPI Error (OR)	0x0	R
0	POR_FLAG	POR Flag	0x0	R

SPI INTERFACE ERROR REGISTER

Register: 0x2E, Reset: 0x00, Name: SPI_DIAG_STATUS

Table 61. Bit Descriptions for SPI_DIAG_STATUS

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
4	ERR_SPI_IGNORE	SPI Ignore Error	0x0	R/W1C
3	ERR_SPI_CLK_CNT	SPI Clock Count Error	0x0	R
2	ERR_SPI_RD	SPI Read Error	0x0	R/W1C
1	ERR_SPI_WR	SPI Write Error	0x0	R/W1C
0	ERR_SPI_CRC	SPI CRC Error	0x0	R/W1C

ADC DIAGNOSTICS OUTPUT REGISTER

Register: 0x2F, Reset: 0x00, Name: ADC_DIAG_STATUS

Table 62. Bit Descriptions for ADC_DIAG_STATUS

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	ERR_DLDO_PSM	DLDO PSM Error	0x0	R
4	ERR_ALDO_PSM	ALDO PSM Error	0x0	R
3	ERR_REF_DET	REF DET Error	0x0	R

REGISTER DETAILS

Table 62. Bit Descriptions for ADC_DIAG_STATUS (Continued)

Bits	Bit Name	Description	Reset	Access
2	FILT_SATURATED	Filter Saturated	0x0	R
1	FILT_NOT_SETTLED	Filter Not Settled	0x0	R
0	ERR_EXT_CLK_QUAL	No Clock Error - Applied to Master Status Register Only	0x0	R

DIGITAL DIAGNOSTICS OUTPUT REGISTER

Register: 0x30, Reset: 0x00, Name: DIG_DIAG_STATUS

Table 63. Bit Descriptions for DIG_DIAG_STATUS

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
4	ERR_MEMMAP_CRC	Memmap CRC Error	0x0	R
3	ERR_RAM_CRC	RAM CRC Error	0x0	R
2	ERR_FUSE_CRC	Fuse CRC Error	0x0	R
[1:0]	RESERVED	Reserved.	0x0	R

MCLK DIAGNOSTIC OUTPUT REGISTER

Register: 0x31, Reset: 0x00, Name: MCLK_COUNTER

Table 64. Bit Descriptions for MCLK_COUNTER

Bits	Bit Name	Description	Reset	Access
[7:0]	MCLK_COUNTER	MCLK Counter. This register increments after every 64 MCLKs.	0x0	R

COEFFICIENT CONTROL REGISTER

Register: 0x32, Reset: 0x00, Name: COEFF_CONTROL

Table 65. Bit Descriptions for COEFF_CONTROL

Bits	Bit Name	Description	Reset	Access
7	COEFF_ACCESS_EN	Setting this bit to a 1 allows access to the coefficient memory.	0x0	R/W
6	COEFF_WRITE_EN	Enables write to the coefficient memory. Write a 1 to enable.	0x0	R/W
[5:0]	COEFF_ADDR	Address to be accessed for the coefficient memory. The address ranges from 0 to 55 for 56 coefficients that form one symmetrical half of the 112 coefficients.	0x00	R/W

COEFFICIENT DATA REGISTER

Register: 0x33, Reset: 0x00, Name: COEFF_DATA

Table 66. Bit Descriptions for COEFF_DATA

Bits	Bit Name	Description	Reset	Access
23	USER_COEFF_EN	Setting this bit to a 1 prevents the coefficients from ROM over writing the user defined coefficients after a sync toggle. A sync pulse is required after every change to the digital filter configuration, including a customized filter upload.	0x0	R/W
[22:0]	COEFF_DATA	Data read from or to be written to coefficient memory. These bits are 23 bits wide.	0x000000	R/W

ACCESS KEY REGISTER

Register: 0x34, Reset: 0x00, Name: ACCESS_KEY

REGISTER DETAILS

Table 67. Bit Descriptions for ACCESS_KEY

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	Key	A specific key must be written to the ACCESS_KEY register prior to any filter upload. If written correctly, the key bit reads back as 1.	0x0	R/W

OUTLINE DIMENSIONS

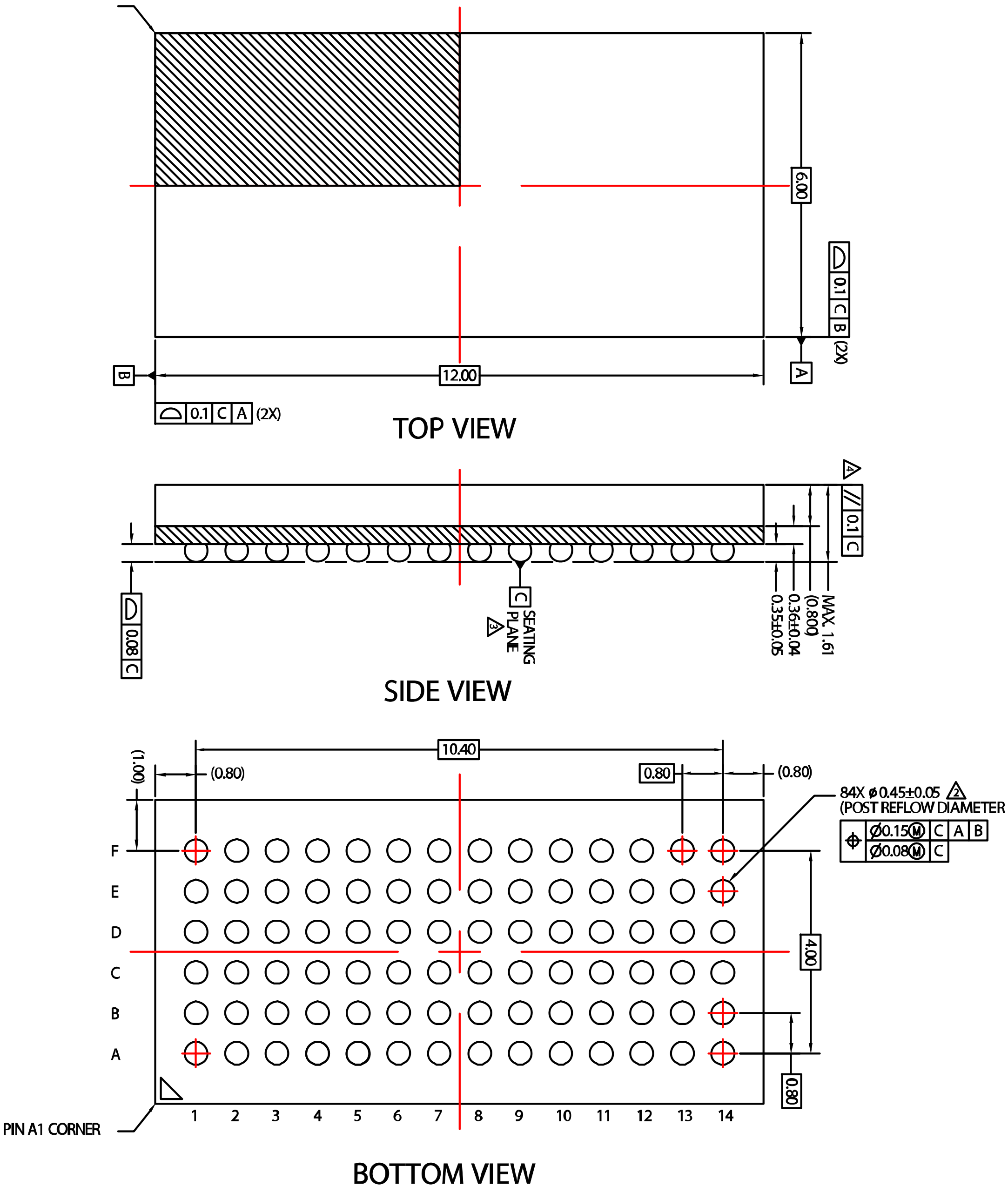

Figure 122. Package Drawings

One Analog Way, Wilmington, MA 01887-2356, U.S.A.