IBM Microelectronics
IBM31T1502 Infrared Communications Controller Data Sheet

Note!

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First Edition (July 1996)

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Contents

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IrDA	Infrared Data Association

1. IBM31T1502 Infrared Communications Controller

1.1 Highlights

- IrDA 1.1**, HP-SIR and Sharp ASK compatible
- Supports IrDA data rates up to 4 Mbps
- 16450 and 16550 standard UART compatibility
- Interfaces directly with the IBM31T1100 and IBM31T1101 infrared transceiver modules, and easily connects to other IrDA transceivers
- General purpose I/O pins for external transceiver control
- ISA and PCMCIA bus interface
- Indirect and Direct ISA configuration
- On-chip and external PCMCIA CIS support
- Host DMA and Shared Memory modes
- Single or Dual DMA channel mode
- Back-to-back packet transmission and reception
- Advanced interrupt configuration
- Power-down modes
- 48 MHz external clock input
- 5V supply voltage
- Small 100-pin Low Quad Flat Pack (LQFP) package

1.2 General Description

The IBM31T1502 is a low-cost, highly integrated Infrared Communications Controller capable of supporting both low-speed and high-speed infrared modulation schemes. The low-speed communication mode supports data rates up to 115.2 Kbps. The high-speed mode supports both 1.152 Mbps and 4 Mbps data rates. Implemented in IBM Microelectronic's 0.8 micron CMOS technology, the IBM31T1502 offers high performance, and many on-chip functions to meet today's and tomorrow's requirements for infrared communications applications.

The IBM31T1502's internal architecture is designed to easily interface to ISA and PCMCIA systems, as well as provide multiple configuration modes to satisfy a wide variety of programming needs.

Typical applications for the IBM31T1502 include: data communications, serial data transfer between notebook computers, desktops and printers, and digital camera technology.

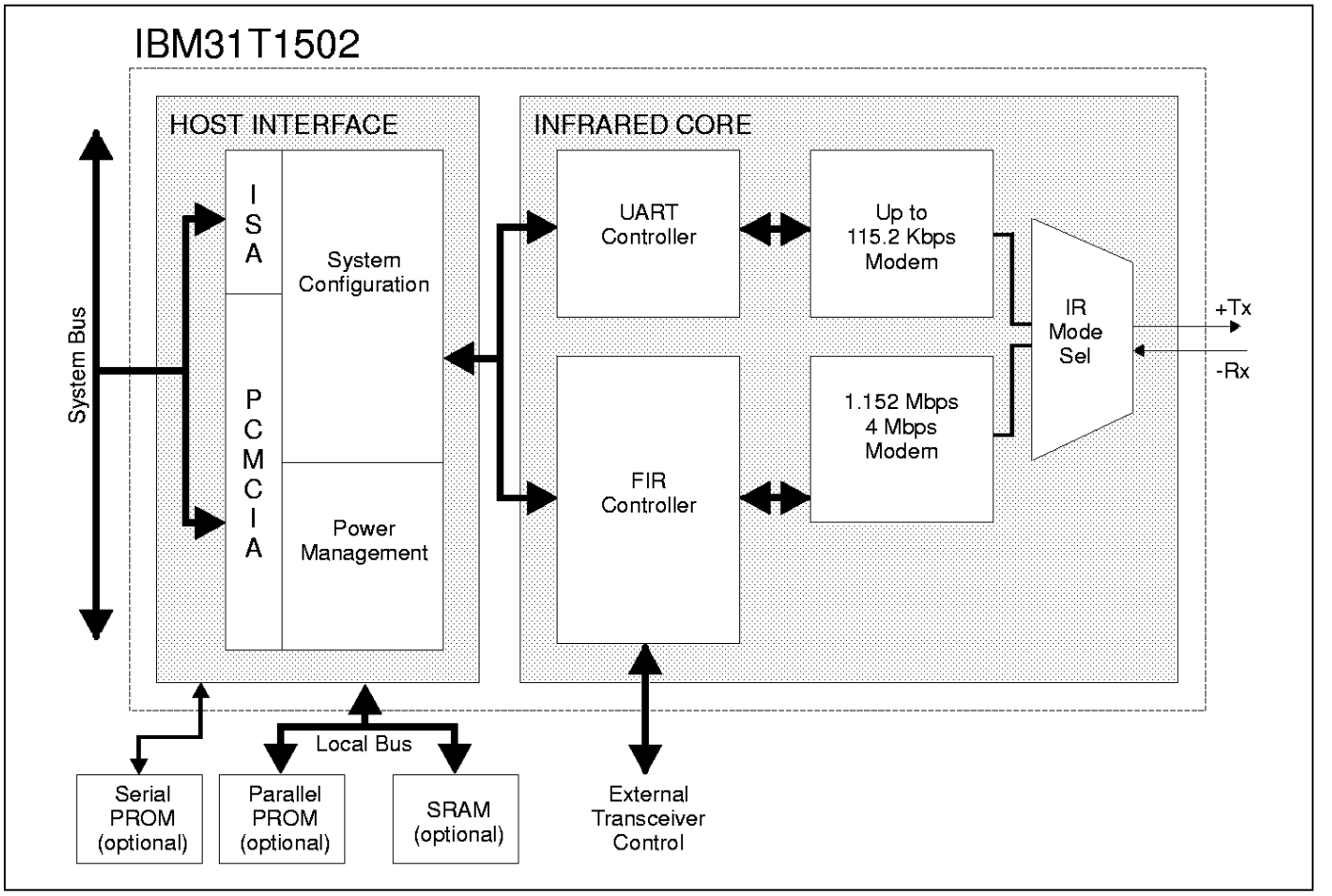


Figure 1-1. IBM31T1502 Functional Block Diagram

1.3 Architecture Description

The IBM31T1502 Infrared Communications Controller consists of an Infrared Core module and a Host Interface module (see Figure 1-1). The Infrared Core module controls all infrared communications functions and is divided into two subsystems: UART and Fast Infrared (FIR). Each subsystem consists of a controller and a modem.

The UART is fully compatible with the industry standard 16550 UART. The UART subsystem modem is capable of HP-SIR and Sharp ASK modulation. The FIR subsystem consists of a serial-to-parallel, parallel-to-serial converter and supports both 1.152 Mbps and 4 Mbps IrDA speeds.

The Host Interface module interfaces with an ISA or PCMCIA bus. It contains the bus interface logic, system configuration registers, power management circuitry, and local DMA control functions. The IBM31T1502 supports two modes of block data transfers: Host DMA and Local Memory Buffer. In Host DMA mode, data is transferred using the host DMA controller. In Local Memory mode, data is first buffered in local RAM, then read by the host for receive or shifted out to the infrared link in transmit.

1.4 ISA System Configuration

In ISA systems, the IBM31T1502 can be configured using one of two methods: indirect or direct configuration. The configuration method is determined by three mode pins: MODE2, MODE1, and MODE0. (See 1.11, "Pin Descriptions" on page 1-10.)

1.4.1 Indirect Configuration Register Access

Two 8-bit I/O ports are used to access the configuration registers: the index port and data port.

The index port is used to address a specified configuration register. The data port is used to read or write to and from the configuration register that is being pointed to by the index port. The destination and source of the data is determined by the last setting of the index port.

To write to a configuration register, the programmer writes the index value of the configuration register to the index port (see Table 5 for index assignments). Next, the programmer loads the 8-bit data value destined for the configuration register in two consecutive write accesses to the data port. To read from a configuration register, the programmer writes the index value of the configuration register to the index port, then reads from the data port.

Note: Only two consecutive write operations to the data port can modify an indirect configuration register. This protection mechanism prevents accidental erasure of any previously set configuration data. A single read from the index and data port may be done at any time.

The table below shows four possible address locations of the index and data ports. The addresses are set by the BADDR0 and BADDR1 pins.

Index and Data Port Locations

Table 1-1. Index and Data Port Locations

BADDR1	BADDR0	Index	Data
0	0	0x398	0x399
0	1	0x26E	0x26F
1	0	0x15C	0x15D
1	1	0x02E	0x02F

The programmer must determine the index port location after power-on-reset. This is done by reading all four index port addresses twice. After a hardware reset, the correct location is determined by an 0x88 value being returned on the first read, and a 0xDF value being returned on the second read. This signifies that the index port has been located successfully.

The IBM31T1502 can be set to a default configuration on power-up. This is accomplished by setting the CFG2-CFG0 pins. This feature is not available if Direct Configuration mode is selected. Appendix B, "Indirect Configuration Register Default Settings" on page B-1 describes the different default configurations.

1.4.2 Direct Configuration Register Access

This type of register access is similar to the one used in PS/2 Micro Channel* systems where configuration (POS) registers are accessed by driving the $\overline{\text{SETUP}}$ line low during I/O cycles, and address lines (A2-A0) select one of eight direct configuration registers.

Note: Direct configuration register bits map directly into corresponding indirect configuration register bits.

1.5 PCMCIA System Configuration

The IBM31T1502 is compatible with the PCMCIA version 2.01 specification. When the PCMCIA card is inserted into a memory or I/O socket, its pin definition is initially in the memory-only configuration. This allows access to the Card Identification Structure (CIS) mapped in attribute memory (see Appendix E, "CIS Information (PCMCIA Mode)" on page E-1). To reconfigure the socket interface to I/O, a valid configuration index must be written into the configuration index register.

The configuration index register is located at offset 0x7FF0 of attribute memory. The configuration status register is located at offset 0x7FF2 of attribute memory.

Note: Signal $\overline{\text{REG}}$ must be active when accessing PCMCIA configuration registers.

1.6 UART Subsystem Configuration

The UART subsystem is a fully compatible version of the NS16550 UART. It has full EIA interface capability, however the EIA interface lines do not go out to the module pins, therefore this UART cannot be used as a fully functional COM port. It is mainly used for the SIR functions. Addressing to the UART is programmable. The UART address registers must be properly set up during system configuration.

The SIR modulation in the IBM31T1502 is fully IrDA 1.0 compatible. The UART is used to serialize the packet data to the infrared link one character at a time. Each character has eight data bits, one start bit and one stop bit. Start character, stop character, transparency character insertion or removal and CRC generation or checking as specified in IrDA 1.0 are all done by software.

Two modulation schemes, HP-SIR or Sharp-ASK are supported. In receive, the HP-SIR pulse width can be 1.6 μs or 3/16ths of a single bit time. In transmit, the pulse width is fixed at 1.6 μs regardless of the data rate. This conserves power.

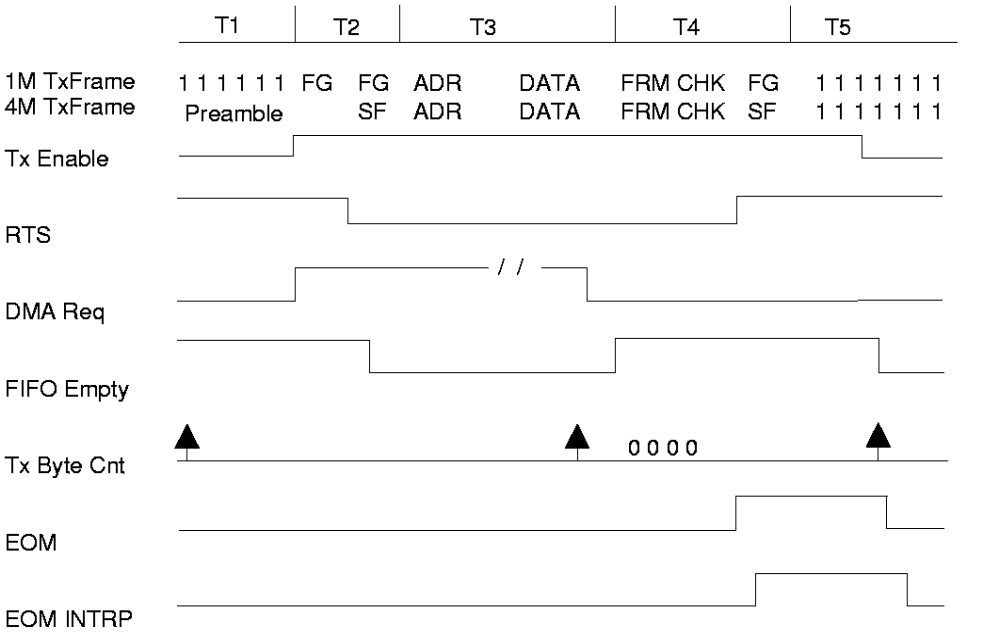
1.7 FIR Subsystem Configuration

The FIR subsystem is fully IrDA 1.1 compatible. It supports the serial infrared link at 576Kbps, 1.152Mbps and 4Mbps. The lower speeds are a Synchronous Data Link Control (SDLC) protocol, packet based with start/stop flags delimiting a data packet encoded by 'zero-insertion'. The 4Mbps bit protocol uses an optical preamble and postamble to delimit the 4 Pulse Position Modulated (4 PPM) packet data.

The FIR High/Low Address Registers must be set up during the system configuration. The Enable Infrared bit must also be set to 1 to grant access to all the FIR internal registers. The FIR Address Registers default to a preset address according to CFG pins settings.

1.7.1 FIR Transmit Operation

The FIR transmit operation is illustrated below:



T1 Set-up phase:

- Set up Transmit Control Registers per desired options.
- Load the byte count to the Transmit Byte Count Register.
- Set up the host DMA controller and the Tx packet.
- Set RTS and Transmit Enable bits.

T2 Start-up phase:

- RTS is active. If no carrier is detected, the transmitter starts transmitting.
- DMA Req is activated if DMA is enabled. The Tx FIFO is filled with transmit data. If DMA is not enabled, the Write Tx FIFO register can be used.
- If the Num Start Flag/Preamble bit is 0, the transmitter starts sending flags (1M) or preambles (4M) until the Tx FIFO is half filled (8 bytes). If the Num Start Flag/Preamble bit is 1, the transmitter waits until the Tx FIFO is half filled, then sends two start flags (1M mode) or preambles and one start flag (4M mode).

T3 Send data phase:

- The transmitter starts sending data stored in the FIFO.
- DMA Req to the host is active when the FIFO is not full.

T4 End of transmission:

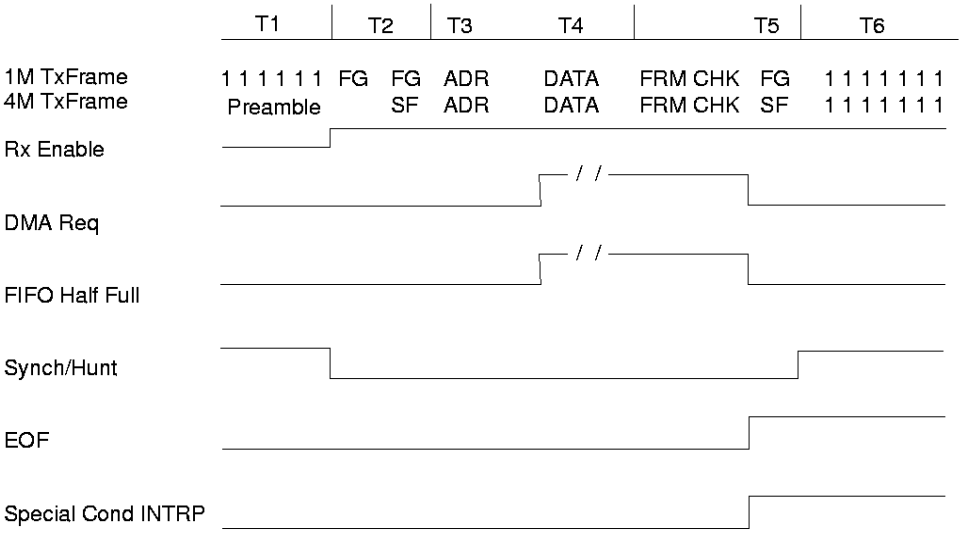
- The Byte Counter counts down to 0.
- DMA Req stops. The transmitter sends out the remaining data in the FIFO.
- CRC generator inverts the CRC and sends it out.
- Closing flag is sent. EOM latch is set. Interrupt is activated.

T5 Idle phase:

- The transmitter continues sending 1s or flags (1M) or preambles (4M), depending on the Idle line setting option.
- The host reads the TxStatus Register to check for transmission completion status.
- Reset EOM, Transmit Enable and RTS bits.
- End of transmission.

1.7.2 FIR Receive Operation

The FIR receive operation is illustrated below:



Receiving logic facilities:

- Receive serialize-deserialize logic and its control circuitry.
- Receive Byte Count Register (keeps track of received bytes).
- Receive FIFO, 16 x 11 bits: 8-bit data, 3-bit status (Frame Error, Abort and End Of Frame).
- Receive Ring Frame Counter (keeps track of the number of receive bytes in the host Rx buffer).
- Receive Ring Frame Pointer (points to the last byte of the most recently received packet in the host Rx buffer).

T1 Start-up phase:

- Set up Receive Control Registers per the receiving options.
- Set Receive Enable bit.
- FIR modem logic detects carrier, receive clock starts running. If continuous 1s are received, the receive clock may not be in sync with the incoming data.

T2 Flag(s)/Preambles detection:

- When the start flag is detected, all counters in the receiver are initialized. Characters can be recognized from this point on.
- 0 deletion starts for 1Mbps mode only.

T3 Address matching: the first non-flag byte after the starting flag is the address. Depending on the address mode option, the frame can be rejected or receiving starts. If the frame is rejected, the receiver will look for the next starting flag and another address match.

T4 Receive data:

- When a byte of data is received, the data and the three status bits are stored in the Rx FIFO.
- If DMA is enabled, DMA Req is activated when the FIFO threshold level is reached. DMA continues until all data stored in the FIFO has been transferred to the host receive buffer. However, the three status bits in the FIFO are not transferred to the host.
- If DMA is not used, the Read Rx FIFO I/O command can be used. Read the status bits first, then read the data byte. If EOF or Abort is set to 1, the data byte just read is the last byte of the packet. If the FIFO is still not empty, the next entry is the beginning of another packet. The Receive Byte counter and Receive Ring Frame counter are increased accordingly.

T5 Closing flag:

- When the closing flag is detected, the End Of Frame bit will set.
- CRC pattern is checked. Frame error is set if CRC is incorrect.

T6 Post-frame phase:

- DMA continues until all the received data in the FIFO has been transferred. Two more bytes will be stored in Rx FIFO and transmitted to the host receive buffer. Their format is:
  First byte: Bits 7-0 - byte count bits 7 to 0
  Second byte: Bit 7 - Abort
  Bit 6 - Frame Error
  Bit 5 - Overrun
  Bits 4 to 0 - Byte Count bits 12 to 8
- DMA deactivates.
- The Receive Ring Frame pointer is updated pointing to the second byte (see above) which has been stored successfully in the host Rx buffer.
- If DMA is not used, the last two bytes will not be stored in the FIFO. Status bit EOF will be set at the last Frame Check byte received.
- Steps T2 to T6 are repeated if continuous frame receiving is required.

1.8 Interrupt Handling

Two subsystems in IBM31T1502 can generate host interrupts: the UART (SIR operation) and FIR controller. There are four interrupt pins on the module that can be connected to any four host interrupts on the system board. They are: UART Interrupt (UIRQ pin 82), FIR Interrupt (FIRQ pin 83), IRQ3 (pin 49) and IRQ4 (pin 50).

The IBM31T1502 provides great flexibility for interrupt merging and routing. Setting the Advanced Interrupt Configuration bit (b3 of the Infrared Control Register) to 1 allows the UART Interrupt and the FIR interrupt to be routed to any of the four external interrupt pins (see Interrupt Select bits in the UARTL and FIRL registers). If the Advanced Interrupt Configuration bit is set to 0, both the UART interrupt and the FIR interrupt are merged and can then be routed to IRQ3 or IRQ4. Once the configuration registers have been locked, further interrupts merging can be done by programming the Infrared Configuration 2 Register, which is one of the general control registers.

In PCMCIA configuration, the UART and FIR interrupts are always merged and appear on pin 82.

1.9 External Transceiver Interface

The IBM31T1502 can directly interface to the IBM31T1100 or IBM31T1101 transceivers with no additional circuitry. Only the following interface lines are used:

$\overline{\text{TXD}}$ Transmit data.

$\overline{\text{RXD}}$ Receive data.

XCVROFF Transceiver off; powerdown and bandwidth switching control.

The IBM31T1100 and the IBM31T1101 transceivers require special control information when switching between low speed IrDA and high speed IrDA modes. A serial interface mechanism serves this purpose.

If other transceivers are used, there are several other transceiver interface lines that can be used:

$\overline{\text{XCVRDET}}$ Transceiver detect.

GPO2-GPO0 General Purpose Output pins, directly driven from an internal register.

GPI0 General Purpose Input pin.

Refer to *IBM31T1502 Infrared Controller Application Note* for information on connecting the IBM31T1502 to various transceivers.

1.10 Power Management Feature

The IBM31T1502 powerdown operates two ways: complete shutdown or partial shutdown. In complete shutdown mode, clocks to all subsystems are disabled and minimum power dissipation is achieved. In partial shutdown mode, the subsystem that is not enabled or not in 'action' has its clocks disabled, leaving only the functional unit consuming required power.

To put the IBM31T1502 in complete powerdown mode in the ISA configuration: set En Power Down (b1 of the Power Down Register) to 1 and set Power Down (b0 of the Power Down Register) to 1, or activate (set low) the $\overline{\text{PWRDWN}}$ pin (this consumes the least amount of power); or, set En Infrared (b0 of the Infrared Configuration Register) to 0.

For partial powerdown mode, set En Power Down to 1, (the default value upon reset). Then, only the circuit that provides the function selected by the Infrared Configuration 1 Register will be active; the others will automatically shut down.

To put the IBM31T1502 in complete powerdown mode in the PCMCIA configuration set $\overline{\text{PWRDWN}}$ (b2 of the Configuration Status Register) to 1. Note that, in PCMCIA configuration, partial powerdown mode is always enabled and cannot be disabled.

1.11 Pin Descriptions

1.11.1 ISA Pin Configuration

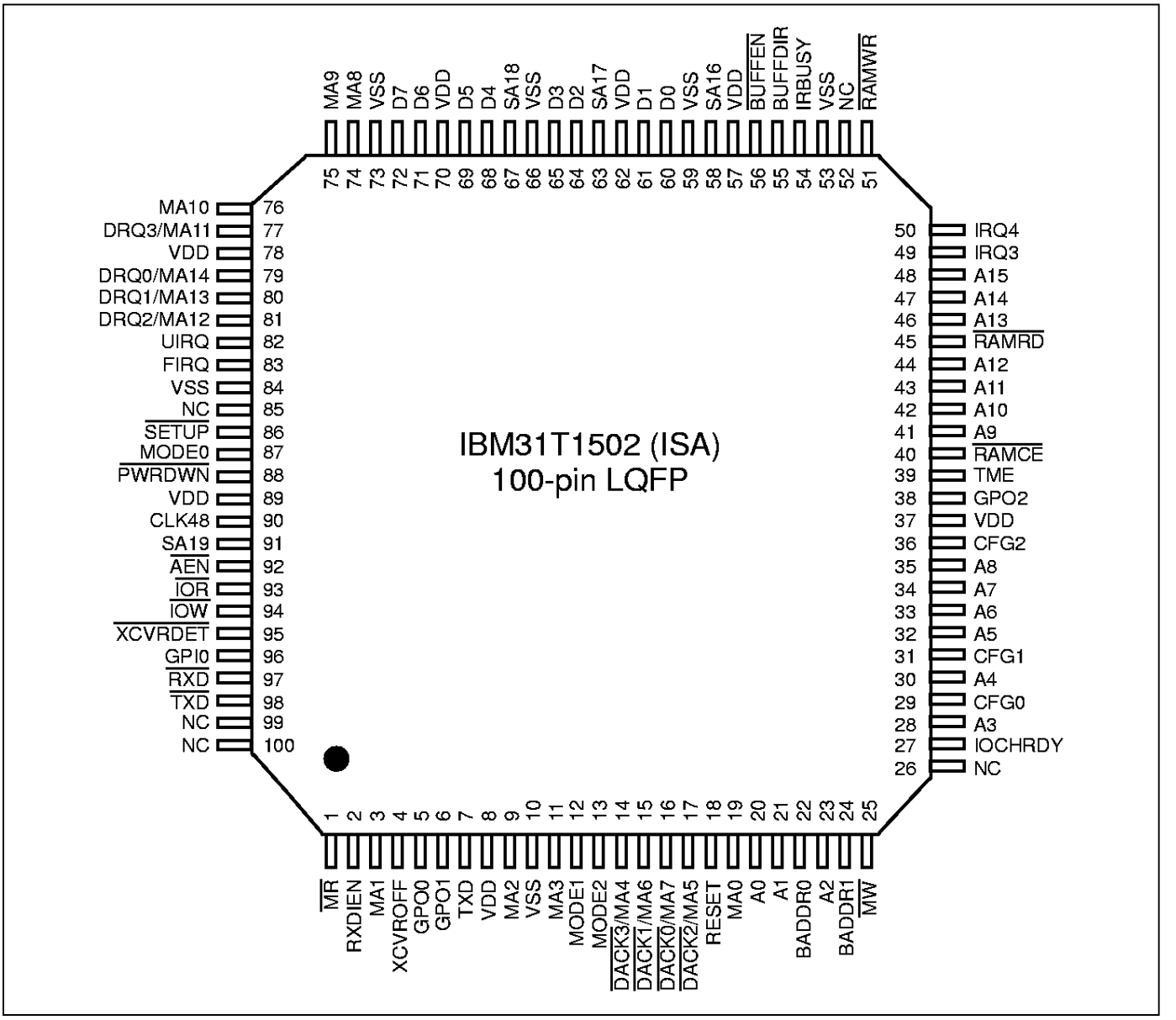


Figure 1-2. Pin Configuration for the ISA Bus Interface Mode

1.11.2 ISA Bus Interface Configuration Signals

Table 1-2 (Page 1 of 2). ISA Bus Interface Configuration Signals

Signal	Pin	Type	Description
BADDR1 -BADDR0	24, 22	I	Base Address Select. Select one of four base addresses of the index and data ports which are used in accessing indirect configuration registers. BADDR1-BADDR0 inputs are used only in Indirect Configuration mode.
CFG2 - CFG0	36, 31, 29	I	Default Register Configuration Select. Sampled during an active chip reset cycle and in conjunction with MODE inputs, select the default settings of the indirect configuration registers. CFG2-CFG0 inputs are used only in Indirect Configuration mode.
A15 - A0	48, 47, 46, 44, 43, 42, 41, 35, 34, 33, 32, 30, 28, 23, 22, 21, 20	I	System Address. 16-bit address bus provides addressing of IBM31T1502 registers and shared memory.
D7 - D0	72, 71, 69, 68, 65, 64, 61, 60	B	System Data. 8-bit bidirectional system data bus transfers data between the IBM31T1502, host processor, and external SRAM device. The data lines are tristated when not being driven.
$\overline{\text{IOR}}$	93	I	I/O Read. This active-low input is asserted by the host processor during reads from the IBM31T1502.
$\overline{\text{IOW}}$	94	I	I/O Write. This active-low input by the host processor during writes to the IBM31T1502.
$\overline{\text{AEN}}$	92	I	Address Enable. When $\overline{\text{AEN}}$ is high, the host DMA controller has control of the ISA bus. $\overline{\text{AEN}}$ must be low before programmed I/O or shared memory accesses can be made to the IBM31T1502.
IOCHRDY	27	O	I/O Channel Ready. When driven low, this output extends I/O and memory bus cycles. It is only used in Shared Memory mode. In Host DMA mode, IOCHRDY is tristated.
IRQ3, IRQ4	49, 50	O	Interrupt Request. When active, either the UART or the FIR Controller is requesting service. IRQ3 and IRQ4 normally operate in pulse mode. Advanced interrupt configuration provides the capability to change IRQ3 and IRQ4 to active-low interrupts. Advanced interrupt configuration also provides independent routing of UART and FIR Controller internal IRQ lines. IRQ3 and IRQ4 are tristated when they are not being driven.
UIRQ	82	O	UART Subsystem Interrupt Request. In Indirect Configuration mode, UAIRQ is a pulse-mode interrupt. In Direct Configuration mode, UAIRQ is an active-high interrupt. By using advanced interrupt configuration, both the UART and FIR Controller can share the single UAIRQ line. Also, advanced interrupt configuration provides the capability to change UAIRQ to an active-low interrupt. UAIRQ is tristated when not being driven.
FIRQ	83	O	FIR Controller Interrupt Request. In Indirect Configuration mode, FIRQ is a pulse-mode interrupt. In Direct Configuration mode, FIRQ is an active-high interrupt. By using advanced interrupt configuration, both the UART and FIR Controller can share the single FIRQ line. Also, advanced interrupt configuration provides the capability to change FIRQ to an active-low interrupt. FIRQ is tristated when not being driven.
DRQ3 - DRQ0	77, 81, 80, 79	O	DMA Request. Used to request a data transfer from the host DMA controller. Up to two DMA request lines, one for transmit and one for receive, may be used (selected during configuration). The remaining DMA request lines are tristated. DRQ3-DRQ0 are used only in Host DMA mode. In Shared Memory mode, these pins become MA14-MA11.
$\overline{\text{DACK3}}$ - $\overline{\text{DACK0}}$	14, 17, 15, 16	I	DMA Acknowledge. When active, indicate the host DMA controller is acknowledging a corresponding DMA request (DRQ3 - DRQ0). Up to two DMA acknowledge lines, one for transmit and one for receive, may be used (selected during configuration). $\overline{\text{DACK3}}$-$\overline{\text{DACK0}}$ lines are used only in Host DMA mode. In Shared Memory mode, these pins act as output pins for MA4-MA7.

I = Input, O = Output, B = Bidirectional, P = Power

Table 1-2 (Page 2 of 2). ISA Bus Interface Configuration Signals

Signal	Pin	Type	Description
SA19 - SA16	91, 67, 63, 58	I	Extended System Address. Extension to System Address bus. Used to address shared memory. **Note:** The host memory window must be enabled. Also, the IBM31T1502 controller does not latch address bits 16 through 19 and so these pins must be connected to the appropriate SA address lines on the ISA and not the LA address lines. In Host DMA mode these pins are ignored.
$\overline{\text{RAMCE}}$	40	O	RAM Chip Enable. This active-low output is asserted by the IBM31T1502 when performing reads and writes to an external SRAM device. $\overline{\text{RAMCE}}$ is used only in Shared Memory mode. In Host DMA mode, $\overline{\text{RAMCE}}$ is tristated.
$\overline{\text{RAMRD}}$	45	O	RAM Read. This active-low output is asserted by the IBM31T1502 when reading from an external SRAM device. $\overline{\text{RAMRD}}$ is used only in Shared Memory mode. In Host DMA mode, $\overline{\text{RAMRD}}$ is tristated.
$\overline{\text{RAMWR}}$	51	O	RAM Write. This active-low output is asserted by the IBM31T1502 when writing to an external SRAM device. $\overline{\text{RAMWR}}$ is used only in Shared Memory mode. In Host DMA mode, $\overline{\text{RAMWR}}$ is tristated.
BUFFDIR	55	O	Buffer Direction. Controls the direction of data when external bidirectional drivers are used for the data pins. BUFFDIR is active when: • The host processor is reading from an internal IBM31T1502 register • The host DMA controller is reading from the IBM31T1502 FIR controller (Host DMA mode) • The host processor is reading from an external SRAM device (Shared Memory mode)
$\overline{\text{BUFFEN}}$	56	O	Buffer Enable. This active-low output can be used to enable external bidirectional drivers for the IBM31T1502 data pins. $\overline{\text{BUFFEN}}$ is active when: • The IBM31T1502 is being accessed by the host processor • The IBM31T1502 is being accessed by the host DMA controller in Host DMA mode • An external SRAM device is being accessed by the host processor in Shared Memory mode **Note:** An external bidirectional driver is required for Shared Memory mode.
MA14 - MA0	79, 80, 81, 77, 76, 75, 74, 16, 15, 17, 14, 11, 9, 3, 19	O	Shared Memory Address. When the IBM31T1502 is operating in Shared Memory mode, these address lines are used to address an external SRAM device. MA3-MA0 and MA10-MA8 pins are tristated in Host DMA mode.
$\overline{\text{MR}}$	1	I	Memory Read. This active-low input is asserted by the host processor when performing memory reads. $\overline{\text{MR}}$ is used only in Shared Memory mode.
$\overline{\text{MW}}$	25	I	Memory Write. This active-low input is asserted by the host processor when performing memory writes. $\overline{\text{MW}}$ is used only in Shared Memory mode.
$\overline{\text{SETUP}}$	86	I	Setup Register Access. This active-low input is used only when making I/O accesses to direct configuration registers. When $\overline{\text{SETUP}}$ is active, the lower three bits of the address bus are decoded to access one of eight direct configuration registers. $\overline{\text{SETUP}}$ must be inactive when performing all other I/O accesses. $\overline{\text{SETUP}}$ is used only in Direct Configuration mode.
$\overline{\text{PWRDWN}}$	88	I	External Power Down. This active-low input is used in powering down the IBM31T1502. The power-down feature must be enabled before activating $\overline{\text{PWRDWN}}$.
IRBUSY	54	O	IR Busy. When active, indicates that the IBM31T1502 is busy.
NC	26, 85,99, 100	-	No Connect.
I = Input, O = Output, B = Bidirectional, P = Power			

1.11.3 PCMCIA Pin Configuration

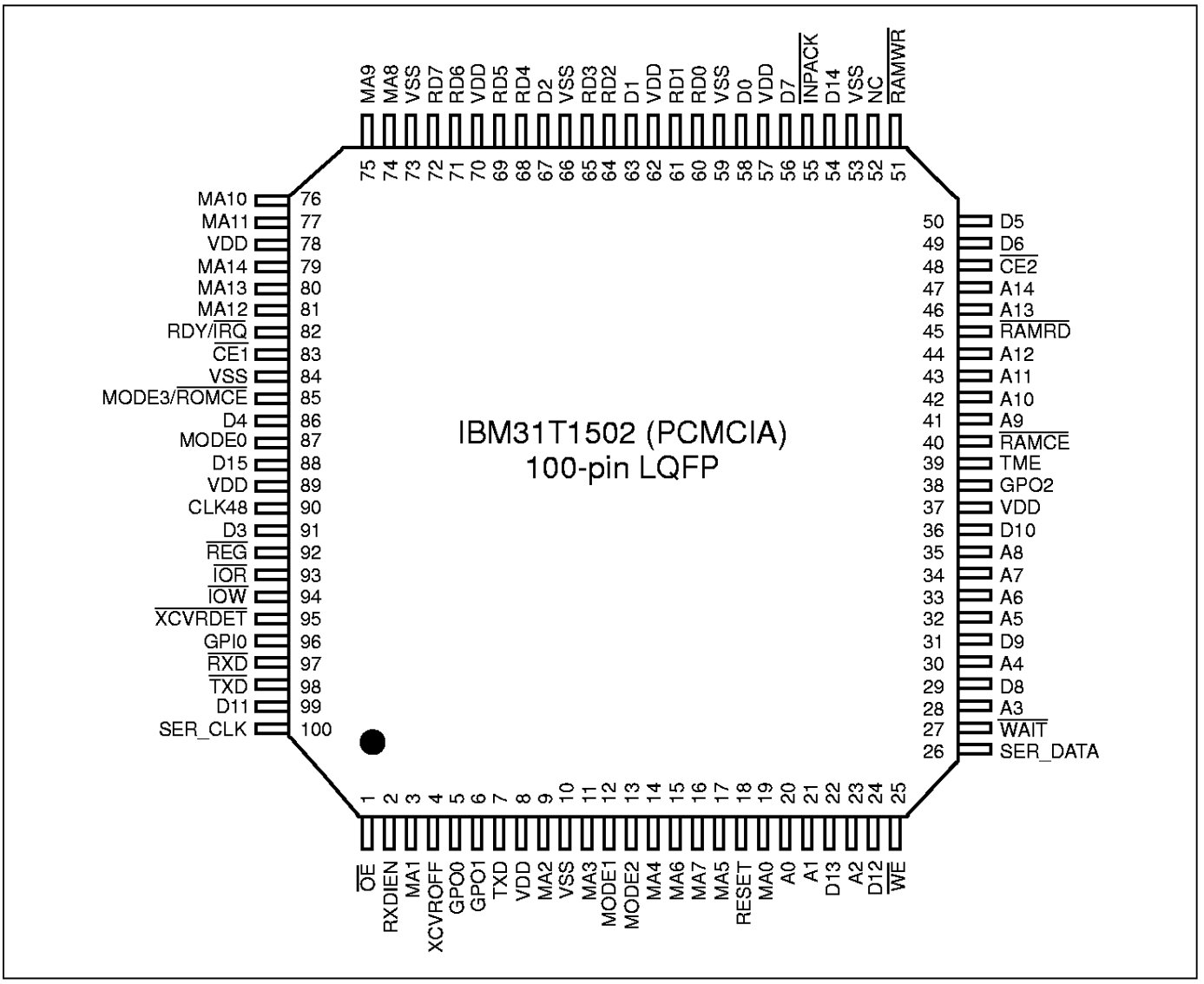


Figure 1-3. Pin Configuration for the PCMCIA Bus Interface Mode

1.11.4 PCMCIA Bus Interface Configuration Signals

Table 1-3 (Page 1 of 2). PCMCIA Bus Interface Configuration Signals

Signal	Pin	Type	Description
A14 - A0	47, 46, 44, 43, 42, 41, 35, 34, 33, 32, 30, 28, 23, 22, 21, 20	I	System Address. 15-bit address bus provides addressing of the IBM31T1502 registers and shared memory.
D15 - D0	88, 54, 22, 24, 99, 36, 31, 29, 56, 49, 50, 86, 91, 67, 63, 58	B	System Data. 16-bit bidirectional data bus used in transferring data between the IBM31T1502 and a host processor. The data lines are tristated when they are not being driven.
$\overline{CE1}$, $\overline{CE2}$	83, 48	I	Card Enable. These active-low inputs specify which data path has valid data during 8- and 16-bit host accesses. $\overline{CE2}$ $\overline{CE1}$ A0 Function 1 1 X No host accesses 1 0 0 8-bit access, valid data on D7-D0, even byte 1 0 1 8-bit access, valid data on D7-D0, odd byte 0 1 X 8-bit access, valid data on D15-D8, odd byte 0 0 X 16-bit access, valid data on D15-D0, even and odd bytes
$\overline{OE}$	1	I	Output Enable. This active-low input is asserted by the host processor when performing memory reads.
$\overline{WE}$	25	I	Write Enable. This active-low input is asserted by the host processor when executing a memory write.
$\overline{REG}$	92	I	Register Select. This active-low input specifies accesses to attribute memory or I/O. Signal State Access Made To High Common Memory Low Attribute Memory Low I/O
SER_DATA	26	B	Serial PROM Data. This bidirectional pin is used in transferring data between the IBM31T1502 and an external serial PROM device.
SER_CLK	100	O	Serial PROM Clock. This output is used to drive the serial clock of an external serial PROM device.
$\overline{WAIT}$	27	O	$\overline{WAIT}$. This active-low output is asserted by the IBM31T1502 when it needs to extend a bus cycle.
$\overline{RAMCE}$	40	O	RAM Chip Enable. This active-low output is asserted by the IBM31T1502 when performing reads and writes to an external SRAM device.
$\overline{RAMRD}$	45	O	RAM Read. This active-low output is asserted by the IBM31T1502 when reading from an external SRAM device or parallel PROM device.
$\overline{RAMWR}$	51	O	RAM Write. This active-low output is asserted by the IBM31T1502 when writing to an external SRAM device.
RD7-RD0	72, 71, 69, 68, 65, 64, 61, 60	B	RAM Data. 8-bit bidirectional data bus used in transferring data between the IBM31T1502 and external SRAM or parallel PROM devices. Data is transferred to the SRAM during a host memory write cycle to common memory space from attribute memory, and read from the SRAM and/or the external parallel PROM during a host memory read cycle.
MA14 - MA0	79, 80, 81, 77, 76, 75, 74, 16, 15, 17, 14, 11, 9, 3, 19	O	Shared Memory Address. Shared Memory mode is also used in the PCMCIA bus interface configuration. In Shared Memory mode, these local address lines are used to address an external SRAM device or external parallel PROM device.

I = Input, O = Output, B = Bidirectional, P = Power

Table 1-3 (Page 2 of 2). PCMCIA Bus Interface Configuration Signals

Signal	Pin	Type	Description
MODE3/ $\overline{\text{ROMCE}}$	85	B	Mode3/ROM Chip Enable. During chip reset, this pin is MODE3 and is used for detecting the presence of an external serial PROM device. $\overline{\text{ROMCE}}$ is an active-low output that gets asserted by the IBM31T1502 when performing reads from an external parallel PROM device. $\overline{\text{ROMCE}}$ either drives the chip-select input of the parallel PROM or is tristated, depending on the PCMCIA CIS mode selected, as shown below. MODE3 MODE2 MODE1 MODE0 PCMCIA CIS Mode $\overline{\text{ROMCE}}$ Function 1 1 0 1 Internal CIS Tristated 0 1 0 1 External CIS in serial PROM Tristated 1 1 1 1 External CIS in parallel PROM Drives chip-select input in parallel PROM MODE3 must not be directly connected to V_{cc} or GND, it must be pulled up or down using a resistor.
$\overline{\text{IOR}}$	93	I	I/O Read. In I/O mode, this active-low input is asserted by the host processor during reads from the IBM31T1502.
$\overline{\text{IOW}}$	94	I	I/O Write. In I/O mode, this active-low input is asserted by the host processor during writes to the IBM31T1502.
$\overline{\text{INPACK}}$	55	O	Input Acknowledge. This active-low output is asserted by the IBM31T1502 when it recognizes a valid address during an I/O read cycle.
RDY/$\overline{\text{IRQ}}$	82	O	Ready/Interrupt Request. This output is driven according to its configuration. While the card is in memory-only mode, this pin is the RDY/$\overline{\text{BSY}}$ signal. Once configured for I/O mode, it is used to interrupt the host processor.

I = Input, O = Output, B = Bidirectional, P = Power

1.11.5 Signals Common to Both ISA and PCMCIA Bus Interface

Table 1-4. Signals Common to Both ISA and PCMCIA Bus Interface Configurations

Signal	Pin	Type	Description
CLK48	90	I	Chip Clock. 48 MHz oscillator input.
RESET	18	I	Chip Reset. Resets all internal registers and configuration settings. RESET must be held active for at least 500 ms to ensure proper reset of the controller
MODE2 - MODE0	13, 12, 87	I	Mode Select. These inputs select the bus and memory configuration. The following describes the mode pin settings for the ISA bus configuration. For PCMCIA bus configuration, see the MODE3/$\overline{\text{ROMCE}}$ pin description. MODE2 MODE1 MODE0 Configuration Mode 0 0 0 ISA Direct Configuration, Host DMA 0 1 0 ISA Indirect Configuration, Host DMA 0 1 1 ISA Indirect Configuration, Shared Memory
TXD	7	O	Transmit Data. Transmits infrared serial data. Connects directly to the transmit data input of the infrared transceiver module.
$\overline{\text{TXD}}$	98	O	-Transmit Data. This negative-going output may be used with the $\overline{\text{TXD}}$ pin to provide a transmit differential output pair.
$\overline{\text{RXD}}$	97	I	Receive Data. This active-low input receives TTL-recovered serial data. Connects directly to the receive data output of the infrared transceiver module.
XCVROFF	4	O	Transceiver Off. Connects to the power-down control input of the external infrared transceiver. Alternatively, it may be used to control external circuitry which provides power directly to the transceiver.
$\overline{\text{XCVRDET}}$	95	I	Transceiver Detect. Senses the presence of an external infrared transceiver. The programmer may use this to generate hardware interrupts to dynamically power the transceiver on and off. **Note:** If using XCVROFF and at the same time not requiring the $\overline{\text{XCVRDET}}$ function, then the $\overline{\text{XCVRDET}}$ pin must be tied low.
GPI0	96	I	General Purpose Inputs. General purpose input which may be used to interface to the external infrared transceiver module.
GPO2 - GPO0	38, 6, 5	O	General Purpose Outputs. General purpose outputs which may be used for external infrared transceiver module control. The states of these pins are controlled through internal registers.
RXDIEN	2	I	Receiver Driver Inhibit Enable. This input is for manufacturing test purposes only and must be tied to ground under normal operation.
TME	39	I	Test Mode Enable. This input is for manufacturing test purposes only and must be tied to ground under normal operation.
VDD	8, 37, 57, 62, 70, 78, 89	P	Digital Supply. Connect to +5V power supply.
VSS	10, 53, 59, 66, 73, 84	P	Digital Ground.
NC	52	-	No Connect.
I = Input, O = Output, B = Bidirectional, P = Power			

1.12 Register Summary

The following tables provide a summary of the IBM31T1502 registers.

1.12.1 Indirect Configuration Register Summary

Table 1-5. Indirect Configuration Register Summary

Index	Register	Register Name	R/W
0x02	PDR	Power Down Register	R/W
0x08	IDR	Identification Register	R
0xA2	DLS SMBA	DMA Line Select Register Shared Memory Base Address Register	R/W R/W
0xA3	IRC	Infrared Control Register	R/W
0xA4	UARTH	UART High Address Register	R/W
0xA5	UARTL	UART Low Address Register	R/W
0xA6	FIRH	FIR High Address Register	R/W
0xA7	FIRL	FIR Low Address Register	R/W

See Appendix B, "Indirect Configuration Register Default Settings" on page B-1 for the default settings of indirect configuration registers.

1.12.2 Direct Configuration Register Summary

Table 1-6. Direct Configuration Register Summary

Address	Register	Register Name	R/W
0x0	ID0	Identification 0 Register	R
0x1	ID1	Identification 1 Register	R
0x2	SET	Setup Register	R/W
0x3	UARTL	UART Low Address Register	R/W
0x4	UARTH	UART High Address Register	R/W
0x5	FIRL	FIR Low Address Register	R/W
0x6	FIRH	FIR High Address Register	R/W
0x7	LDMAC	Local DMA Control Register	R/W

1.12.3 PCMCIA Configuration Register Summary

Table 1-7. PCMCIA Configuration Register Summary

Offset	Register	Register Name	R/W
0x7FF0	CIR	Configuration Index Register	R/W
0x7FF2	CSR	Configuration Status Register	R/W

1.12.4 UART Control Register Summary

Table 1-8. UART Control Register Summary

DLAB	A2-A0	Register	Register Name	R/W
0	0x0	RBR	Receiver Buffer Register	R
0	0x0	THR	Transmitter Holding Register	W
0	0x1	IER	Interrupt Enable Register	R/W
X	0x2	IIR	Interrupt Identification Register	R
x	0x2	FCR	FIFO Control Register	W
x	0x3	LCR	Line Control Register	R/W
x	0x4	MCR	Modem Control Register	R/W
x	0x5	LSR	Line Status Register	R/W
x	0x6	MSR	Modem Status Register	R/W
x	0x7	SCR	Scratch Register	R/W
1	0x0	DLL	Divisor Latch LSB	R/W
1	0x1	DLM	Divisor Latch MSB	R/W

See Appendix C, "UART Information" on page C-1 for the default settings of the UART control registers.

1.12.5 FIR Control Register Summary

Table 1-9. FIR Control Register Summary

Bank	Address	Register Name	R/W
0	0x0	Master Control Register	R/W
0	0x1	Master Status Register	R
0	0x1	Miscellaneous Control Register	W
0	0x2	RxFIFO Register	R
0	0x2	TxFIFO Register	W
0	0x3	TxControl 1 Register	R/W
0	0x4	TxControl 2 Register	R/W
0	0x5	TxStatus Register	R
0	0x6	RxControl Register	R/W
0	0x7	RxStatus Register	R
0	0x7	Reset Command Register	W
1	0x0	Master Control Register	R/W
1	0x1	Frame Address Register	R/W
1	0x2	Rx Byte Count Low Register	R
1	0x3	Rx Byte Count High Register	R
1	0x4	Rx Ring Frame Pointer Low Register	R
1	0x5	Rx Ring Frame Pointer High Register	R
1	0x6	Tx Byte Count Low Register	R/W
1	0x7	Tx Byte Count High Register	R/W
2	0x0	Master Control Register	R/W
2	0x1	Infrared Configuration 1 Register	R/W
2	0x2	Infrared Transceiver Control Register	R/W
2	0x3	Infrared Configuration 2 Register	R/W
2	0x4	Timer Register	R/W
2	0x5	Infrared Configuration 3 Register	R/W
2	0x6	Reserved	
2	0x7	Reserved	
3	0x0	Master Control Register	R/W
3	0x1	Shared Memory Page Register	R/W
3	0x2	TxDMA Start Address Low Register	R/W
3	0x3	TxDMA Start Address High Register	R/W
3	0x4	Reserved	
3	0x5	Reserved	
3	0x6	Reserved	
3	0x7	Revision ID Register	R

Note: Shared Memory Page Register and TxDMA Start Address Registers of Bank 3 are part of the DMA Control subsystem and therefore accessible only in Shared Memory mode.

2. Register Description

2.1 Indirect Configuration Registers

2.1.1 Power Down Register (PDR, Index=0x02)

Table 2-1. Power Down Register (PDR)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Software Reset	Lock Configuration	En Test Mode	En UART APM	Reserved	En Infrared Wakeup	En Power Down	Power Down

Bit 0 Power Down

Setting this bit to 1 causes all subsystems to be powered down, provided that En Power Down (b1) has already been set to 1. Alternatively, the IBM31T1502 can be powered down by driving the $\overline{\text{PWRDWN}}$ pin low.

Bit 1 En Power Down

Setting this bit to 1 enables the IBM31T1502 to be powered down using the power down bit (b0), or via the $\overline{\text{PWRDWN}}$ pin. It also activates the Power Conservation mode, in which subsystems automatically shut down when they are not being used. For example, when FIR and UART are not enabled, all clocks to the FIR and UART subsystems are disabled, providing the maximum power savings. If FIR is enabled and UART is not, then only the FIR subsystem is running and the UART is still in power-down mode, and vice-versa.

Note: This bit is set to 1 by default. It may be cleared after reset if Power Conservation mode is not desired.

Bit 2 En Infrared Wakeup

Setting this bit to 1 enables wakeup interrupts on the FIR subsystem interrupt request line to occur whenever infrared traffic is detected while the IBM31T1502 is powered down.

Note: After receiving an infrared wakeup interrupt, it is the software's responsibility to take the IBM31T1502 out of power-down in order to receive any incoming infrared data.

Bit 4 En UART APM

Setting this bit enables Automatic Power Management (APM) in the UART subsystem. This bit is cleared upon reset. When En Power Down is set to 1, the IBM31T1502 performs the power managing functions by disabling clocks to the subsystems that are not enabled. The UART subsystem has an additional feature in that it can power down its circuit automatically when it is not being accessed, even when the main UART clock is running.

Bit 5 En Test Mode

This bit is used for manufacturing test only. It is cleared upon reset. Setting this bit will corrupt the proper function of the GPO2, GPO1 and GPO0 pins, because internal signals are multiplexed on these pins.

Bit 6 Lock Configuration

Setting this bit to 1 prevents all write accesses to configuration registers.

Note: After setting Lock Configuration, only a hardware reset can then clear it.

Bit 7 Software Reset

Setting this bit to 1 activates an internal signal which resets the infrared controller. Setting this bit to 0 deactivates the internal reset signal.

Note: Software Reset must be held in the 1 state (active state) for at least 500 ms. Both the UART and FIR subsystem registers are inaccessible during software reset. Software reset does not affect configuration registers; however, the UART and FIR control registers are reset.

2.1.2 Identification Register (IDR, Index=0x08)

Table 2-2. Identification Register (IDR)

Bits 7 - 0
IBM31T1502 ID:
11100010 Host DMA Mode
11100011 Local DMA Mode

Bits 7 - 0 Identification

In Host DMA mode, this read-only register returns 0xE2 on reads. In Shared Memory mode, it returns 0xE3 on reads.

2.1.3 DMA Line Select Register (DLS, Index=0xA2)

Table 2-3. DMA Line Select Register (DLS) Host DMA Mode

Bit 7	Bits 6 - 4	Bit 3	Bits 2 - 0
Reserved	Infrared DRQ 2 Line Select	Reserved	Infrared DRQ 1 Line Select

Bits 2 - 0 iDRQ1 Line Select

Selects the external DMA request/acknowledge (DRQn/$\overline{\text{DACK}}$n) output pins to map into the FIR subsystem's internal DMA request (iDRQ1) line.

Bits 6 - 4 iDRQ2 Line Select

Selects the external DMA request/acknowledge (DRQn/$\overline{\text{DACK}}$n) output pins to map into the FIR subsystem's internal DMA request (IDRQ2) line.

2.1.4 Shared Memory Base Address Register (SMBA, Index=0xA2)

Table 2-4. Shared Memory Base Address Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A19	A18	A17	A16	A15	A14	A13	Reserved

Bits 7 - 1 Shared Memory Base Address, A19 - A13

Specifies the base address of the 8 Kbyte system memory window mapped to local memory in the system address space. The memory window is enabled when the IBM31T1502 is in Shared Memory mode and the En Host Mem Window bit (b5 of the Infrared Control Register) is set to 1.

2.1.5 Infrared Control Register (IRC, Index=0xA3)

Table 2-5. Infrared Control Register (IRC)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	En Host Memory Window	En Level Mode	Advanced Interrupt Configuration	Shared Interrupt Select	Reserved	En Infrared

Bit 0 En Infrared

Setting this bit to 1 enables the Infrared Core module. Setting this bit to 0 disables the Infrared Core module. The infrared core module automatically powers down. The XCVROFF output pin is asserted to power down the external infrared transceiver. Power-down occurs regardless of the setting of En Power Dow n (b1) in the Power Down Register

Bit 2 Shared Interrupt Select

When Advanced Interrupt Configuration is disabled (b3=0), this bit selects the IRQn line that will carry the shared interrupt request. 0 = IRQ3 and 1 = IRQ4.

Bit 3 Advanced Interrupt Configuration

Setting this bit to 1 enables Advanced Interrupt Configuration. The Shared Interrupt Select bit (b2) is ignored, and each subsystem's internal interrupt request line can be independently routed to one of four interrupt request output pins in either pulse or level mode: IRQ3, IRQ4, UIRQ, or FIRQ. If both the UART and FIR subsystems drive the same interrupt request line, they form a shared interrupt. The Advanced Interrupt Select bits (b1-b0 of UART Address Low Register and FIR Address Low Register) determine which interrupt request output pin receives the UART and FIR subsystem interrupts respectively.

Setting this bit to 0 puts the interrupt request output pins in pulse mode:

- UIRQ becomes the UART subsystem interrupt request line
- FIRQ becomes the FIR subsystem interrupt request line
- IRQ3 or IRQ4 carry the shared interrupt request line (specified by the Shared Interrupt Select bit)

Bit 4 En Level Mode

Selects the type of interrupt generated when Advanced Interrupt Configuration is enabled (b3=1). Setting this bit to 1 puts the interrupt request output pins in level mode. A level mode interrupt generates an active-low signal that remains in the active state until the interrupt condition is cleared. Setting this bit to 0 puts the interrupt request output pins in pulse mode. A pulse mode interrupt generates an active-low pulse ranging from 0.5 ms to 1 ms in duration.

Bit 5 En Host Memory Window

Setting this bit to 1 enables the 8 Kbyte system memory window specified in the Shared Memory Base Address Register. This bit is only valid in Shared Memory mode.

2.1.6 UART High Address Register (UARTH, Index=0xA4)

Table 2-6. UART High Address Register (UARTH)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A15	A14	A13	A12	A11	A10	A9	A8

Bits 7 - 0 UART Base Address, A15 - A8

Specifies the high-order base address of the UART subsystem.

2.1.7 UART Low Address Register (UARTL, Index=0xA5)

Table 2-7. UART Low Address Register (UARTL)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bits 1 - 0
A7	A6	A5	A4	A3	Reserved	Advanced Interrupt Selection

Bits 1 - 0 Advanced Interrupt Select

Selects the interrupt request output pin that will carry the UART subsystem interrupts when Advanced Interrupt Configuration is enabled (b3 of IRC is set to 1).

Bits 7 - 3 UART Base Address, A7 - A3

Specifies the low-order base address of the UART subsystem.

2.1.8 FIR High Address Register (FIRH, Index=0xA6)

Table 2-8. FIR High Address Register (FIRH)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A15	A14	A13	A12	A11	A10	A9	A8

Bits 7 - 0 FIR Base Address, A15 - A8

Specifies the high-order base address of the FIR subsystem.

2.1.9 FIR Low Address Register (FIRL, Index=0xA7)

Table 2-9. FIR Low Address Register (FIRL)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bits 1 - 0
A7	A6	A5	A4	A3	Reserved	Advanced FIR Interrupt Configuration

Bits 1 - 0 Advanced Interrupt Select

Selects the interrupt request output pin that will carry the FIR subsystem interrupts when Advanced Interrupt Configuration is enabled (b3 of IRC is set to 1).

Bits 7 - 4 FIR Base Address, A7 - A3

Specifies the low-order base address of the FIR subsystem.

2.2 Direct Configuration Registers

2.2.1 Identification 0 Register (ID0, Index=0x0)

Table 2-10. Identification Register 0 (ID0)
Bits 7 - 0
IBM31T1502 ID0 11100010 (0xE2)

Bits 7 - 0 Identification 0

Returns 0xE2 on reads.

2.2.2 Identification 1 Register (ID1, Index=0x1)

Table 2-11. Identification Register 1 (ID1)
Bits 7 - 0
IBM31T1502 ID1 11011111 (0xDF)

Bits 7 - 0 Identification 1

Returns 0xDF on reads.

2.2.3 Setup Register (SET, Index=0x2)

Table 2-12. Setup Register (SET)

Bit 7	Bit 6	Bit 5	Bit 4	Bits 3 - 2	Bit 1	Bit 0
En Level Mode	Software Reset	En Infrared Wakeup	En Advanced Interrupt Selection	Advanced Interrupt Selection	Reserved	En Infrared

Bit 0 En Infrared

Setting this bit to 1 enables the Infrared Core module. Setting this bit to 0 disables the Infrared Core module. The Infrared Core module automatically powers down. The XCVROFF output pin is asserted to power down the external infrared transceiver.

Bits 3 - 2 Advanced Interrupt Select

When En Advanced Interrupt (b4) is set to 1, the shared interrupt will be routed to one of the four interrupt pins.

Bit 4 En Advanced Interrupt

When this bit is set to 1 it enables advanced interrupt selection for direct configuration. The FIR and The UART interrupts are merged and can be routed as specified by b3 and b2. When this bit is '0', the FIR interrupt is fixed to the FIRQ pin and the UART interrupt is fixed to the UIRQ pin. Both interrupts become active high. That is, FIRQ is high when FIR interrupt is pending, and low when FIR interrupt is reset.

Bit 5 En Infrared Wakeup

Setting this bit to 1 enables wakeup interrupts on the FIR subsystem interrupt request line to occur whenever infrared traffic is detected while the IBM31T1502 is powered down.

Note: After receiving an infrared wakeup interrupt, it is the software's responsibility to take the IBM31T1502 out of power-down in order to receive any incoming infrared data.

Bit 6 Software Reset

Setting this bit to 1 activates an internal signal which resets the infrared controller. Setting this bit to 0 deactivates the internal reset signal.

Note: Software Reset must be held in the 1 state (active state) for at least 500 ms. Both the UART and FIR subsystem registers are inaccessible during software reset. Software reset does not affect configuration registers; however, the UART and FIR control registers are reset.

Bit 7 En Level Mode

This bit works in conjunction with En Advanced Interrupt (b4). When this bit is 1, it enables level mode interrupt, which is active low. Clearing this bit enables pulse mode interrupt.

2.2.4 UART Low Index Register (UARTL, Index=0x3)

Table 2-13. UART Low Address Register (UARTL)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A7	A6	A5	A4	A3	Reserved	Reserved	Reserved

Bits 7 - 3 UART Base Address, A7 - A3

Specifies the low-order base address of the UART subsystem.

2.2.5 UART High Index Register (UARTH, Index=0x4)

Table 2-14. UART High Address Register (UARTH)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A15	A14	A13	A12	A11	A10	A9	A8

Bits 7 - 0 UART Base Address, A15 - A8

Specifies the high-order base address of the UART subsystem.

2.2.6 FIR Low Index Register (FIRL, Index=0x5)

Table 2-15. FIR Low Address Register (FIRL)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A7	A6	A5	A4	A3	Reserved	Reserved	Reserved

Bits 7 - 3 FIR Base Address, A7 - A3

Specifies the low-order base address of the FIR subsystem.

2.2.7 FIR High Index Register (FIRH, Index=0x6)

Table 2-16. FIR High Address Register (FIRH)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A15	A14	A13	A12	A11	A10	A9	A8

Bits 7 - 0 FIR Base Address, A15 - A8

Specifies the high-order base address of the FIR subsystem.

2.2.8 Local DMA Control Register (LDMAC, Index=0x7)

Table 2-17. Local DMA Control Register (LDMAC)

Bits 7 - 4	Bits 3 - 2	Bits 1 - 0
Reserved	iDRQ2 Line Select	iDRQ1 Line Select

Bits 1 - 0 iDRQ1 Line Select

Selects the external DRQn/$\overline{\text{DACKn}}$ output pins to map into the FIR subsystem's internal iDRQ1 line.

Bits 3 - 2 iDRQ2 Line Select

Selects the external DRQn/$\overline{\text{DACKn}}$ output pins to map into the FIR subsystem's internal iDRQ2 line.

2.3 PCMCIA Configuration Registers

2.3.1 Configuration Index Register (Offset=0x7FF0)

Table 2-18. PCMCIA Configuration Index

Bit 7	Bit 6	Bits 5 - 0
Software Reset	En Level Mode	Configuration Index

Bits 5 - 0 Configuration Index

A valid index value reconfigures the socket interface from memory-only to I/O. Three configuration I/O modes are supported:

Low Speed IrDA
In this configuration, only the UART subsystem is enabled in HP-SIR mode. I/O accesses to the FIR subsystem are disabled. The shared memory window in common memory is disabled. This configuration is primarily meant for super-client drivers which may configure the IrDA card.

Low/High Speed IrDA
This configuration provides full IrDA function, with the UART subsystem in the 0x8 to 0xF range of the I/O window, and the FIR subsystem in the 0x0 to 0x7 range of the I/O window.

High/Low Speed IrDA
This configuration also provides full IrDA function, except the UART subsystem is in the 0x0 to 0x7 range of the I/O window, and the FIR subsystem is in the 0x8 to 0xF range of the I/O window.

In full IrDA mode, system address lines A3-A0 are decoded. Address bit A3 selects between the UART and FIR subsystem. Address bits A2-A0 are decoded by the individual subsystems. Common memory accesses transfer data to and from local memory. Accesses to local memory are normally done through a paged 8 Kbyte system memory window (see 2.1.4, "Shared Memory Base Address Register (SMBA, Index=0xA2)" on page 2-3).

The UART and FIR subsystems may occupy non-consecutive 8-byte windows in system address space, as long as the lower 4 bits of the address are not the same. For example, the UART subsystem can occupy 0x2F8-0x2FF and the FIR subsystem can occupy 0x330-0x33 7; however the FIR subsystem cannot occupy 0x338-0x33F.

Bit 6 En Level Mode

Setting this bit to 1 puts the interrupt request output pins in level mode. A level-mode interrupt generates an active-low signal that remains in the active state until the interrupt condition is cleared. Setting this bit to 0 puts the interrupt request output pins in pulse mode. A pulse-mode interrupt generates an active-low pulse ranging from 0.5 ms to 1 ms in duration.

Bit 7 Software Reset

Setting this bit to 1 activates an internal signal which resets the infrared controller. Setting this bit to 0 deactivates the internal reset signal.

Note: Software Reset must be held in the 1 state (active state) for at least 500 ms.

The recommended reset sequence is:

- Write 0x08 to the Configuration Index Register
- Wait 500 ms or more
- Write 0x00 to the Configuration Index Register to deactivate reset
- The card is in memory-only mode; wait for the RDY/BSY signal to go active, indicating that the card is ready
- Write the desired configuration index value to the Configuration Index Register

2.3.2 Configuration Status Register (Offset=0x7FF2)

Table 2-19. PCMCIA Configuration Status

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status Change Detected	En Signal Change	I/O Cycles Occur Only as 8-bit Transfers	Reserved	Audio Enable	Power Down	Interrupt Request Pending	Reserved

Bit 1 Interrupt Request Pending

When set to 1, indicates an interrupt request is pending. This bit remains true until the interrupt condition has been serviced.

Bit 2 Power Down ($\overline{\text{PWRDWN}}$)

When set to 1, powers the IBM31T1502 down completely. Note that the Power Conservation mode (see 2.1.1, "Power Down Register (PDR, Index=0x02)" on page 2-1) is always enabled in PCMCIA mode. It cannot be disabled.

Bit 3 Audio Enable

Not used; returns 0 on reads.

Bit 5 I/O Cycles Occur Only as 8-bit Transfers

All registers can be programmed with 8-bit or 16-bit I/O; therefore this bit returns 0 on reads.

Bit 6 Signal Change Enable/Disable

Not used; returns 0 on reads.

Bit 7 Status Change Detected

Not used; returns 0 on reads.

2.4 UART Control Registers

2.4.1 Receive Buffer Register (RBR, Index=0x0, DLAB=0)

Table 2-20. Receive Buffer Register (RBR)
Bits 7 - 0
Data Bits 7 - 0

Bits 7 - 0 Receive Data, D7 - D0

Holds deserialized data from the Receive Shift Register (RSR).

2.4.2 Transmit Holding Register (THR, Index=0x0, DLAB=0)

Table 2-21. Transmit Holding Register (THR)
Bits 7 - 0
Data Bits 7 - 0

Bits 7 - 0 Transmit Data, D7 - D0

Holds transmit data. The Transmit Shift Register (TSR) serializes the data and shifts it out through the selected modulator.

2.4.3 Interrupt Enable Register (IER, Index=0x1)

Table 2-22. Interrupt Enable Register (IER)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	En Modem Status Interrupt	En Receiver Line Status Interrupt	En Transmitter Holding Register Empty Interrupt	En Received Data Available Interrupt

Bit 0 En Rx Data Available

Setting this bit to 1 enables the Received Data Available interrupt. In FIFO mode, this bit enables the Timeout interrupt.

Bit 1 En THR Empty

Setting this bit to 1 enables the Transmit Holding Register Empty interrupt.

Bit 2 En Rx Line Status

Setting this bit to 1 enables the Receiver Line Status interrupt.

Bit 3 En Modem Status

Setting this bit to 1 enables the Modem Status interrupt.

2.4.4 Interrupt Identification Register (IIR, Index=0x2)

Table 2-23. Interrupt Identification Register (IIR)

Bits 7 - 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FIFOs Enabled	0	0	Interrupt ID Bit 2	Interrupt ID Bit 1	Interrupt ID Bit 0	Interrupt Pending

Bit 0 Interrupt Pending

When set to 0, indicates an interrupt is pending.

Bits 3 - 1 Interrupt Identification, ID2 - ID0

Indicates the highest priority interrupt pending. In 16450 mode, ID2 is always 0. See C.2, "UART Interrupt Priority Settings Of the Interrupt Identification Register" on page C-2.

Bits 7 - 6 FIFOs Enabled

These bits are set to 11 when the FIFO Enable bit (b0 of FCR) is set to 1.

2.4.5 FIFO Control Register (FCR, Index=0x2)

Table 2-24. FIFO Control Register (FCR)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Rx Trigger Level (MSB)	Rx Trigger Level (LSB)	Reserved	Reserved	Reserved	TxFIFO Reset	RxFIFO Reset	FIFO Enable

Bit 0 FIFO Enable

Setting this bit to 1 puts the UART in FIFO mode. Both the transmit and receive FIFOs are enabled. Resetting this bit will clear all bytes in both FIFOs. Also, when changing from FIFO mode to 16450 mode and vice versa, data is automatically cleared from the FIFOs.

Note: This bit must be set to 1 before any of the remaining bits of the FCR can be programmed.

Bit 1 RxFIFO Reset

Setting this bit to 1 clears all bytes in the receiver FIFO. However, the Receive Shift Register (RSR) is not affected. This bit is self-clearing.

Bit 2 TxFIFO Reset

Setting this bit to 1 clears all bytes in the transmit FIFO. However, the Transmit Shift Register (TSR) is not affected. This bit is self-clearing.

Bits 7 - 6 Rx Trigger Level

Specifies the trigger level for the RxFIFO interrupt. When the number of bytes in RxFIFO equal the selected trigger level, a Received Data Available interrupt is set.

2.4.6 Line Control Register (LCR, Index=0x3)

Table 2-25. Line Control Register (LCR)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Divisor Latch Access Bit	Set Break	Stick Parity	Parity Select	Parity Enable	Number of Stop Bits	Character Length Select Bit 1	Character Length Select Bit 0

Bits 1 - 0 Character Length

Specifies the number of bits in each transmitted or received serial character.

Bit 2 Number of Stop Bits

Specifies the number of stop bits transmitted with each serial character. If this bit is set to 1 and the character length is set to 6, 7, or 8 bits, the UART generates two stop bits. If this bit is set to 0, one stop bit is generated regardless of the Character Length setting.

Note: The receiver only checks the first stop bit even if the UART is programmed to receive two stop bits.

Bit 3 Parity Enable

Setting this bit to 1 enables parity generation and checking during transmission and reception.

Bit 4 Parity Select

Specifies odd or even parity.

Bit 5 Stick Parity

When even parity is enabled (b3=1 and b4=1), setting this bit to 1 causes the parity bit to be transmitted and checked as a 0. When odd parity is enabled (b3=1 and b4=0), setting this bit to 1 causes the parity bit to be transmitted and checked as a 1. Setting this bit to 0 disables stick parity.

Bit 6 Set Break

Setting this bit to 1 causes a break (transmission of all zeros) to be transmitted.

Bit 7 Divisor Latch Access Bit

This bit is used to access the DLL and DLM registers. Table 1-8 on page 1-18 shows all UART Control Registers' address assignment in conjunction with the DLAB. This bit is initialized to 0 after reset. When DLAB is 1, the DLL can be accessed through offset address 0x and the DLM can be accessed through offset address 1x. When DLAB is 0, the RBR/THR can be accessed through offset address 0x and the IER can be accessed through offset address 1x.

2.4.7 Modem Control Register (MCR, Index=0x4)

Table 2-26. Modem Control Register (MCR)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	Loop	IRQ Enable	Output 1	Request to Send	Data Terminal Ready

Bit 0 Data Terminal Ready

Controls the Data Terminal Ready (DTR) output signal. Setting this bit to 1 forces the DTR output signal low (active). Setting this bit to 0 forces DTR high (inactive).

Bit 1 Request to Send

Controls the Request to Send (RTS) output signal. Setting this bit to 1 forces the RTS output signal low (active). Setting this bit to 0 forces RTS high (inactive).

Bit 2 Output 1

Controls the user-designated OUT1 output signal. Setting this bit to 1 forces the Output 1 output signal low (active). Setting this bit to 0 forces OUT1 high (inactive).

Bit 3 IRQ Enable

Setting this bit to 1 enables all UART interrupts.

Bit 4 Loop

Setting this bit to 1 puts the UART into Loopback mode for diagnostic testing of the transmit and receive data paths within the UART.

Note: Although b0, b1, and b2 can be written to and read from, their signals are not connected to any physical pins of the IBM31T1502. They are merely present for maintaining compatibility with existing UART-based software, and do not affect the operation of the controller.

2.4.8 Line Status Register (LSR, Index=0x5)

Table 2-27. Line Status Register (LSR)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RxFIFO Error	Transmitter Empty	Transmitter Holding Register Empty	Break Interrupt	Framing Error	Parity Error	Overrun Error	Data Ready

Bit 0 Data Ready

When set to 1, indicates a complete incoming character was received and transferred to RBR or RxFIFO. This bit is cleared by reading RBR or the FIFO.

Bit 1 Overrun Error

When set to 1, indicates the host processor was not fast enough in reading the data from RBR before it was overwritten by the next incoming data character. This bit is cleared by reading LSR.

In FIFO mode, if data continues to fill the FIFO beyond the trigger level, an overrun error will occur at the point where the FIFO is full and the next character has completely been received by the shift register (RSR). As data continues to be received, only RSR is overwritten, and no data is transferred to the FIFO.

Note: The overrun error condition generates a Receiver Line Status interrupt when the En Rx Line Status bit (b2 of IER) is enabled.

Bit 2 Parity Error

When set to 1, indicates the received character did not have the correct even or odd parity, as specified by the Parity Select bit (b4 of LCR). This bit is cleared by reading LSR. In FIFO mode, parity error is associated with the particular character in the FIFO. The parity error is reported to the host processor when the associated character is at the top of the FIFO.

Note: The parity error condition generates a Receiver Line Status interrupt when the En Rx Line Status bit (b2 of IER) is enabled.

Bit 3 Framing Error

When set to 1, indicates the received character had an invalid stop bit (i.e. stop bit was detected as a logic 0). This bit is cleared by reading LSR. In FIFO mode, a framing error is associated with the particular character in the FIFO. The framing error is reported to the host processor when the associated character is at the top of the FIFO.

Note: The framing error condition generates a Receiver Line Status interrupt when the En Rx Line Status bit (b2 of IER) is enabled.

Bit 4 Break Interrupt

When set to 1, indicates a break character was received (i.e. receive data input to the UART was held in logic 0 state for longer than one full-word transmission time). This bit is cleared by reading LSR. When a break occurs in FIFO mode, only one zero character is loaded into the FIFO. The next character transfer is enabled after the receive data input line goes to the logic 1 state (idle) and receives the next valid start bit.

Note: The break interrupt condition generates a Receiver Line Status interrupt when the En Rx Line Status bit (b2 of IER) is enabled.

Bit 5 Transmit Holding Register Empty

When set to 1, indicates the UART is ready to accept a new character for transmission. This occurs when a character is transferred from THR to TSR. If the En Transmitter Holding Register (THR) Empty bit (b1 of IER) is enabled, an interrupt is issued to the host processor. The THRE bit is cleared when data is written to THR. In FIFO mode, this bit is set to 1 when TxFIFO becomes empty, and set to 0 when TxFIFO is written to.

Bit 6 Transmitter Empty

When set to 1, indicates THR and TSR are both empty. This bit is cleared when THR or TSR contain data. In FIFO mode, this bit is set to 1 when TxFIFO and TSR are both empty.

Bit 7 RxFIFO Error

When set to 1, indicates there is at least one parity error, frame error, or break interrupt condition in RxFIFO. This bit is cleared by reading LSR (only if there are no subsequent errors in the FIFO).

Note: In 16450 mode, this bit is always 0.

Note: LSR is intended for read-only operations. Writing to this register is recommended only for manufacturing test purposes. In FIFO mode, the programmer must load a data byte in RxFIFO in Loopback mode when intending to write to b4-b3. Also, b0 and b7 cannot be written to in FIFO mode.

2.4.9 Modem Status Register (MSR, Index=0x6)

Table 2-28. Modem Status Register (MSR)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Data Carrier Detect	Ring Indicator	Data Set Ready	Clear to Send	Delta Data Carrier Detect	Trailing Edge Ring Indicator	Delta Data Set Ready	Delta Clear to Send

Bit 0 Delta Clear To Send

When set to 1, indicates Clear to Send input to the UART has changed state since the last time it was read by the CPU. This bit is cleared by reading MSR.

Note: A Modem Status interrupt is generated by DCTS when the En Modem Status bit (b3 of IER) is enabled.

Bit 1 Delta Data Set Ready

When set to 1, indicates Data Set Ready input to the UART has changed state since the last time it was read by the CPU. This bit is cleared by reading MSR.

Note: A Modem Status interrupt is generated by DDSR when the En Modem Status bit (b3 of IER) is enabled.

Bit 2 Trailing Edge Ring Indicator

When set to 1, indicates Ring Indicator input to the UART has changed from a low to high state. This bit is cleared by reading MSR.

Note: A Modem Status interrupt is generated by TERI when the En Modem Status bit (b3 of IER) is enabled.

Bit 3 Delta Data Carrier Detect

When set to 1, indicates Delta Clear to Send input to the UART has changed state since the last time it was read by the CPU. This bit is cleared by reading MSR.

Note: A Modem Status interrupt is generated by Delta Data Carrier Detect when the En Modem Status bit (b3 of IER) is enabled.

Bit 4 Clear To Send

This bit is the complement of the Clear to Send input. In Loopback mode, this bit is equivalent to the Request to Send bit in MCR.

Bit 5 Data Set Ready

This bit is the complement of the Data Set Ready input. In Loopback mode, this bit is equivalent to the Data Terminal Ready bit in MCR.

Bit 6 Ring Indicator

This bit is the complement of the Ring Indicator input. In Loopback mode, this bit is equivalent to the Output 1 bit in MCR.

Bit 7 Data Carrier Detect

This bit is the complement of the Data Carrier Detect input. In Loopback mode, this bit is equivalent to the IRQ Enable bit in MCR.

Note: The CTS, DSR, and DCD inputs to the UART are tied high internally and therefore will never change states. The Modem Status Register will always read 0x00.

2.4.10 Scratch Register (SCR, Index=0x7)

Table 2-29. Scratchpad Register (SCR)
Bits 7 - 0
No Function

Bits 7 - 0 Scratch Pad Data, D7 - D0

This register has no effect on the UART and may be used to hold data temporarily.

2.4.11 Divisor Latch LSB Register (DLL, Index=0x0, DLAB=1)

Table 2-30. Divisor Latch LSB Holding Register (DLL)
Bits 7 - 0
Data Bits 7 - 0

Bits 7 - 0 Divisor Latch LSB, D7 - D0

Specifies the low-order byte of the 16-bit divisor used to program the Baud Rate Generator. The Divisor Latch must be loaded during initialization to ensure proper operation of the Baud Rate Generator. See C.3, "Programmable Baud Rate Generator" on page C-3 for divisor settings.

2.4.12 Divisor Latch MSB Register (DLM, Index=0x1, DLAB=1)

Table 2-31. Divisor Latch MSB Holding Register (DLM)
Bits 7 - 0
Data Bits 7 - 0

Bits 7 - 0 Divisor Latch MSB, D15 - D8

Specifies the high-order byte of the 16-bit divisor used to program the Baud Rate Generator. The Divisor Latch must be loaded during initialization to ensure proper operation of the Baud Rate Generator. See C.3, "Programmable Baud Rate Generator" on page C-3 for divisor settings.

2.5 FIR Control Registers

2.5.1 Master Control Register (All Banks, Index=0x0)

Table 2-32. Master Control Register: All Banks, Address 0, R/W)

Bit 7	Bit 6	Bit 5	Bits 4 - 0
Interrupt Enable	Tx Enable	Rx Enable	Bank Select

Bits 4 - 0 Bank Select

Selects the current active register bank.

Note: Only banks 0 through 3 are valid.

Bit 5 Rx Enable

Setting this bit to 1 enables the receiver logic in the FIR Controller. No packets are received until the receiver has been enabled.

Bit 6 Tx Enable

Setting this bit to 1 enables the transmitter logic in the FIR Controller. No packets are transmitted until the transmitter has been enabled.

Bit 7 Interrupt Enable

Setting this bit to 1 enables all FIR Controller interrupts.

2.5.2 Master Status Register (Bank=0, Index=0x1)

Table 2-33. Master Status Register (Bank 0, Address 1, Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bits 3 - 1	Bit 0
Transceiver Interrupt	Timer Interrupt	Tx Interrupt	Rx Interrupt	Interrupt Identification (ID2-ID0)	Reserved

Bits 3 - 1 Interrupt Identification, ID2 - ID0

This 3-bit identification code provides an alternative method for identifying the interrupt source by indicating the interrupt type and priority level as shown in the following table.

Table 2-34. Interrupt Identification

Interrupt Type	ID2	ID1	ID0	Priority
Rx Special Condition: • FIFO Overrun • Frame Error • EOF • Rx Abort • Sync/Hunt	1	0	0	Highest
Rx Data Available	1	0	1	Second
Tx Buffer Empty	1	1	0	Third
Tx Special Condition: • FIFO Underrun • EOM • Early EOM	1	1	1	Fourth

Bit 4 Rx Interrupt

When set to 1, indicates a receiver interrupt is pending. The following conditions clear the Rx Interrupt condition:

- Reading the Rx Ring Frame Counter Low Register
- Issuing a Reset Rx Special Condition Interrupt command
- Clearing the Rx Enable bit (b5 of Master Control Register)
- Hardware Reset
- Software Reset

Bit 5 Tx Interrupt

When set to 1, indicates a transmitter interrupt is pending.

Bit 6 Timer Interrupt

When set to 1, indicates a timer interrupt is pending.

Bit 7 Transceiver Interrupt

When set to 1, indicates a transceiver insertion/removal event has occurred. See b4 of the Infrared Configuration 3 Register (2.5.23) for more information.

2.5.3 Miscellaneous Control Register (Bank=0, Index=0x1)

Table 2-35. Miscellaneous Control Register (Bank 0, Address 1, Write)

Bits 7 - 6	Bit 5	Bit 4	Bit 3	Bits 2 - 0
DMA Channel Select	Controller Loopback	4Mbps Loopback	En Zero Hold Time	Reserved

Bit 3 En Zero Hold Time

During a DMA I/O Write cycle the IBM31T1502 requires a minimum data hold time ($\overline{IOW}$ rising edge to data becomes invalid) of 10ns. Some systems reduce the hold time to close to 0ns, causing incorrect data to be loaded into the transmit FIFO. Setting this bit activates a pair of double latches that extend the system data for more than 40ns, thus eliminating the hold time. However, this also delays the data arrival time by 40ns. This bit is cleared upon reset.

Bit 4 4Mbps Loopback

Setting this bit to 1 causes the 4Mbps modem's transmit data output signal to internally loop back to its receive data input. This allows for diagnostic testing of the modem transmit and receive data paths.

Bit 5 Controller Loopback

Setting this bit to 1 causes the FIR Controller's transmit data output to internally loop back to its receive data input. This allows diagnostic testing of the FIR Controller transmit and receive data paths.

Bit 7 - 6 DMA Channel Select

Specifies single or dual DMA channel usage. The internal iDRQ1 line carries all channel 1 DMA requests, and iDRQ2 carries all channel 2 DMA requests. See 2.1.3, “DMA Line Select Register (DLS, Index=0xA2)” on page 2-3 for information on mapping internal iDRQ1 and iDRQ2 lines to external DRQn/$\overline{DACKn}$ pins.

Note: When using Shared Memory mode, DMA channel 1 must be used for receive and DMA channel 2 must be used for send.

2.5.4 RxFIFO Register (Bank=0, Index=0x2)

Table 2-36. Read Receive FIFO (Bank 0, Address 2, Read Only)
Bits 7 - 0
Data Bits 7 - 0

Bits 7 - 0 Receive Data, D7 - D0

Used to read receive packet data from RxFIFO.

2.5.5 TxFIFO Register (Bank=0, Index=0x2)

Table 2-37. Write Transmit FIFO (Bank 0, Address 2, Write Only)
Bits 7 - 0
Data Bits 7 - 0

Bits 7 - 0 Transmit Data, D7 - D0

Used to write transmit packet data to TxFIFO.

2.5.6 TxControl 1 Register (Bank=0, Index=0x3)

Table 2-38. TxControl 1 Register (Bank 0, Address 3, R/W)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Request to Send	En TxFIFO Ready Int	En FIFO Underrun /EOM Int	TxFIFO Level	Auto Reset RTS	Auto Reset EOM	Tx Idle	Underrun Abort

Bit 0 Underrun Abort

When a FIFO underrun condition occurs, the software has two options before transmission is terminated. One option is to send an abort sequence to the receiving end. The other option is to transmit a CRC and an ending/stop flag following the transmission of the last data byte in TxFIFO.

Setting this bit to 1 causes the transmitter to transmit an abort sequence when underrun occurs.

Setting this bit to 0 causes the transmitter to transmit a CRC and an ending/stop flag immediately following the transmission of the last data byte in TxFIFO before the underrun condition occurred.

Bit 1 Tx Idle

Setting this bit to 1 causes the TXD output line to remain in the inactive state (high) when the transmitter is idle.

Setting this bit to 0 causes the transmitter to transmit continuous flags (1Mbps mode) or continuous preambles (4Mbps mode) when the transmitter is idle.

Bit 2 Auto Reset EOM

Used in back-to-back packet transmissions to enable automatic resetting of the end-of-message (EOM) status indication after a successful packet transmission. This eliminates the requirement to issue a Reset FIFO Underrun/EOM Latch command after every successful packet transmission.

Setting this bit to 1 causes the EOM bit to automatically clear when the TxStatus Register is read.

Setting this bit to 0 causes the EOM bit to remain set after the TxStatus Register has been read. Only a Reset FIFO Underrun/EOM Latch command or a hardware reset can clear it.

Bit 3 Auto Reset RTS

Setting this bit to 1 enables automatic deactivation of the modem Request To Send line at the end of transmission.

For back-to-back transmission, it is desirable that the Request To Send signal remain active for the entire duration in which packets are transmitted one by one. It is therefore recommended that Auto Reset RTS be disabled while running back-to-back transmissions.

Bit 4 TxFIFO Level

Setting this bit to 1 sets the TxFIFO threshold to half-empty level (less than 8 bytes of transmit data remaining).

Setting this bit to 0 sets the TxFIFO threshold to not-full level.

Bit 5 En FIFO Underrun/EOM Int

Setting this bit to 1 enables FIFO underrun and EOM interrupts.

Bit 6 En TxFIFO Ready Int

Setting this bit to 1 enables TxFIFO Ready interrupts (TxFIFO reaches its threshold level).

Bit 7 Request To Send

Setting this bit to 1 activates the Request To Send (RTS) signal to the modem.

Note: The Tx Enable bit (b6 of the Master Control Register) must be set, and TxFIFO must contain transmit data prior to activating RTS. Setting this bit to 0 deactivates the RTS signal to the modem.

2.5.7 TxControl 2 Register (Bank=0, Index=0x4)

Table 2-39. TxControl 2 Register (Bank 0, Address 4, R/W)

Bit 7	Bit 6	Bits 5 - 4	Bit 3	Bits 2 - 0
Reserved	En Tx CRC	SIR Interaction Pulse (SIP) Control	Num Start Flag/Preamble	Early EOM Interrupt Level

Bits 2 - 0 Early EOM Interrupt Level

Specifies the number of bytes that must remain in Tx Byte Count before an Early EOM interrupt is generated. The reason for having an interrupt occur before transmission has actually completed is to allow enough time for the software to enter the proper interrupt handler routine, turn the DMA channel around for reception (Single DMA mode), or prepare for another back-to-back transmission. Once in the interrupt handler routine, the software can poll the EOM bit in TxStatus Register to determine exactly when the transmission ends.

Bit 3 Num Start Flag/Preamble

Specifies the number of starting flags (1Mbps mode) or preambles (4Mbps mode) to transmit for a given packet.

Setting this bit to 1 causes only two starting flags (1Mbps mode) or a single preamble (4Mbps mode) to be transmitted per packet.

Setting this bit to 0 causes several starting flags (1Mbps mode) or preambles (4Mbps mode) to be transmitted. Since the transmitter does not start transmitting data until the FIFO is half full, or the entire packet is stored, the transmitter continues to transmit starting flags/preambles. Therefore, the number of starting flags/preambles transmitted is controlled by the rate at which the FIFO is filled.

Bit 4 SIR Interaction Pulse (SIP) Control

Commands the 4Mbps modem to send a SIR Interaction Pulse (SIP) based on the bit setting. A 01 bit setting instructs the 4Mbps modem to transmit a SIP at the end of the current packet. A 10 bit setting instructs the 4Mbps modem to transmit a SIP immediately, regardless of the modem's current activity.

Note: SIP Control bits are self-clearing.

Bit 5 En Tx CRC

Setting this bit to 1 enables automatic CRC generation of all outgoing packets. The CRC is automatically generated by the transmitter logic and transmitted after the data field, but before the ending flag. Setting this bit to 0 disables CRC generation. This allows transmission of packets already containing a valid CRC.

Note: The En Tx CRC bit is set to 1 on power-up.

Bit 7 Reserved

This bit must be set to 0 for proper transmit operation

2.5.8 TxStatus Register (Bank=0, Index=0x5)

Table 2-40. Transmit Status Register (Bank 0, Address 5, Read Only)

Bits 7 - 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	FIFO Underrun	EOM	TxFIFO Ready	Early EOM

Bit 0 Early EOM

When set to 1, indicates the Tx Byte Count has reached the count level set by the Early EOM Interrupt Level (b2-b0 in TxControl 2 Register) bits. This bit is cleared by reading TxStatus.

Bit 1 TxFIFO Ready

When set to 1, indicates TxFIFO is ready for more data transfers. When the En TxFIFO Ready Int bit (b6 of the TxControl 1 Register) is set, an interrupt is generated whenever this condition becomes true. Alternatively, this bit may be polled when the interrupt is disabled. When TxFIFO is full, this bit is set to 0.

Bit 2 End of Message

When set to 1, indicates transmission completed successfully. The EOM interrupt occurs immediately after the CRC and ending flag have been transmitted. If Auto Reset EOM (b2 of TxControl 1 Register) is enabled, the EOM bit will automatically clear when the TxStatus Register is read. The EOM bit can also be cleared by a Reset FIFO Underrun/EOM Latch command from the Reset Command Register.

Bit 3 FIFO Underrun

When set to 1, indicates TxFIFO ran out of data before the transmitter could finish transmitting all the data (i.e. TxFIFO is empty, and the Tx Byte Count value is greater than zero). This bit must be reset by an explicit FIFO Underrun/EOM Latch command

2.5.9 RxControl Register (Bank=0, Index=0x6)

Table 2-41. Receive Control Register 1 (Bank 0, Address 6, R/W)

Bit 7	Bit 6	Bits 5 - 4	Bit 3	Bit 2	Bit 1	Bit 0
RxFIFO Level	En Rx CRC	Rx Address Mode	En Sync/Hunt Change Int	Reserved	En RxFIFO Ready Int	En Rx Special Cond Int

Bit 0 En Rx Special Cond Int

Setting this bit to 1 enables the following receive special condition interrupts:

- Overrun
- Frame Error
- End of Frame (EOF)
- Rx Abort

Bit 1 En RxFIFO Ready Int

Setting this bit to 1 enables RxFIFO Ready interrupts.

Bit 3 En Sync/Hunt Change Int

Setting this bit to 1 enables Sync/Hunt Change interrupts.

Bits 5 - 4 Rx Address Mode

Specifies the type of address filtering to apply for determining which receive frames to accept.

Note: Packets with a universal address 0x7F are always accepted.

Bit 6 En Rx CRC

Setting this bit to 1 enables automatic CRC checking of all incoming packets. Setting this bit to 0 disables CRC checking. Disabling this bit results in no CRC errors being reported.

Note: The En Rx CRC bit is set to 1 on power-up.

Bit 7 RxFIFO Level

Setting this bit to 1 sets the RxFIFO threshold to half-full (more than 8 bytes of receive data are still remaining in FIFO). Setting this bit to 0 sets the RxFIFO threshold to not empty (more than 1 byte of receive data remaining in FIFO).

2.5.10 RxStatus Register (Bank=0, Index=0x7)

Table 2-42. Receive Status Register (Bank 0, Address 7, Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Rx Abort	Frame Error	FIFO Overrun Int	EOF	Rx Data Available	Sync/Hunt Change	Reserved	Reserved

Bit 2 Sync/Hunt Change

When set to 1, indicates a transition or status change occurred on the internal Sync/Hunt signal. The following conditions cause the Sync/Hunt signal to change states:

- When an Enter Hunt Mode command is issued
- Valid SDLC start or stop flag is detected (1Mbps mode)
- Valid preamble or stop flag is detected (4Mbps mode)

If the En Sync/Hunt Change Int bit (b3 of RxControl Register) is enabled, the setting of the Sync/Hunt Change bit causes an interrupt to the host processor. Reading the RxStatus Register after the interrupt has occurred clears the Sync/Hunt Change bit.

Note: If the En Sync/Hunt Change Int bit is disabled, reading the RxStatus Register will provide the status of the Sync/Hunt signal directly and will not clear this bit.

Bit 3 Rx Data Available

When set to 1, indicates RxFIFO is not empty (i.e. the FIFO contains receive data). When set to 0, indicates RxFIFO is empty. The Rx Data Available bit, when set, does not cause an interrupt; rather it is used to unload the FIFO by polling.

Note: RxFIFO Level (b7 of RxControl Register) has no effect on the Rx Data Available bit.

Bit 4 End-of-Frame

When set to 1, indicates an ending/stop flag or abort sequence was detected in the incoming data stream. This bit is automatically cleared upon detection of the beginning/start flag of the next incoming packet.

Bit 5 FIFO Overrun Int

When set to 1, indicates the host processor was not fast enough in removing the data from RxFIFO before it overflowed with receive data.

Note: FIFO overrun is a non-recoverable error. The receiver terminates reception as soon as the overrun condition is detected. Upon receiving the overrun interrupt, the host processor must issue a Reset Rx Special Condition Interrupt command from the Reset Command Register in order to re-enable the receiver for packet reception.

Bit 6 Frame Error

When set to 1, indicates a CRC or alignment error was detected in the incoming data stream. This bit is automatically cleared upon detection of the beginning/start flag of the next incoming packet.

Bit 7 Rx Abort

When set to 1, indicates that an abort sequence was detected in the receive data stream of the current packet. In 1Mbps mode, the abort sequence is characterized by seven or more consecutive 1's in the data stream. In 4Mbps mode, the abort sequence is represented by two or more illegal symbols after a valid start flag but before a complete stop flag; or an illegal symbol, which is not part of a valid stop flag field, received any time after a valid start flag.

Note: This bit is automatically cleared upon detection of the beginning/start flag of the next incoming packet.

Note: The values of Rx Abort, Frame Error, and End-of-Frame status bits are stored in a status FIFO. The status FIFO is a 3-bit extension of the RxFIFO (i.e. RxFIFO is 11 bits wide, of which 8 bits are for receive data and 3 bits for the status). During packet reception, each FIFO entry will have an 8-bit receive data field and a 3-bit status field associated with that received byte. Thus, when the RxStatus Register is read, the values of Rx Abort, Frame Error, and End-of-Frame are read out from the top of the status FIFO. Reading the RxStatus Register does not advance the FIFO pointer. Only reading the FIFO data itself will advance the FIFO pointer.

2.5.11 Reset Command Register (Bank=0, Index=0x7)

Table 2-43. Reset Command Register (Bank 0, Address 7, Write Only)	
Bits 7 - 4	**Bits 3 - 0**
Reset Command	Reserved

Bits 7 - 4 Reset Command

Used to send a reset signal to the appropriate hardware in order to clear a particular status condition, a counter, or general reset. Issuing an Enter Hunt Mode command sets the Sync/Hunt Change status bit from a 0 to a 1.

Note: These bits are self-clearing (i.e. a programmer does not need to reset the Reset Command bit value to 0000).

2.5.12 Frame Address Register (Bank=1, Index=0x1)

Table 2-44. Frame Address Register (Bank 1, Address 1, R/W)	
Bits 7 - 1	**Bit 0**
Rx Frame Address	Reserved and set to 0

Bits 7 - 1 Rx Frame Address, A7-A1

Specifies the address value that must be contained in the address field of incoming frames. Bit 0 is not checked and is always 0. See also the Rx Address Mode setting (b5-b4 in RxControl Register) in 2.5.9, “RxControl Register (Bank=0, Index=0x6)” on page 2-32.

2.5.13 Rx Byte Count Low Register (Bank=1, Index=0x2)

Table 2-45. Rx Byte Count Low Byte (Bank 1, Address 2, Read Only)
Bits 7 - 0
Rx Byte Count

Bits 7 - 0 Rx Byte Count, D7-D0

Provides a running count (low-order value) of the number of bytes of data being received. This information is useful when receiving back-to-back packets.

2.5.14 Rx Byte Count High Register (Bank=1, Index=0x3)

Table 2-46. Rx Byte Count High Byte (Bank 1, Address 3, Read Only)	
Bits 7 - 5	**Bits 4 - 0**
Reserved	Rx Byte Count

Bits 4 - 0 Rx Byte Count, D12-D8

Provides a running count (high-order value) of the number of bytes of data being received. This information is useful when receiving back-to-back packets.

2.5.15 Rx Ring Frame Pointer Low Register (Bank=1, Index=0x4)

Table 2-47. Receive Ring Frame Pointer (RFP) Low Byte (Bank 1, Address 4, Read Only)
Bits 7 - 0
Ring Frame Pointer (RFP)

Bits 7 - 0 Ring Frame Pointer (RFP), D7-D0

Used in back-to-back packet reception to provide the end-of-packet pointer value (i.e. a pointer to the last byte of a frame received in RxBuffer).

The RFP value is initially set to 0000. This does not necessarily mean that the pointer is initially pointing to the end of a packet received. Thus, software should not use the RFP value for any computation prior to receiving the first packet.

Note: The order of byte access to the Ring Frame Pointer is critical for ensuring valid pointer values are always obtained. The programmer must ensure that the low byte is read first, followed by the high byte.

2.5.16 Rx Ring Frame Pointer High Register (Bank=1, Index=0x5)

Table 2-48. Receive Ring Frame Pointer (RFP) High Byte (Bank 1, Address 5, Read Only)	
Bits 7 - 6	**Bits 5 - 0**
Reserved	Ring Frame Pointer (RFP)

Bits 5 - 0 Ring Frame Pointer (RFP), D13-D8

Used in back-to-back packet reception to provide the end-of-frame pointer value (i.e. a pointer to the last byte of a frame received in RxBuffer). See 2.5.15, “Rx Ring Frame Pointer Low Register (Bank=1, Index=0x4).”

2.5.17 Tx Byte Count Low Register (Bank=1, Index=0x6)

Table 2-49. Tx Byte Count Low Byte (Bank 1, Address 6, R/W)
Bits 7 - 0
Byte Count Bit 7 - 0

Bits 7 - 0 Tx Byte Count, D7 - D0

Provides a running count of the number of bytes remaining to be transmitted. Before enabling transmission, software loads this register with the low-order byte length of the data packet. Each time TxFIFO is written to, the value of this counter decrements by 1. When the counter reaches zero, the transmitter ceases to make DMA requests. Transmission continues until TxFIFO is depleted.

2.5.18 Tx Byte Count High Register (Bank=1, Index=0x7)

Table 2-50. Tx Byte Count High Byte (Bank 1, Address 7, R/W)	
Bits 7 - 5	**Bits 4 - 0**
Reserved	Byte Count Bits 12 - 8

Bits 4 - 0 Tx Byte Count, D12 - D8

Specifies the high-order byte length of the data packet to be transmitted. See 2.5.17, "Tx Byte Count Low Register (Bank=1, Index=0x6)."

2.5.19 Infrared Configuration 1 Register (Bank=2, Index=0x1)

Table 2-51. Infrared Configuration 1 Register (Bank 2, Register 1, R/W)

Bits 7 - 4	Bits 3 - 0
Infrared Speed	Infrared Modulation

Bits 7 - 4 Infrared Speed

Specifies the data rate for 1Mbps FIR modulation. For HP-SIR and Sharp ASK, the data rate is set via divisor latch registers in the UART.

IR Speed				
7	6	5	4	Infrared Data Rate
0	0	0	0	1.152Mbps SDLC
0	0	0	1	576Kbps SDLC
0	0	1	0	288Kbps SDLC
0	0	1	1	Reserved
1	X	X	X	Reserved
X	1	X	X	Reserved

Bits 3 - 0 Infrared Modulation

Specifies the modulation mode for infrared communication.

IR Modulation				
3	2	1	0	Infrared Modulation
0	0	0	0	HP-SIR
0	0	0	1	Sharp ASK
0	0	1	0	1.152Mbps IrDA (1Mbps mode)
0	0	1	1	TV Direct
0	1	0	0	4Mbps IrDA (4Mbps mode)
0	1	1	X	Reserved
0	1	X	1	Reserved
1	X	X	X	Reserved

2.5.20 Infrared Transceiver Control Register (Bank=2, Index=0x2)

Table 2-52. Transceiver Control Register (Bank 2, Register 2, R/W)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GPO0	GPO1	GPO2	XCVROFF	Echo On	IRBUSY	$\overline{\text{TXD}}$ Force	GPI0

Bit 0 General Purpose Input, GPI0

This read-only bit indicates the state of the external general purpose input pin.

Bit 1 $\overline{\text{TXD}}$ Force

Setting this bit to 1 causes the external $\overline{\text{TXD}}$ pin to be asserted. Setting this bit to 0 causes the external $\overline{\text{TXD}}$ pin to be deasserted.

Note: This bit must be set to 0 for normal operation. Also, this bit is set to 0 on power-up.

Bit 2 IRBUSY

Setting this bit to 1 causes the external IRBUSY pin to be asserted. Setting this bit to 0 causes the external IRBUSY pin to be deasserted.

Bit 3 Echo On

Setting this bit to 1 enables the SIR optical modem to loop back its modulated transmit data to its receive path. This bit is set to 0 on power-up.

Bit 4 XCVROFF

Setting this bit to 1 causes the external XCVROFF pin to be asserted. Setting this bit to 0 causes the external XCVROFF pin to be deasserted. When IRBUSY is active, shutdown of the controller is inhibited.

Bit 5 General Purpose Output, GPO2

Setting this bit to 1 causes the external GPO2 pin to be asserted. Setting this bit to 0 causes the external GPO2 pin to be deasserted.

Bit 6 General Purpose Output, GPO1

Setting this bit to 1 causes the external GPO1 pin to be asserted. Setting this bit to 0 causes the external GPO1 pin to be deasserted.

Bit 7 General Purpose Output, GPO0

Setting this bit to 1 causes the external GPO0 pin to be asserted. Setting this bit to 0 causes the external GPO0 pin to be deasserted.

2.5.21 Infrared Configuration 2 Register (Bank=2, Index=0x3)

Table 2-53. Infrared Configuration 2 Register (Bank 2, Register 3, R/W)

Bit 7	Bits 6 - 5	Bit 4	Bits 3 - 2	Bits 1 - 0
4M Pulse Chop Enable	Min Pulse Ctl	4M Pulse Adjust	4M Pulse Test Ctl	IRQ Merge

Bits 6 - 5 Min Pulse Ctl1 and Min Pulse Ctl0

In receiving, the pulse width output from the transceiver may vary even though the optical pulse width it detects is of fixed width. This is due to the sensitivity characteristics of the transceiver. These two bits control the minimum pulse width that is acceptable by the IBM31T1502 as a valid received bit.

Table 2-54. Pulse Control

Min Pulse Ctl1	Min Pulse Ctl0	4M Pulse Min	1M Pulse Min	HP & Sharp Min
0	0	63ns	104ns	751ns
0	1	83ns	125ns	917ns
1	0	42ns	83ns	586ns
1	1	21ns	63ns	419ns

In the case of the 4M demodulator, this minimum should be treated more as a sensitivity level. The minimum set by these two bits is used as an absolute minimum, but the actual minimum pulse width in an individual packet is adjusted on a packet-by-packet basis. The way this works is that the absolute minimum pulse size is accepted at the beginning of a packet during the preamble phase. Halfway through the preamble phase of a packet, a typical single pulse width is sampled. The minimum pulse width set for this packet is based on the sample made, but it will never be less than the minimum set by these two bits. The double pulse (back-to-back pulse) width is adjusted as well.

Bit 4 4M Min Pulse Adjust

This bit is 0 upon reset. By default, the pulse minimum for a packet is 42ns less than the pulse width sampled during the preamble. But the overall pulse minimum will not be smaller than the minimum width set by b6 and b5. By setting this bit to 1, 21 ns is used rather than 42ns.

Bit 7 4M Pulse Chop En

In 4Mbps receive, some transceivers may deliver a single pulse greater than 165ns. This will be interpreted as a back-to-back pulse. Setting this bit to 1 allows the IBM31T1502 to handle this situation automatically. Here is how this works: If the single pulse width sampled during the preamble phase is less than 125ns, then any pulse less then 165ns in the entire packet is considered a single pulse and any pulse greater than 188ns is considered a back-to-back pulse. This relationship is illustrated as follows:

Table 2-55. 4M Pulse Enable

Preamble pulse sampled	Maximum single pulse width allowed	Minimum back-to-back pulse width allowed
< 125ns	165ns	188ns
104-145ns	187ns	209ns
125-165ns	208ns	229ns
>145ns	229ns	249ns

Bits 3 - 2 4M Pulse Test Ctl1 and 4M Test Ctl0

These two bits are used for 4Mbps pulse testing purpose only and should never be set to 1. They are cleared upon reset.

Bits 1 - 0 IRQMerge1, IRQMerge0

These two bits control the Dynamic Interrupt Merge function. This feature allows for a software driver to force the merging of the FIR and the UART interrupts dynamically.

Table 2-56. IRQMerge

IRQMerge1	IRQMerge0	Effect
0	0	No merge. Default mode.
0	1	Merged IRQ appears at UIRQ pin.
1	0	Merged IRQ appears at FIRQ pin.
1	1	Interrupt disabled.

Setting these two bits to 1 is another way to disable all interrupts to the host system.

2.5.22 General Purpose Timer Register (Bank=2, Index=0x4)

Table 2-57. General Purpose Timer Register (Bank 2, Register 4, R/W)

Bits 7 - 0
Timer Value

Bits 7 - 0 Timer Value, D7 - D0

Specifies the initialization value for the down-counter. The counter has a period of 128 ms. When the counter reaches a value of zero, an interrupt is generated.

2.5.23 Infrared Configuration 3 Register (Bank=2, Index=0x5)

Table 2-58. Infrared Configuration 3 Register (Bank 2, Register 5, R/W)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
En Sharp CD Int	Sharp Carrier Detect Int	Reserved	$\overline{\text{XCVRDET}}$	En Transceiver Change Int	Transceiver Change Int	En Timer Int	Timer Int

Bit 0 Timer Int

When set to 1, indicates a timer interrupt is pending. A timer interrupt occurs when the value in the Timer Register reaches zero. To clear the interrupt, software must write a 1 to this bit. This bit is self-clearing.

Bit 1 En Timer Int

Setting this bit to 1 enables Timer interrupts.

Bit 2 Transceiver Change Int

When set to 1, indicates the infrared transceiver was either inserted or removed from the IBM31T1502 controller chip and caused an interrupt. To clear the interrupt, software must write a 1 to this bit. This bit is self-clearing.

Bit 3 En Transceiver Change Int

Setting this bit to 1 enables Transceiver Change interrupts.

Bit 4 $\overline{\text{XCVRDET}}$

This read-only status bit indicates the state of the external $\overline{\text{XCVRDET}}$ input pin. When $\overline{\text{XCVRDET}}$ is high (inactive), it indicates the infrared transceiver is not connected to the IBM31T1502 controller chip, and the XCVROFF output pin will be asserted. When $\overline{\text{XCVRDET}}$ is low (active), the transceiver is connected to the IBM31T1502 controller, and the XCVROFF output pin will be controlled directly by the XCVROFF control bit (b4 of the Infrared Transceiver Control Register, see 2.5.20, “Infrared Transceiver Control Register (Bank=2, Index=0x2)” on page 2-39).

Bit 6 Sharp Carrier Detect Interrupt

When set to 1, this read-only status bit indicates a 500 KHz Sharp DASK carrier has been detected. To clear the interrupt, software must write a 0 to this bit.

Bit 7 En Sharp CD Int

Setting this bit to 1 enables Sharp Carrier Detect interrupts.

2.5.24 Shared Memory Page Register (Bank=3, Index=0x1)

Table 2-59. Shared Memory Page Register (Bank 3, Register 1, R/W)	
Bits 7 - 4	**Bits 3 - 0**
Transmit Page	Receive Page

In shared memory mode this register controls the paging of RAM connected locally to the controller to a smaller memory window in host system memory space. This RAM is used for transmit and receive buffers.

When the controller is in ISA mode, 8 Kbytes of system memory space is mapped using this page register into 32 Kbytes of local RAM. The 8 Kbytes of system memory space is divided into a lower block of 4 Kbytes, which acts as the receive buffer, and an upper 4 Kbyte block of memory, which is the transmit buffer. The lower 4 Kbyte receive buffer maps into the lower 16 Kbytes of local RAM according to the Receive Buffer Page value, while the upper 4 Kbyte transmit buffer maps into the upper 16 Kbytes of local RAM as per the setting of the Transmit Page Buffer.

In PCMCIA mode, 8 Kbytes of system memory can also be mapped into 32 Kbytes of local memory as described above for ISA operation, or shared memory paging can be disabled via bit b6 in the TxDMA Start Address High Register (see 2.5.26, "TxDMA Start Address High Register (Bank=3, Index=0x3)" on page 2-44). If shared memory paging is disabled, the full 32 Kbytes of local memory (upper 16 Kbytes for transmit, lower 16 Kbytes for receive) is mapped directly into 32 Kbytes of system memory space. Note that the maximum shared memory size is 32 Kbytes and this is dictated by the controller design. Shared memory sizes less than 32 Kbytes will result in address shadowing.

The address mapping is done in the following manner:

System address bits are SA12 - SA0 (8K)
Shared Memory Address bits are SMA14 - SMA0 (32K)

The Shared Memory Address bits are generated as follows: SA12 => SMA14 SA9 to SA0 => SMA9 to SMA0
IF SA12 = 1 (host access transmit buffer)
TxPage3 to 0 + SA11 to 10 => SMA13 to SMA10
IF SA12 = 0 (host access receive buffer)
RxPage3 to 0 + SA11 to 10 => SMA13 to SMA10

So, for example:
SA12-0 is 0x0CA5, RxPage3-0 is 0x3
SMA14-0 becomes 001 1000 1010 0101

And also:
SA14-0 is 0x1CA5, TxPage3-0 is 0xA
SMA14-0 becomes 111 0100 1010 0101

Wraparound is automatic at the 16 Kbyte boundary.

Bits 3 - 0 Receive Page Buffer, RxPage3 - RxPage0

These 4 bits determine the base address of a 4 Kbyte memory page in the lower 16 Kbytes of shared memory. The 4 bits allow for 16 possible locations for the Receive Page Buffer, i.e. the page may start on any 1 Kbyte boundary within the lower 16 Kbytes of shared memory.

Bits 7 - 4 Transmit Page Buffer, TxPage3 - TxPage0

These 4 bits determine the base address of a 4 Kbyte memory page in the upper 16 Kbytes of shared memory. The 4 bits allow for 16 possible locations for the Transmit Page Buffer, i.e. the page may start on any 1 Kbyte boundary within the upper 16 Kbytes of shared memory.

2.5.25 TxDMA Start Address Low Register (Bank=3, Index=0x2)

Table 2-60. Tx DMA Start Address Low Byte (Bank 3, Register 2, R/W)
Bits 7 - 0
Tx DMA Start Address

Bits 7 - 0 TxDMA Start Address, A7-A0

Specifies the low-order starting address of transmit packet data in shared memory.

2.5.26 TxDMA Start Address High Register (Bank=3, Index=0x3)

Table 2-61. Tx DMA Start Address High Byte (Bank 3, Register 3, R/W)		
Bit 7	**Bit 6**	**Bits 5 - 0**
Reserved	Page Disable	Tx DMA Start Address

Bits 5 - 0 TxDMA Start Address, A13 - A8

Specifies the high-order starting address of transmit packet data in shared memory.

Bit 6 Page Disable

Setting this bit to 1 disables shared memory paging. This only applies to PCMCIA systems.

2.5.27 Revision ID Register (Bank=3, Index=0x7)

Table 2-62. Revision ID Register (Bank 3, Register 7, Read Only)
Bits 7 - 0
Revision ID

Bits 7 - 0 Revision ID, ID7 - ID0

These bits indicate the revision level of the IBM31T1502. For example, the value 0x03 would indicate revision 3 of the controller.

3. Electrical Specifications

3.1 Recommended Operating Conditions

Table 3-1. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	V_{dd}	4.75	5.0	5.25	V
Operating Ambient Temperature	Ta	0		+60	C

3.2 Power Requirements

Table 3-2. Power Requirements (Preliminary Estimate)

Mode of Operation	Typical Power at V_{dd}=5
Power Down	50 mW
Low Speed (SIR)	223 mW
High Speed (FIR)	430 mW

3.3 DC Specifications

All TTL I/O interface specifications are from 4.75 V to 5.25 V.

3.3.1 Driver DC Voltage Specifications (in Volts)

Table 3-3. Driver DC Voltage Specifications (in Volts)

Function	MAUL	MPUL	LPUL	MPDL	LPDL	MADL
TTL	5.50	3.80	2.40	0.50	0.00	-0.50

3.3.2 Driver DC Currents at Rated Voltages

Table 3-4. Driver DC Currents at Rated Voltages

Driver Type	V_{high} (V)	I_{high} (mA)	V_{low} (V)	I_{low} (mA)
4-mA TTL Driver Outputs	2.40	-4.00	0.50	4.00
6-mA TTL Driver Outputs	2.40	-6.00	0.50	6.00
24-mA TTL Driver Outputs	2.40	-24.00	0.50	24.00

3.3.3 Receiver DC Voltage Specifications (in Volts)

Table 3-5. Receiver DC Voltage Specifications (in Volts)

Function	MAUL	MPUL	LPUL	MPDL	LPDL	MADL
TTL	5.50	5.50	2.00	0.80	0.00	-0.50

3.3.4 Receiver DC Current Specifications

Table 3-6. Receiver DC Current Specifications

Function	Iil (μa)	Iih (μa)
All receivers, no pull-up	>-1 at V_{in}=LPDL	<1 at V_{in}=MPUL
All receivers with pull-up	250 at V_{in}=LPDL	<1 at V_{in}=MPUL

Definition of terms:

MAUL (Maximum Allowable Up Level)
The maximum voltage that may be applied for extended periods without affecting the specified reliability. Circuit functionality is not implied.

MPUL (Most Positive Up Level)
The most positive voltage that maintains circuit functionality. The maximum positive logic level.

LPUL (Least Positive Up Level)
The least positive voltage that maintains circuit functionality. The minimum positive logic level.

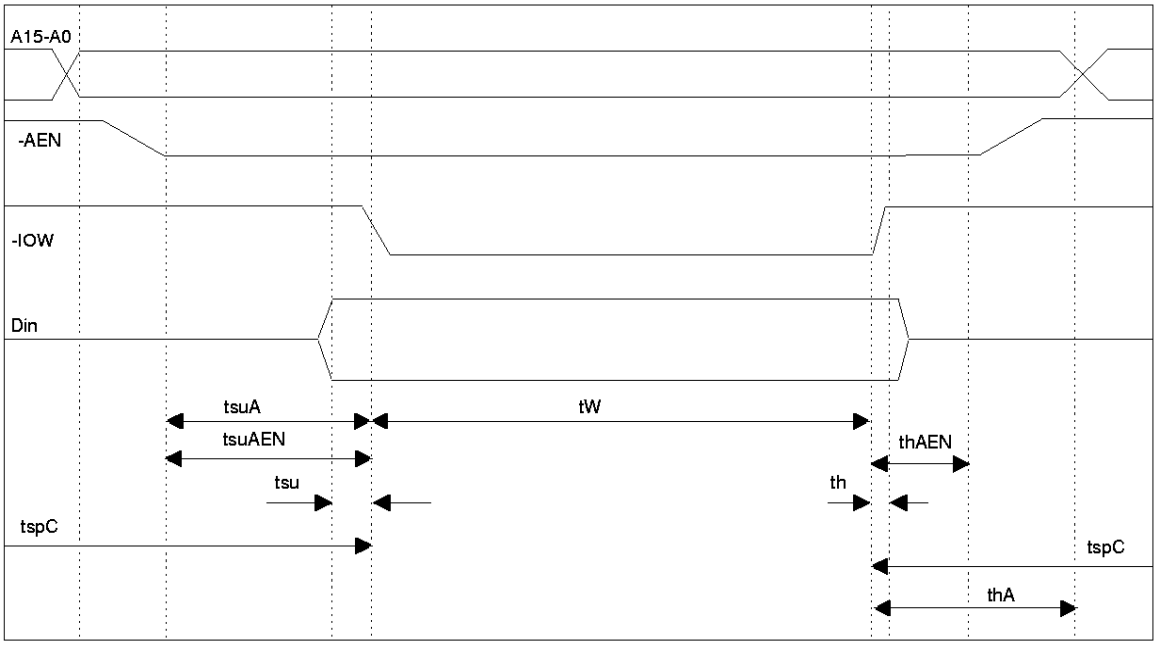
MPDL (Most Positive Down Level)
The most positive voltage that maintains circuit functionality. The maximum negative logic level.

LPDL (Least Positive Down Level)
The least positive voltage that maintains circuit functionality. The minimum negative logic level.

MADL (Minimum Allowable Down Level)
The minimum voltage that may be applied for extended periods without affecting the specified reliability. Circuit functionality is not implied.

4. Timing Diagrams

4.1 ISA Host I/O Write

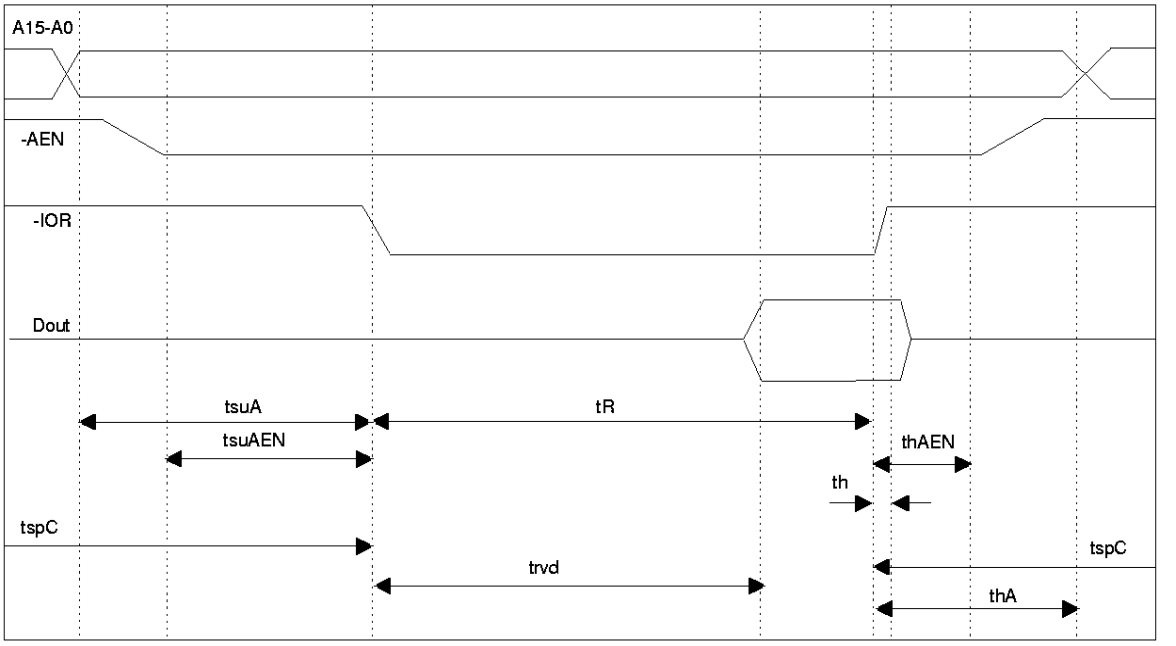


ISA Host I/O Write Timing Specification

Table 4-1. ISA Host I/O Write Timing Specification

Symbol	Description	Min (ns)	Max (ns)
tsuA	Address Setup Time	20	
tsuAEN	$\overline{\text{AEN}}$ Setup Time	20	
tsu	Data Setup Time	0	
tW	Write Time	209	
th	Data Hold Time	8	
thAEN	$\overline{\text{AEN}}$ Hold Time	20	
thA	Address Hold Time	20	
tspC	Command (Access) Separation Time	131	

4.2 ISA Host I/O Read

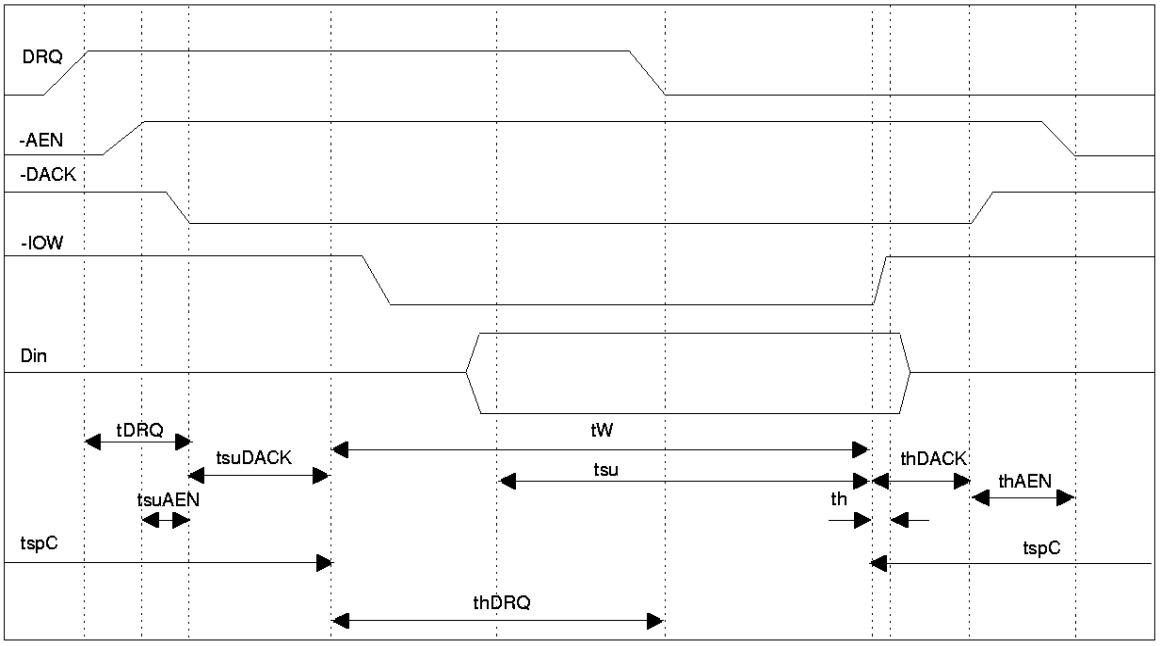


ISA Host I/O Read Timing Specification

Table 4-2. ISA Host I/O Read Timing Specification

Symbol	Description	Min (ns)	Max (ns)
tsuA	Address Setup Time	20	
tsuAEN	$\overline{AEN}$ Setup Time	20	
trvd	Active Read to Valid Data		84
tR	Read Time	168	
th	Data Hold Time	0	30
thAEN	$\overline{AEN}$ Hold Time	20	
thA	Address Hold Time	20	
tspC	Command (Access) Separation Time	131	

4.3 ISA DMA Read (I/O Write)

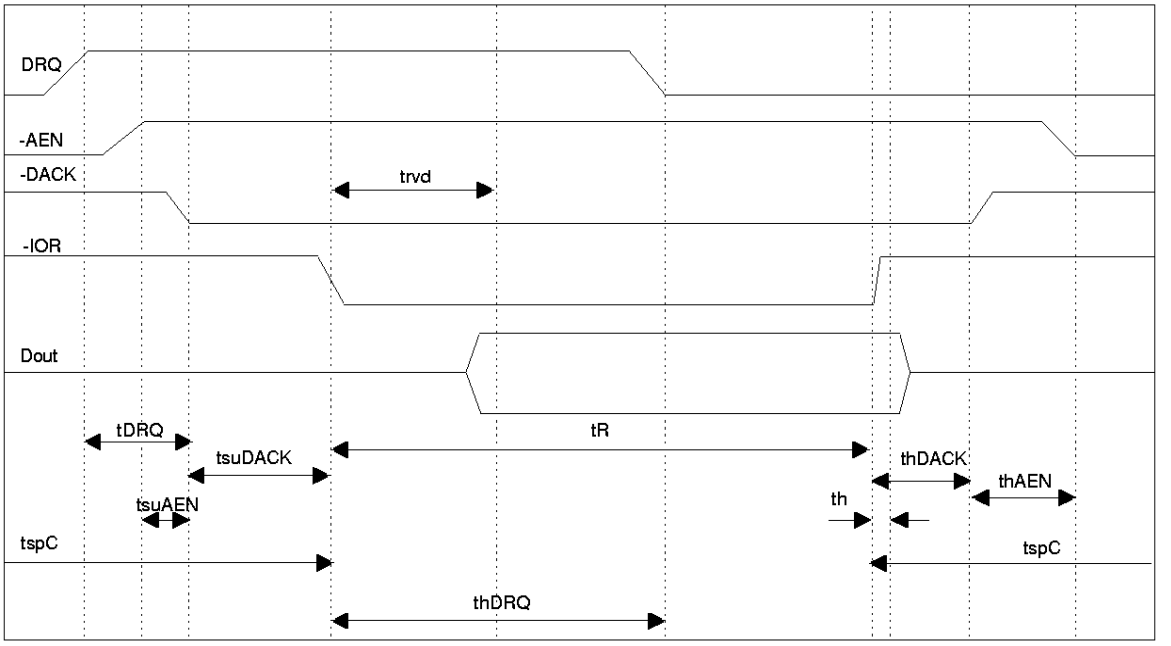


ISA DMA Read (I/O Write) Timing Specification

Table 4-3. ISA DMA Read (I/O Write) Timing Specification

Symbol	Description	Min (ns)	Max (ns)
tDRQ	DMA Request Setup Time (on first transfer)	0	
tsuAEN	$\overline{\text{AEN}}$ Setup Time (on first transfer)	0	
tsuDACK	DMA Acknowledge Setup Time (on first transfer)	20	
thDRQ (on last transfer)	DMA Request Deassertion from Active $\overline{\text{IOW}}$		160
tW	Write Time	209	
tsu	Data Setup Time	42	
th	Data Hold Time	10	
thDACK	DMA Acknowledge (on last transfer)	20	
thAEN	$\overline{\text{AEN}}$ Hold Time (on last transfer)	20	
tspC	Command (Access) Separation Time	131	

4.4 ISA DMA Write (I/O Read)

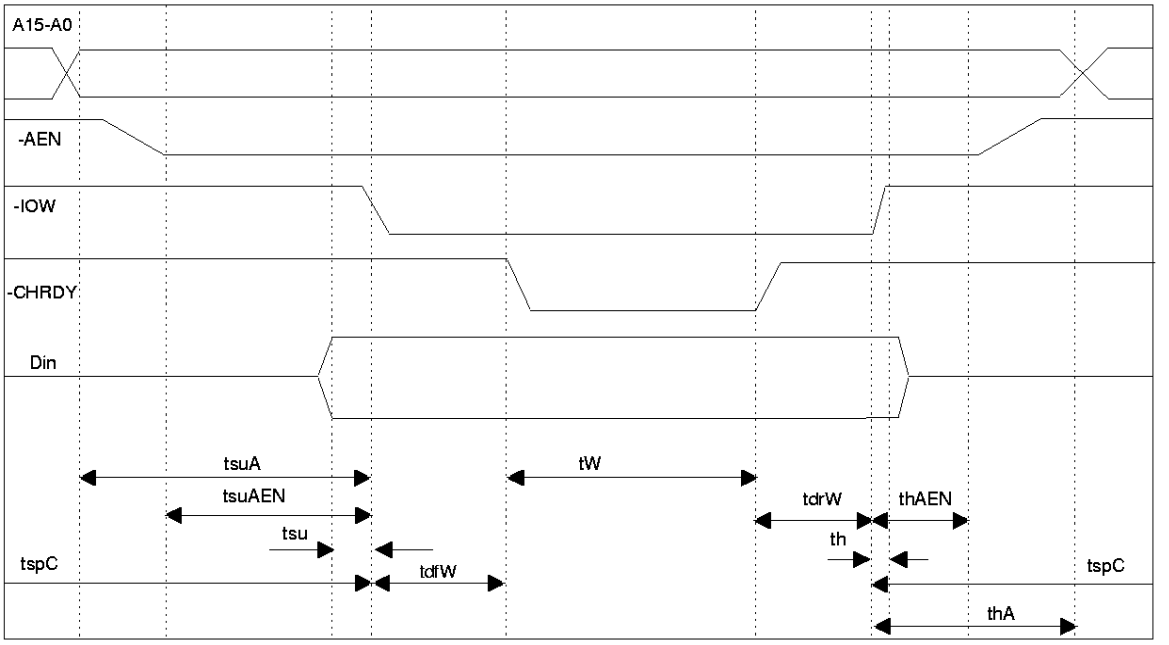


ISA DMA Write (I/O Read) Timing Specification

Table 4-4. ISA DMA Write (I/O Read) Timing Specification

Symbol	Description	Min (ns)	Max (ns)
tDRQ	DMA Request Setup Time (on first transfer)	0	
tsuAEN	$\overline{AEN}$ Setup Time (on first transfer)	0	
tsuDACK	DMA Acknowledge Setup Time (on first transfer)	20	
thDRQ (on last transfer)	DMA Request Deassertion from Active $\overline{IOR}$		160
trvd	Data Valid from Active $\overline{IOR}$		31
tR	Read Time	168	
th	Data Hold Time	0	30
thDACK	DMA Acknowledge (on last transfer)	20	
thAEN	$\overline{AEN}$ Hold Time (on last transfer)	20	
tspC	Command (Access) Separation Time	131	

4.5 Host I/O Write With Wait State (Shared Memory Configuration)

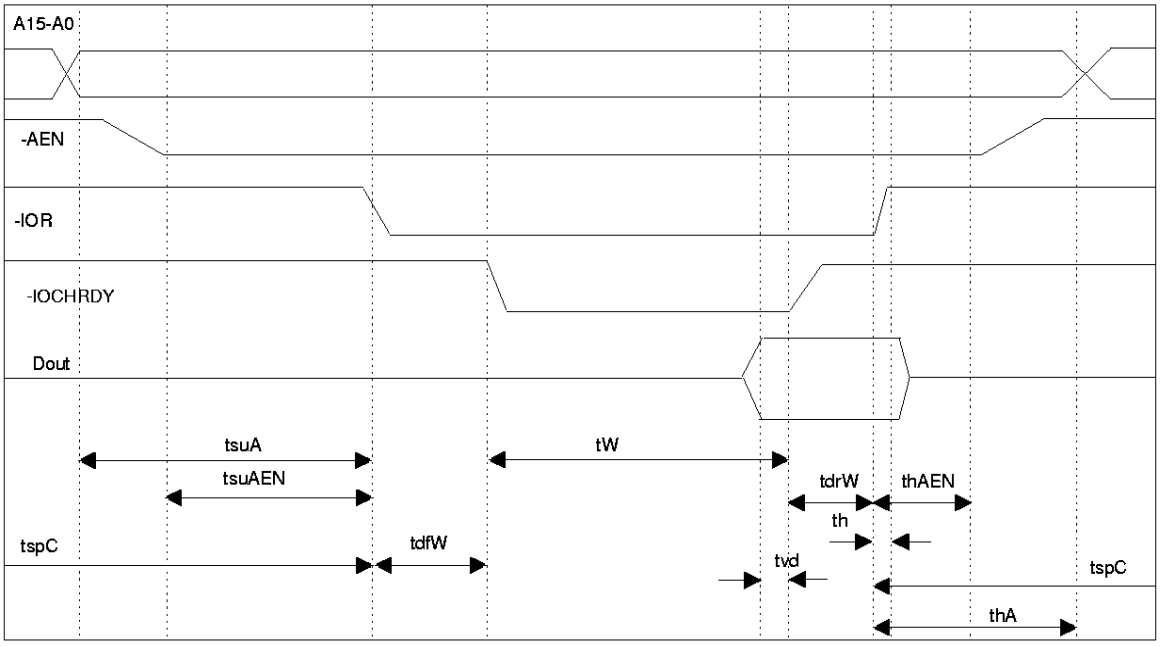


Host I/O Write with Wait State Timing Specification

Table 4-5. Host I/O Write with Wait State Timing Specification

Symbol	Description	Min (ns)	Max (ns)
tsuA	Address Setup Time	20	
tsuAEN	$\overline{\text{AEN}}$ Setup Time	20	
tsu	Data Setup Time	0	
tdfW	IOCHRDY Assertion Delay		20
tW	IOCHRDY Time		8000
tdrW	IOCHRDY Hold Time	1	
th	Data Hold Time	8	
thAEN	$\overline{\text{AEN}}$ Hold Time	20	
thA	Address Hold Time	20	
tspC	Command (Access) Separation Time	131	

4.6 Host I/O Read With Wait State (Shared Memory Configuration)

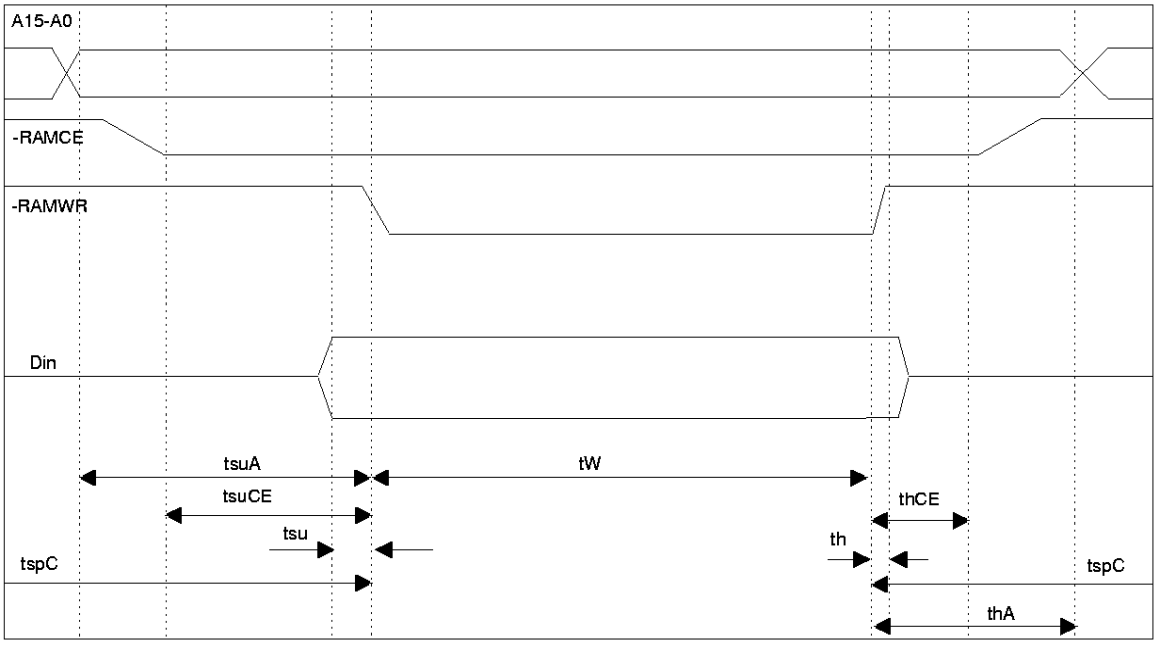


Host I/O Read with Wait State Timing Specification

Table 4-6. Host I/O Read with Wait State Timing Specification

Symbol	Description	Min (ns)	Max (ns)
tsuA	Address Setup Time	20	
tsuAEN	$\overline{\text{AEN}}$ Setup Time	20	
tvd	Data Valid to $\overline{\text{IOCHRDY}}$ Deassertion	0	
tdfW	IOCHRDY Assertion Delay		20
tW	IOCHRDY Time		8000
tdrW	IOCHRDY Hold Time	0	
th	Data Hold Time	0	30
thAEN	$\overline{\text{AEN}}$ Hold Time	20	
thA	Address Hold Time	20	
tspC	Command (Access) Separation Time	131	

4.7 Local Shared Memory Write (IBM31T1502 Access)

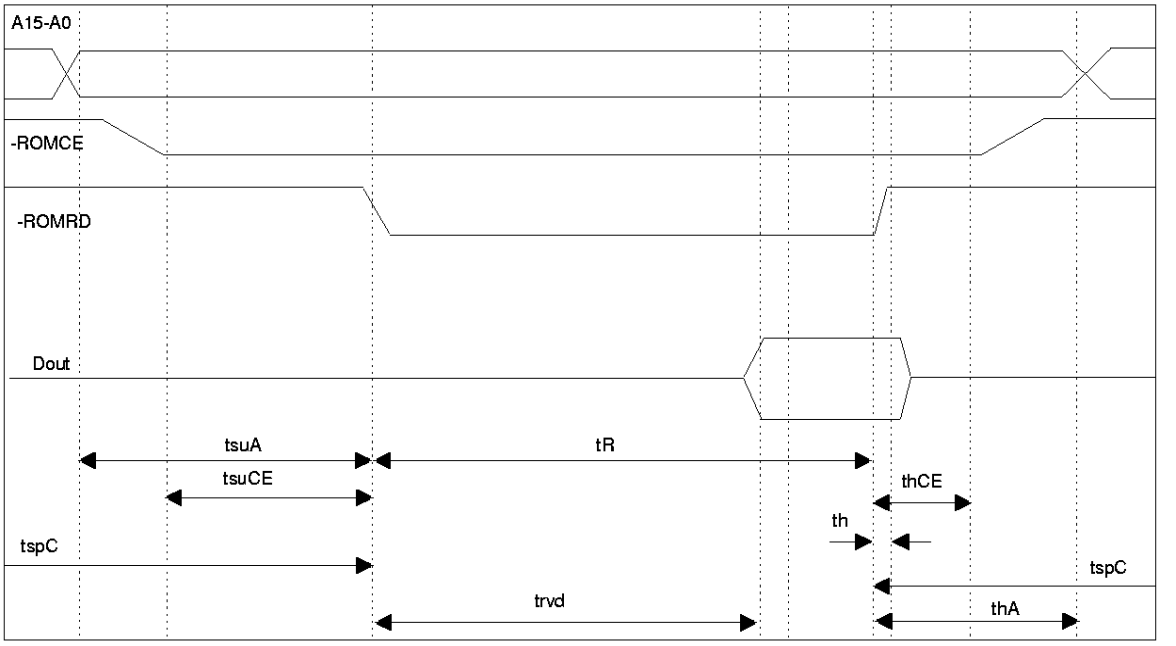


Local Shared Memory Write Timing Specification

Table 4-7. Local Shared Memory Write Timing Specification

Symbol	Description	Min (ns)	Max (ns)
tsuA	Address Setup Time	40	
tsuCE	$\overline{\text{RAMCE}}$ Setup Time	40	0
tsu	Data Setup Time	0	
tW	Write Time	209	
th	Data Hold Time	40	
thCE	$\overline{\text{RAMCE}}$ Hold Time	40	
thA	Address Hold Time	40	
tspC	Command (Access) Separation Time	96	

4.8 Local Shared Memory Read (IBM31T1502 Access)

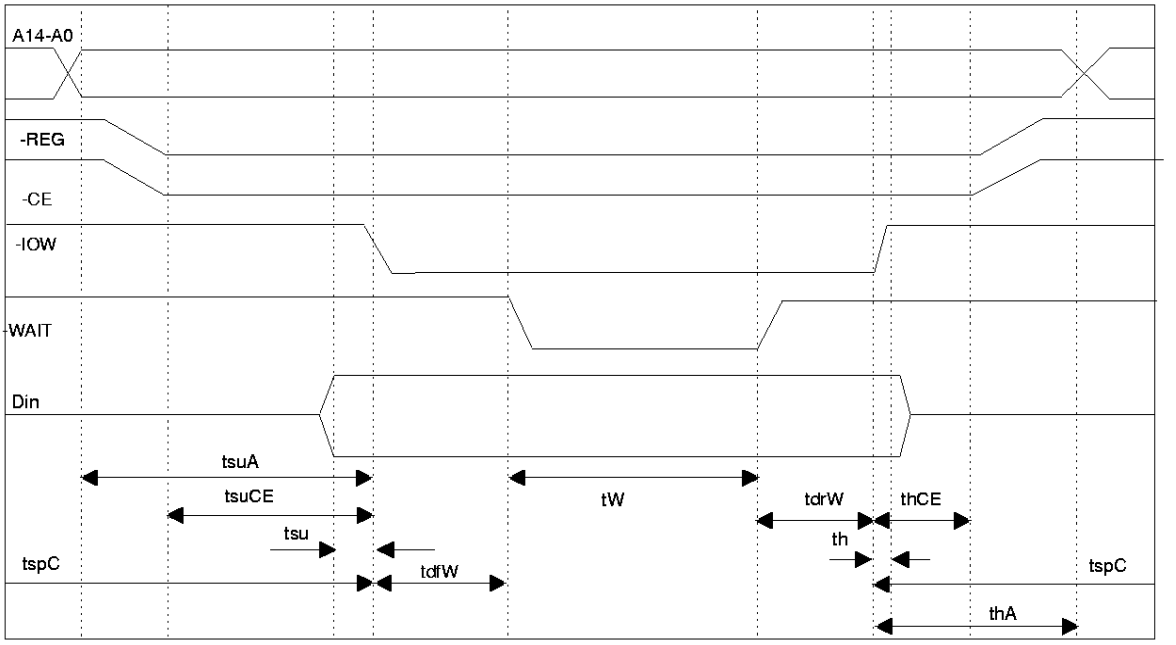


Local Shared Memory Read Timing Specification

Table 4-8. Local Shared Memory Read Timing Specification

Symbol	Description	Min (ns)	Max (ns)
tsuA	Address Setup Time	40	
tsuCE	$\overline{\text{ROMCE}}$ Setup Time	40	0
tsrvd	Data Valid from active -ROMRD		80
tR	Read Time	200	
th	Data Hold Time	0	40
thCE	$\overline{\text{ROMCE}}$ Hold Time	40	
thA	Address Hold Time	40	
tspC	Command (Access) Separation Time	96	

4.9 PCMCIA I/O and Memory Write

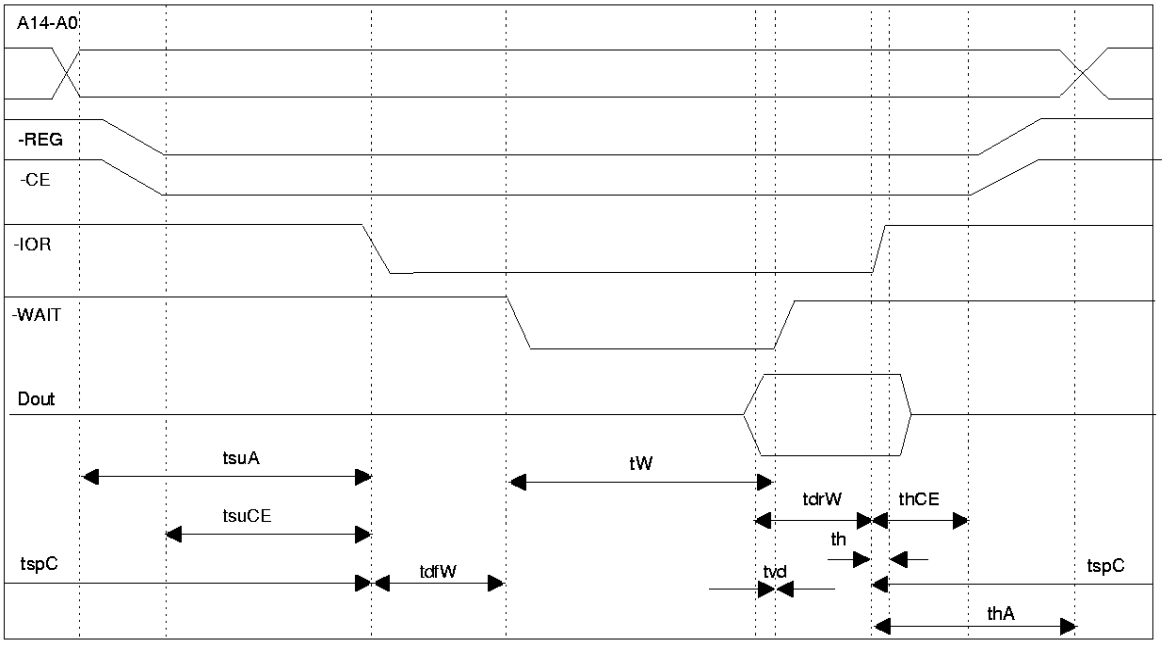


PCMCIA I/O and Memory Write Timing Specification

Table 4-9. PCMCIA I/O and Memory Write Timing Specification

Symbol	Description	Min (ns)	Max (ns)
tsuA	Address Setup Time	20	
tsuCE	$\overline{CE}$ $\overline{REG}$ Setup Time	20	
tsu	Data Setup Time	0	
tdfW	Wait Assertion Delay		20
tW	Wait Time		8000
tdrW	Wait Hold Time	0	
th	Data Hold Time	8	
thCE	CE Hold Time	20	
thA	Address Hold Time	20	
tspC	Command (Access) Separation Time	131	

4.10 PCMCIA I/O and Memory Read



PCMCIA I/O and Memory Read Timing Specification

Table 4-10. PCMCIA I/O and Memory Read Timing Specification

Symbol	Description	Min (ns)	Max (ns)
tsuA	Address Setup Time	20	
tsuCE	$\overline{CE}$ $\overline{REG}$ Setup Time	20	
tvd	Data Valid to -WAIT Deassertion	0	
tdfW	Wait Assertion Delay		20
tW	Wait Time		8000
tdrW	Wait Hold Time	0	
th	Data Hold Time	0	30
thCE	CE Hold Time	20	
thA	Address Hold Time	20	
tspC	Command (Access) Separation Time	131	

Appendix A. IR Modulation Schemes

A.1 HP-SIR Modulation

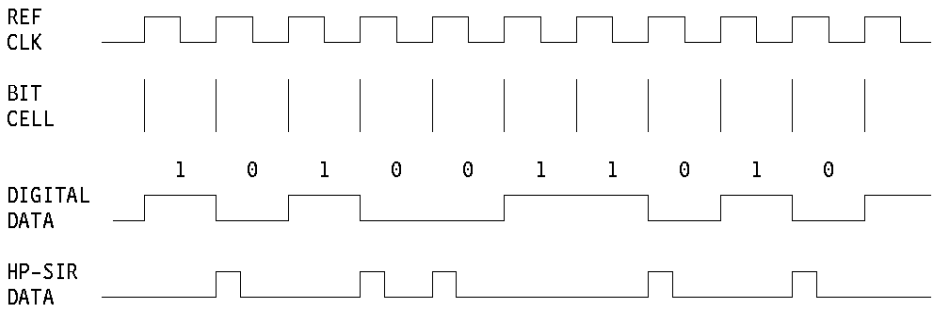


Figure A-1. HP-SIR Modulation

The HP-SIR modulation used for low speed IrDA (up to 115.2 Kbps) can be either a pulse, 3/16 of the bit time wide, or 1.6 μs wide, at the start of the bit time for a zero value. 1.6 μs is 3/16 of the bit time for the highest baud rate of 115.2 Kbps. For a one value, no pulse is sent. Data is sent on a byte basis with a Start and Stop bit sent with each byte.

A.2 Sharp Modulation

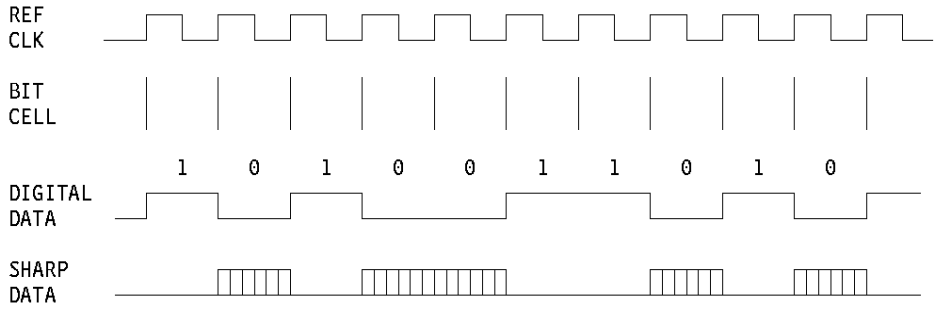


Figure A-2. SHARP ASK Modulation

Sharp Modulation is called either Amplitude Shift Keying (ASK) or Digital Amplitude Shift Keying (DASK). The infrared light is modulated with a sub-carrier with a duty cycle of 50 percent. The sub-carrier has a nominal value of 500 KHz but can range from 450 KHz to 550 KHz. When a zero is sent, the modulated infrared carrier is sent for the entire bit time. For a one, the carrier is not transmitted.

As with the HP mode, data is sent one byte at a time with a Start and Stop bit. An odd parity bit is included with each byte.

A.3 1.152 Mbps Modulation

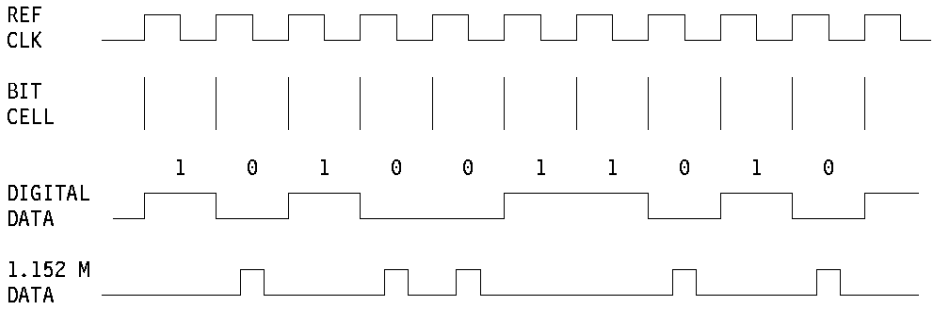


Figure A-3. 1.152 Mbps Modulation

1.152 Mbps modulation is called RZI/Flash. For a zero bit a pulse 4/16 of the bit time is sent at the middle of the bit time. For a one value, no pulse is sent.

Data is sent using an SDLC protocol, with flags and bit stuffing used to synchronize and extract the data.

A.4 4 Mbps 4PPM Modulation

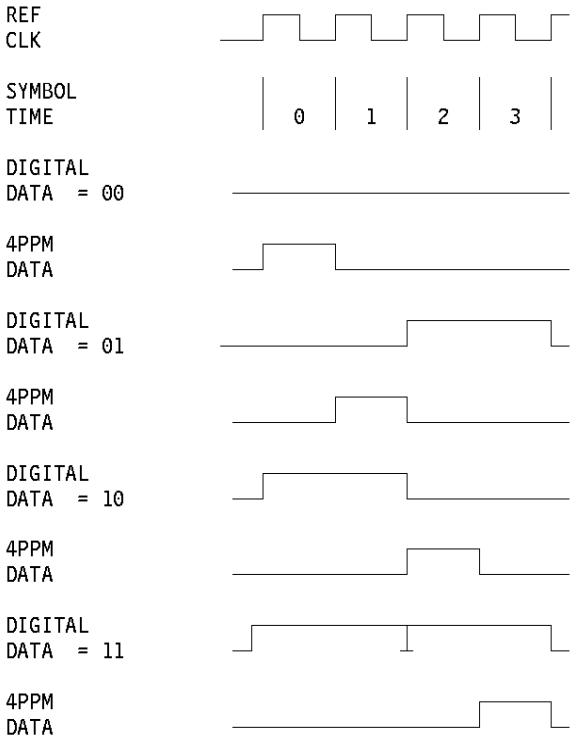


Figure A-4. 4 PPM Modulation

Four Position Pulse Modulation (4 PPM) encodes two data bits into one of four possible pulse positions. For every two data bits, only one PPM pulse will be sent.

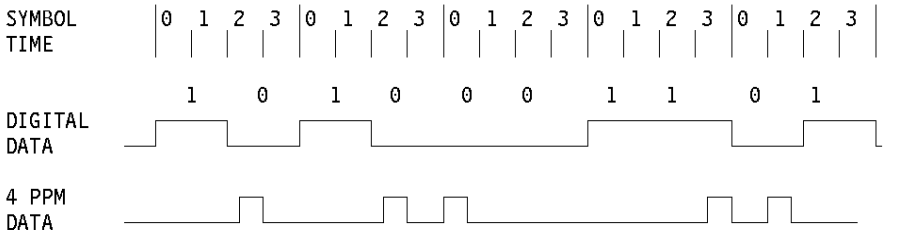


Figure A-5. 4 Mbps 4 PPM Modulation

A.4.1 4 Mbps 4 PPM Format

Figure A-6. 4 Mbps 4 PPM Frame Format

The format of the 4 Mbps 4 PPM frame is:

1. Preamble
   - 1000 0000 1010 1000
   - Repeated 16 times
2. Start Flag
   - 0000 1100 0000 1100 0110 0000 0110 0000
3. Link Layer Frame
4. Stop Flag
   - 0000 1100 0000 1100 0000 0110 0000 0110

A.4.2 4 PPM Baud Rate

The symbol time or pulse width for the 4 Mbps 4 PPM modulation is 125 ns. Each 4 PPM symbol will occur once every 500 ns or at a data rate of 2 M symbols/second. The baud rate will then be two times the data rate because each symbol represents two bits or 4 Mbps.

```
Baud Rate = Symbol rate x bits/symbol
          = 2 Mbps X 2
          = 4 Mbps
```

Appendix B. Indirect Configuration Register Default Settings

Table B-1 (Page 1 of 2). Indirect Configuration Register Default Settings

MODE0 CFG2 CFG1 CFG0	Register	Bits 7-0	Notes
X 0 0 0	**IRC**	0 0 0 0 0 1 0 0	All functions are disabled.
	FIRH	0 0 0 0 0 0 1 1	
	FIRL	0 0 0 0 0 0 0 0	
	DLS	0 0 0 0 0 0 0 0	
	UARTL	1 1 1 1 1 0 0 0	
	UARTH	0 0 0 0 0 0 1 1	
X 0 0 1	**IRC**	0 0 0 0 0 1 0 1	• UART = 0x3F8 - 0x3FF (COM1) • FIR = 0x300 - 0x307 • IRQ4 used
	FIRH	0 0 0 0 0 0 1 1	
	FIRL	0 0 0 0 0 0 0 0	
	DLS	0 0 0 0 0 0 0 0	
	UARTL	1 1 1 1 1 0 0 0	
	UARTH	0 0 0 0 0 0 1 1	
X 0 1 0	**IRC**	0 0 0 0 0 0 0 1	• UART = 0x2F8 - 0x2FF (COM2) • FIR = 0x300 - 0x307 • IRQ3 used
	FIRH	0 0 0 0 0 0 1 1	
	FIRL	0 0 0 0 0 0 0 0	
	DLS	0 0 0 0 0 0 0 0	
	UARTL	1 1 1 1 1 0 0 0	
	UARTH	0 0 0 0 0 0 1 0	
X 0 1 1	**IRC**	0 0 0 0 0 1 0 1	• UART = 0x3E8 - 0x3EF (COM3) • FIR = 0x310 - 0x317 • IRQ4 used
	FIRH	0 0 0 0 0 0 1 1	
	FIRL	0 0 0 1 0 0 0 0	
	DLS	0 0 0 0 0 0 0 0	
	UARTL	1 1 1 0 1 0 0 0	
	UARTH	0 0 0 0 0 0 1 1	
0 1 0 0	**IRC**	0 0 0 0 0 0 0 1	• UART = 0x2E8 - 0x2EF (COM4) • FIR = 0x310 - 0x317 • IRQ3 used
	FIRH	0 0 0 0 0 0 1 1	
	FIRL	0 0 0 1 0 0 0 0	
	DLS	0 0 0 0 0 0 0 0	
	UARTL	1 1 1 0 1 0 0 0	
	UARTH	0 0 0 0 0 0 1 0	
0 1 0 1	**IRC**	0 0 0 0 0 1 0 1	• UART = 0x338 - 0x33F (COM3) • FIR = 0x330 - 0x337 • IRQ4 used
	FIRH	0 0 0 0 0 0 1 1	
	FIRL	0 0 1 1 0 0 0 0	
	DLS	0 0 0 0 0 0 0 0	
	UARTL	0 0 1 1 1 0 0 0	
	UARTH	0 0 0 0 0 0 1 1	

Table B-1 (Page 2 of 2). Indirect Configuration Register Default Settings

MODE0 CFG2 CFG1 CFG0	Register	Bits 7-0	Notes
0 1 1 0	**IRC**	0 0 0 0 0 0 0 1	• UART = 0x2F8 - 0x2FF (COM2) • FIR = 0x300 - 0x307 • IRQ3 used • DMA channel 1 connected to FIR DMA channel 1
	FIRH	0 0 0 0 0 0 1 1	
	FIRL	0 0 0 0 0 0 0 0	
	DLS	0 0 0 0 0 0 0 1	
	UARTL	1 1 1 1 1 0 0 0	
	UARTH	0 0 0 0 0 0 1 0	
0 1 1 1	**IRC**	0 0 0 0 0 0 0 1	• UART = 0x2F8 - 0x2FF (COM2) • FIR = 0x300 - 0x307 • IRQ3 used • DMA channel 1 and 2 connected to FIR DMA channel 1 and 2 respectively
	FIRH	0 0 0 0 0 0 1 1	
	FIRL	0 0 0 0 0 0 0 0	
	DLS	0 0 1 0 0 0 0 1	
	UARTL	1 1 1 1 1 0 0 0	
	UARTH	0 0 0 0 0 0 1 0	
1 1 0 0	**IRC**	0 0 1 0 0 0 0 1	• UART = 0x2E8 - 0x2EF (COM4) • FIR = 0x310 - 0x317 • IRQ3 used • Local Memory window enabled at system memory location 0xC800:0x0000-0x1FFF
	FIRH	0 0 0 0 0 0 1 1	
	FIRL	0 0 0 1 0 0 0 0	
	DLS	1 1 0 0 1 0 0 0	
	UARTL	1 1 1 0 1 0 0 0	
	UARTH	0 0 0 0 0 0 1 0	
1 1 0 1	**IRC**	0 0 1 0 0 1 0 1	• UART = 0x3E8 - 0x3EF (COM3) • FIR = 0x310 - 0x317 • IRQ4 used • Local Memory window enabled at system memory location 0xD000:0x0000-0x1FFF
	FIRH	0 0 0 0 0 0 1 1	
	FIRL	0 0 0 1 0 0 0 0	
	DLS	1 1 0 1 0 0 0 0	
	UARTL	1 1 1 0 1 0 0 0	
	UARTH	0 0 0 0 0 0 1 1	
1 1 1 0	**IRC**	0 0 1 0 0 0 0 1	• UART = 0x2F8 - 0x2FF (COM2) • FIR = 0x300 - 0x307 • IRQ3 used • Local Memory window enabled at system memory location 0xC400:0x0000-0x1FFF
	FIRH	0 0 0 0 0 0 1 1	
	FIRL	0 0 0 0 0 0 0 0	
	DLS	1 1 0 0 0 1 0 0	
	UARTL	1 1 1 1 1 0 0 0	
	UARTH	0 0 0 0 0 0 1 0	
1 1 1 1	**IRC**	0 0 1 0 0 0 0 1	• UART = 0x2F8 - 0x2FF (COM2) • FIR = 0x300 - 0x307 • IRQ3 used • Local Memory window enabled at system memory location 0xD400:0x0000-0x1FFF
	FIRH	0 0 0 0 0 0 1 1	
	FIRL	0 0 0 0 0 0 0 0	
	DLS	1 1 0 1 0 1 0 0	
	UARTL	1 1 1 1 1 0 0 0	
	UARTH	0 0 0 0 0 0 1 0	

Appendix C. UART Information

C.1 UART Reset Control

Table C-1. UART Reset Control

Register/Signal	Reset Control	Reset State
IER	Chip Reset	**0000** 0001 (see note 1)
IIR	Chip Reset	00**00** 0001
FCR	Chip Reset	00**00** 0000
LCR	Chip Reset	0000 0000
MCR	Chip Reset	**000**0 0000
LSR	Chip Reset	0110 0000
MSR	Chip Reset	xxxx 0000 (see note 2)
Signal SOUT	Chip Reset	High
Receiver Line Status Interrupt	Read LSR/Chip Reset	Low/Hi-Z
Receive Data Available Interrupt	Read LSR/Chip Reset	Low/Hi-Z
THR Empty Interrupt	Read IIR/Write THR/Chip Reset	Low/Hi-Z
Modem Status Interrupt	Read MSR/Chip Reset	Low/Hi-Z
RTS	Chip Reset	High
DTR	Chip Reset	High
RxFIFO	Chip Reset/RxFIFO Reset	All Bits Low
TxFIFO	Chip Reset/TxFIFO Reset	All Bits Low

Notes:

1. Boldface bits are permanently low
2. Bits 7-4 are driven by the input signals

C.2 UART Interrupt Priority Settings Of the Interrupt Identification Register

The following table shows the priority level of the interrupts for the Interrup Identification register when an interrupt is pending.

Table C-2. UART Interrupt Priority Settings Of Interrupt Identification Register When An Interrupt Is Pending

ID2	ID1	ID0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	1	1	Highest	Receiver Line Status	• Overrun Error • Parity Error • Framing Error • Break Interrupt	Reading LSR
0	1	0	Second	Receive Data Available	• Receiver Data Available • FIFO Trigger Level Reached	• Reading RBR • FIFO drops below trigger level
1	1	0	Second	Character Timeout	No characters have been read from or written to RxFIFO during the last 4 character times, and there is at least 1 character in RxFIFO during this time	Reading RBR
0	0	1	Third	THR Empty	Transmitter Holding Register Empty	• Reading IIR Register (if source of interrupt) • Writing to THR
0	0	0	Fourth	Modem Status	• Clear To Send (CTS) • Data Set Ready (DSR) • Ring Indicator (RI) • Data Carrier Detect (DCD)	Reading MSR

C.3 Programmable Baud Rate Generator

Table C-3 provides the divisor latch settings for programming the Baud Rate Generator. The Baud Rate Generator accepts a 1.8462 MHz clock generated from chip clock, and divides it by any divisor from 1 to 2^{16}-1. The output frequency of the Baud Rate Generator is 16 times the Baud [divisor# = (frequency input) ÷ (baud rate * 16)], and is used to drive the receiver and transmitter logic of the UART.

Note: Using a divisor of zero is not recommended.

Table C-3. UART Divisor Latch Settings

Desired Baud Rate	Decimal Divisor
50	2304
75	1536
110	1047
134.5	857
150	768
300	384
600	192
1200	96
1800	64
2000	58
2400	48
3600	32
4800	24
7200	16
9600	12
19.2K	6
38.4K	3
57.6K	2
115.2K	1

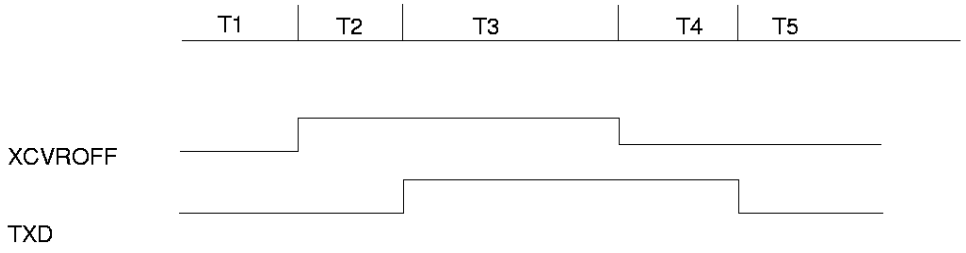
Appendix D. Bandwidth Switching with the IBM31T1101, IBM31T1100 and TFDS6000 Transceivers

Because of the optical pulse width differences between the various infrared data protocols (115.2 Kbps and below, 1.152 Mbps, and 4 Mbps), the IBM31T1100, IBM31T1101, and TFDS6000 transceivers need to have their receiver amplifier gain ratio adjusted for proper reception. The transceivers cannot do this automatically; the controller must do the necessary switching. Two serial interface lines are used: the XCVROFF line which acts like a sampling clock (sampling at the falling edge), and the TXD line which provides the speed information (high for 4 Mbps IrDA, low for 1.152 Mbps and slower IrDA data rates).

In the IBM31T1502, the XCVROFF line is directly driven by the XCVROFF bit (b4) of the Infrared Transceiver Control Register. The TXD line can also be forced to high or low under the control of the $\overline{\text{TXD}}$ Force bit (b1) of the same register. Extreme care should be taken when setting the $\overline{\text{TXD}}$ Force bit to logic 1. *Leaving this bit at a logic 1 value for too long can burn out the LED's of some transceivers, since it directly forces the LED's on.* The following illustrations show programming examples for the transceivers.

D.1.1 Switching from SIR Mode to FIR Mode

To change from HP-SIR (115.2 Kbps or lower) mode or 1.152 Mbps mode to 4 Mbps mode, the TXD and the XCVROFF lines must be pulsed in this fashion:



T1 The transceiver is currently operating in 1.152 Mbps or lower IrDA mode.

T2 Set XCVROFF bit in the Infrared Transceiver Register to 1. This drives the XCVROFF line high. The transceiver enters into a power-down state.

T3 Wait a minimum of 2 μs, then set the $\overline{\text{TXD}}$ Force bit to 1. This drives the TXD line high.[1]

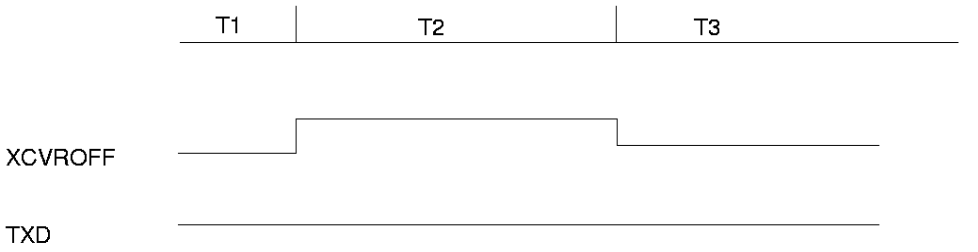
T4 Wait a minimum of 2 μs, then set the XCVROFF bit to 0. The TXD line is sampled by the transceiver and now programmed for 4 Mbps IrDA mode.

T5 Wait a minimum of 2 μs, then set the $\overline{\text{TXD}}$ Force bit to 0. Now both the controller and the transceiver are ready for receive or transmit operations.

[1] The programmer must be careful when setting the $\overline{\text{TXD}}$ Force Bit to a value of 1. This bit should not be left at a 1 state for long periods, depending on the application. With transceivers where the TXD line directly affects the turning on and off of an LED, the $\overline{\text{TXD}}$ Force Bit = 1 state (which will force the state of the TXD line to be high) will force the LED on. LED's may burn out and be irreparably damaged if left turned on for an extended period.

D.1.2 Switching from FIR Mode to SIR Mode

To change from 4 Mbps IrDA mode to 1.152 Mbps or lower IrDA mode:



T1 The transceiver is currently operating in 4 Mbps IrDA mode. Ensure that data is not being transmitted. It is important that no transmissions take place during this programming sequence since the state of the TXD line must be 0.

T2 Set the XCVROFF bit in the Infrared Transceiver Register to 1. The transceiver enters into a power-down state.

T3 Wait a minimum of 2 μs, then set the XCVROFF bit to 0. Since the $\overline{\text{TXD}}$ Force bit should always be 0 there should be no need to alter this bit (it is 0 on power-up, and should never be set and left at a 1 value, lest transceiver damage occur). The TXD line is sampled by the transceiver on the high-to-low transition. The transceiver is now programmed for 1.152 Mbps or lower speeds IrDA mode. Both the controller and the transceiver are ready for receive or transmit operations.

Appendix E. CIS Information (PCMCIA Mode)

Three sources can provide the Card Identification Structure:

- Internal chip ROM
- External Serial PROM
- External Parallel PROM

E.1 Internal CIS

The IBM31T1502 internal CIS contains the minimum amount of information required for software to uniquely identify the device, as well as configure it.

Table E-1 (Page 1 of 3). Internal CIS

Address	Value	Description
0x0000	0x01	Device Information Tuple
0x0002	0x03	Link to Next Tuple
0x0004	0xDA	= 218 Dual-Ported Memory, NO WPS Control, Access Time = 200ns
0x0006	0x1A	= 26 Maximum Window Size = 32K, calculated as 4(3 + 1)*8K units
0x0008	0xFF	Termination Byte
******	****	End of Tuple
0x000A	0x20	Manufacturer Identification Tuple
0x000C	0x04	Link to Next Tuple
0x000E	0xA4	Manufacturer = 164
0x0010	0x00	
0x0012	0x3B	Product Code = 59
0x0014	0x00	Revision Information = 0
******	****	End of Tuple
0x0016	0x21	Function Identification Tuple
0x0018	0x02	Link to Next Tuple
0x001A	0x02	= 2 Serial Device
0x001C	0x00	= 0
******	****	End of Tuple
0x001E	0x1A	Configuration Table Tuple
0x0020	0x05	Link to Next Tuple
0x0022	0x01	= 1
0x0024	0x03	= 3 Last Configuration Index
0x0026	0xF0	= 32752 (Base Address = 0x7FF0)
0x0028	0x7F	
0x002A	0x03	= 3 CFG_IDX and CFG_STS present
******	****	End of Tuple
0x002C	0x1B	Configuration Table Entry
0x002E	0x0D	Link to Next Tuple

Table E-1 (Page 2 of 3). Internal CIS		
Address	**Value**	**Description**
0x0030	0xC1	Configuration Index = 193 idx = 1 (UART only) and Default (64) and Function Spec (128)
0x0032	0x81	Interface Description Byte = 129 Wait Support Required, Function Spec = IO
0x0034	0x9D	Feature Selection Byte
0x0036	0x01	Power Description Byte
0x0038	0x55	= 85 Vnominal = 5V
0x003A	0xE0	Timing Description Byte Wait Scale = x1, Ready Busy Scale = x1
0x003C	0x7B	= 123 Wait 8 μs Max
0x003E	0x37	= 55 RDY/$\overline{\text{BSY}}$ 25 ms maximum
0x0040	0x63	I/O Description Byte UART Only, 8-bit and 16-bit I/O supported, 3 lines decoded
0x0042	0x70	Interrupt Description Byte Pulse or Level Mask Specification
0x0044	0xFE	= 65534 Allow IRQ 1-15 to be used
0x0046	0xFF	
0x0048	0x20	Miscellaneous Description Byte Power-Down Bit Supported
******	****	End of Tuple
0x004A	0x1B	Configuration Table Entry
0x004C	0x0B	Link to Next Tuple
0x004E	0x42	Configuration Index = 66 idx = 2 and Default (64)
0x0050	0x68	Feature Selection Byte
0x0052	0xE4	I/O Description Byte Range specified, 8-bit and 16-bit I/O supported, 4 lines decoded
0x0054	0x51	Length/Size Descriptor = 81 Length 1 byte, Address 1 byte, 2 ranges
0x0056	0x08	Start Address = 8 UART = 0x8 - 0xF
0x0058	0x07	Length of Address Block = 7
0x005A	0x00	Start Address = 0 FIR = 0x0 - 0x7
0x005C	0x07	Length of Address Block = 7
0x005E	0x09	TPCE_MEM Table_Definition = 9 (two possible windows available specified by length only)
0x0060	0x20	Length (value/256) = 32 8K Paged Window
0x0062	0x80	Length (value/256) = 128 32K Non-paged Window
******	****	End of Tuple
0x0064	0x1B	Configuration Table Entry
0x0066	0x08	Link To Next Tuple
0x0068	0x03	Configuration Index = 3
0x006A	0x08	Feature Selection Byte

Table E-1 (Page 3 of 3). Internal CIS		
Address	**Value**	**Description**
0x006C	0xE4	I/O Description Byte Range specified, 8-bit and 16-bit I/O supported, 4 lines decoded
0x006E	0x51	Length/Size Descriptor = 81 Length 1 byte, Address 1 byte, 2 ranges
0x0070	0x00	Start Address = 0 UART = 0x0 - 0x7
0x0072	0x07	Length of Address Block = 7
0x0074	0x08	Start Address = 8 FIR = 0x8 - 0xF
0x0076	0x07	Length of Address Block = 7
******	****	End of Tuple
0x0078	0x14	Tuple Code = 20 CISTPL_NO_LINK tuple, this is the only chain of tuples on the card
0x007A	0x00	Link to Next Tuple
******	****	End of Tuple
0x007C	0xFF	Termination Tuple

E.2 External Serial PROM CIS

When a serial PROM is used to hold the CIS, its contents get loaded into local memory address space 0x7F00 to 0x7FFE after a reset. Both hardware and software reset cause the CIS to be reloaded. After a reset, the PCMCIA is in memory-only interface, and the READY/BUSY signal is held in a busy state until the CIS has been transferred to local memory. The programmer must not attempt to access the card until the READY/BUSY signal has gone inactive.

Appendix F. Pinout Cross Reference

Notes on the following table:

- All inputs and outputs are TTL compatible.
- The pull-up resistor option guarantees that a logic 1' is applied to the internal receiver circuit when the input pin is left floating. Because of V_t, shift of the receiver isolation device, the user should not expect a logic 1's voltage at the external net. The external voltage will be slightly lower even though a logic 1' is shown in the truth table.

Table F-1 (Page 1 of 3). Pinout Cross Reference

Pin	I/O	Maximum Output Current	Input Capacity	PCMCIA Mode	ISA Mode
48	Input		4 pF	$\overline{CE2}$	A15
47	Input		4 pF	A14	A14
46	Input		4 pF	A13	A13
44	Input		4 pF	A12	A12
43	Input		4 pF	A11	A11
42	Input		4 pF	A10	A10
41	Input		4 pF	A9	A9
35	Input		4 pF	A8	A8
34	Input		4 pF	A7	A7
33	Input		4 pF	A6	A6
32	Input		4 pF	A5	A5
30	Input		4 pF	A4	A4
28	Input		4 pF	A3	A3
23	Input		4 pF	A2	A2
21	Input		4 pF	A1	A1
20	Input		4 pF	A0	A0
88	Bidirectional	4mA	4 pF	D15	$\overline{PWRDWN}$
54	Bidirectional	4mA	4 pF	D14	IRBUSY
22	Bidirectional	4mA	4 pF	D13	BADDR0
24	Bidirectional	4mA	4 pF	D12	BADDR1
99	Bidirectional	4mA	4 pF	D11	
36	Bidirectional	4mA	4 pF	D10	CFG2
31	Bidirectional	4mA	4 pF	D9	CFG1
29	Bidirectional	4mA	4 pF	D8	CFG0
56	Bidirectional	4mA	0.6 pF	D7	$\overline{BUFFEN}$
49	Bidirectional	6mA	0.6 pF	D6	IRQ3
50	Bidirectional	6mA	0.6 pF	D5	IRQ4
86	Bidirectional	4mA	0.6 pF	D4	$\overline{SETUP}$
91	Bidirectional	4mA	0.6 pF	D3	SA19
67	Bidirectional	4mA	0.6 pF	D2	SA18
63	Bidirectional	4mA	0.6 pF	D1	SA17
58	Bidirectional	4mA	0.6 pF	D0	SA16
72	Bidirectional	24mA	0.6 pF	RD7	D7
71	Bidirectional	24mA	0.6 pF	RD6	D6
69	Bidirectional	24mA	0.6 pF	RD5	D5

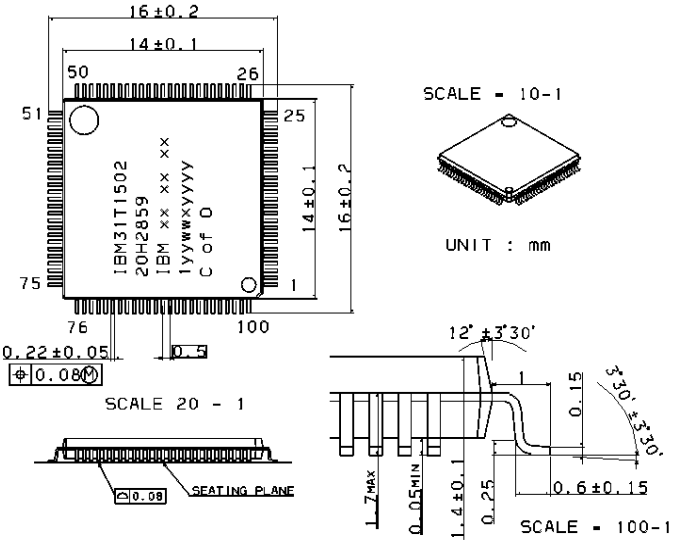
Table F-1 (Page 2 of 3). Pinout Cross Reference

Pin	I/O	Maximum Output Current	Input Capacity	PCMCIA Mode	ISA Mode
68	Bidirectional	24mA	0.6 pF	RD4	D4
65	Bidirectional	24mA	0.6 pF	RD3	D3
64	Bidirectional	24mA	0.6 pF	RD2	D2
61	Bidirectional	24mA	0.6 pF	RD1	D1
60	Bidirectional	24mA	0.6 pF	RD0	D0
18	Input		4 pF	RESET	RESET
93	Input		4 pF	$\overline{IOR}$	$\overline{IOR}$
94	Input		4 pF	$\overline{IOW}$	$\overline{IOW}$
1	Input		4 pF	$\overline{OE}$	$\overline{MR}$
25	Input		4 pF	$\overline{WE}$	$\overline{MW}$
92	Input		4 pF	$\overline{REG}$	$\overline{AEN}$
83	Bidirectional	6mA		$\overline{CE1}$	FIRQ
82	Output	6mA		RDY/$\overline{BSY}$/$\overline{IRQ}$	UIRQ
27	Output	24mA		$\overline{WAIT}$	IOCHRDY
55	Output	4mA		$\overline{INPACK}$	BUFFDIR
79	Output	6mA		MA14	MA14 (DRQ0)
80	Output	6mA		MA13	MA13 (DRQ1)
81	Output	6mA		MA12	MA12 (DRQ2)
77	Output	6mA		MA11	MA11 (DRQ3)
76	Output	6mA		MA10	MA10
75	Output	6mA		MA9	MA9
74	Output	6mA		MA8	MA8
16	Bidirectional	4mA	0.6 pF	MA7	MA7 ($\overline{DACK0}$)
15	Bidirectional	4mA	0.6 pF	MA6	MA6 ($\overline{DACK1}$)
17	Bidirectional	4mA	0.6 pF	MA5	MA5 ($\overline{DACK2}$)
14	Bidirectional	4mA	0.6 pF	MA4	MA4 ($\overline{DACK3}$)
11	Bidirectional	4mA	0.6 pF	MA3	MA3
9	Bidirectional	4mA	0.6 pF	MA2	MA2
3	Bidirectional	4mA	0.6 pF	MA1	MA1
19	Output	4mA		MA0	MA0
85	Bidirectional	4mA	0.6 pF	MODE3/$\overline{ROMCE}$	
40	Output	4mA		$\overline{RAMCE}$	$\overline{RAMCE}$
45	Output	4mA		$\overline{RAMRD}$	$\overline{RAMRD}$
51	Output	4mA		$\overline{RAMWR}$	$\overline{RAMWR}$
7	Output	24mA		TXD	TXD
98	Output	24mA		$\overline{TXD}$	$\overline{TXD}$
4	Output	4mA		XCVROFF	XCVROFF
38	Output	4mA		GP02	GP02
6	Output	4mA		GP01	GP01
5	Output	4mA		GPO0	GPO0
95	Input		4 pF	$\overline{XCVRDET}$	$\overline{XCVRDET}$
96	Input		4 pF	GPI0	GPI0
97	Input		4 pF	$\overline{RXD}$	$\overline{RXD}$

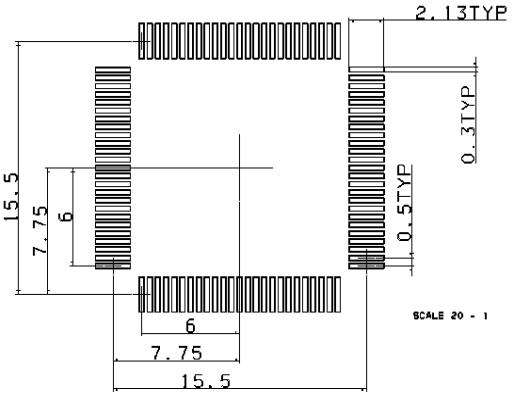
Table F-1 (Page 3 of 3). Pinout Cross Reference

Pin	I/O	Maximum Output Current	Input Capacity	PCMCIA Mode	ISA Mode
78	Input			VDD	VDD
90	Input		4 pF	CLK48	CLK48
100	Output	4mA		SER_CLK	
26	Bidirectional	4mA	0.6 pF	SER_DATA	
13	Input		4 pF	MODE2	MODE2
12	Input		4 pF	MODE1	MODE1
87	Input		4 pF	MODE0	MODE0
2	Input			RXDIEN	RXDIEN
39	Input			TME	TME
52	Input				
70	Power			VDD	VDD
62	Power			VDD	VDD
8	Power			VDD	VDD
37	Power			VDD	VDD
89	Power			VDD	VDD
57	Power			VDD	VDD
10	Power			VSS	VSS
53	Power			VSS	VSS
59	Power			VSS	VSS
66	Power			VSS	VSS
73	Power			VSS	VSS
84	Power			VSS	VSS

Appendix G. Packaging Information



G.1 IBM31T1502 Footprint



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