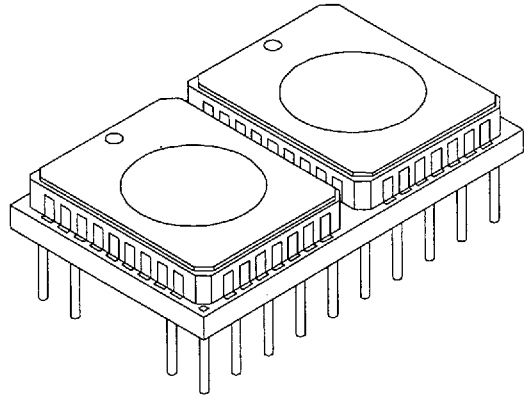


### DESCRIPTION:

The DPV32X16A is a 40-pin Pin Grid Array (PGA) consisting of two 32K X 8 UVEPROM devices in ceramic LCC packages surface mounted on a co-fired ceramic substrate with matched thermal coefficients. The LCC's are mounted in a pattern resulting in the smallest possible module outline.

The pins have been arranged around a central 0.3" gap which can accommodate a heat rail, if desired. In this central gap is a cavity containing two 0.1  $\mu$ f decoupling capacitors.



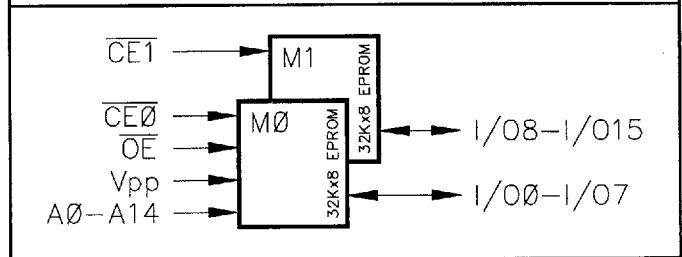
### FEATURES:

- Organizations Available:  
64K x 8 or 32K x 16
- Access Times:  
55\*, 70, 90, 120, 150, 170, 200, 250ns
- Fully Static Operation  
- No clock or refresh required
- Programming Voltage 13.0 Vdc
- Simple Programming Requirements
- Three-State Outputs
- High Speed Programming Algorithm  
(1.0ms Pulses Typ.)
- Common Data Inputs and Outputs
- TTL-compatible Inputs and Outputs
- 40-Pin PGA (Pin Grid Array) Package

\* Commercial only.

| PIN NAMES                        |                     |
|----------------------------------|---------------------|
| A0 - A14                         | Address Inputs      |
| I/O0 - I/O15                     | Data In/Out         |
| $\overline{CE0}, \overline{CE1}$ | Chip Enables        |
| $\overline{OE}$                  | Output Enable       |
| VDD                              | Power (+ 5V)        |
| VSS                              | Ground              |
| VPP                              | Programming Voltage |
| N.C.                             | No Connect          |

### FUNCTIONAL BLOCK DIAGRAM



### PIN-OUT DIAGRAM

(TOP VIEW)

|                  |    |                 |    |    |    |    |    |    |       |    |                  |
|------------------|----|-----------------|----|----|----|----|----|----|-------|----|------------------|
| $\overline{CE0}$ | 1  | I/O6            | 11 | 1  | 11 | 21 | 31 | 21 | I/O7  | 31 | VDD              |
| A9               | 2  | I/O5            | 12 | 2  | 12 | 22 | 32 | 22 | I/O2  | 32 | A0               |
| A10              | 3  | I/O4            | 13 | 3  | 13 | 23 | 33 | 23 | I/O1  | 33 | A1               |
| A11              | 4  | I/O3            | 14 | 4  | 14 | 24 | 34 | 24 | I/O0  | 34 | A2               |
| A12              | 5  | $\overline{OE}$ | 15 | 5  | 15 | 25 | 35 | 25 | A3    | 35 | A4               |
| A13              | 6  | A14             | 16 | 6  | 16 | 26 | 36 | 26 | N.C.  | 36 | A5               |
| VPP              | 7  | I/O14           | 17 | 7  | 17 | 27 | 37 | 27 | I/O15 | 37 | A6               |
| N.C.             | 8  | I/O13           | 18 | 8  | 18 | 28 | 38 | 28 | I/O10 | 38 | A7               |
| N.C.             | 9  | I/O12           | 19 | 9  | 19 | 29 | 39 | 29 | I/O9  | 39 | A8               |
| VSS              | 10 | I/O11           | 20 | 10 | 20 | 30 | 40 | 30 | I/O8  | 40 | $\overline{CE1}$ |

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| ABSOLUTE MAXIMUM RATINGS <sup>1</sup> |                                   |               |      |
|---------------------------------------|-----------------------------------|---------------|------|
| Symbol                                | Parameter                         | Value         | Unit |
| T <sub>STG</sub>                      | Storage Temperature               | -65 to +125   | °C   |
| T <sub>BIAS</sub>                     | Temperature Under Bias            | -55 to +125   | °C   |
| V <sub>DD</sub>                       | Supply Voltage <sup>2</sup>       | -0.5 to +7.0  | V    |
| V <sub>I/O</sub>                      | Input/Output Voltage <sup>2</sup> | -0.5 to +7.0  | V    |
| V <sub>PP</sub>                       | Programming Voltage <sup>2</sup>  | -0.5 to +14.0 | V    |

| AC TEST CONDITIONS: Including Programming |            |
|---|------------|
| Input Pulse Levels                        | 0V to 3.0V |
| Input Pulse Rise and Fall Time            | ≤ 20ns     |
| Input Timing Reference Levels             | 1.5V       |
| Output Timing Reference Levels            | 1.5V       |

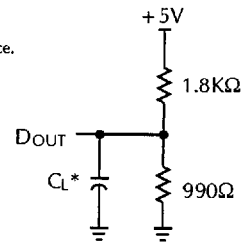
| RECOMMENDED OPERATING RANGE <sup>2</sup> |   |       |      |                      |      |
|--|---|-------|------|----------------------|------|
| Symbol                                   | Characteristic                              | Min.  | Typ. | Max.                 | Unit |
| V <sub>DD</sub>                          | Supply Voltage <sup>4</sup>                 | 4.5   | 5.0  | 5.5                  | V    |
| V <sub>IH</sub>                          | Input HIGH Voltage                          | 2.2   |      | V <sub>DD</sub> +1.0 | V    |
| V <sub>IL</sub>                          | Input LOW Voltage                           | -0.2  |      | 0.8                  | V    |
| V <sub>PP</sub>                          | V <sub>PP</sub> Supply Voltage <sup>5</sup> | 12.75 | 13.0 | 13.25                | V    |

| Output Load |                |   |
|-------------|----------------|---|
| Float       | C <sub>L</sub> | Parameters Measured                         |
| 1           | 100 pF         | except t <sub>DF</sub> and t <sub>DFF</sub> |
| 2           | 5 pF           | t <sub>DF</sub> and t <sub>DFF</sub>        |

| CAPACITANCE <sup>3</sup> : T <sub>A</sub> = 25°C, F = 1.0MHz |                   |      |      |                      |
|--|-------------------|------|------|----------------------|
| Symbol   | Parameter         | Max. | Unit | Condition            |
| C <sub>CE</sub>  | Chip Enable       | 15   | pF   | V <sub>IN</sub> = 0V |
| C <sub>ADR</sub>   | Address Input     | 35   |      |                      |
| C <sub>OE</sub>  | Output Enable     | 35   |      |                      |
| C <sub>I/O</sub>   | Data Input/Output | 25   |      |                      |

Figure 1. Output Load

\* Including Scope and Jig Capacitance.



| DC OPERATING CHARACTERISTICS <sup>6</sup> : Over operating ranges |   |   |           |                    |      |                    |      |
|---|---|---|-----------|--------------------|------|--------------------|------|
| Symbol  | Characteristics   | Test Conditions   | X8        |                    | X16  |                    | Unit |
|   |   |   | Min.      | Max.               | Min. | Max.               |      |
| I <sub>IN</sub>   | Input Leakage Current   | V <sub>IN</sub> = V <sub>DD</sub>   | -20       | 20                 | -20  | 20                 | μA   |
| I <sub>OUT</sub>  | Output Leakage Current  | CE = V <sub>IH</sub> , V <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub>   | -20       | 20                 | -10  | 10                 | μA   |
| I <sub>CC</sub>   | V <sub>DD</sub> Operating Current, Read                         | V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OUT</sub> = 0mA<br>Cycle = min., Duty = 100%                | 120-250ns |                    | 30   | 50                 | mA   |
|   |   |   | 55-90ns   |                    | 90   | 110                |      |
| I <sub>SB1</sub>  | V <sub>DD</sub> Standby Current<br>I <sub>OUT</sub> = 0mA (TTL) | CE = V <sub>IH</sub> , V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>   | 120-250ns |                    | 6    | 6                  | mA   |
|   |   |   | 55-90ns   |                    | 70   | 70                 |      |
| I <sub>SB2</sub>  | V <sub>DD</sub> Standby Current (CMOS)                          | CE = V <sub>DD</sub> ± 0.3V, I <sub>OUT</sub> = 0mA<br>V <sub>IN</sub> ≥ V <sub>DD</sub> - 3.0V or V <sub>IN</sub> ≤ 0.3V | 120-250ns |                    | 400  | 400                | μA   |
|   |   |   | 55-90ns   |                    | 60   | 60                 |      |
| I <sub>PP1</sub>  | V <sub>PP</sub> Supply Current Programming                      | CE, OE = V <sub>IL</sub> , OE = V <sub>IH</sub>   |           | 30                 |      | 60                 | mA   |
| I <sub>PP3</sub>  | V <sub>PP</sub> Supply Current Read <sup>4</sup>                | CE, OE = V <sub>IL</sub> , I <sub>OUT</sub> > 0mA   |           | 40                 |      | 40                 | μA   |
| V <sub>OL</sub>   | Output LOW Voltage  | I <sub>OUT</sub> = 2.1mA  |           | 0.45               |      | 0.45               | V    |
| V <sub>OH1</sub>  | Output HIGH Voltage   | I <sub>OUT</sub> = -400μA   | 2.4       |                    | 2.4  |                    | V    |
| V <sub>IL</sub>   | Input LOW Level   |   | -0.2      | 0.8                | -0.2 | 0.8                | V    |
| V <sub>IH</sub>   | Input HIGH Level  |   | 2.2       | V <sub>DD</sub> +1 | 2.2  | V <sub>DD</sub> +1 | V    |

| FUNCTIONS AND PIN CONNECTIONS                       |                 |                 |                 |          |          |                |
|---|-----------------|-----------------|-----------------|----------|----------|----------------|
| Mode  | Function        | $\overline{CE}$ | $\overline{OE}$ | $V_{PP}$ | $V_{DD}$ | I/O0 - I/O15   |
| Read Operations                                     | Read            | L               | L               | 5V       | 5V       | Data Out       |
|   | Output Deselect | L               | H               |          |          | High Impedance |
|   | Standby         | H               | X               |          |          | High Impedance |
| Program Operations<br>( $T_A = +25 \pm 5^\circ C$ ) | Program         | L               | H               | 13.0V    | 6.5V     | Data In        |
|   | Program Inhibit | H               | H               |          |          | High Impedance |
|   | Program Verify  | H               | L               |          |          | Data Out       |

L = LOW, H = HIGH and X = Don't Care

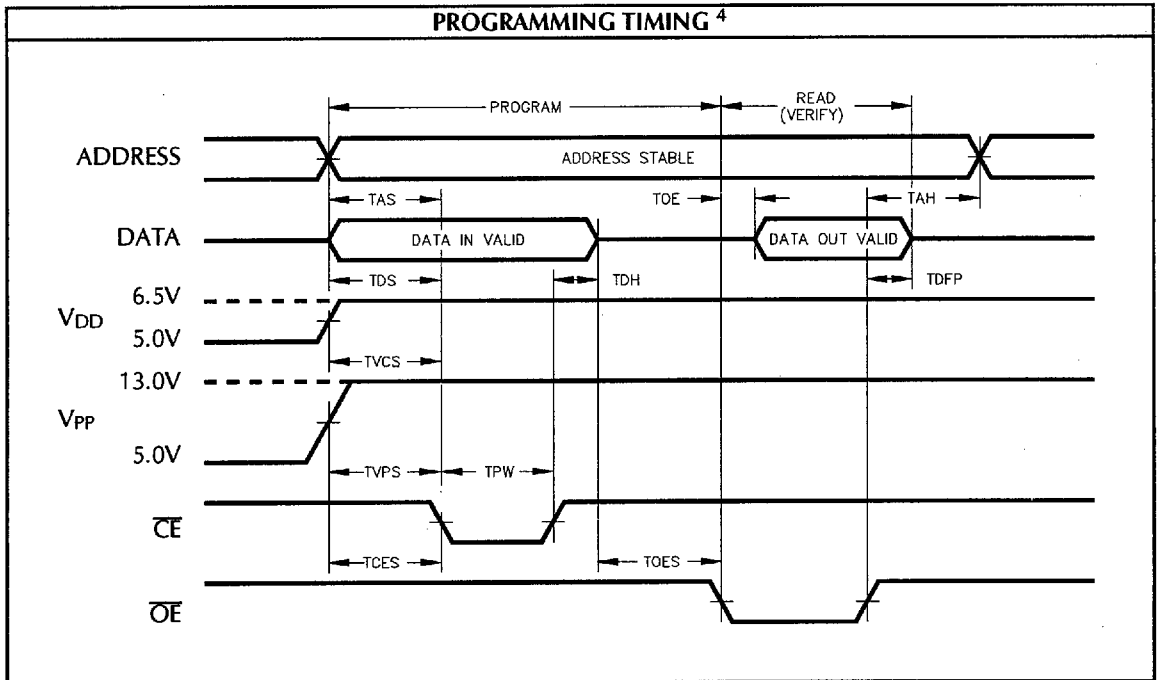
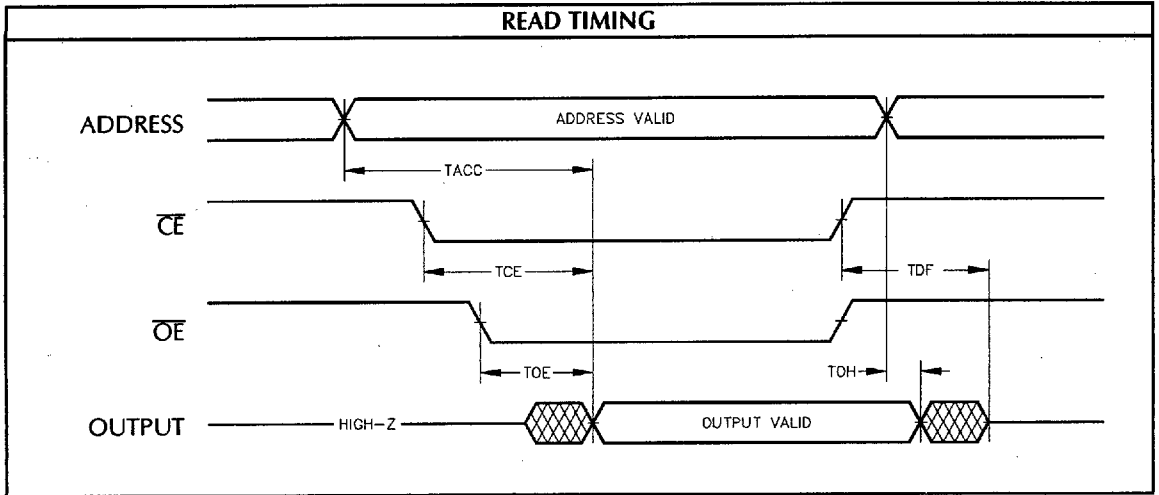
| AC OPERATING CONDITIONS AND CHARACTERISTICS - READ: Over operating ranges |           |  |       |      |      |      |      |      |       |      |      |
|---|-----------|--|-------|------|------|------|------|------|-------|------|------|
| No.   | Symbol    | Parameter  | 55ns* |      | 70ns |      | 90ns |      | 120ns |      | Unit |
|   |           |  | Min.  | Max. | Min. | Max. | Min. | Max. | Min.  | Max. |      |
| 1   | $t_{ACC}$ | Address Access Time <sup>8</sup>                                       |       | 55   |      | 70   |      | 90   |       | 120  | ns   |
| 2   | $t_{CE}$  | Chip Enable to Output Valid <sup>7</sup>                               |       | 55   |      | 70   |      | 90   |       | 120  | ns   |
| 3   | $t_{OE}$  | Output Enable to Output Valid <sup>7,8</sup>                           |       | 25   |      | 30   |      | 30   |       | 50   | ns   |
| 4   | $t_{DF}$  | $\overline{OE}$ or $\overline{CE}$ HIGH to Output Float <sup>3,9</sup> | 0     | 25   | 0    | 30   | 0    | 30   | 0     | 45   | ns   |
| 5   | $t_{OH}$  | Output Hold from Address Change  | 0     |      | 0    |      | 0    |      | 0     |      | ns   |

\* Commercial only.

| AC OPERATING CONDITIONS AND CHARACTERISTICS - READ: Over operating ranges |           |  |       |      |       |      |       |      |       |      |      |
|---|-----------|--|-------|------|-------|------|-------|------|-------|------|------|
| No.   | Symbol    | Parameter  | 150ns |      | 170ns |      | 200ns |      | 250ns |      | Unit |
|   |           |  | Min.  | Max. | Min.  | Max. | Min.  | Max. | Min.  | Max. |      |
| 1   | $t_{ACC}$ | Address Access Time <sup>8</sup>                                       |       | 150  |       | 170  |       | 200  |       | 250  | ns   |
| 2   | $t_{CE}$  | Chip Enable to Output Valid <sup>7</sup>                               |       | 150  |       | 170  |       | 200  |       | 250  | ns   |
| 3   | $t_{OE}$  | Output Enable to Output Valid <sup>7,8</sup>                           |       | 60   |       | 70   |       | 75   |       | 100  | ns   |
| 4   | $t_{DF}$  | $\overline{OE}$ or $\overline{CE}$ HIGH to Output Float <sup>3,9</sup> | 0     | 50   | 0     | 50   | 0     | 55   | 0     | 60   | ns   |
| 5   | $t_{OH}$  | Output Hold from Address Change  | 0     |      | 0     |      | 0     |      | 0     |      | ns   |

| AC PROGRAMMING CONDITIONS AND CHARACTERISTICS: Over operating ranges |           |  |      |      |         |
|--|-----------|--|------|------|---------|
| No.  | Symbol    | Parameter  | Min. | Max. | Unit    |
| 6  | $t_{AS}$  | Address Set-up Time                                | 2    |      | $\mu s$ |
| 7  | $t_{CES}$ | Chip Enable Set-up Time                            | 2    |      | $\mu s$ |
| 8  | $t_{OES}$ | Output Enable Set-up Time                          | 2    |      | $\mu s$ |
| 9  | $t_{DS}$  | Data Set-up Time                                   | 2    |      | $\mu s$ |
| 10   | $t_{VCS}$ | $V_{CC}$ Set-up Time <sup>5</sup>                  | 2    |      | $\mu s$ |
| 11   | $t_{VPS}$ | $V_{PP}$ Set-up Time <sup>5</sup>                  | 2    |      | $\mu s$ |
| 12   | $t_{AH}$  | Address Hold Time                                  | 0    |      | $\mu s$ |
| 13   | $t_{DH}$  | Data Hold Time                                     | 2    |      | $\mu s$ |
| 14   | $t_{DFP}$ | Output Enable HIGH Output Float Delay <sup>3</sup> | 0    | 130  | ns      |
| 15   | $t_{PW}$  | Programming Pulse Width <sup>10</sup>              | 95   | 105  | $\mu s$ |

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## PROGRAMMING AND ERASING INFORMATION

## PROGRAMMING

Upon delivery from Dense-Pac, or after erasure (See *Erasure section*), the DPV32X16A contains "1's" in every location, and read data is in the high state. "0's" are written into the DPV32X16A through the procedure of programming. A 0.1 $\mu$ F capacitor between  $V_{PP}$  and  $V_{SS}$  is required to prevent excessive voltage transients during programming which could damage the device. Programming modes require +6.5V and +13.0V to be applied to  $V_{DD}$  and  $V_{PP}$  respectively.

Individual bytes or address locations can be selected and programmed by using the programming algorithm shown in Figure 2. In the programming mode,  $\overline{OE}$  is set at  $V_{IH}$ ,  $V_{DD}$  is set at +6.5V, and then  $V_{PP}$  is set at +13.0V. After the applied address and input data signals are stable, programming is accomplished by a 100 $\mu$ s  $V_{IL}$  pulse on the  $\overline{CE}$  pin (refer to the *Programming Timing Diagram*).

First program each address with a 100 $\mu$ s pulse on the  $\overline{CE}$  without verification. Then return to first address and start a verification loop verifying each address. If an address location fails verification, apply up to 10 consecutive 100 $\mu$ s  $\overline{CE}$  pulses with a verification after each pulse.

If the device fails to program after 10 attempts, the programming is considered failed. After the byte is verified, continue the algorithm through all the required addresses. Lower  $V_{PP}$  to 5.0V and then lower  $V_{DD}$  to +5.0V and compare the data programmed with the original data to determine if the device passes. A programming adapter for programming on standard EPROM programmers is available, contact Dense-Pac sales for more information.

## ERASURE

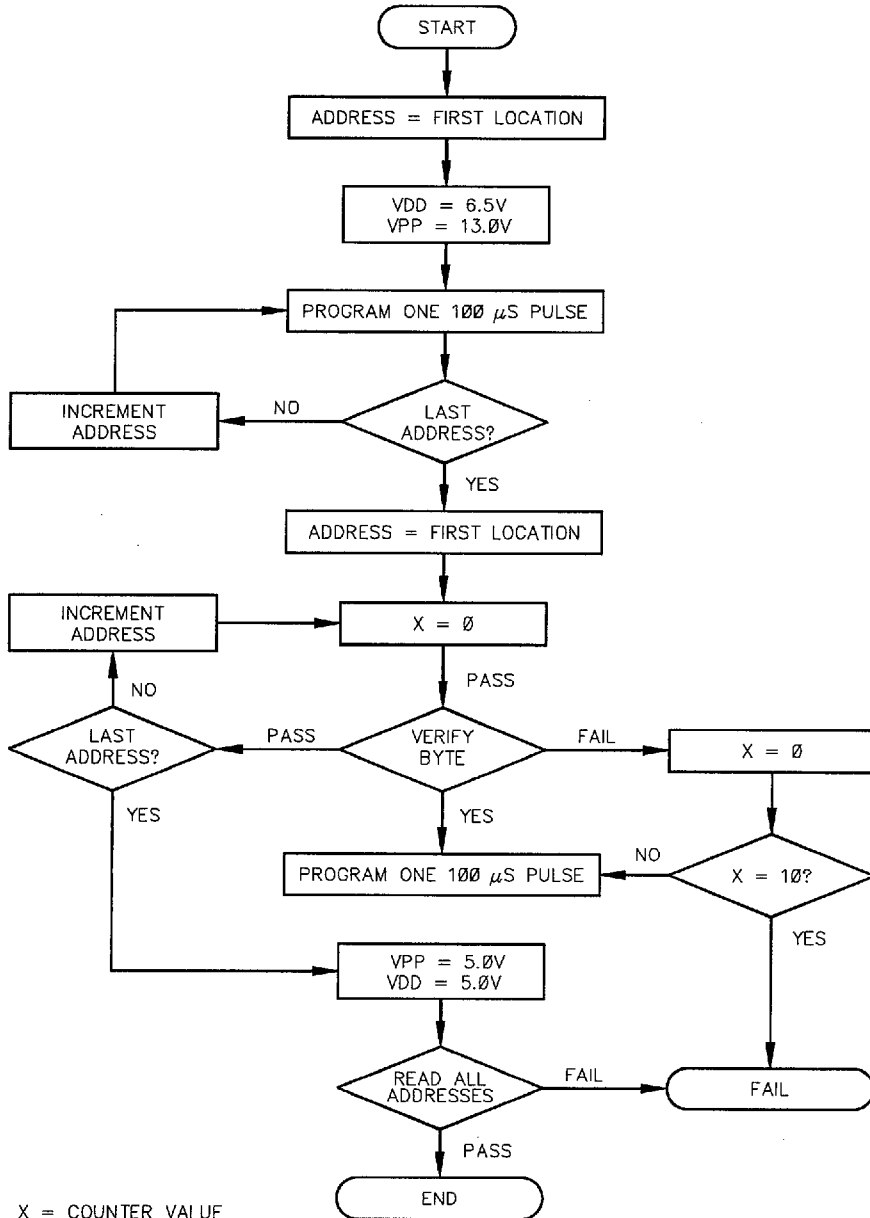
To clear all locations of their programmed contents it is necessary to expose the DPV32X16A to an ultraviolet light source. A dosage of 15W-seconds/cm<sup>2</sup> is required to completely erase a DPV32X16A. This dosage can be obtained by exposure to an ultraviolet lamp [wavelength of 2537 Angstroms (A) with an intensity of 12,000 $\mu$ W/cm<sup>2</sup>] for 20 minutes.

The DPV32X16A and similar devices can be erased by light sources having wavelengths shorter than 4000A. Although erasure time will be much longer than with UV sources at 2537A, nevertheless the exposure to fluorescent light or sunlight will eventually erase the DPV32X16A. After programming, the package windows should be covered by an opaque label or substance, to prevent inadvertent erasure.

## NOTES:

1. Stresses greater than those listed under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All voltages are with respect to  $V_{SS}$ .
3. This parameter is guaranteed and not 100% tested.
4.  $V_{DD}$  must be applied either coincident with or before  $V_{PP}$  and removed either coincident with or after  $V_{PP}$ .
5.  $V_{PP}$  must not be greater than 14.0V including overshoot. Permanent device damage may occur if the device is taken out or put into socket with  $V_{PP} = 13.0V$ . Also, during  $\overline{CE} = V_{IL}$ ,  $V_{PP}$  must not be switched from 5.0V to 13.0V or vice-versa.
6.  $t_A = -55^\circ C$  to  $+125^\circ C$ ,  $V_{DD} = 5.0V \pm 0.5V$ , and  $V_{PP} = V_{DD}$  reading.  $t_A = +25^\circ C \pm 5^\circ C$ ,  $V_{DD} = 6.5 \pm 0.25V$ ,  $V_{PP} = 13.0V \pm 0.25V$  programming.
7.  $\overline{OE}$  may be delayed up to  $t_{CE} - t_{OE}$  after the following edge of  $\overline{CE}$  without impact on  $t_{CE}$ .
8.  $\overline{OE}$  may be delayed up to  $t_{ACC} - t_{OE}$  after the following Address is valid without impact on  $t_{ACC}$ .
9.  $T_{DF}$  is specified from  $\overline{OE}$  or  $\overline{CE}$ , whichever occurs first.
10. Initial Program Pulse Width Tolerance is 100 $\mu$ s  $\pm$  5%.

Figure 2. Programming Flow Chart

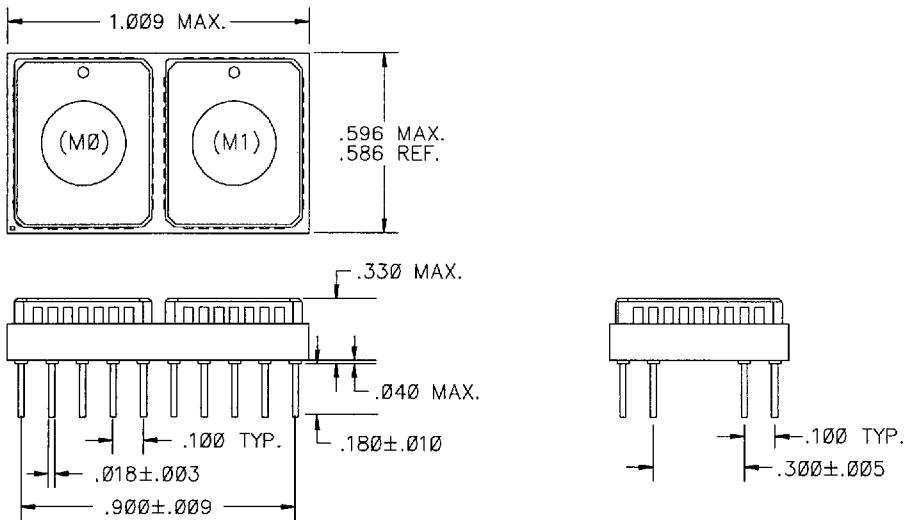


**ORDERING INFORMATION**

| <u>DP</u><br>PREFIX | <u>V32X16</u><br>DEVICE TYPE | <u>A</u><br>PACKAGE | <u>XX</u><br>SPEED | <u>X</u><br>GRADE |     |                               |
|---------------------|------------------------------|---------------------|--------------------|-------------------|-----|-------------------------------|
|                     |                              |                     |                    |                   | C   | COMMERCIAL 0°C to +70°C       |
|                     |                              |                     |                    |                   | I   | INDUSTRIAL -40°C to +85°C     |
|                     |                              |                     |                    |                   | M   | MILITARY -55°C to +125°C      |
|                     |                              |                     |                    |                   | B * | MIL-PROCESSED -55°C to +125°C |
|                     |                              |                     |                    |                   | 55  | 55ns (COMMERCIAL ONLY)        |
|                     |                              |                     |                    |                   | 70  | 70ns                          |
|                     |                              |                     |                    |                   | 90  | 90ns                          |
|                     |                              |                     |                    |                   | 12  | 120ns                         |
|                     |                              |                     |                    |                   | 15  | 150ns                         |
|                     |                              |                     |                    |                   | 17  | 170ns                         |
|                     |                              |                     |                    |                   | 20  | 200ns                         |
|                     |                              |                     |                    |                   | 25  | 250ns                         |
|                     |                              |                     |                    |                   | A   | 40-PIN PGA MODULE             |
|                     |                              |                     |                    |                   |     | UVEPROM 64KX8 OR 32KX16       |

\* B grade modules are constructed with 883 devices.

**MECHANICAL DIAGRAM**



**Dense-Pac Microsystems, Inc.**

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