16M x 4-Bit Dynamic RAM
(4k & 8k Refresh)

HYB 3164400J/T -50/-60
HYB 3165400J/T -50/-60

Preliminary Information

- 16 777 216 words by 4-bit organization
- 0 to 70 °C operating temperature
- Fast access and cycle time
  RAS access time:
  50 ns (-50 version)
  60 ns (-60 version)
  Cycle time:
  90 ns (-50 version)
  110 ns (-60 version)
  CAS access time:
  13 ns (-50 version)
  15 ns (-60 version)
- Fast page mode cycle time
  35 ns (-50 version)
  40 ns (-60 version)
- Single + 3.3 V (± 0.3V) power supply
- Low power dissipation
  max. 396 active mW (HYB 3164400J/T-50)
  max. 360 active mW (HYB 3164400J/T-60)
  max. 504 active mW (HYB 3165400J/T-50)
  max. 432 active mW (HYB 3165400J/T-60)
- 7.2 mW standby (TTL)
  720 µW standby (MOS)
- Read, write, read-modify-write, $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh (CBR),
  $\overline{\text{RAS}}$-only refresh, hidden refresh and self refresh modes
- Fast page mode capability
- 8192 refresh cycles/128 ms , 13 R/ 11C addresses (HYB 3164400J/T)
- 4096 refresh cycles/ 64 ms , 12 R/ 12C addresses (HYB 3165400J/T)
- Plastic Package:
  P-SOJ-34-1 500 mil HYB 3164(5)400J
  P-TSOPII-34-1 500 mil HYB 3164(5)400T

Ordering Information

Type	Ordering Code	Package		Descriptions
HYB 3164400J-50	on request	P-SOJ-34-1	500 mil	DRAM (access time 50 ns)
HYB 3164400J-60	on request	P-SOJ-34-1	500 mil	DRAM (access time 60 ns)
HYB 3164400T-50	on request	P-TSOPII-34-1	500 mil	DRAM (access time 50 ns)
HYB 3164400T-60	on request	P-TSOPII-34-1	500 mil	DRAM (access time 60 ns)
HYB 3165400J-50	on request	P-SOJ-34-1	500 mil	DRAM (access time 50 ns)
HYB 3165400J-60	on request	P-SOJ-34-1	500 mil	DRAM (access time 60 ns)
HYB 3165400T-50	on request	P-TSOPII-34-1	500 mil	DRAM (access time 50 ns)
HYB 3165400T-60	on request	P-TSOPII-34-1	500 mil	DRAM (access time 60 ns)

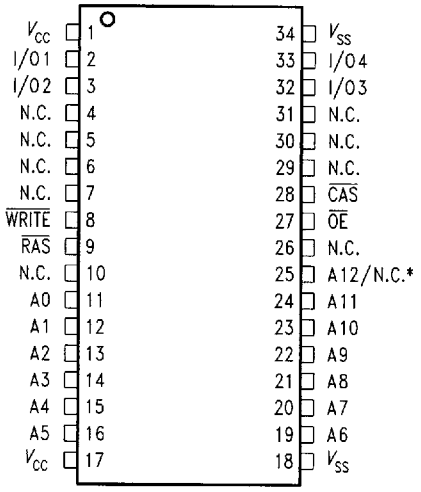
This device is a dynamic RAM organized 16 777 216 by 4 bits. The device is fabricated in SIEMENS/IBM most advanced first generation 64Mbit CMOS silicon gate process technology. The circuit and process design allow this device to achieve high performance and low power dissipation. This DRAM operates with a single 3.3 ± 0.3 V power supply and interfaces with either LVTTL or LVCMOS levels. Multiplexed address inputs permit the HYB 3164(5)400J/T to be packaged in a 500mil wide SOJ-34 or TSOP-34 plastic package. These packages provide high system bit densities and are compatible with commonly used automatic testing and insertion equipment.

Pin Definition and Functions

Pin No.	Function
A0-A12	Address Inputs for HYB 3164400J/T
A0-A11	Address Inputs for HYB 3165400J/T
$\overline{RAS}$	Row Address Strobe
$\overline{OE}$	Output Enable
I/O1-I/O4	Data Input/Output
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power Supply (+ 3.3 V)
V_{SS}	Ground

Pin Configuration
(top view)

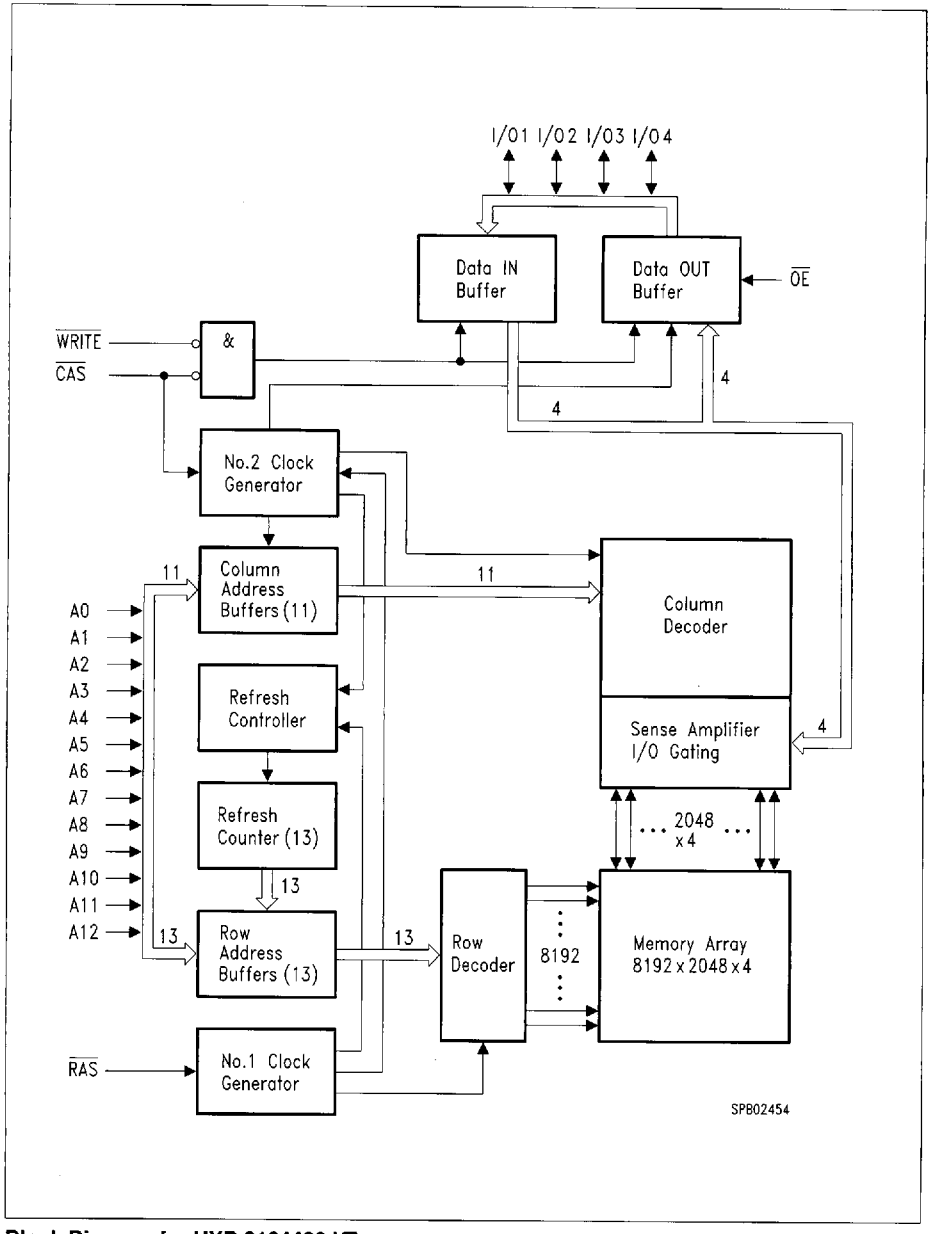
P-SOJ-34-1 (500 mil)
P-TSOPII-34-1 (500 mil)



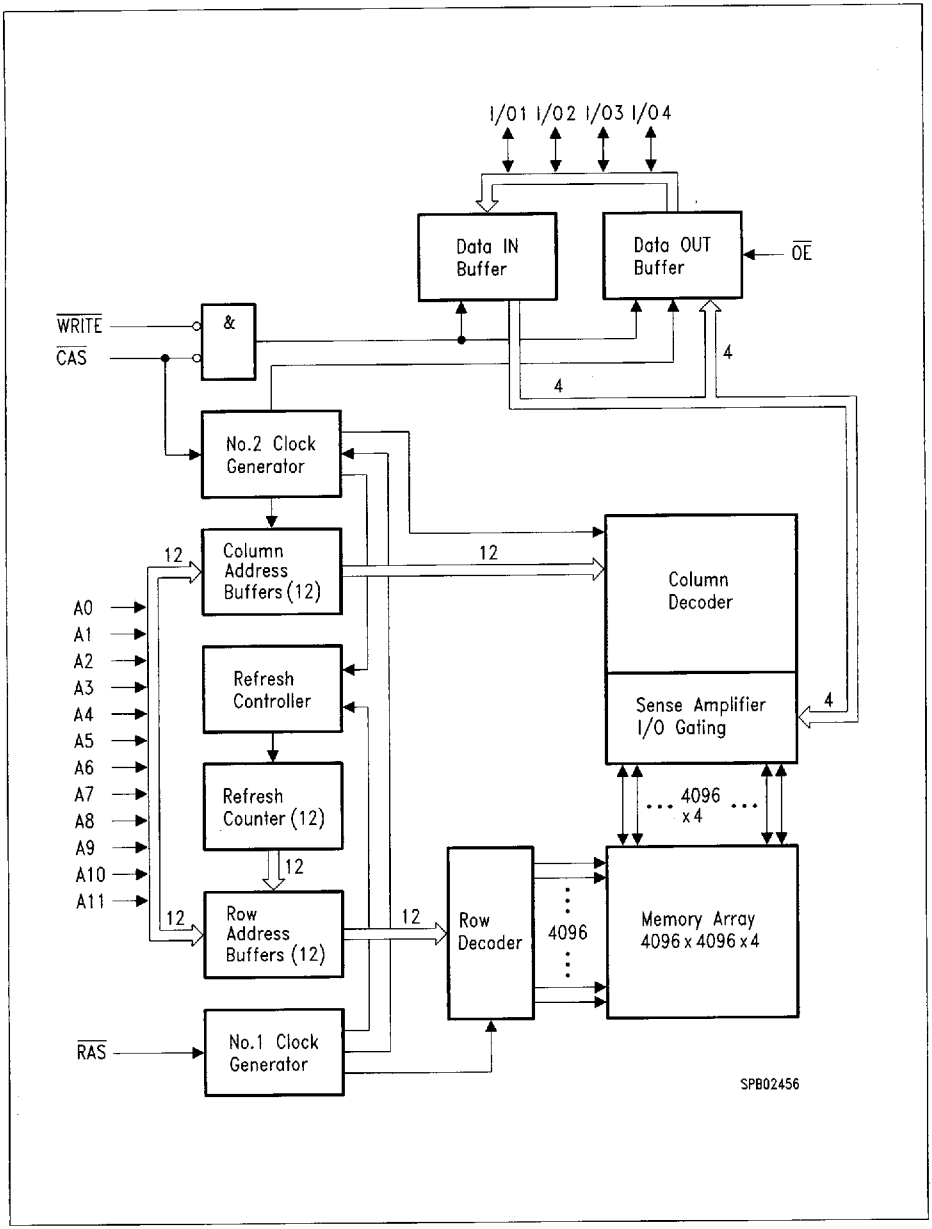
* Pin 25 is A12 for HYB 3164400J/T and N.C. for HYB 3165400J/T

TRUTH TABLE

FUNCTION		RAS	CAS	WRITE	OE	ROW ADDR	COL ADDR	I/O1-I/O4
Standby		H	H - X	X	X	X	X	High Impedance
Read		L	L	H	L	ROW	COL	Data Out
Early-Write		L	L	L	X	ROW	COL	Data In
Delayed-Write		L	L	H - L	H	ROW	COL	Data In
Read-Modify-Write		L	L	H - L	L - H	ROW	COL	Data Out, Data In
Fast Page Mode Read	1st Cycle	L	H - L	H	L	ROW	COL	Data Out
	2nd Cycle	L	H - L	H	L	n/a	COL	Data Out
Fast Page Mode Early Write	1st Cycle	L	H - L	L	X	ROW	COL	Data In
	2nd Cycle	L	H - L	L	X	n/a	COL	Data In
Fast Page Mode RMW	1st Cycle	L	H - L	H - L	L - H	ROW	COL	Data Out, Data In
	2st Cycle	L	H - L	H - L	L - H	n/a	COL	Data Out, Data In
RAS only refresh		L	H	X	X	ROW	n/a	High Impedance
CAS-before-RAS refresh		H - L	L	H	X	X	n/a	High Impedance
Test Mode Entry		H - L	L	L	X	X	n/a	High Impedance
Hidden Refresh	READ	L-H-L	L	H	L	ROW	COL	Data Out
	WRITE	L-H-L	L	L	X	ROW	COL	Data In



Block Diagram for HYB 3164400J/T



Block Diagram for HYB 3165400J/T

Absolute Maximum Ratings [1]

Operating temperature range ..... 0 to 70 °C
Storage temperature range ..... – 55 to 150 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 0.5 to min (V_{CC} + 0.5, 4.6) V
Power supply voltage ..... – 0.5 V to 4.6 V
Power dissipation ..... 1.0 W
Data out current (short circuit) ..... 50 mA

DC Characteristics

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 3 V ± 0.3 V, (values in brackets for HYB 3165400J/T)

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
Input high voltage	V_{IH}	2.0	V_{CC} + 0.3	V	2)
Input low voltage	V_{IL}	– 0.3	0.8	V	2)
Output high voltage (LVTTL) Output „H" level voltage (I_{out} = – 2m A)	V_{OH}	2.4	–	V	
Output low voltage (LVTTL) Output „L"level voltage (I_{out} = + 2m A)	V_{OL}	–	0.4	V	
Output high voltage (LVCMOS) Output „H" level voltage (I_{out} = – 100 uA)	V_{OH}	V_{CC} – 0.2	-	V	6)
Ouput low voltage (LVCMOS) Output „L" level voltage (I_{out} = + 100uA)	V_{OL}	–	0.2	V	6)
Input leakage current,any input (0 V < V_{in} < V_{CC} , all other pins = 0 V	$I_{I(L)}$	– 2	2	µA	
Output leakage current (DO is disabled, 0 V < V_{out} < V_{CC})	$I_{O(L)}$	– 2	2	µA	
Average V_{CC} supply current: -50 ns version -60 ns version ($\overline{RAS}$, $\overline{CAS}$, address cycling: t_{RC} = t_{RC} min.)	I_{CC1}	 – –	 110 (140) 100 (120)	 mA mA	3) 4) 5)
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{ih})	I_{CC2}	–	2	mA	–
Average V_{CC} supply current, during RAS-only refresh cycles: -50 ns version -60 ns version (RAS cycling: CAS = V_{IH}; t_{RC} = t_{RC} min.)	I_{CC3}	 – –	 110 (140) 100 (120)	 mA mA	3) 5)

DC Characteristics (cont'd)

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 3 V ± 0.3 V, (values in brackets for HYB 3165400J/T)

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
Average V_{CC} supply current, during fast page mode: -50 ns version -60 ns version ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling: t_{PC}=t_{PC} min.)	I_{CC4}	– –	85 (85) 75 (75)	mA mA	3) 4) 5)
Standby V_{CC} supply current ($\overline{RAS}$=$\overline{CAS}$= V_{CC} – 0.2 V)	I_{CC5}	–	200	A	–
Average V_{CC} supply current, during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode: -50 ns version -60 ns version ($\overline{RAS}$, $\overline{CAS}$ cycling: t_{RC} = t_{RC} min.)	I_{CC6}	– –	110 (140) 100 (120)	mA mA	3) 4)
Self Refresh Current Average Power Supply Current during Self Refresh. ($\overline{CBR}$ cycle with t_{RAS}>t_{RASS} min, $\overline{CAS}$ held low, $\overline{WE}$ = V_{CC} – 0.2 V, Address and Din=V_{cc} – 0.2 V or 0.2 V)	I_{CC7}	–	200	A	

AC Characteristics (Notes: 7,8,9,10)
T_A = 0 to 70 °C, V_{CC} = 3.3 ± 0.3 V

Parameter	Symbol	Limit Values				Unit	Note
		HYB 3164(5)400 J/T-50		HYB 3164(5)400 J/T-60			
		min.	max.	min.	max.		
Random read or write cycle time	t_{RC}	90	–	110	–	ns	11
Read-write cycle time	t_{RWC}	126	–	150	–	ns	
Fast page mode cycle time	t_{PC}	35	–	40	–	ns	11
Fast page mode read-write cycle time	t_{PRWC}	71	–	80	–	ns	11
Access time from RAS	t_{RAC}	–	50	–	60	ns	11,12 13,18
Access time from CAS	t_{CAC}	–	13	–	15	ns	11,12 18
Access time from column address	t_{AA}	–	25	–	30	ns	11,12 18
Access time from CAS precharge	t_{CPA}	–	30	–	35	ns	11 18
CAS to output in low-Z	t_{CLZ}	0	–	0	–	ns	18
Output buffer turn-off delay	t_{OFF}	–	13	–	15	ns	20
Transition time (rise and fall)	t_T	3	30	3	30	ns	8
RAS precharge time	t_{RP}	30	–	40	–	ns	
RAS pulse width	t_{RAS}	50	100k	60	100k	ns	11
RAS pulse width (fast page mode)	t_{RASP}	50	200k	60	200k	ns	11
$\overline{CAS}$ precharge to $\overline{RAS}$ Delay (fast page mode)	t_{RHCP}	30	–	35	–	ns	
$\overline{CAS}$ precharge to $\overline{WE}$ (FPM RMW)	t_{CPW}	48	–	55	–	ns	16
RAS hold time	t_{RSH}	13	–	15	–	ns	
CAS hold time	t_{CSH}	50	–	60	–	ns	
CAS pulse width	t_{CAS}	13	100k	15	100k	ns	11
RAS to CAS delay time	t_{RCD}	18	37	20	45		12
RAS to column address delay time	t_{RAD}	13	25	15	30	ns	13

AC Characteristics (Notes: 7,8,9,10) (cont'd)
T_A = 0 to 70 °C, V_{CC} = 3.3 ± 0.3 V

Parameter	Symbol	Limit Values				Unit	Note
		HYB 3164(5)400 J/T-50		HYB 3164(5)400 J/T-60			
		min.	max.	min.	max.		
CAS to RAS precharge time	t_{CRP}	5	–	5	–	ns	11
CAS precharge time	t_{CP}	10	–	10	–	ns	
Row address setup time	t_{ASR}	0	–	0	–	ns	
Row address hold time	t_{RAH}	8	–	10	–	ns	
Column address setup time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	10	–	10	–	ns	
Column address to RAS lead time	t_{RAL}	25	–	30	–	ns	11
Read command setup time	t_{RCS}	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	ns	19
Read command hold time referenced to RAS	t_{RRH}	0	–	0	–	ns	
Write command hold time	t_{WCH}	8	–	10	–	ns	
Write command pulse width	t_{WP}	8	–	10	–	ns	
Write command to RAS lead time	t_{RWL}	13	–	15	–	ns	
Write command to CAS lead time	t_{CWL}	13	–	15	–	ns	
Data setup time	t_{DS}	0	–	0	–	ns	17
Data hold time	t_{DH}	10	–	10	–	ns	17
Refresh period for HYB 3164400J/T	t_{REF}	–	128	–	128	ms	
Refresh period for HYB 3165400J/T	t_{REF}	–	64	–	64	ms	
Write command setup time	t_{WCS}	0	–	0	–	ns	16
CAS to WRITE delay time (RMW)	t_{CWD}	31	–	35	–	ns	16
RAS to WRITE delay time (RMW)	t_{RWD}	68	–	80	–	ns	16
Column address to WRITE delay time (RMW)	t_{AWD}	43	–	50	–	ns	16
CAS setup time (CAS-before-RAS cycle)	t_{CSR}	5	–	5	–	ns	

AC Characteristics (Notes: 7,8,9,10) (cont'd)
T_A = 0 to 70 °C, V_{CC} = 3.3 ± 0.3 V

Parameter	Symbol	Limit Values				Unit	Note
		HYB 3164(5)400 J/T-50		HYB 3164(5)400 J/T-60			
		min.	max.	min.	max.		
CAS hold time (CAS-before-RAS cycle)	t_{CHR}	10	–	10	–	ns	
RAS to CAS precharge time	t_{RPC}	5	–	5	–	ns	
CAS precharge time (CAS-before-RAS counter test cycle)	t_{CPT}	25	–	30	–	ns	
Write command setup time (in test mode entry cycle)	t_{WTS}	10	–	10	–	ns	
Write command hold time (in test mode entry cycle)	t_{WTH}	10	–	10	–	ns	
Write to RAS precharge time (CAS-before-RAS cycle)	t_{WRP}	10	–	10	–	ns	
Write hold time referenced to RAS (CAS-before-RAS cycle)	t_{WRH}	10	–	10	–	ns	
OE command hold time	t_{OEH}	13	–	15	–	ns	
OE access time	t_{OEA}	–	13	–	15	ns	11,18
Output buffer turn-off delay from OE	t_{OEZ}	–	13	–	15	ns	20
CAS delay time from Din	t_{DZC}	0	–	0	–	ns	15
Data to OE low delay	t_{DZO}	0	–	0	–	ns	15
CAS high to data delay	t_{CDD}	13	–	15	–	ns	14
OE high to data delay	t_{ODD}	13	–	15	–	ns	14
RAS pulse width during self refresh cycle	t_{RASS}	100k	–	100k	–	ns	21
RAS precharge time during self refresh	t_{RPS}	90	–	110	–		21
CAS hold time during self refresh	t_{CHS}	50	–	50	–	ns	21

Capacitance

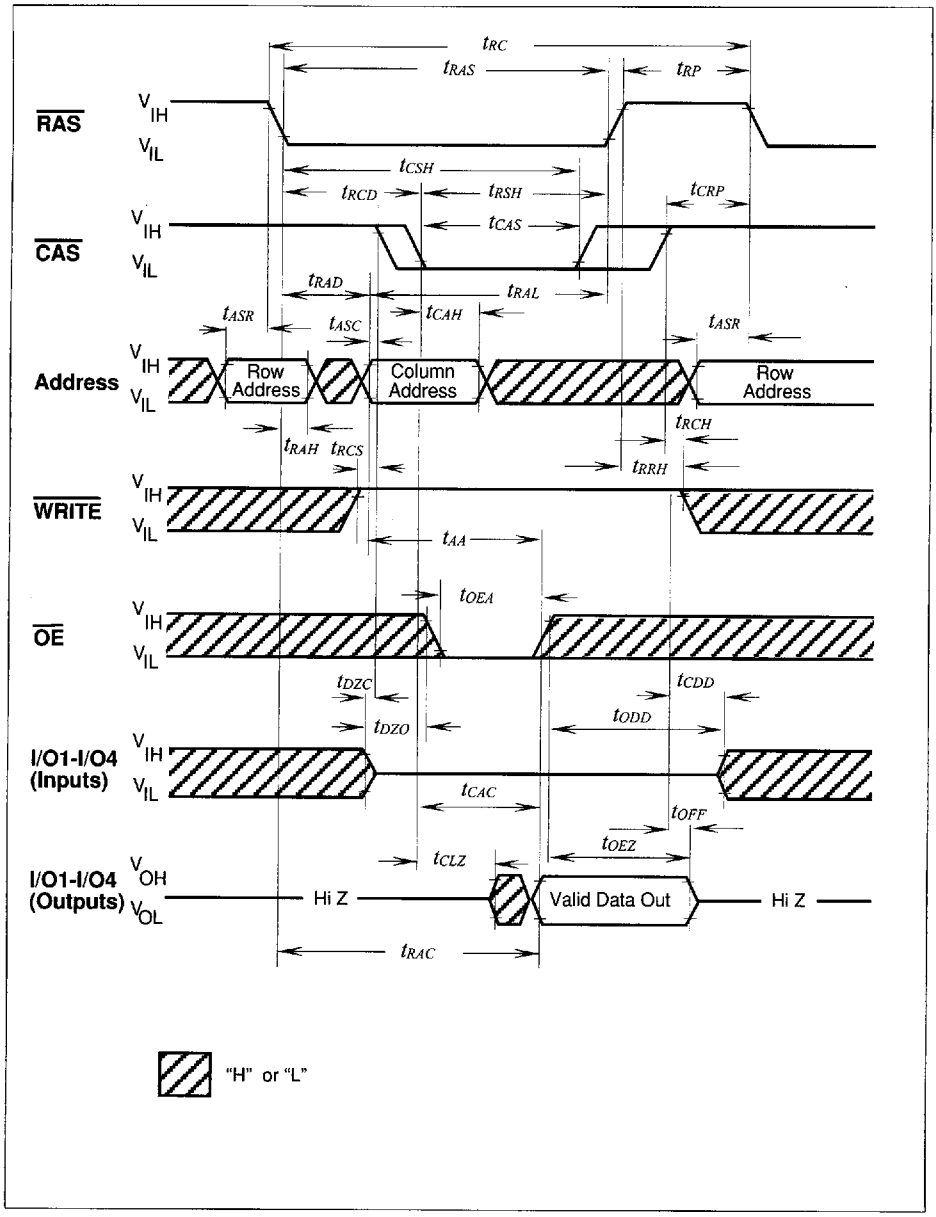
T_A = 0 to 25 °C, V_{CC} = 3.3 V ± 0.3 V, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A11,A12)	C_{I1}	–	5	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	C_{I2}	–	7	pF
I/O capacitance (I/O1-I/O4)	C_{IO}	–	7	pF

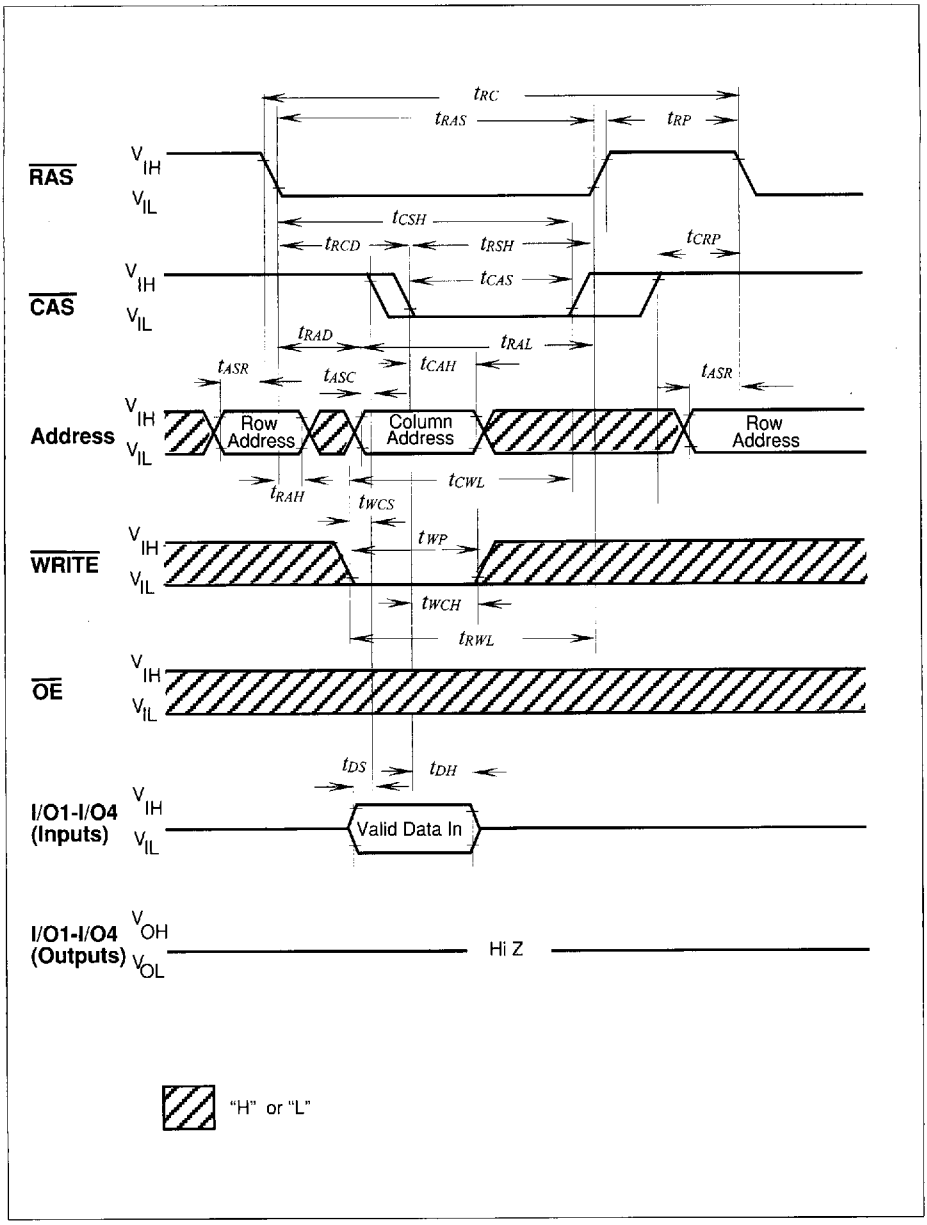
Notes:

1) Stresses greater than listed under „Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ration conditions for extended periods may affect relialibity.
2) All voltages are referenced to V_{SS}.
3) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} and I_{CC7} depend on cycle rate.
4) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.
5) Column address can be changed once or less while RAS = V_{il} and CAS = V_{ih}
6) V_{ol} (LVCMOS) and V_{oh} (LVCMOS) levels are not inteded for use as timing reference levels. LVCMOS levels are the quiescent state of a low impedance output driver, under the specified load conditions.
7) An initial pause of 100 µs is required after power-up followed by 8 $\overline{\text{RAS}}$-only-refresh cycles, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ initialization cycles instead of 8 $\overline{\text{RAS}}$ cycles are required.
8) AC measurements assume tT = 5 ns.
9) $V_{IH\ (min.)}$ and $V_{IL\ (max.)}$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{iH} and V_{iL}.
10) Valid column addresses are only A0 through A10 for HYB 3164400 and A0 through A11 for HYB 316500..
11) In a Test mode Read cylce, the value of t_{RAS}, t_{AA}, t_{CAC} and t_{CPA} are delayed by 5ns, from the specified value. These parameters must be adjusted in Test Mode cycles by adding 5ns to the specified value. Associated timings must also be adjusted by 5ns.
12) Operation within the $t_{RCD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RCD\ (max.)}$ is specified as a reference point only: If t_{RCD} is greater than the specified $t_{RCD\ (max.)}$ limit, then access time is controlled by t_{CAC}.
13) Operation within the $t_{RAD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RAD\ (max.)}$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD\ (max.)}$ limit, then access time is controlled by t_{AA}.
15) Either t_{DZC} or t_{DZO} must be satisfied.
16) Either t_{CDD} or t_{ODD} must be satisfied.
16) t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS\ (min.)}$, the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} > t_{RWD\ (min.)}$, $t_{CWD} > t_{CWD\ (min.)}$, $t_{AWD} > t_{AWD\ (min.)}$ and $t_{CPWD} > t_{CPWD\ (min.)}$, the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.
17) These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{WRITE}}$ leading edge in Read-Modify-Write cycles.
18) Measured with the specified current load and 100 pF.
19) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
20) $t_{OFF\ (max.)}$ and $t_{OEZ\ (max.)}$ define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels.
22) When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:
    If row addresses are being refresh in an evenly distributed manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediatly after exit from Self Refresh.
    If row addresses are being refresh in any other manner (ROR - Distributed/Burst or CBR-Burst) over the refresh interval, then a full set of row refreshed must be performed immediately before entry to and immediatey after exit from Self Refresh.

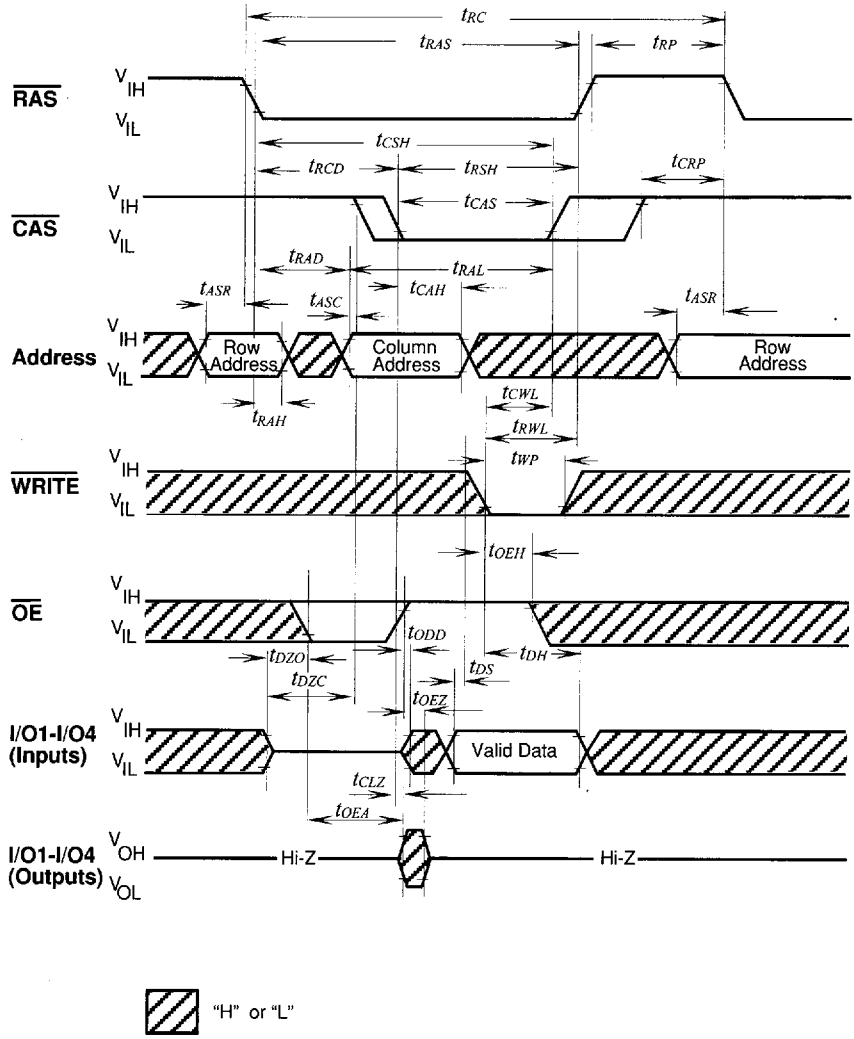
WAVEFORMS



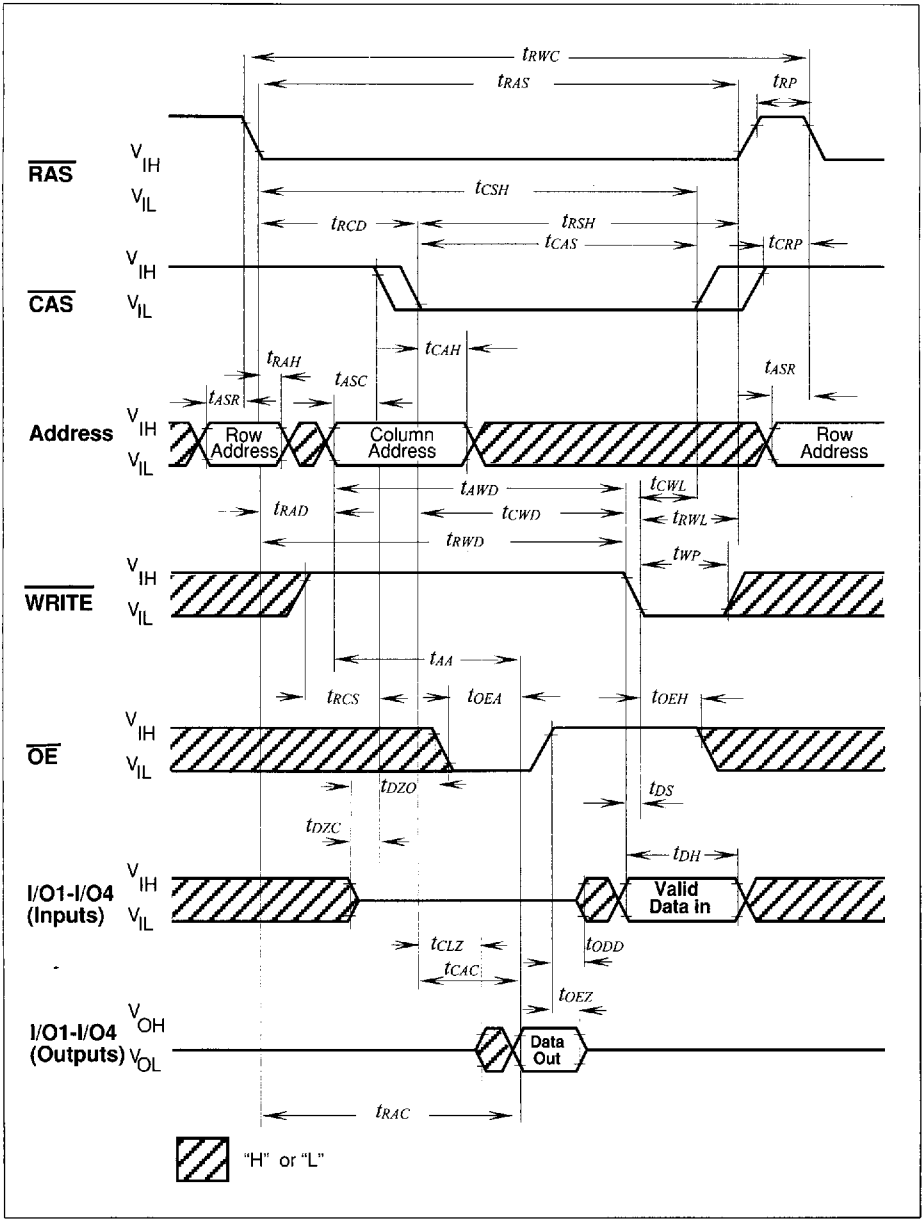
Read Cycle



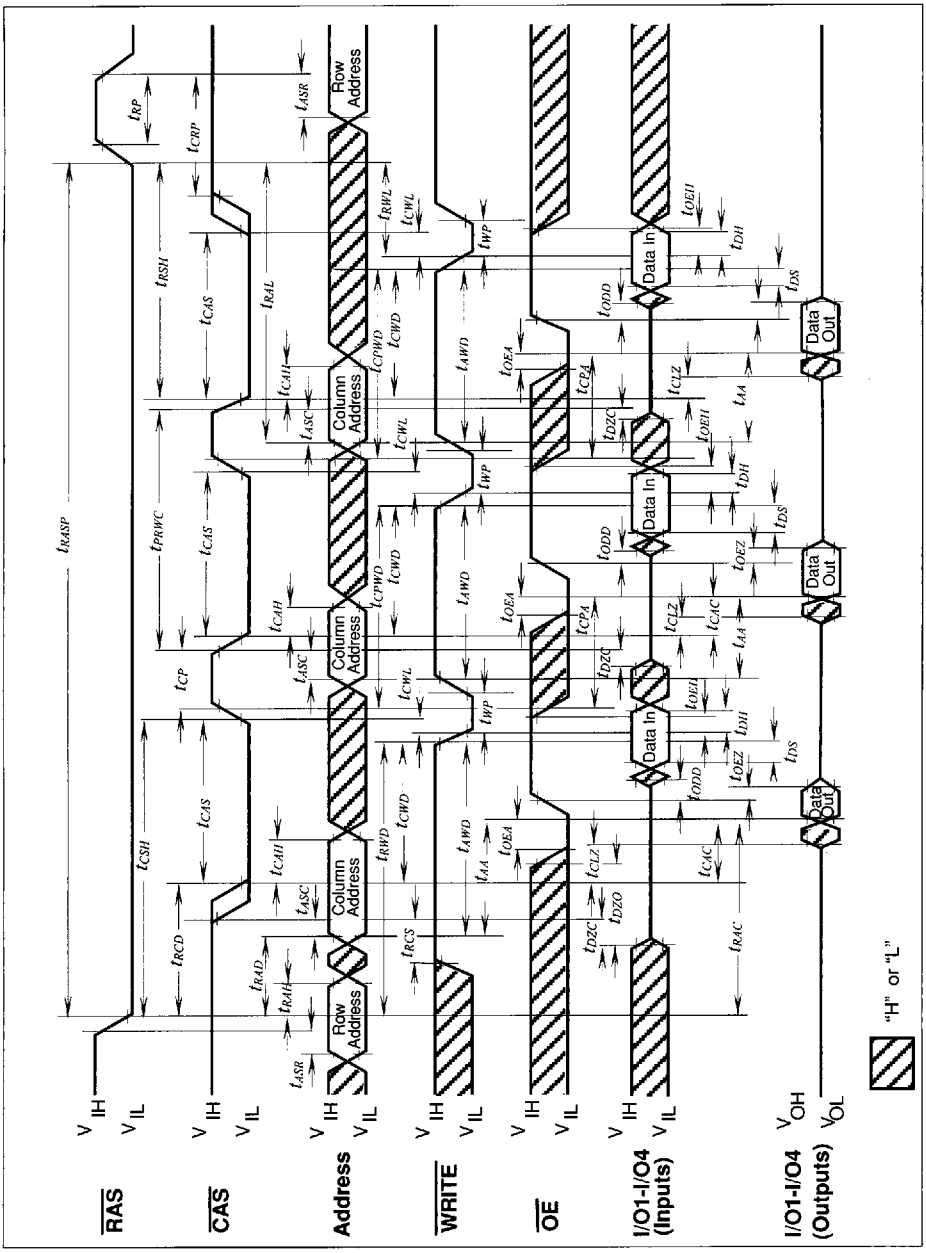
Write Cycle (Early Write)



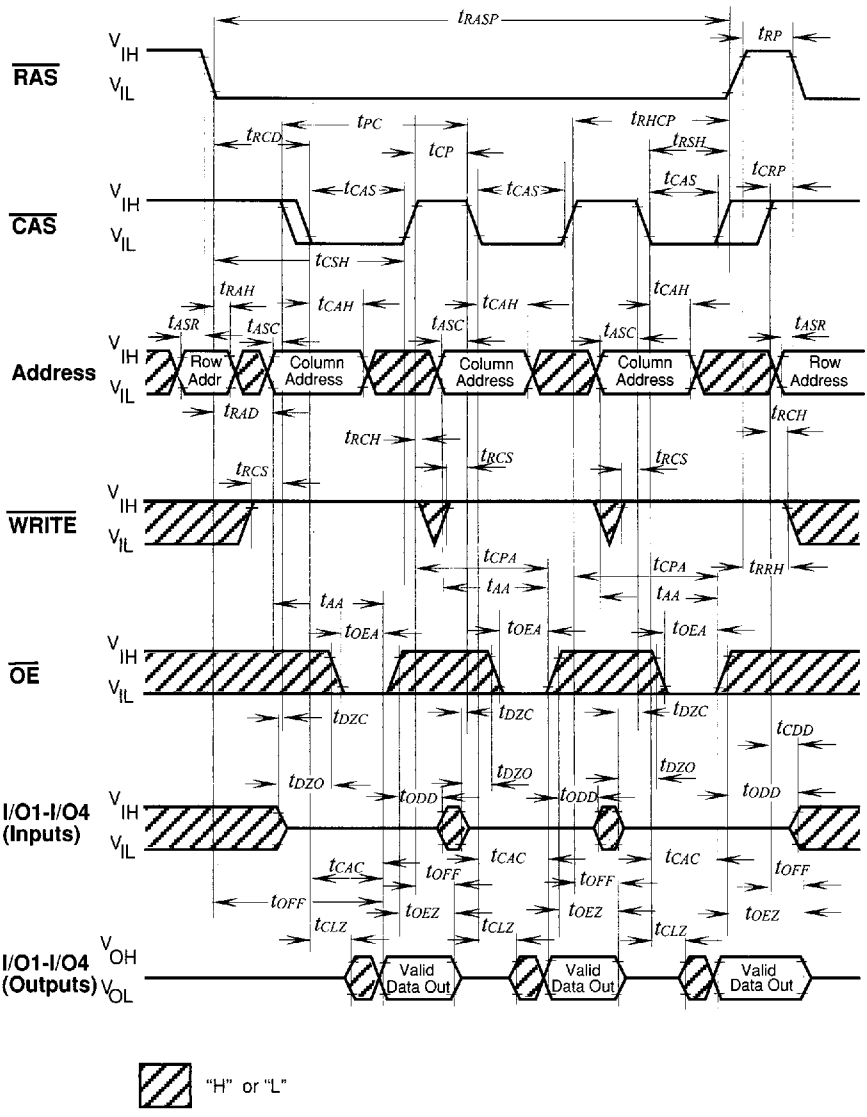
Write Cycle ($\overline{OE}$ Controlled Write)



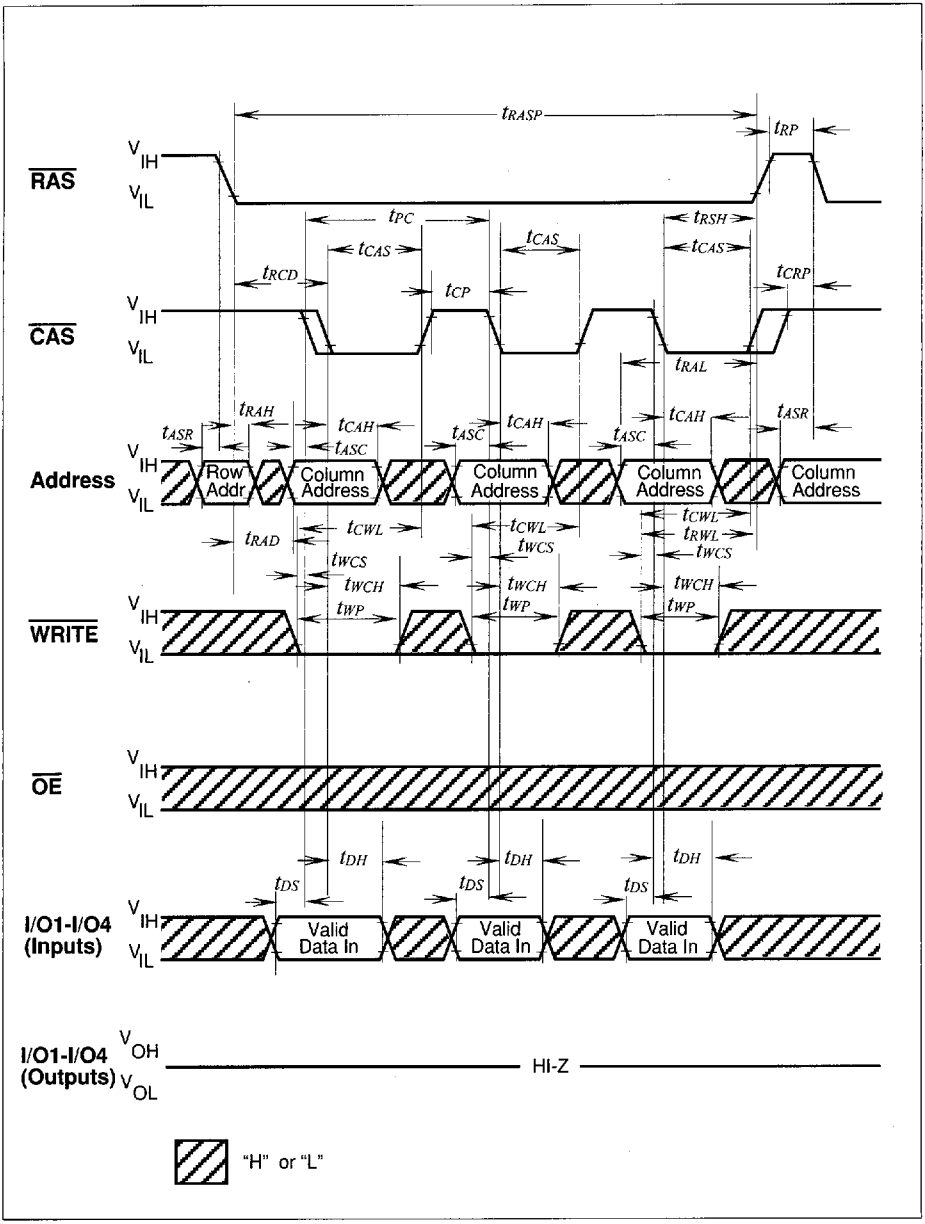
Read-Write (Read-Modify-Write) Cycle



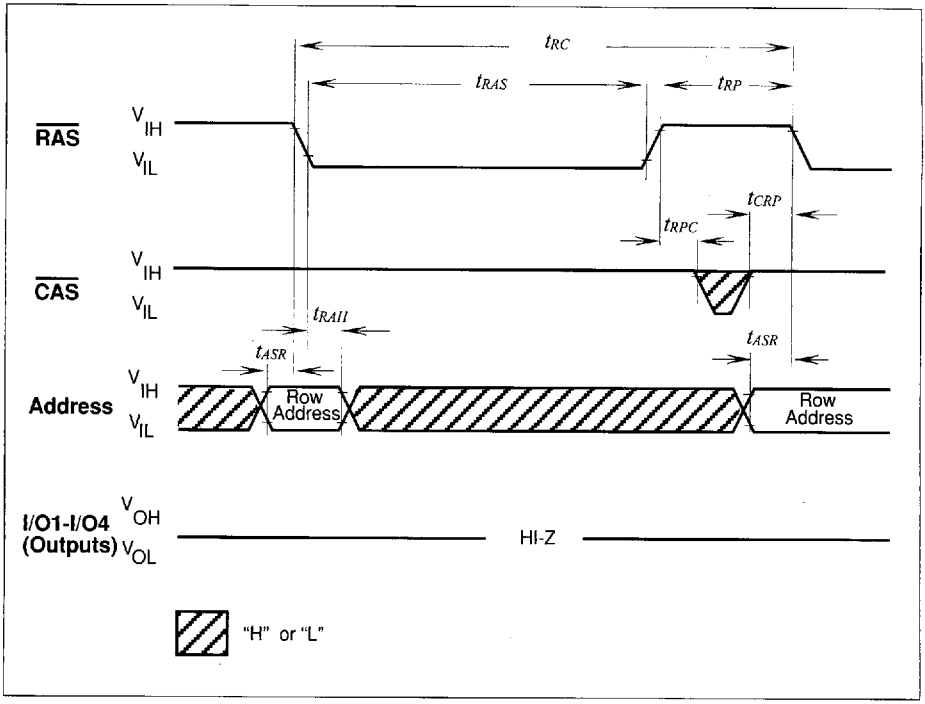
Fast Page Mode Read-Modify-Write Cycle



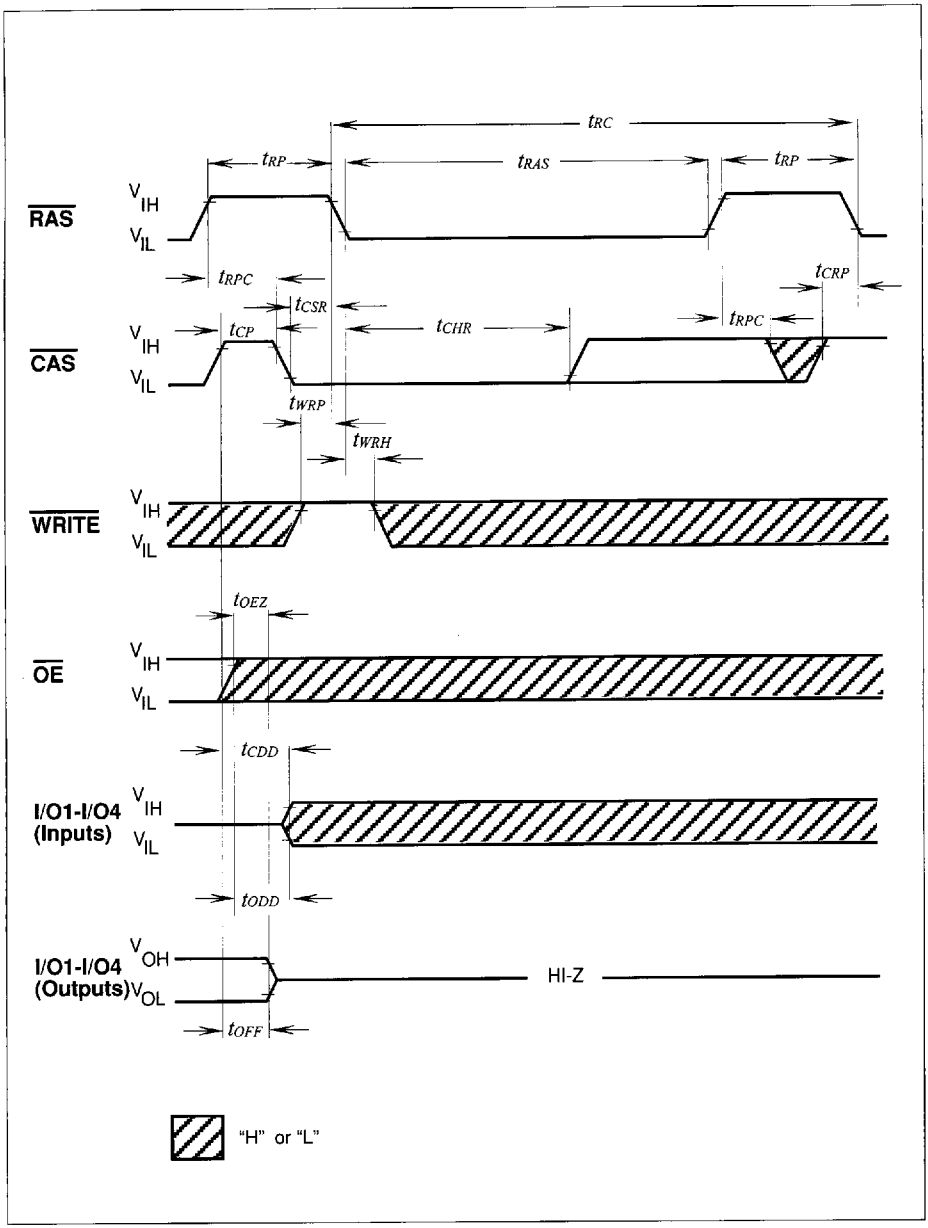
Fast Page Mode Read Cycle



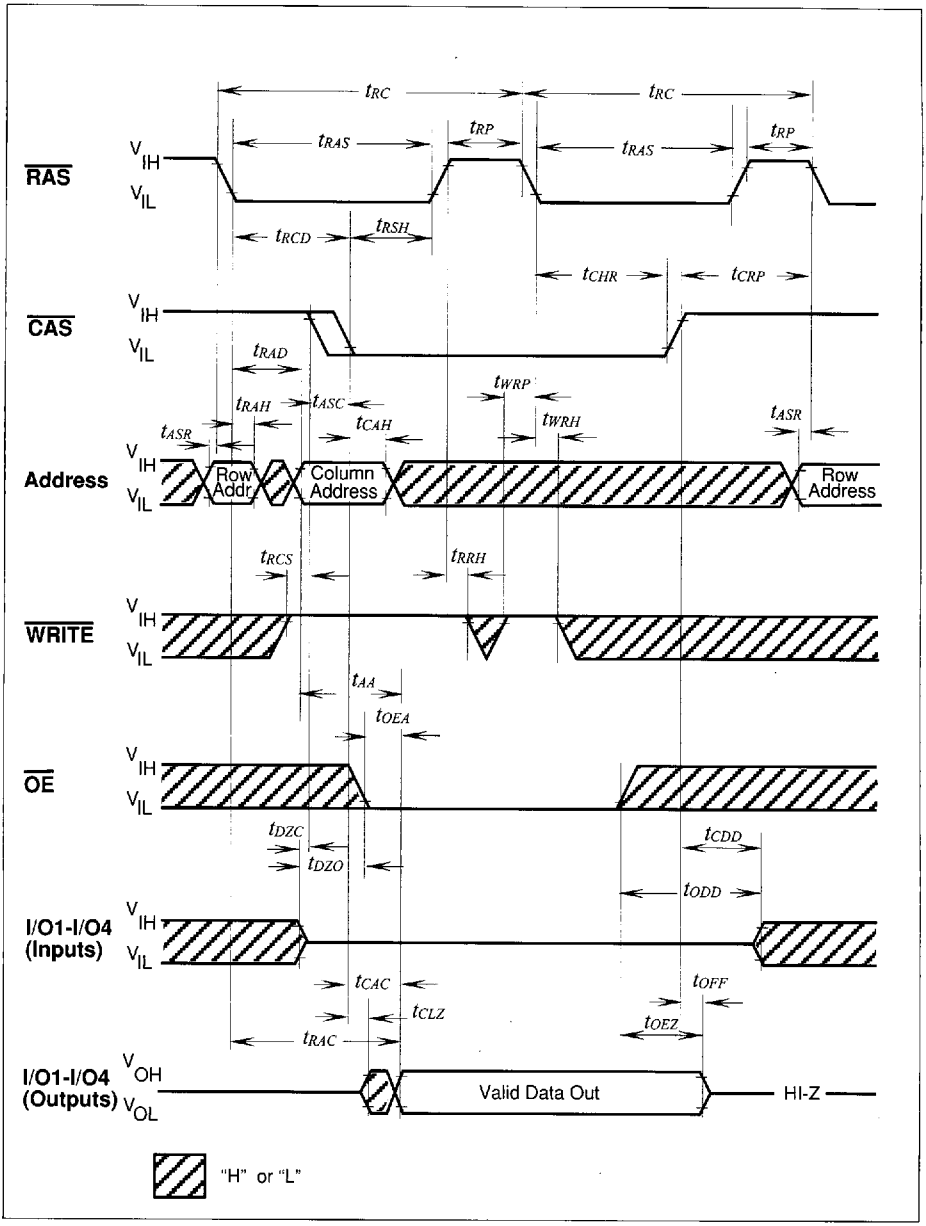
Fast Page Mode Early Write Cycle



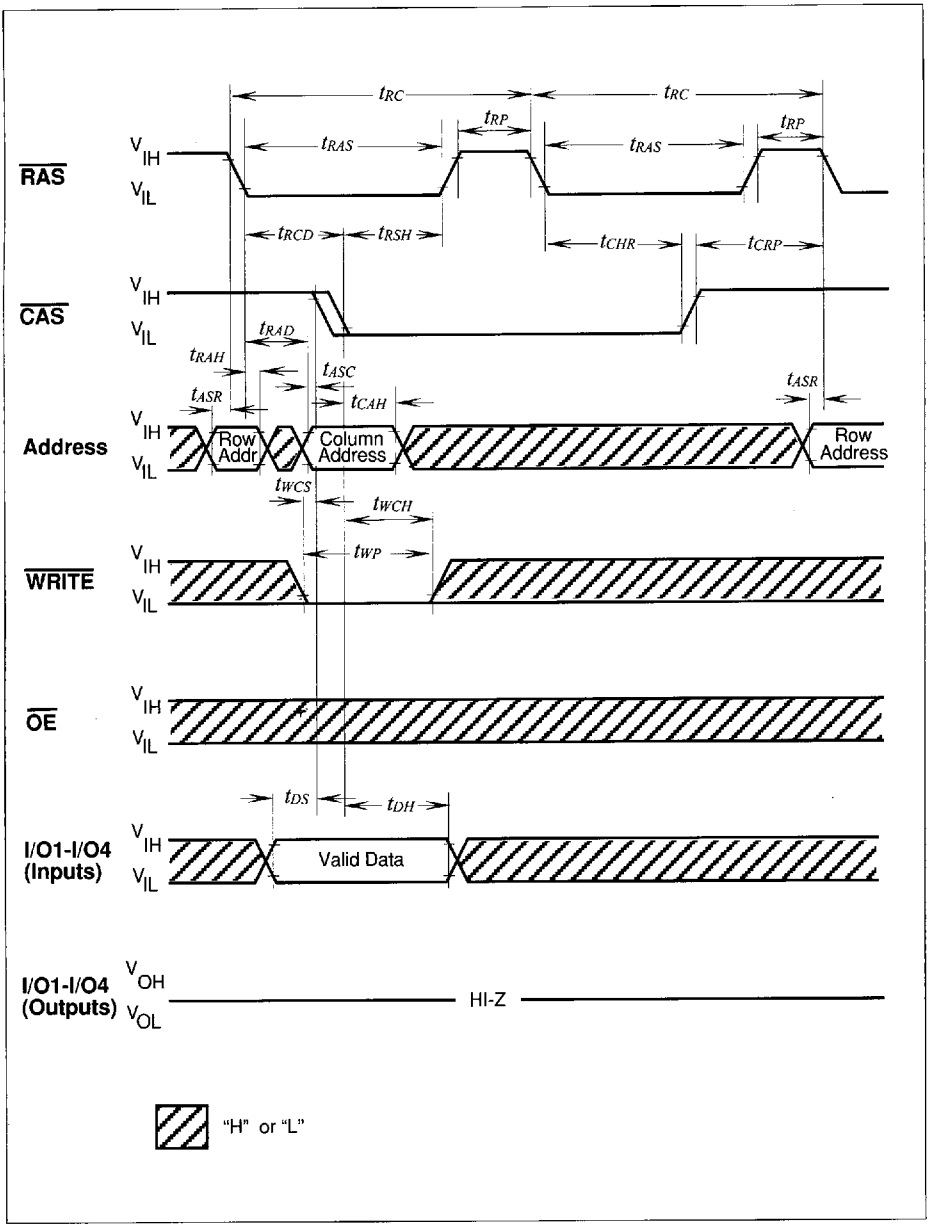
RAS-Only Refresh Cycle



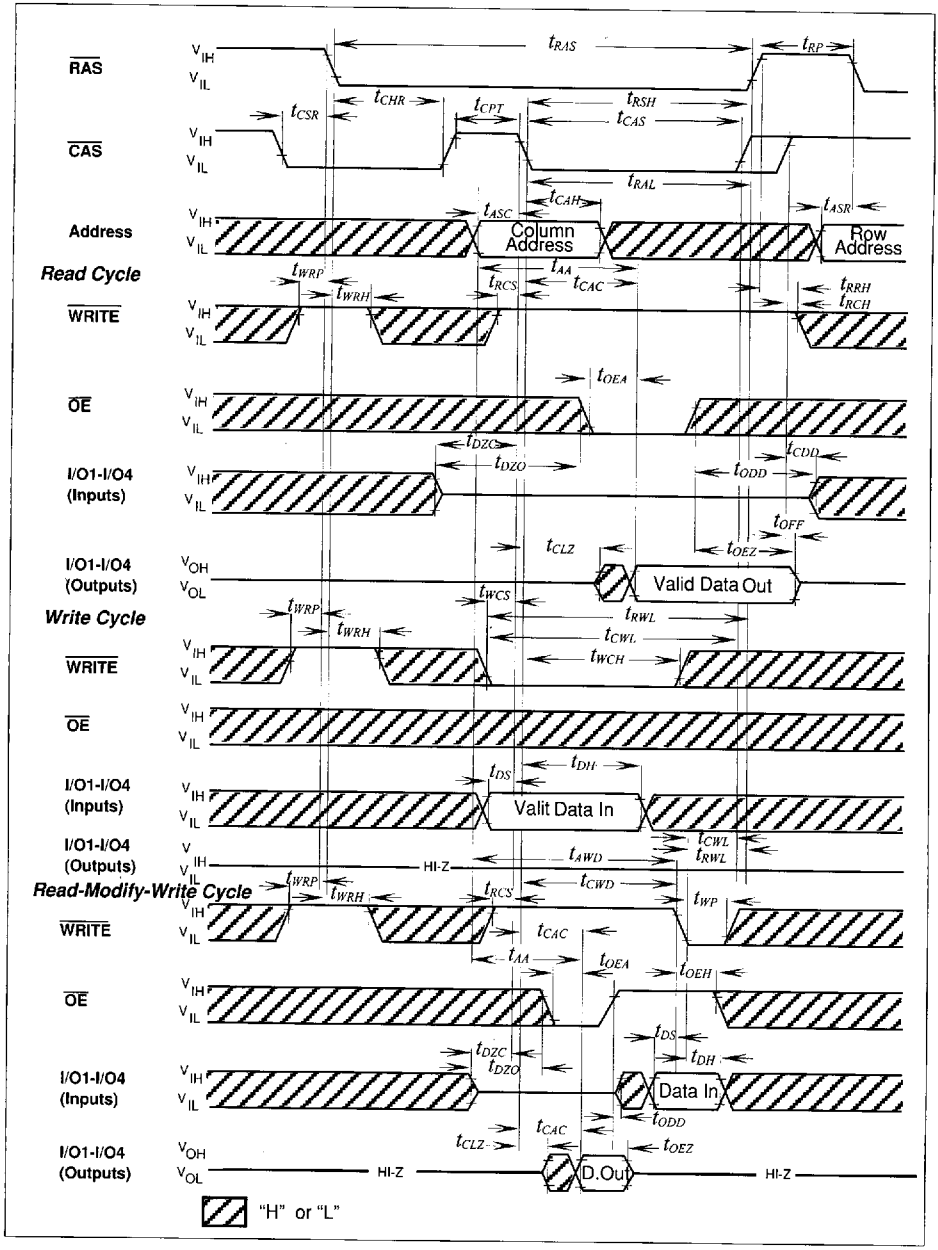
CAS-Before-RAS Refresh Cycle



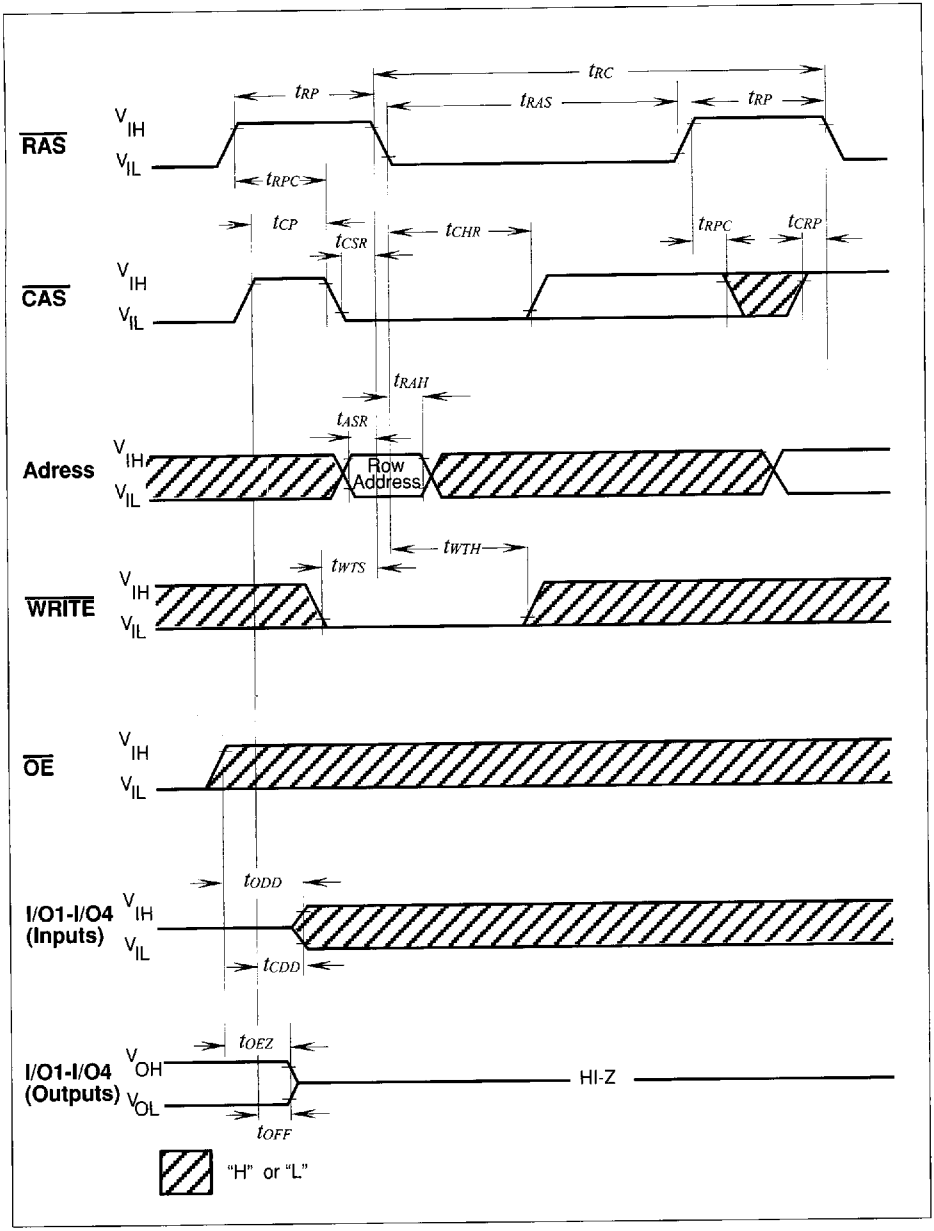
Hidden Refresh Cycle (Read)



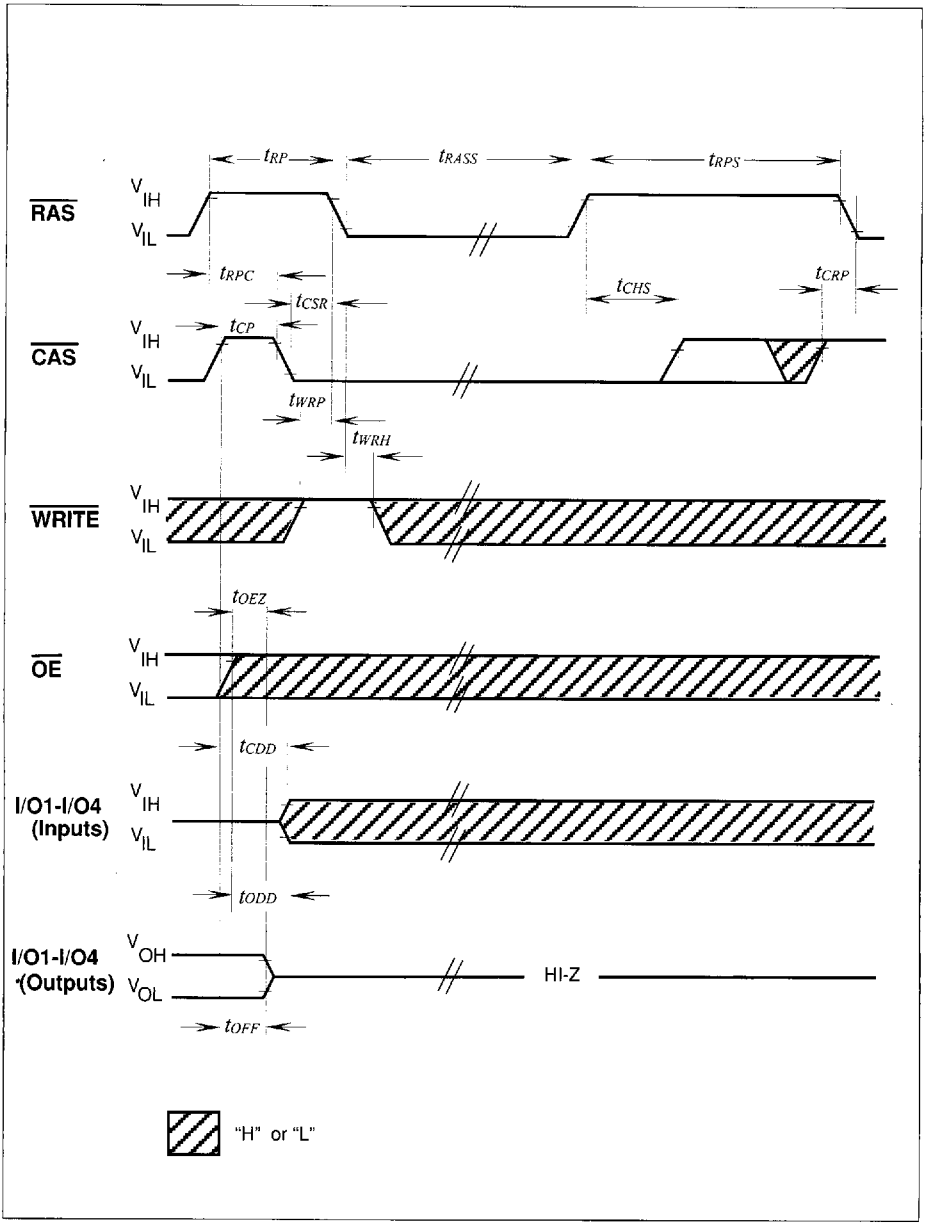
Hidden Refresh Cycle (Early Write)



CAS-Before-RAS Refresh Counter Test Cycle



Test Mode Entry



CAS-before-RAS Self Refresh