To our customers,

## Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

MOS INTEGRATED CIRCUIT

# μPD16310

## HIGH VOLTAGE CMOS DRIVER FOR PDP, EL, VFD

### DESCRIPTION

μPD16310 is high voltage driver for PDP, EL or VFD graphic panel structured by CMOS process. Logic power supply is 5.0 V connecting direct to control logic. Maximum output voltage is 80 V and maximum current is 50 mA.

### FEATURES

- 80 V Output Voltage Swing Capability
- 50 mA Output Sink and Source Current Capability
- 40 bit Shift-register and Latch
- High Speed Serial DATA Transferring ($f_{max.}$ = 20 MHz MIN.)
- Low Standby Current 100 μA

### ORDERING INFORMATION

| Part Number | Package |
|---|---|
| μPD16310GF-3L9 | 80-pin plastic QFP (3 direction lead) |

Document No. IC-2859 (1st edition)
Date Published March 1997 P
Printed in Japan

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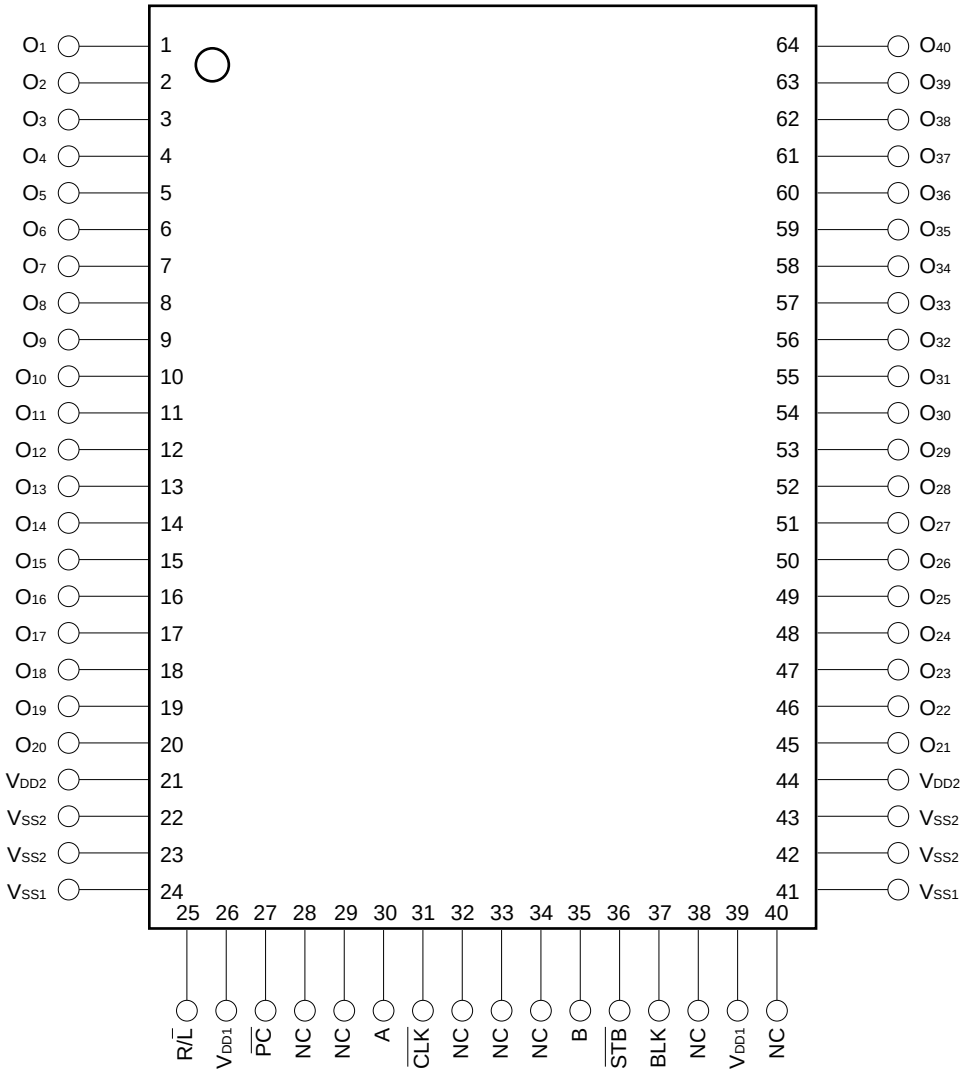
**PIN CONNECTION DIAGRAM (Top View)**




**Note** The 33 pin (NC) should be open.

All the power supply terminals should be used.

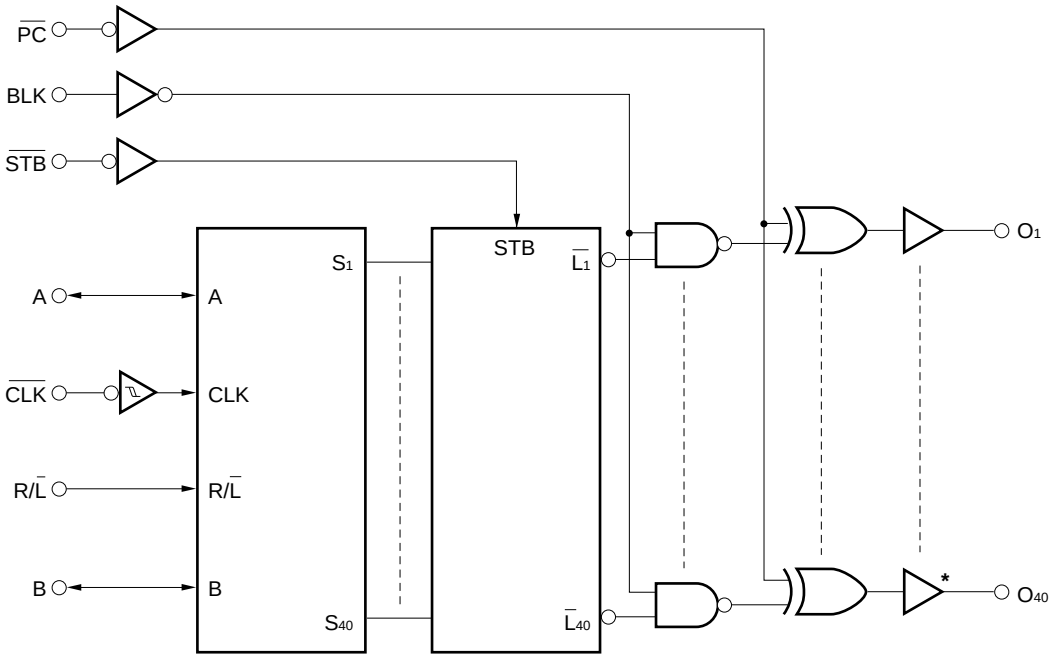
$V_{SS1}$ and $V_{SS2}$ should be respectively connected with themselves outside.

To prevent latch up breakdown, the power should be turned ON in order $V_{DD1}$, logic input, $V_{DD2}$.

It should be turned OFF in the opposite order.

This relationship should be followed during transition period as well.

## BLOCK DIAGRAM




40 bit Shift Register

40 bit Latch

* High Voltage CMOS Driver 80 V ± 50 $mA_{MAX}$.

## PN CONFIGURATION

| PIN No. | SYMBOL | PIN NAME | FUNCTION |
|---|---|---|---|
| 27 | $\overline{PC}$ | Polarity Change Input | All driver outputs' level are inverted while $\overline{PC}$ is L. |
| 37 | BLK | Blank Input | All driver outputs are H or L while BLK is H. |
| 36 | $\overline{STB}$ | Latch Strobe Input | Latch's status is data through while $\overline{STB}$ is L. |
| 30 | A | Right Data Input/Output | R/$\overline{L}$ = H : A = IN, B = OUT<br>R/$\overline{L}$ = L : A = OUT, B = IN |
| 35 | B | Left Data Input/Output | |
| 31 | $\overline{CLK}$ | Clock Input | Data of shift-register is shifted while $\overline{CLK}$ is going H to L. (Negative edge is active.) |
| 25 | R/$\overline{L}$ | Shift Direction Control Input | H: Right Shift Mode<br>A → $O_1$ ⋯ $O_{40}$ → B<br>L: left Shift Mode<br>B → $O_{40}$ ⋯ $O_1$ → A |
| 1 - 20<br>45 - 64 | $O_1$ - $O_{40}$ | Driver Outputs | High voltage output 80 V, 50 mA |
| 26, 39 | $V_{DD1}$ | Logic Power Supply | 5.0 V ± 10 % |
| 21, 44 | $V_{DD2}$ | Driver Power Supply | 10 to 70 V |
| 24, 41 | $V_{SS1}$ | Ground (for Logic) | Connect to the system ground. |
| 22, 23, 42, 43 | $V_{SS2}$ | Ground (for Driver) | Connect to the system ground. |
| 28, 29, 32 - 34<br>38, 40 | NC | No Connect | No. 33 pin should be open. |

## TRUTH TABLE 1 (Shift-Register part)

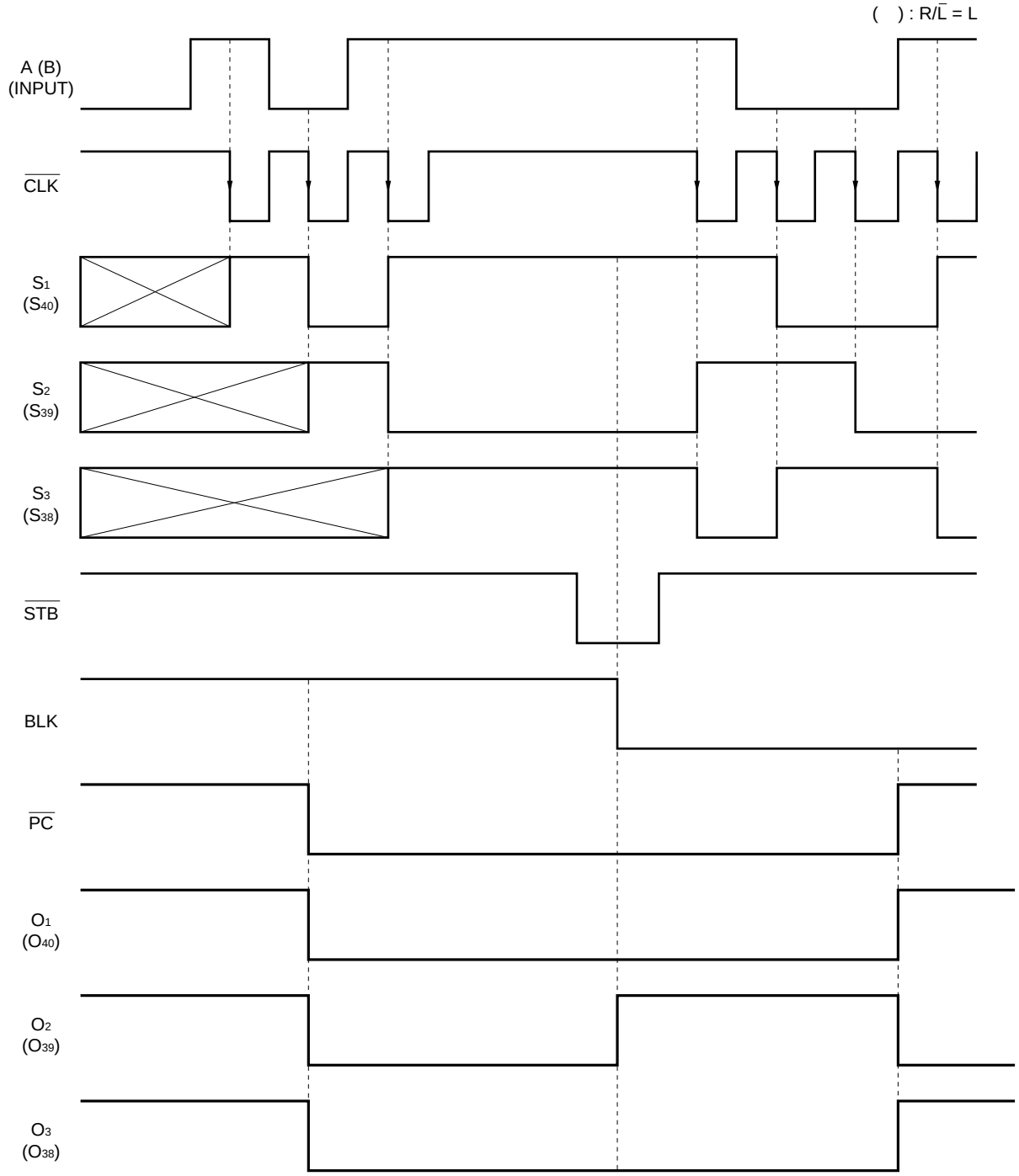
| INPUT | | IN/OUT | | SHIFT-REGISTER |
|---|---|---|---|---|
| R/$\overline{L}$ | CLK | A | B | |
| H | ↓ | IN | OUT | DATA is shifted. |
| H | H or L | IN | OUT | No Change. |
| L | ↓ | OUT | IN | DATA is shifted. |
| L | H or L | OUT | IN | No Change. |

## TRUTH TABLE 2 (Latch, Driver part)

| INPUT | | | | DRIVER OUTPUT |
|---|---|---|---|---|
| A (B) | $\overline{STB}$ | BLK | $\overline{PC}$ | |
| X | X | H | H | ALL H |
| X | X | H | L | ALL L |
| H | L | L | H | H |
| H | L | L | L | L |
| L | L | L | H | L |
| L | L | L | L | H |
| X | H | L | H | Latch's data output |
| X | H | L | L | Latch's data output (inverting) |

X = H or L, H = High Level, L = Low Level

## TIMING CHART



## ABSOLUTE MAXIMUM RATINGS ($T_a$ = 25 °C, $V_{SS1}$ = $V_{SS2}$ = 0 V)

| PARAMETER | SYMBOL | RATINGS | UNIT |
|---|---|---|---|
| Logic Power Supply | $V_{DD1}$ | –0.5 to +7.0 | V |
| Input Voltage | $V_I$ | –0.5 to $V_{DD1}$ + 0.5 | V |
| Logic Output Voltage | $V_{O1}$ | –0.5 to $V_{DD1}$ + 0.5 | V |
| Driver Power Supply | $V_{DD2}$ | –0.5 to 80 | V |
| Driver Output Voltage | $V_{O2}$ | –0.5 to $V_{DD2}$ + 0.5 | V |
| Drive Maximum Current | $I_{O2}$ | ±50 | mA |
| Power Dissipation | $P_D$ | 1 000 | mW |
| Operating Temperature | $T_{opt}$ | –40 to +85 | °C |
| Storage Temperature | $T_{stg}$ | –65 to +150 | °C |

## RECOMMENDED OPERATING CONDITIONS ($T_a$ = 25 °C, $V_{SS1}$ = $V_{SS2}$ = 0 V)

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| Logic Power Supply | $V_{DD1}$ | 4.5 | 5.0 | 5.5 | V |
| High Level Input Voltage | $V_{IH}$ | 0.7 · $V_{DD1}$ | | $V_{DD1}$ | V |
| Low Level Input Voltage | $V_{IL}$ | 0 | | 0.2 · $V_{DD1}$ | V |
| Driver Power Supply | $V_{DD2}$ | 10 | | 70 | V |
| Driver Output Current | $I_{OL2}$ | | | +40 | mA |
| | $I_{OH2}$ | | | –40 | mA |

## DC CHARACTERISTICS ($T_a$ = 25 °C, $V_{DD1}$ = 5.0 V, $V_{DD2}$ = 70 V, $V_{SS1}$ = $V_{SS2}$ = 0 V)

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| Hight Level Output Voltage | $V_{OH1}$ | 0.9 · $V_{DD1}$ | | | V | Logic, $I_{OH1}$ = –1.0 mA |
| Low Level Output Voltage | $V_{OL1}$ | | | 0.1 · $V_{DD1}$ | V | Logic, $I_{OL1}$ = 1.0 mA |
| High Level Output Voltage | $V_{OH21}$ | 69 | | | V | $O_1$ - $O_{40}$, $I_{OH2}$ = –1.0 mA |
| | $V_{OH22}$ | 65 | | | V | $O_1$ - $O_{40}$, $I_{OH2}$ = –10 mA |
| Low Level Output Voltage | $V_{OL21}$ | | | 1.0 | V | $O_1$ - $O_{40}$, $I_{OL2}$ = 5.0 mA |
| | $V_{OL22}$ | | | 10 | V | $O_1$ - $O_{40}$, $I_{OL2}$ = 40 mA |
| High Level Input Current | $I_{IH}$ | | | 1.0 | μA | $V_I$ = $V_{DD1}$ |
| Low Level Input Current | $I_{IL}$ | | | –1.0 | μA | $V_I$ = 0 V |
| High Level Input Voltage | $V_{IH}$ | 0.7 · $V_{DD1}$ | | | V | |
| Low Level Input Voltage | $V_{IL}$ | | | 0.2 · $V_{DD1}$ | V | |
| Standby Current | $I_{DD1}$ | | | 10 | μA | for $V_{DD1}$, $T_a$ = 25 °C |
| | $I_{DD1}$ | | | 100 | μA | for $V_{DD1}$, $T_a$ = –40 to +85 °C |
| | $I_{DD2}$ | | | 100 | μA | for $V_{DD2}$, $T_a$ = 25 °C |
| | $I_{DD2}$ | | | 1 000 | μA | for $V_{DD2}$, $T_a$ = –40 to +85 °C |

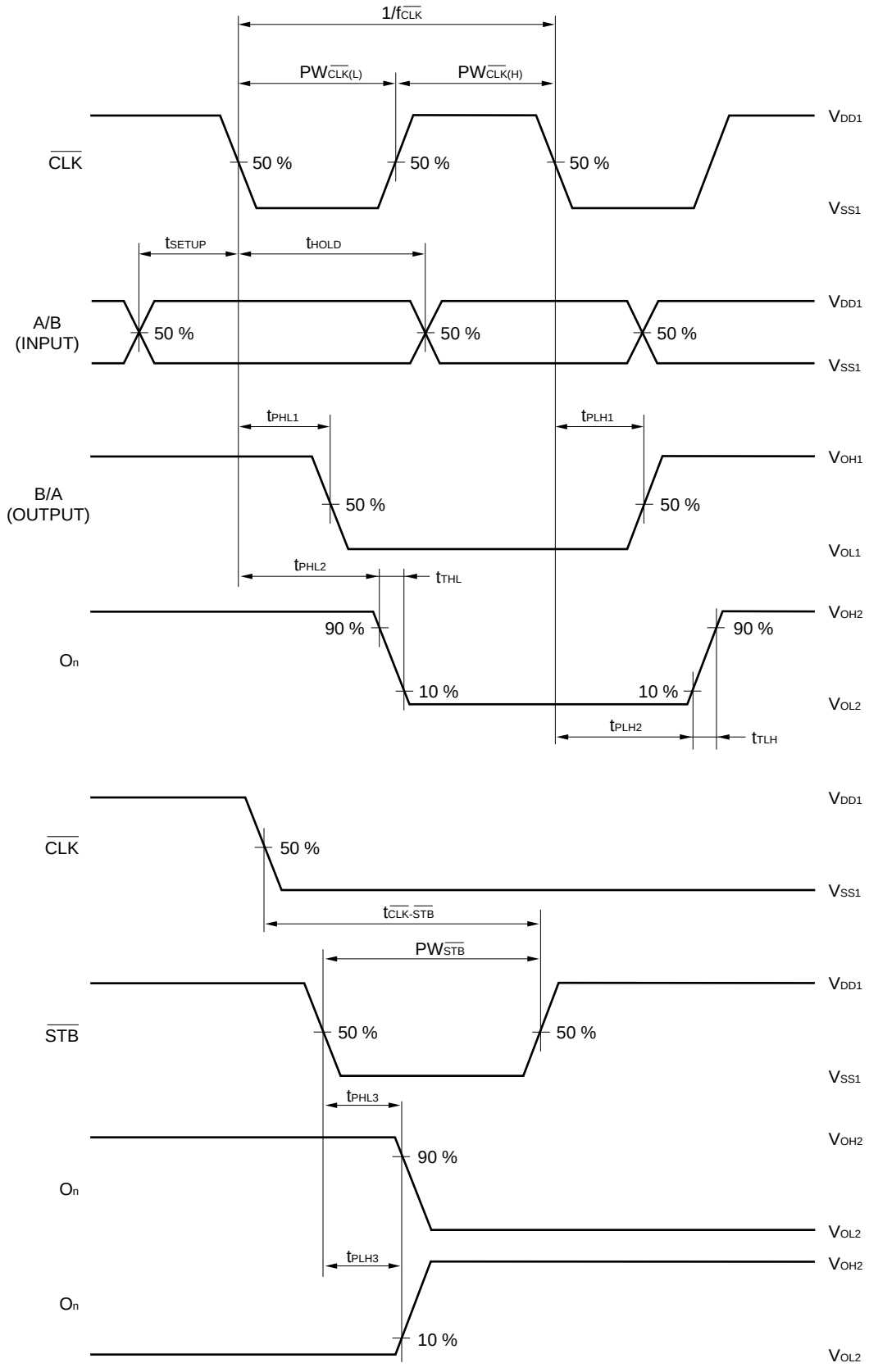
**AC CHARACTERISTICS ($T_a$ = 25 °C, $V_{DD1}$ = 5.0 V, $V_{DD2}$ = 70 V, $V_{SS1}$ = $V_{SS2}$ = 0 V, Logic $C_L$ = 15 pF, Driver $C_L$ = 50 pF)**

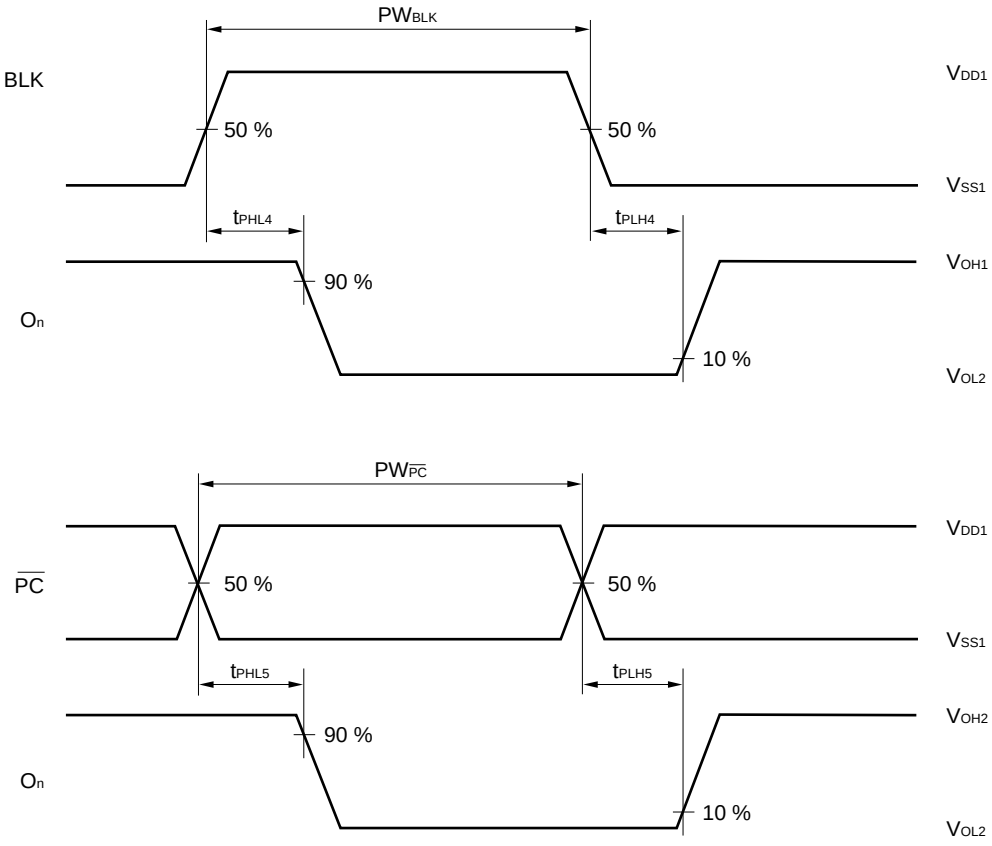
| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| Delay Time | $t_{PHL1}$ | | | 50 | ns | $\overline{CLK} \rightarrow$ A/B |
| | $t_{PLH1}$ | | | 50 | ns | |
| | $t_{PHL2}$ | | | 160 | ns | $\overline{CLK} \rightarrow O_1$ - $O_{40}$ |
| | $t_{PLH2}$ | | | 160 | ns | |
| | $t_{PHL3}$ | | | 150 | ns | $\overline{STB} \rightarrow O_1$ - $O_{40}$ |
| | $t_{PLH3}$ | | | 150 | ns | |
| | $t_{PHL4}$ | | | 145 | ns | BLK $\rightarrow O_1$ - $O_{40}$ |
| | $t_{PLH4}$ | | | 145 | ns | |
| | $t_{PHL5}$ | | | 140 | ns | $\overline{PC} \rightarrow O_1$ - $O_{40}$ |
| | $t_{PLH5}$ | | | 140 | ns | |
| Rise Time | $t_{TLH}$ | | | 70 | ns | $O_1$ - $O_{40}$ |
| Fall Time | $t_{THL}$ | | | 70 | ns | $O_1$ - $O_{40}$ |
| Maximum Frequency | $f_{max.}$ | 20 | 30 | | MHz | Duty = 50 %, for CLK |
| Input Capacitance | $C_I$ | | 10 | 20 | pF | |

**AC TIMING REQUIREMENT ($T_a$ = –40 to +85 °C, $V_{DD1}$ = 4.5 to 5.5 V, $V_{DD2}$ = 10 to 70 V $V_{SS1}$ = $V_{SS2}$ = 0 V)**

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| Clock Pulse Width | $PW_{\overline{CLK}}$ | 20 | | | ns | |
| Strobe Pulse Width | $PW_{\overline{STB}}$ | 20 | | | ns | |
| Blank Pulse Width | $PW_{BLK}$ | 200 | | | ns | |
| Polarity Change Pulse Width | $PW_{\overline{PC}}$ | 200 | | | ns | |
| Data Setup Time | $t_{SETUP}$ | 10 | | | ns | |
| Data Hold Time | $t_{HOLD}$ | 10 | | | ns | |
| Setup Time | $t_{\overline{CLK}\text{-}\overline{STB}}$ | 50 | | | ns | for $\overline{CLK}$ ↓ to $\overline{STB}$ ↑ |

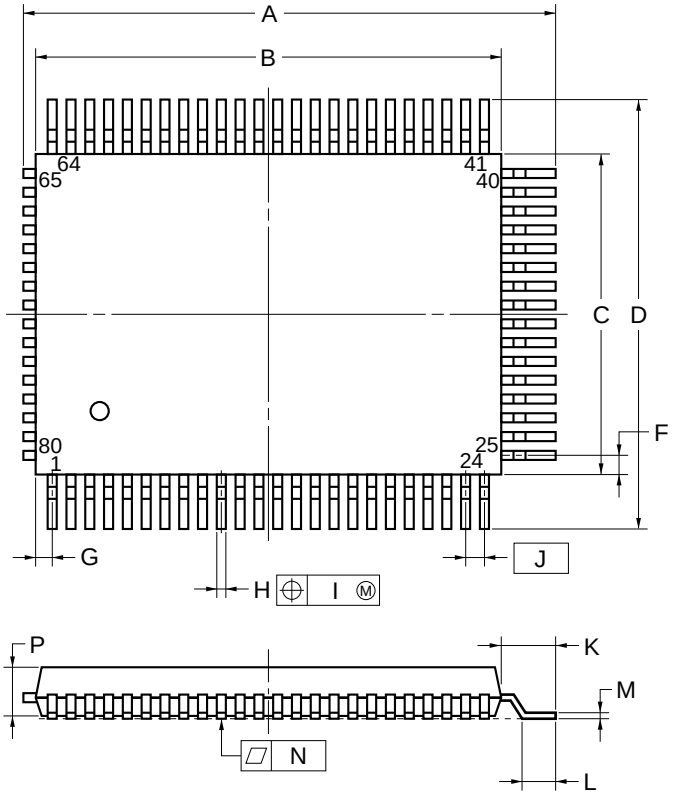
## AC CHARACTERISTICS WAVEFORM



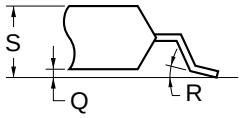

PWBLK
BLK
VDD1
50 %
50 %
VSS1
tPHL4
tPLH4
VOH1
90 %
On
10 %
VOL2
PWPC
VDD1
PC
50 %
50 %
VSS1
tPHL5
tPLH5
VOH2
90 %
On
10 %
VOL2

**PACKAGE DIMENSIONS**

## 80 PIN PLASTIC QFP (THREE DIRECTIONS) (14×20)




detail of lead end




**NOTE**

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 22.3±0.4 | 0.878±0.016 |
| B | 20.0±0.2 | $0.795^{+0.009}_{-0.008}$ |
| C | 14.0±0.2 | $0.551^{+0.009}_{-0.008}$ |
| D | 17.6±0.4 | 0.693±0.016 |
| F | 1.0 | 0.039 |
| G | 0.8 | 0.031 |
| H | 0.35±0.10 | $0.014^{+0.004}_{-0.005}$ |
| I | 0.15 | 0.006 |
| J | 0.8 (T.P.) | 0.031 (T.P.) |
| K | 1.8±0.2 | $0.071^{+0.008}_{-0.009}$ |
| L | 0.8±0.2 | $0.031^{+0.009}_{-0.008}$ |
| M | $0.15^{+0.10}_{-0.05}$ | $0.006^{+0.004}_{-0.003}$ |
| N | 0.10 | 0.004 |
| P | 2.7 | 0.106 |
| Q | 0.1±0.1 | 0.004±0.004 |
| R | 5°±5° | 5°±5° |
| S | 3.0 MAX. | 0.119 MAX. |

**P80GF-80-3L9-2**

## RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) must be met when soldering this product. Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

μPD16310GF-3L9

| Soldering process | Soldering conditions | Symbol |
|---|---|---|
| Infrared ray reflow | Peak package's surface temperature: 230 °C or below,<br>Reflow time: 30 seconds or below (210 °C or higher),<br>Number of reflow process: 1, Exposure limit*: None | IR30-00-1 |
| VPS | Peak package's surface temperature: 215 °C or below,<br>Reflow time: 40 seconds or below (200 °C or higher),<br>Number of reflow process: 1, Exposure limit*: None | VP15-00-1 |
| Partial heating method | Terminal temperature: 300 °C or below,<br>Flow time: 10 seconds or below,<br>Exposure limit*: None | |

***** Exposure limit before soldering after dry-pack package is opened.
Storage coditions: 25 °C and relative humidity at 65 % or less.

**Note** Do not apply more than a single process at once, except for "Partial heating method."

**[MEMO]**

**[MEMO]**

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M4 96.5