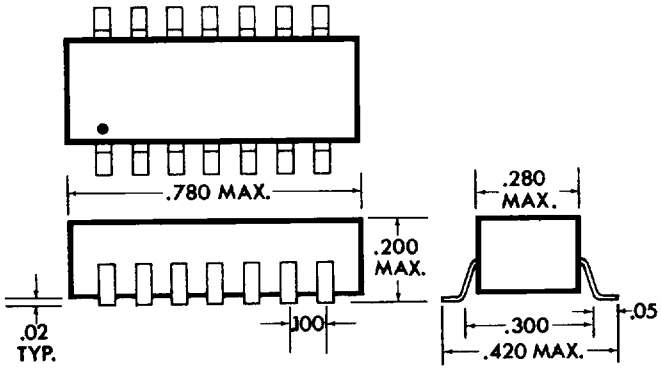
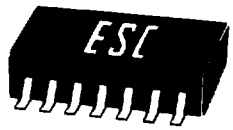
SURFACE MOUNTING
DIGITAL DELAY LINES
TTL COMPATIBLE • 14 PIN PACKAGE
5 TAPS • SINGLE • DUAL • TRIPLE
G LEADS

SERIES 14SGT, 14SGG, 14SGD AND 14SGP
*SERIES 14LSGT, 14LSGG, 14LSGD AND 14LSGP



White Dot locates Pin 1



ONLY ACTIVE PINS ARE SUPPLIED

SERIES 14SGT (5 TAP)		
MODEL NO. (Fig. 1)	Delay ns	Delay/Tap ns
14SGT25	25	5
14SGT30	30	6
14SGT35	35	7
14SGT40	40	8
14SGT45	45	9
14SGT50	50	10
14SGT60	60	12
14SGT75	75	15
14SGT100	100	20
14SGT125	125	25
14SGT200	200	40
14SGT250	250	50
14SGT300	300	60
14SGT400	400	80
14SGT500	500	100
14SGT750	750	150
14SGT1000	1000	250

Delay/ line (ns)	MODEL NUMBERS		
	Series 14SGG	Series 14SGD	Series 14SGP
	One output (Fig. 2)	Dual output (Fig. 3)	Triple output (Fig. 4)
5	14SGG5	14SGD5	14SGP5
10	14SGG10	14SGD10	14SGP10
15	14SGG15	14SGD15	14SGP15
20	14SGG20	14SGD20	14SGP20
25	14SGG25	14SGD25	14SGP25
50	14SGG50	14SGD50	14SGP50
75	14SGG75	14SGD75	14SGP75
100	14SGG100	14SGD100	14SGP100
150	14SGG150	14SGD150	14SGP150
200	14SGG200	14SGD200	14SGP200
250	14SGG250	—	
300	14SGG300	—	—
400	14SGG400	—	—
500	14SGG500	—	—
750	14SGG750	—	—
1000	14SGG1000	—	—

DC PARAMETERS		LIMITS	
		Min.	Max.
V_{oh}	Vcc = min I_{oh} = 1.0 mA	2.5V	-
V_{ol}	Vcc = min I_{ol} = 20 mA	-	0.5V
I_{ih}	Vcc = max V_{ih} = 2.7V	-	50 µA
I_{il}	Vcc = max V_{il} = 0.5V	-2.0 mA	-
I_i	Vcc = max V_i = 5.5V	-	1.0 mA
V_i	Vcc = min I_{in} = -18 madc	-1.2vdc	-
I_{cc}	Vcc = max outputs low	Series 14SGT 70mA Series 14SGG 55mA Series 14SGD 100mA Series 14SGP 120mA	

Intermediate delay values available upon request.

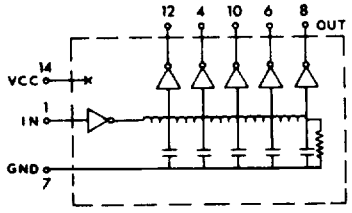


FIG. 1

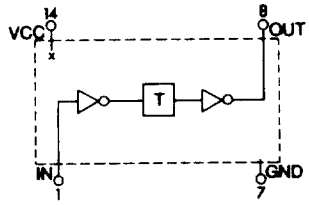


FIG. 2

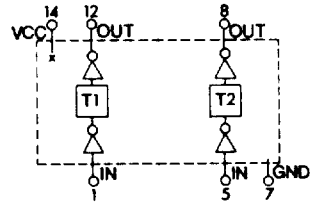


FIG. 3

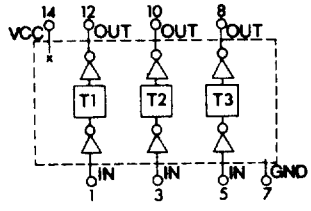


FIG. 4

*Also available as Low Power Schottky type. Specify Series 14LSGG (Single), 14LSGD (dual), 14LSGP (triple) and 14LSGT (5 Tap) when ordering.

SPECIFICATIONS:

- Supply voltage: 5.0VDC ± 10%
- Delay tolerances: ± 2ns or ± 5% wig
- Rise Time: 4ns max
- Minimum Pulse Width: 40% of Total Delay
- Maximum Duty Cycle: 50%
- Operating temp. range: 0°C to + 70°C
- Temp. coeff. of delays: 1.0ns + 500ppm/°C
- Terminals: Electro tin plated Alloy 42 .020w x .010th

TEST CONDITIONS:

- Vcc=5.0VDC, Temp. 25° ± 5°C
- Time delay measured at the 1.5V level
- Rise time measured from .75V to 2.4V
- All outputs loaded with 15pf
- Input Test Pulse:
  - Pulse voltage: 3.0V
  - Pulse rise time: 2ns
  - Pulse width: 1.2 x max Td
  - Pulse spacing: 5 x max Td

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