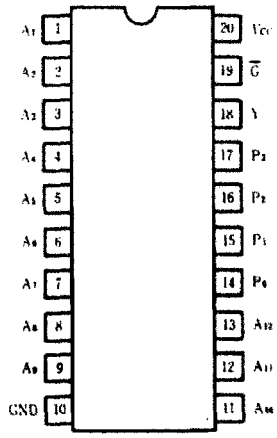
HD74HC679 ● 12-bit Address Comparator

The HD74HC679 address comparator simplifies addressing of memory boards and/or other peripheral devices. The four P inputs are normally hard wired with a preprogrammed address. An internal decoder determines what input information applied to the 12 A inputs must be low or high to cause a low state at the output (Y). For example, a positive-logic bit combination of 0111 (decimal 7) at the P input determines that inputs A_1 through A_7 must be low and that inputs A_8 through A_{12} must be high to cause the output to go low. Equality of the address applied at the A inputs to the preprogrammed address is indicated by the output being low.

The HD74HC679 features an enable input ($\overline{G}$). When $\overline{G}$ is low, the device is enabled. When $\overline{G}$ is high, the device is disabled and the output is high regardless of the A and P inputs.

■ PIN ARRANGEMENT

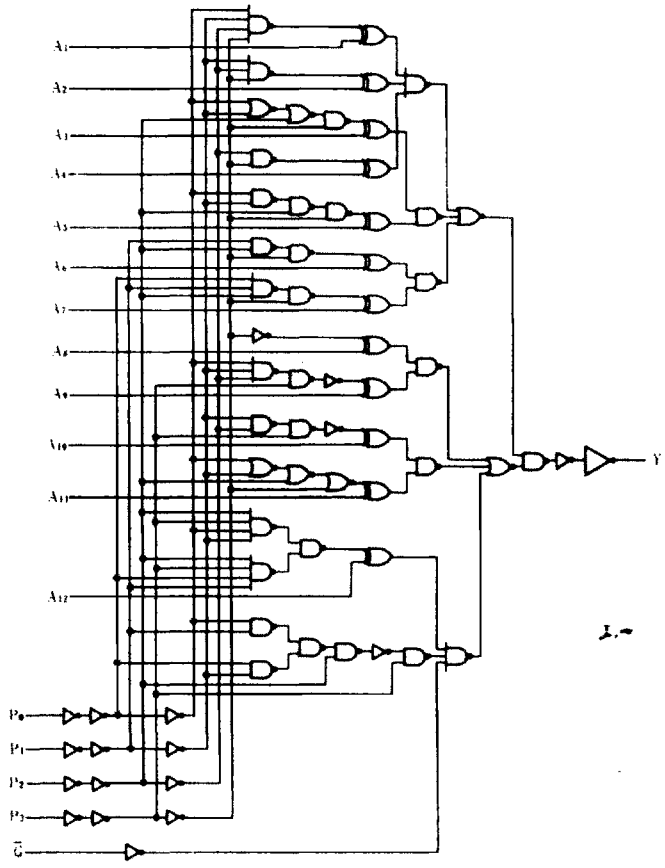


(Top View)

■ FEATURES

- High Speed Operation: tpd (A to Y)=18ns typ.(C_L=50pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: V_{CC}=2~6V
- Low Input Current: 1μA max.
- Low Quiescent Supply Current: I_{CC} (static)=4μA max. (Ta=25°C)

■ LOGIC DIAGRAM



FUNCTION TABLE

	Inputs																Output
$\bar{G}$	P_3	P_2	P_1	P_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	Y
L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L
L	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	L
L	L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	H	L
L	L	H	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L
L	L	H	L	H	L	L	L	L	L	H	H	H	H	H	H	H	L
L	L	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H	H	H	H	H	L
L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L
L	H	L	L	H	L	L	L	L	L	L	L	L	L	H	H	H	L
L	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	L
L	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	L
L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	H	L	H	X	X	X	X	X	X	X	X	X	X	X	X	H
L	H	H	H	L	X	X	X	X	X	X	X	X	X	X	X	X	H
L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	All other combinations																H
H	Any combination																H

DC CHARACTERISTICS

Item	Symbol	V_{CC}(V)	Test Conditions		Ta=25°C min	typ	max	Ta=−40~+85°C min	max	Unit
Input Voltage	V_{IH}	2.0			1.5	−	−	1.5	−	V
		4.5			3.15	−	−	3.15	−	
		6.0			4.2	−	−	4.2	−	
	V_{IL}	2.0			−	−	0.5	−	0.5	V
		4.5			−	−	1.35	−	1.35	
		6.0			−	−	1.8	−	1.8	
Output Voltage	V_{OH}	2.0	V_{in}=V_{IH} or V_{IL}	I_{OH}=−20μA	1.9	2.0	−	1.9	−	V
		4.5			4.4	4.5	−	4.4	−	
		6.0			5.9	6.0	−	5.9	−	
		4.5		I_{OH}=−4mA	4.18	−	−	4.13	−	
		6.0		I_{OH}=−5.2mA	5.68	−	−	5.63	−	
	V_{OL}	2.0	V_{in}=V_{IH} or V_{IL}	I_{OL}=20μA	−	0.0	0.1	−	0.1	V
		4.5			−	0.0	0.1	−	0.1	
		6.0			−	0.0	0.1	−	0.1	
		4.5		I_{OL}=4mA	−	−	0.26	−	0.33	
		6.0		I_{OL}=5.2mA	−	−	0.26	−	0.33	
Input Current	I_{in}	6.0	V_{in}=V_{CC} or GND		−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	6.0	V_{in}=V_{CC} or GND, I_{out}=0μA		−	−	4.0	−	40	μA

AC CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

Item	Symbol	V_{CC}(V)	Test Conditions	Ta=25°C min.	typ.	max.	Ta=−40~+85°C min.	max.	Unit
Propagation Delay Time	t_{PLH} t_{PHL}	2.0	P to Y	−	−	310	−	390	ns
		4.5		−	27	62	−	78	
		6.0		−	−	52	−	66	
	t_{PLH} t_{PHL}	2.0	A to Y	−	−	180	−	225	ns
		4.5		−	18	36	−	45	
		6.0		−	−	31	−	38	
	t_{PLH} t_{PHL}	2.0	$\bar{G}$ to Y	−	−	125	−	155	ns
		4.5		−	14	25	−	31	
		6.0		−	−	21	−	26	
Output Rise/Fall Time	t_{TLH} t_{THL}	2.0		−	−	75	−	95	ns
		4.5		−	5	15	−	19	
		6.0		−	−	13	−	16	
Input Capacitance	C_{in}	−		−	5	10	−	10	pF