P54/74FCT3521C/D
3.3 VOLT ULTRA-HIGH SPEED CMOS 8-BIT IDENTITY COMPARATORS

FEATURES

- Function and Drive Compatible with the Fastest TTL Logic
- Inputs and Outputs Interface with TTL Logic Levels
- 3.3V ± 0.2V Power Supply and CMOS for Lowest Power Dissipation
- FCT3-D speed at 3.8ns max. (Com'l)
  FCT3-C speed at 4.5ns max. (Com'l)
- Edge-rate Control Circuitry for Significantly Improved Switching Characteristics
- ESD protection exceeds 2000V
- 48 mA Sink Current (Com'l), 32 mA (Mil)
  15mA Source Current (Com'l), 12 mA (Mil)
- Designed for Easy Expansion to Wider Word Widths
- Operational over the Full Commercial and Military Temperature Range
- Input Clamp Diodes to Limit Bus Reflections
- Manufactured in 0.4 micron PACE Technology™

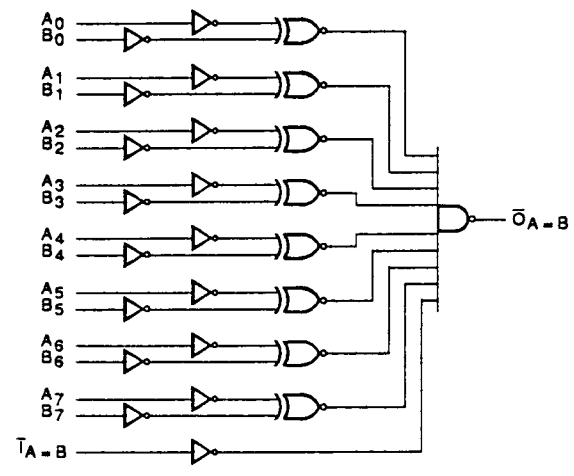
DESCRIPTION

The 'FCT3521 are ultra-fast expandable eight- (8) bit comparators. Each device compares two words of upto 8 bits each. The output goes to a low level when the two words being compared match bitwise. The word width maybe expanded by cascading (i. e., connecting the output of the comparator to the expansion input $\overline{I}_{A=B}$ of another 'FCT3521 device) or by logically ORing the outputs of several 'FCT3521 devices. If not used for expansion, $\overline{I}_{A=B}$ must be set at CMOS low voltage. The CMOS comparator typically dissipates one-third the power of its slower bipolar equivalents.

The 'FCT3521s are members of the PACE LOGIC™ Family which includes byte-wide bus interface and memory related components. PACE LOGIC is manufactured using PACE III Technology™ which is Performance Advanced CMOS Engineered to use 0.4 micron effective channel lengths giving 250 picoseconds loaded* internal gate delays. The nominal supply voltage is reduced from the conventional 5.5V to 3.3V, thus reducing output swings dramatically. This, together with the (lower inductance) center power and ground pins, significantly improves switching noise characteristics that would otherwise occur in very high speed circuitry.

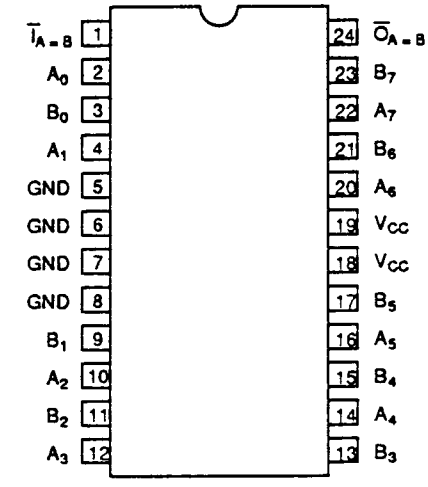
*For a fan-in/fan-out of 4, at 85°C junction temperature and 3.3V supply. For a fan-in/fan-out of 1, the internal gate delay is 200 picoseconds at room temperature and 3.3V supply.

FUNCTIONAL BLOCK DIAGRAM



1746 01

PIN CONFIGURATION



DIP (P4, D4), SOIC (S4)

1746 02

PERFORMANCE SEMICONDUCTOR CORPORATION

Means Quality, Service and Speed

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temp Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +5.0	V
I_{IN}	Input Current	–30 to +5.0	mA

1746 Tbl 01

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to V_{CC} + 0.5	V
V_{OUT}	Voltage Applied to Output	–0.5 to V_{CC} + 0.5	V

1746 Tbl 02

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

1746 Tbl 03

Supply Voltage (V_{CC})	Min	Max
Military	+3.1V	+3.5V
Commercial		

1746 Tbl 04

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0		V_{CC} + 0.5	V		
V_{IL}	Input LOW Voltage		–0.5		0.8	V		
V_H	Hysteresis			0.35		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military/Commercial (CMOS)	V_{CC} – 0.2	V_{CC}		V	MIN	I_{OH} = –300µA
		Military (TTL)	2.4			V	MIN	I_{OH} = –12mA
		Commercial (TTL)	2.4			V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military/Commercial (CMOS)		GND	0.2	V	MIN	I_{OL} = 300µA
		Military (TTL)		0.3	0.5	V	MIN	I_{OL} = 32mA
		Commercial (TTL)		0.3	0.5	V	MIN	I_{OL} = 48mA
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = V_{CC}
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = GND
I_{IH}	Input HIGH Current[3]				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current[3]				–5	µA	MAX	V_{IN} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
C_{IN}	Input Capacitance[3]			5	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[3]			9	12	pF	MAX	All outputs

1746 Tbl 05

Notes:

1. Typical limits are at V_{CC} = 3.3V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{os} tests should be performed last.
3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	V_{CC} = MAX, f_1 = 0, Outputs Open, V_{IN} = V_{CC} – 0.6V[2]
I_{CCD}	Dynamic Power Supply Current[3]	0.15	0.25	mA/ mHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current[5]	1.7	4.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, f_1 = 10MHz, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.0	5.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, f_1 = 10MHz, and V_{IN} = V_{CC} – 0.6V or V_{IN} = GND

1746 Tbl 06

Notes:

1. Typical values are at V_{CC} = 3.3V, +25°C ambient and maximum loading.
2. Per TTL driven input (V_{IN} = V_{CC} – 0.6V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = V_{CC} – 0.6V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1
   All currents are in milliamps and all frequencies are in megahertz.

TRUTH TABLE

Inputs		Output
$\overline{I}_{A=B}$	A, B	$\overline{O}_{A=B}$
L	A = B*	L
L	A ≠ B	H
H	A = B*	H
H	A ≠ B	H

1746 Tbl 07

H = HIGH Voltage Level
L = LOW Voltage Level
*$A_0 = B_0$, $A_1 = B_1$, $A_2 = B_2$, etc.

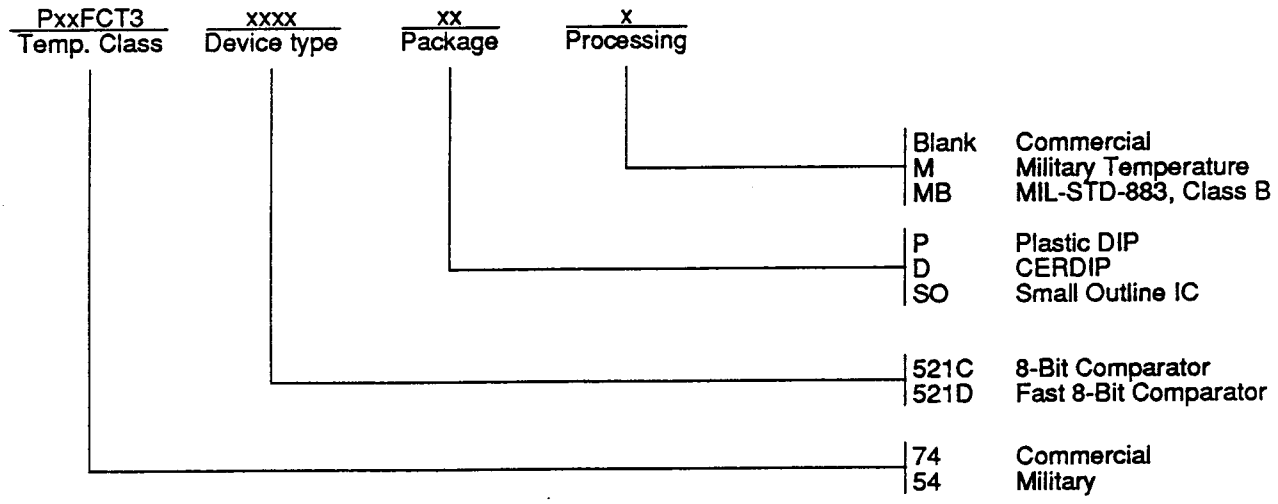
AC CHARACTERISTICS ('FCT3521)

Symbol	Parameter	'FCT3521C				'FCT3521D				Units	Fig. No.
		MIL		COM'L		MIL		COM'L			
		Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.		
t_{PLH} t_{PHL}	Propagation Delay A_N or B_N to $\overline{O}_{A=B}$	1.5	5.1	1.5	4.5	1.5	4.5	1.5	3.8	ns	1, 2, 3
t_{PLH} t_{PHL}	Propagation Delay $I_{A=B}$ to $\overline{O}_{A=B}$	1.5	4.5	1.5	4.1	1.5	4.1	1.5	3.5	ns	1, 3

1746 Tbl 08

Notes:
1. Minimum limits are guaranteed but not tested on Propagation Delays.
2. AC Characteristics guaranteed with C_L = 50pF.

ORDERING INFORMATION



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