Beckman Series 7545 and 7546 MICROPROCESSOR COMPATIBLE CMOS 12-BIT D-TO-A CONVERTERS

Effective date: June, 1979

Beckman Series 7545 and 7546 are the first CMOS 12-bit Digital-to-Analog Converters to offer the combination of complete 8-bit microprocessor compatibility, real 12-bit accuracy and TTL or CMOS logic input compatibility within a single package.

Their features include:

- 12-Bit Resolution
- ±0.012% linearity (± ½ LSB in 12 bits) guaranteed over the operating temperature range (7545)
- Double buffered inputs—separate input and holding registers
- Microprocessor compatible 4-bit/8-bit byte input for 12-bit inputs from 8-bit microprocessors
- Serial or parallel input formats—switchable upon command
- TTL or CMOS input compatibility
- Commercial and military temperature range versions
- Low power CMOS internal circuitry
- All thin film application resistors included for superior stability and precision performance
- Low reference feedthrough for precision AC reference applications

Microprocessor Compatibility

Both Series 7545 and 7546 have two input registers separate from the switch holding register which can separately be enabled to accept a 12-bit input data word in 4-bit (most significant bits) and 8-bit (least significant bits) bytes from an 8-bit microprocessor bus.

True 12-Bit Performance

± ½ LSB linearity (±0.012% FSR) is guaranteed over the full operating temperature range for each model of series 7545. Similarly, worst case limits are specified for initial gain setting error and gain error temperature coefficient for both the 7545 and 7546 and for the Series 7546, zero offset and zero offset temperature coefficient are guaranteed.

Serial or Parallel Operation

Both series can operate in a serial input mode or a parallel input mode and, in fact, can alternately be switched from one mode to the other. In the serial mode, the four least significant bit input registers can be bypassed to allow processing 8-bit input words in the eight most significant bit locations.

The input registers and holding register are configured to allow either switch updating upon command using the enable lines, or in a continuous conversion mode by permanently enabling the transfer lines for parallel operation.

TTL or CMOS Compatible

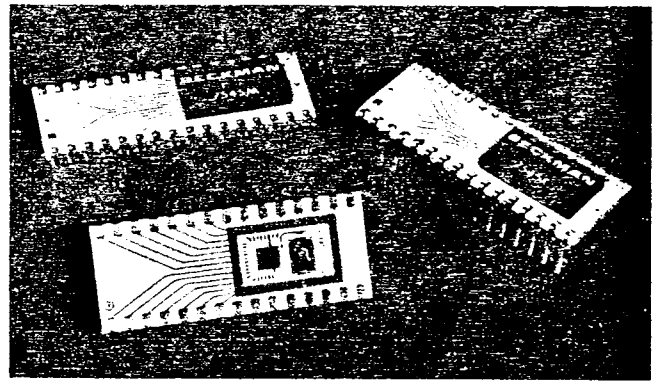
Both input registers utilize input translators which can accept either TTL inputs using a +5 volt supply or CMOS inputs using supply levels from +5 to +15 volts. Separate holding register and input register power supply lines allow this flexibility without compromising linearity.

Military and Commercial Versions

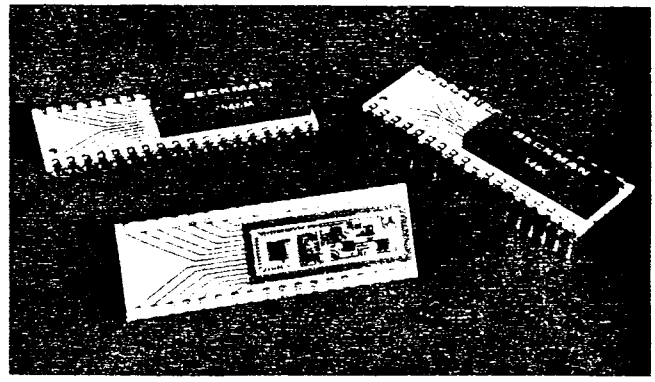
Commercial versions are available in a polymer sealed package (e.g., 7545C and 7546C) with performance specifications guaranteed over 0°C to +70°C. The MIL range performance versions utilize an hermetically sealed package with performance guaranteed over −55°C to +125°C (e.g., 7545M and 7546M).

Internal Configuration

Precision thin film nichrome resistors are deposited on an alumina substrate to achieve optimum stability and uncompromised linearity and tracking performance. A separate CMOS chip contains the input level translators and shift registers, the DAC switch



Series 7545 Multiplying D-to-A Converter



Series 7546 General Purpose D-to-A Converter

holding register, the switch drivers and analog switches and is silicon nitride passivated to insure high reliability performance for both commercial and military requirements. These devices are assembled on a thick film substrate to provide the most cost effective overall assembly.

All units receive 100% electrical testing over the specified temperature range to assure reliable performance capabilities for both commercial and military versions.

General Purpose and Multiplying Models

Series 7545 is the four quadrant multiplying configuration designed for use with an external AC reference. Four quadrant multiplication is implemented by the bipolar digital proportioning of the AC reference. Two quadrant multiplication can be implemented by either unipolar proportioning of an AC reference or bipolar proportioning of a unipolar DC reference. The use of external reference and amplifier circuitry allows the maximum flexibility for supply levels and signal processing levels. For example, the maximum reference and output levels are determined by the amplifiers selected and their output voltage swing capability with respect to power supply levels. Series 7545 can be used with a wide range of supplies to accommodate TTL or CMOS system standard supply levels where the digital and analog subsystems operate on different supplies.

Series 7545 typically requires less than 10 mW of power consumption, making it an ideal choice for operation with low power

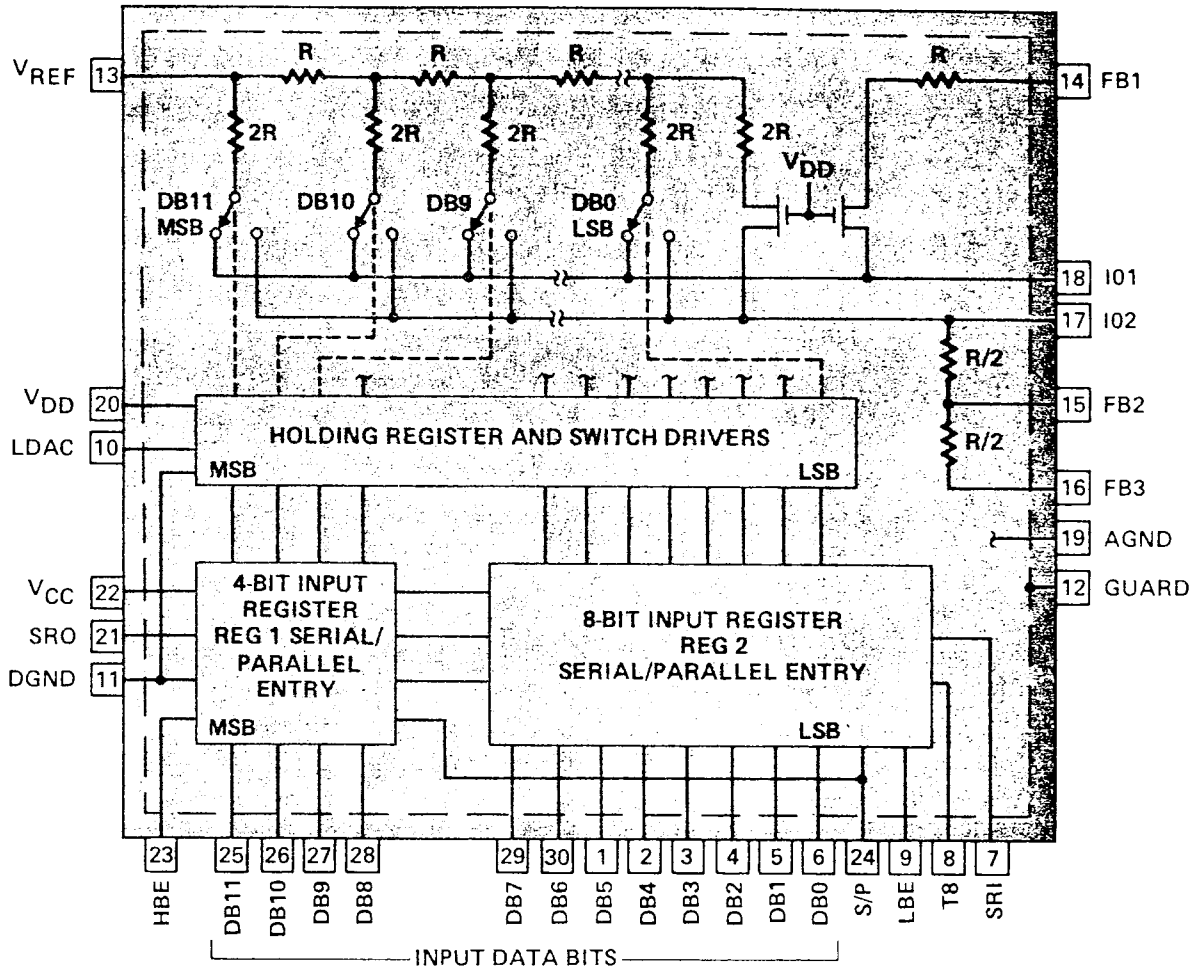


Figure 1. Series 7545 Block Diagram

external amplifiers in battery powered, portable instrumentation applications.

Series 7546 allows higher system density by providing a complete general purpose converter which contains a 10 volt DC reference and the op amp and feedback circuitry to achieve up to 5 mA of output drive capability without the addition of other external components.

The complete general purpose converter also eases the design and manufacturing task by incorporating preadjusted zero offset for the output buffer amplifier, the biasing amplifier for bipolar operation and, also, the internal reference. Each is precisely pretrimmed to guarantee initial tolerances which will satisfy most applications, although external adjustment is possible, if required.

Series 7546 can also utilize the wide variety of supply levels anticipated for most digital systems applications utilizing a combination of CMOS or TTL and analog interface sections.

Series 7545 Operation

As shown in Figure 1, the input voltage, V_{REF}, is applied to a 20K binary weighted, R-2R ladder. Each 2R leg is connected to a pair of N-channel, MOS transistors. These transistors switch the binary weighted currents that flow in each 2R leg to either the I01 bus (logic "1" input) or to the I02 bus (logic "0" input). Normal operation requires operational amplifiers at I01 and I02 which maintain these nodes at ground or virtual ground potential.

Internal Compensation

The "on" resistance of the MOS transistor switches are binary weighted with the MSB set at 25 ohms. The linearity of the DAC is dependent upon the ratio accuracies of the switch resistances and not upon their absolute values. Excellent switch ratio tolerances account for small linearity errors even over the operating temperature range of the DAC. Also, the low power density in the switching transistors eliminates transient thermal gradients normally encountered with bipolar current switches.

Feedback gain compensation for switch resistance is provided by an "on" switch in series with the internal "R" feedback resistor. This compensation transistor reduces gain drift errors to less than $2p/10^{n}/°C$ and provides outstanding power supply rejection.

A second compensation transistor (unique to Series 7545 and 7546) compensates the R-2R ladder terminating resistor.

Digital Inputs

The input buffer register is divided into a 4-bit shift register that controls the four MSB's and an 8-bit shift register that controls the eight LSB's. A serial/parallel control line (S/P) allows data to be applied to the serial input through SRI or the parallel inputs, DB0-DB11. Separate enable lines (HBE and LBE) are provided for these registers. In the parallel mode when S/P is logic "0", data bits DB11 through DB8 will enter the input register when HBE is set to a logic "1". Data inputs DB0 through DB7 will enter their input buffer register when LBE is set to logic "1". This arrangement allows sequential loading of a 2-byte, 12-bit word from a single 8-bit data bus.

In the serial mode when S/P is logic "1", serial data appearing at the serial input (SRI) will be clocked into the input register on the positive transition of a pulse train applied simultaneously to HBE and LBE. The serial data in the input buffer can be recovered from the serial output pin, SRO.

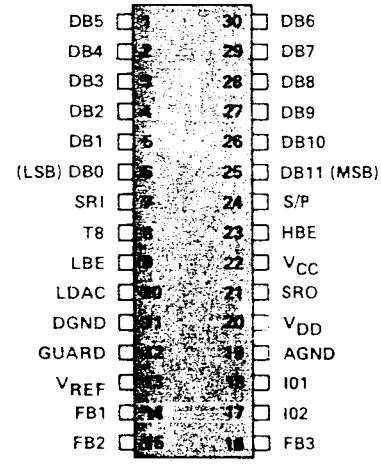
All logic inputs are provided with level shifters that operate from V_{CC}. All digital inputs are compatible with TTL logic levels when V_{CC} is connected to +5V and CMOS levels when V_{CC} is connected to a CMOS supply (see operating limits).

Table I—Series 7545 Performance Specifications (Note 1)

Parameter			Conditions	Minimum	Typical	Maximum	Units
Converter Transfer Characteristics	Resolution		T8="1"			12	bits
	Non-linearity	7545C	$0°C \leq T_C \leq +70°C$			±0.012	% FSR
		7545M	$-55°C \leq T_C \leq +125°C$			±0.012	% FSR
	Differential Non-linearity				±0.012		% FSR
	Inital Gain Setting		(Note 2)			±0.02	% FSR
	Gain Setting Tempco	7545C	$0°C \leq T_C \leq +70°C$		1	10	p.p.m./°C
		7545M	$-55°C \leq T_C \leq +125°C$		1	2	p.p.m./°C
	Reference Feedthrough		V_{REF} = 20V p-p; 10 kHz		1	10	mV p-p
Analog Output Characteristics	Settling Time		(Note 3)		2		µs
	Output Leakage Current (I01, I02)	7545C	$0°C \leq T_C \leq +70°C$			25	nA
		7545M	$-55°C \leq T_C \leq +125°C$			100	nA
	Output Capacitance (at I01, I02)	C01	All Data Bits High		200		pF
		C02	All Data Bits High		150		pF
		C01	All Data Bits Low		125		pF
		C02	All Data Bits Low		70		pF
Reference Characteristics	Input Voltage Range					±10	V
	Input Resistance			18	20	22	kΩ
Digital Input Characteristics	TTL Logic Levels (Note 4)	Logic "1"	V_{CC} = +5V	3.0			V
		Logic "0"	V_{CC} = +5V			0.8	V
		I_{IL}; I_{IH}	All Input Levels		±10^{-3}	±1	µA
	Parallel Data & Serial 8-Bit Word						
	Data Set-up		tDW	750			nsec
	Data Hold		tDH	50			nsec
	Pulse Width		LDAC, HBE, LBE t0	500			nsec
	Serial Data 12-Bit Word						
	Data Set-up		tDW	300			nsec
	Data Hold		tDH	450			nsec
	Pulse Width		LDAC, HBE, LBE t0	500			nsec
	Serial Clock Frequency		V_{CC} = +5V			500	kHz
Power Supply Characteristics	V_{CC}, V_{DD} Current					2	mA
	V_{CC}, V_{DD} Supply Rejection					10	p.p.m. FSR/%
Temperature Ranges	Operating Temp. Range	7545C	Worst Case Limits Apply	0		+70	°C
		7545M	Worst Case Limits Apply	−55		+125	°C
	Storage Temp. Range		Non-operating	−65		+150	°C

Notes: (7545)

1. Unless otherwise specified, performance guarantees apply for $+10V \leq V_{DD} \leq +15V$, $+5V \leq V_{CC} \leq V_{DD}$ and $V_{REF} = \pm 10V$ and specifications for 7545C apply over $0°C \leq T_C \leq +70°C$ and for 7545M over $-55°C \leq T_C \leq +125°C$.
2. The Internal feedback resistor, R (FB1 at pin 14) has been laser pre-trimmed to establish the proper gain ratio against the ladder impedance "R."
3. The output settling time for the multiplying configuration is almost entirely dependent on the external amplifier selected. The specification shown is for the output current I01 for an FSR step settling to within 0.01% FSR.
4. Threshold levels shown are for TTL logic levels. For different V_{CC} levels typical in CMOS systems, see Figure 3.



Series 7545 Pin Assignments

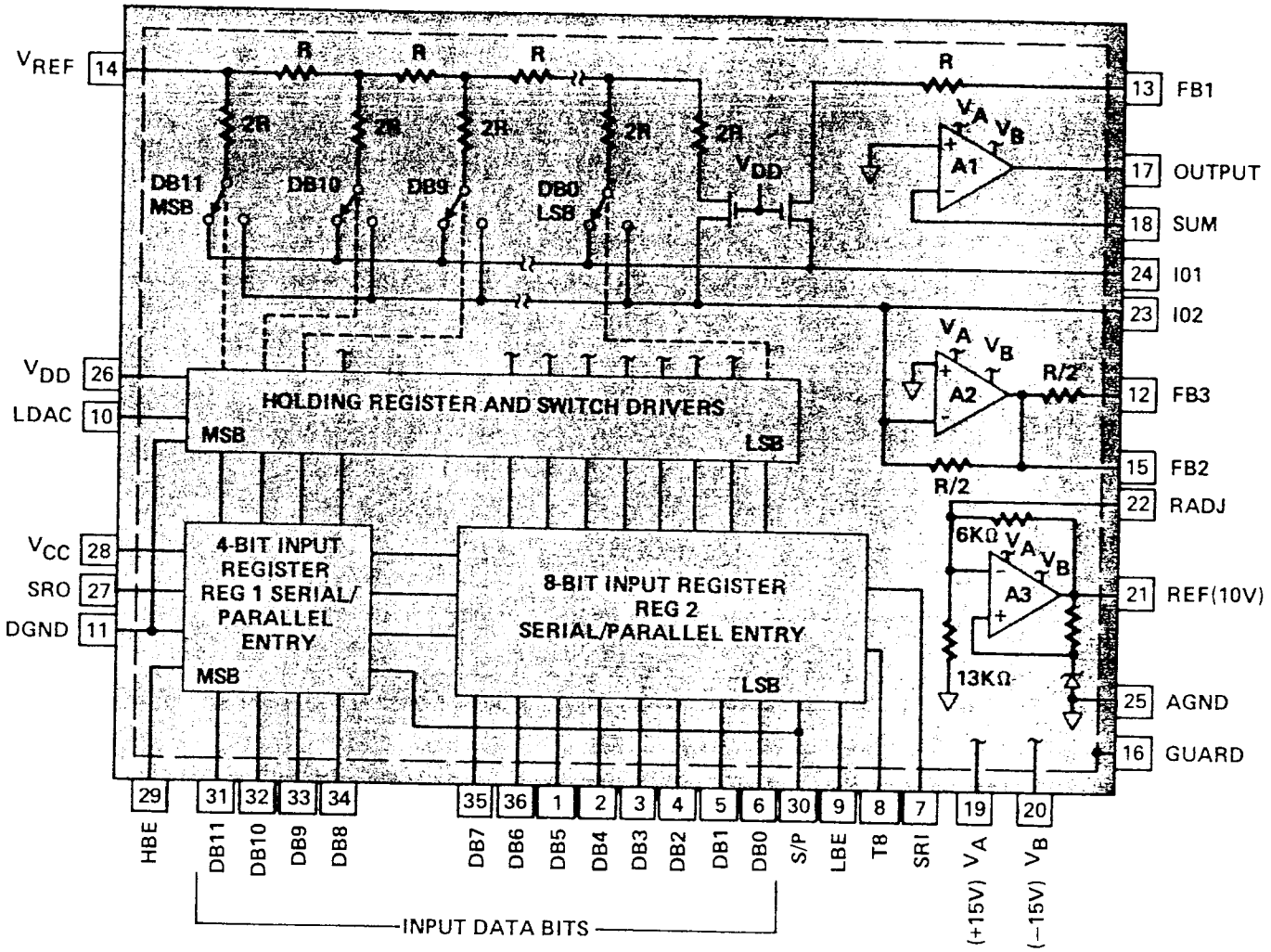


Figure 2. Series 7546 Block Diagram

Series 7546 Operation

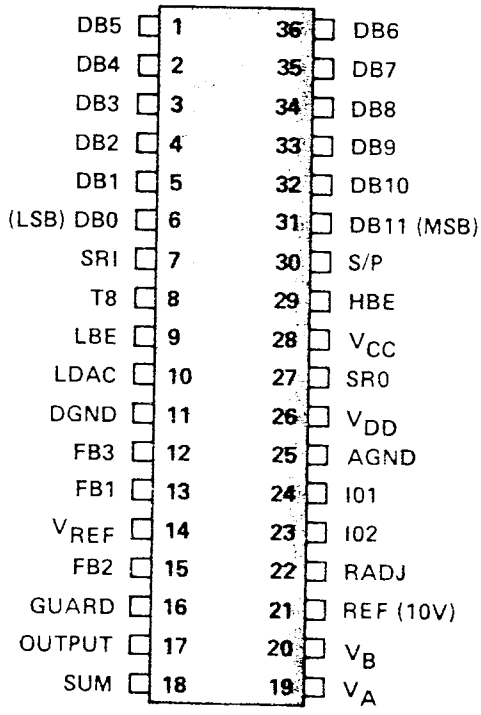
Series 7546 includes all of the logic controls and flexibility of the 7545 plus the output amplifiers for both unipolar and bipolar operation and a precision +10V reference. Each amplifier is laser adjusted for zero offset and the precision thin film ladder network and feedback resistors (see Figure 2) are ratio matched to achieve the performance guarantees shown in Table II.

Precision Internal Reference

As shown in Figure 2, a precision voltage reference is included so that the converter can be configured as a general purpose D-to-A converter. Although the reference is preset and specified to +10V ±10mV, an adjustment pin (RADJ) is available for setting the reference to a slightly different value within the range of +10 ±0.5V. The reference has excellent rejection to variations in supply voltage, and is buffered and available through pin 21 for connection to the D-to-A converter input, (V_{REF}) and other external circuits at 5mA load without degradation of specifications.

Package Construction

Series 7545 and 7546 D-to-A Converters utilize thick film conductors fired to an alumina substrate. Interconnections between these conductors, the thin film resistor network, and the CMOS and bipolar IC's are made by thermal compression gold wire bonding. A ceramic cover is then sealed to the substrate using a polymer seal for 7545C and 7546C and a hermetic seal for 7545M and 7546M. The lead frame is reflow soldered to terminal pads on the substrate.



Series 7546 Pin Assignments

Table II—Series 7546 Performance Specifications (Note 1)

Parameter			Conditions	Minimum	Typical	Maximum	Units
Converter Transfer Characteristics	Resolution		T8 = "1"			12	bits
	Non-linearity		T_C = +25°C			±0.012	% FSR
	Non-linearity Tempco					±2	p/10⁶/FSR/°C
	Differential Non-linearity				±0.012		% FSR
	Zero Offset — Unipolar		All Inputs "0" (Note 2)			±0.025	% FSR
	Zero Offset Tempco — Bipolar	7546C	0°C ≤ T_C ≤ +70°C (Note 2)		±5	±15	p/10⁶/°C
		7546M	−55°C ≤ T_C ≤ +125°C (Note 2)		±5	±10	p/10⁶/°C
	Initial Gain Setting		T_C = +125°C			±0.2	% FSR
	Gain Setting Tempco (Note 3)	7546C	0°C ≤ T_C ≤ +70°C		±10	±30	p/10⁶/°C
		7546M	−55°C ≤ T_C ≤ +125°C		±10	±20	p/10⁶/°C
	Reference Feedthrough		V_{REF} = 20V p-p; 10 kHz		1	10	mV p-p
Analog Output Characteristics	Settling Time		To 0.01% FSR for FSR step			10	μs
	Output Range		Int. or Ext. Reference			±10	V
	Output Resistance				0.02		Ω
Reference Characteristics	Input Voltage Range		External Reference			±10	V
	Input Resistance		Pin 14	18	20	22	kΩ
Digital Input Characteristics	TTL Logic Levels (Note 4)	Logic "1"	V_{CC} = +5V	3.0			V
		Logic "0"	V_{CC} = +5V			0.8	V
		I_{IL}, I_{IH}	All Input Levels		+10⁻⁵	+1	μA
	Parallel Data & Serial 8-Bit Word						
	Data Set-up		tDW	750			nsec
	Data Hold		tDH	50			nsec
	Pulse Width		LDAC, HBE, LBE t0	500			nsec
	Serial Data 12-Bit Word						
	Data Set-up		tDW	300			nsec
	Data Hold		tDH	450			nsec
	Pulse Width		LDAC, HBE, LBE t0	500			nsec
	Serial Clock Frequency		V_{CC} = +5V			500	kHz
Internal Reference Characteristics	Output Voltage Accuracy		V_{REF} = +10V, T_C = +25°C			±0.1	%
	Output Voltage Tempco				20		p/10⁶/°C
	Output Current					+5	mA
Power Supply Characteristics	V_A, V_B Current					10	mA
	V_{CC}, V_{DD} Current					2	mA
	V_A, V_B Supply Rejection					5	p/10⁶ FSR/%
	V_{CC}, V_{DD} Supply Rejection					10	p/10⁶ FSR/%
Temperature Ranges	Operating Temp. Range	7546C	Worst Case Limits Apply	0		+70	°C
		7546M	Worst Case Limits Apply	−55		+125	°C
	Storage Temp. Range		Non-operating	−65		+150	°C

Notes: (7546)

1. Unless otherwise specified, performance guarantees apply for +10V ≤ V_{DD} ≤ +15V, +5V ≤ V_{CC} ≤ V_{DD}, V_A = +15V, V_B = −15V and V_{REF} = ±10V, and pin 21 is connected to pin 14. Specifications for 7546C apply over 0°C ≤ T_C ≤ +70°C, and for 7546M over −55°C ≤ T_C ≤ +125°C.
2. Zero offset specifications apply over the operating temperature range for each model (7546C or 7546M). Zero Offset — Unipolar includes only the zero offset characteristic of output amplifier A1. Zero Offset Tempco—Bipolar includes the temperature characteristics of gain, the zero offset of amplifier A1 and A2 and the reference tempco.
3. For Series 7546C and 7546M the Gain Setting and Gain Setting Tempco specifications include the ratio of the feedback resistor R (FB1 at pin 13) to the ladder equivalent resistance R, plus the initial setting and tempco of the internal +10V reference (pin 21 connected to pin 14).
4. Threshold levels shown are for TTL logic levels. For different V_{CC} levels typical for CMOS systems, see Figure 3.

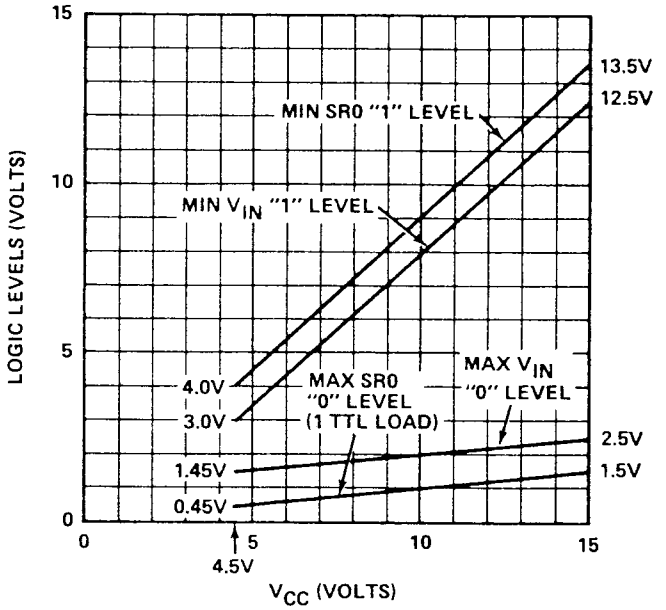


Figure 3. Logic Levels

Terminology

Differential Linearity is the difference between the actual output and the theoretical output between any two adjacent steps in the transfer function.

Gain is the ratio of the full scale range (FSR) to V_{REF} after the zero output error has been removed.

Gain Drift is the maximum change in gain at the temperature end points with respect to the +25°C value, divided by the corresponding temperature change expressed in parts per million of full scale range (p/10⁶/°C).

Non-Linearity is the deviation of the analog output from a straight line drawn between the two end points (all bit ON and all bits OFF).

Offset Drift is the maximum change in offset voltage at the temperature end points with respect to the +25°C value, divided by the corresponding temperature change expressed in parts per million of full scale range (p/10⁶/°C).

Settling Time is the total time (including slew time) for the output to settle to within the error band (±0.01% FSR) about its value following an input change.

FSR is full scale range—FSR = 10V for unipolar 0 to −10V output, FSR = 20V for bipolar +10V to −10V output.

Digital Input Codes (7545 and 7546)

The digital input codes for Series 7545 and 7546 D-to-A Converters are natural binary code. The MSB has a weight of (2^{-1}), and second bit has a weight of (2^{-2}), and so forth down to the LSB, which has a weight of 2^{-12}. Table III below shows the full-scale, half-scale and zero codes, and their respective analog outputs for both unipolar output and bipolar output.

Terminal Designations

AGND — *Analog Ground* (see Power Supply Considerations).

DB0-DB11 — *Input Data Bits.*

DGND — *Digital Ground* (see Power Supply Considerations).

FB1,2,3, — *Feedback* Resistors (see Figures 1 and 2).

GUARD — *Ground Plane* (see Power Supply Considerations).

HBE — **High Byte Enable*—In the parallel mode data at DB8 through DB11 is transferred into the input register when HBE reaches logic "1". In the serial mode, HBE is tied to LBE and is used to clock serial data into the input register.

I01,2 — Current output buses normally at ground or virtual ground.

LBE — **Low Byte Enable*—In the parallel mode data at DB0 through DB7 is transferred into the input register when LBE reaches logic "1". In the serial mode, LBE is tied to HBE and is used to clock serial data into the input register.

LDAC — **Load DAC*—Logic "1" at LDAC transfers data from the input register to the holding register to update the DAC output.

OUTPUT — Converter Voltage Output (7546 only).

RADJ — *Reference Adjust* (see Applications Section).

REF(10V) — *Internal Reference* Output (7546 only) normally connected to V_{REF} reference input.

S/P — *Serial/Parallel Control*—Set at logic "1" for serial operation and logic "0" for parallel operation.

SRI — *Serial Register Input.*

SRO — *Serial Register Output.*

SUM — Output amplifier summing junction (7546 only).

T8 — *Truncate 8* allows 8-bit serial words to enter the eight most significant bit locations bypassing the four least significant bit locations. Set T8 at logic "0" for 8-bit serial operation. Also, DB0 through DB3 must be held at logic "0" during 8-bit operation. For 12-bit operation set T8 at logic "1".

*In parallel operation, LDAC, HBE and LBE can either be controlled by system timing or permanently wired to logic "1" to allow continuous parallel updating.

Maximum Ratings (7545 and 7546)

V_{REF} to GND ..... ±25V
V_{DD} to GND ..... +17V
V_{CC} to GND ..... +17V
V_{CC} to V_{DD} ..... +0.4V
I01, I02 ..... ±5 mA
I01 to GND; I02 to GND ..... −300 mV to V_{DD}
Operating Temperature Range ..... −55°C to +125°C
Storage Temperature Range ..... −65°C to +150°C
Digital Input Voltage Range ..... V_{DD} to GND

Operation Cautions

1. Do not apply voltages higher than V_{CC} to SRO.
2. Do not apply voltages higher than V_{DD} or less than −300 mV with respect to GND to any other input/output terminal except V_{REF}, FB1 or FB2.
3. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Store units in conductive foam.
4. V_{CC} should never exceed V_{DD} by more than 0.4V.
5. Unused inputs should be grounded or connected to V_{CC}.
6. A 50 ohm resistor should be connected in series with V_{DD} next to the decoupling capacitor, thus protecting the device during power on sequencing.

Table III—Series 7545 and 7546 Digital Input Codes. (V_{REF} = +10.000V)

MSB	Digital Input (DB11-DB0)	LSB	Unipolar Configuration Output (Fig. 7, 9)	Unipolar Configuration Output (V)	Bipolar Configuration Output (Fig. 8, 11)	Bipolar Configuration Output (V)
1	1 1 1 1 1 1 1 1 1 1 1 1	1	$-V_{REF}(1.0-2^{-12})$	−9.9976	$-V_{REF}(1.0-2^{-11})$	−9.9952
1	0 0 0 0 0 0 0 0 0 0 0 1	1	$-V_{REF}(0.5+2^{-12})$	−5.0024	$-V_{REF}(2^{-11})$	−0.00488
1	0 0 0 0 0 0 0 0 0 0 0 0	0	$-V_{REF}/2$	−5.0000	0	0
0	1 1 1 1 1 1 1 1 1 1 1 1	1	$-V_{REF}(0.5-2^{-12})$	−4.9976	$+V_{REF}(2^{-11})$	+0.00488
0	0 0 0 0 0 0 0 0 0 0 0 1	1	$-V_{REF}(2^{-12})$	−0.00244	$+V_{REF}(1-2^{-11})$	+9.9952
0	0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	$+V_{REF}$	+10

Power Supply Considerations

Significant improvement in high frequency noise rejection will result if individual converter circuits are decoupled from the power supply with small R-C networks. These should be located as close to the circuit as practical. Separate digital and analog ground returns designated DGND and AGND respectively, are provided so that noisy ground currents, normally associated with digital circuits can be separately returned to the system power supply ground. Both AGND and DGND must be connected to a common ground potential within the system. The converter will perform within specification with up to ±0.5V between the two grounds.

A separate ground plane built into the DAC (GUARD) may be used to reduce leakage currents and feedthrough capacitance. It is recommended that this be connected to the analog ground (AGND) in most system applications.

Protective diodes shown in the application diagrams protect the device against voltage transients during power "on" and "off" sequencing. If V_{CC} and V_{DD} are derived from a common supply and the device's Absolute Maximum Ratings are strictly adhered to, these protective measures may be omitted.

12-Bit Parallel Loading (7545 and 7546)

The logic connections for loading 12-bit parallel data into the input register is shown in Figure 4. Data is transferred from the input buffer register to the holding register when the update line, LDAC is logic "1". (LDAC is a level-actuated function and must be held "high" at least 500 nanoseconds for proper data transfer to occur). When data is stable on the parallel inputs (DB0-DB12), it can be transferred on the positive edge of the enable pulse (logic "1" applied to HBE and LBE simultaneously for 500 ns min.). If LDAC is logic "0", the contents of the holding register are unaffected by the signals appearing on the data bit inputs.

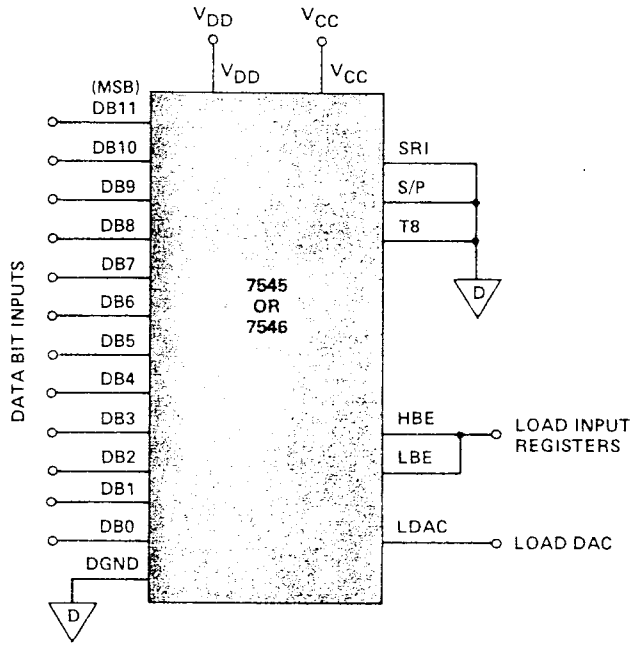


Figure 4. 12-Bit Parallel Loading

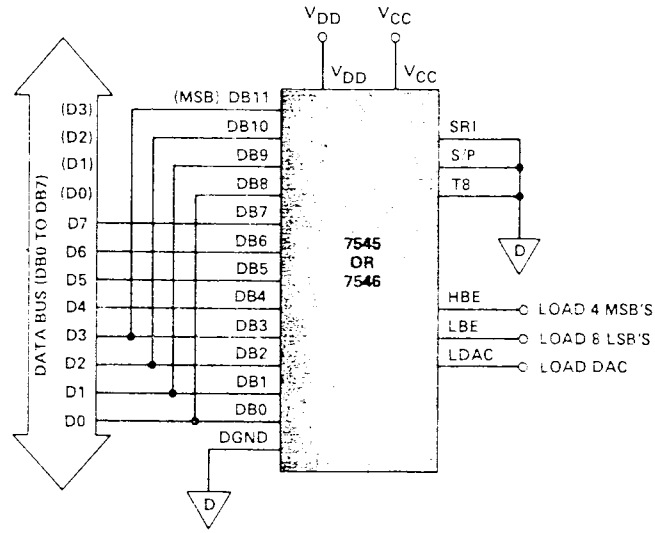
Two Byte Parallel Loading (7545 and 7546)

The configuration for two-byte loading of parallel data from a data bus is shown in Figure 5. As shown in the timing diagram, the least significant data byte (DB0-DB7) is loaded into the input buffer register on the positive transition of LBE. When the most significant data byte (DB8-DB11) is available on the bus, the input buffer register is loaded on the positive edge of HBE. Data is transferred from the input buffer register to the holding register when the DAC update line LDAC is logic "1".

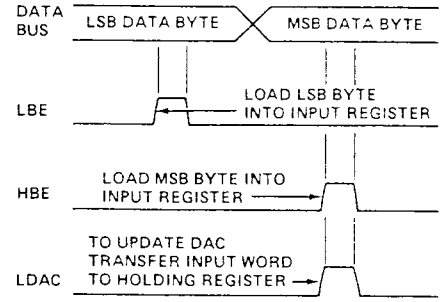
Serial Data Input Loading (7545 and 7546)

The connection and timing diagrams for serial loading are shown in Figure 6. Either an 8-bit or a 12-bit word may be loaded into the input register at SRI. If T8 is held to logic "0", the four least significant input latches in the input register are bypassed to provide serial loading of eight-bit words into the eight most significant bit locations. If T8 is held to a logic "1", the DAC will accept a 12-bit serial word. When loading a 12-bit word, exactly 12 positive edges of the clock are required at HBE and LBE to load serial data into the input register. Only 8 positive edges of the clock are required for an 8-bit word.

The serial data in the input buffer can be recovered from the serial output pin, SRO. The first bit loaded into the input register will appear at the shift register output, (SRO) either on the 12th positive clock edge (T8 = "1") or on the 8th positive clock edge (T8 = "0"). S/P must be held at logic "1" for serial operation.

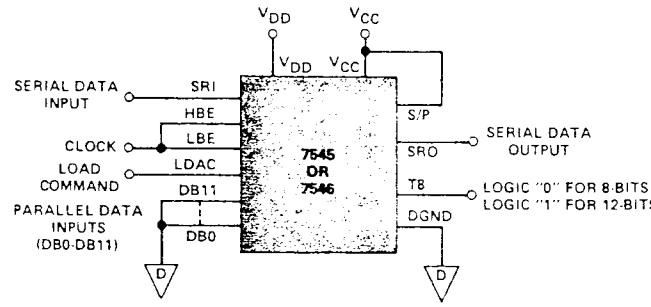


(a) Connection Diagram

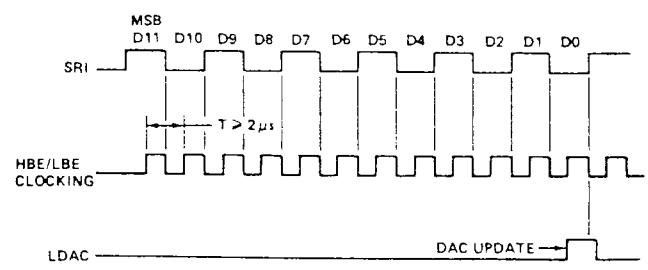


(b) Timing Diagram

Figure 5. Two Byte Parallel Loading (7545 and 7546)



(a) Connection Diagram



(b) Timing Diagram for 12-Bit Word

Figure 6. Serial Data Input Loading

Unipolar Operation (7545)

Figure 7 shows the circuit configuration for 7545 unipolar operation (0V to −10V). A protective diode is shown across the amplifier input which limits the amount of voltage which can appear across the terminals I01 to ground during power turn-on or turn-off. Note that I02 is connected to analog ground (AGND). Both DGND and AGND must be tied to a common ground somewhere in the system.

The specific zero offset circuit will be determined by the external amplifier selected. If a summing node approach is required, typical component values are shown in Figure 9. If a fast output amplifier is used, the feedback capacitor C1 is used to compensate for summing node capacitance.

The Zero Offset and Gain adjustments should be performed in the following order.

1. Zero Offset Adjustment—Adjust the amplifier output to zero (within ±0.5 mV). (A zero offset appearing at the summing junction (I01) will produce a gain error, therefore, the output should be set to zero by a method that will also set the summing junction voltage to zero.)
2. Gain Adjustment—Set R1 and R2 to zero ohms. Set DB0-DB11 to logic "1". If the output is greater than the required full scale value increase R1. If the output is less than the required full scale value increase R2.

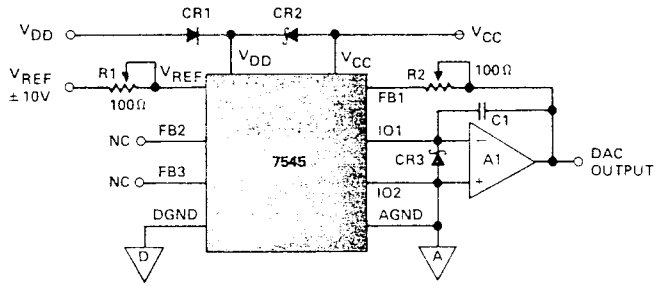


Figure 7. Unipolar Operation

Bipolar Operation (7545)

Figure 8 shows the circuit configuration for Series 7545 bipolar operation. Protective diodes and the feedback compensation capacitor are shown.

1. Zero Offset Adjustment—Adjust the offset of amplifiers A1 and A2 to zero. (A zero offset appearing at the summing junction will produce a gain error, therefore, the outputs should be set to zero by a method that will also set the summing junctions to zero.)
2. Gain Adjustment—Set the DAC register to all "0's". Set R1 and R2 to zero. If the DAC output is greater than $+V_{REF}$, increase R2 until it reads $+V_{REF}$. If the DAC output is less than $+V_{REF}$, increase R1 until it reads $+V_{REF}$. This assumes that reference adjustment which would otherwise be preferred is not possible.

   Note that the bipolar gain resistors at FB2 and FB3 are precisely preset internal thin film resistors and their specification impact is included in the limits for "Gain Setting."

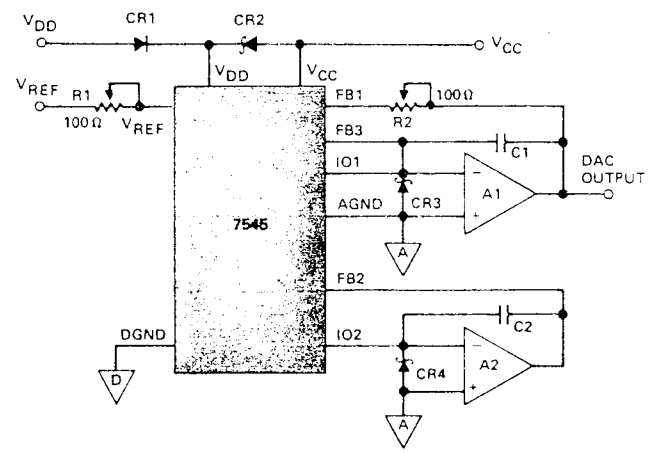


Figure 8. Bipolar Operation

Unipolar Operation (7546)

The 7546 general purpose converter includes the output buffer amplifiers A1 and A2 and an internal precision −10V reference. Each amplifier has been individually laser preadjusted for zero offset at +25°C. The feedback resistors (FB1, FB2 and FB3) have also been ratio matched to meet the gain tolerances specified.

Additional adjustment may be accomplished as shown in Figure 9 for unipolar operation.

1. Zero Offset Adjustment—The DAC output can be adjusted to read precisely zero for a code of 000000000000 by adjusting the summing current into or out of the summing junction (SUM) as shown.
2. Gain Adjustment—Set all bits to "1" and adjust the reference potentiometer until the DAC output reads −0.9976V.

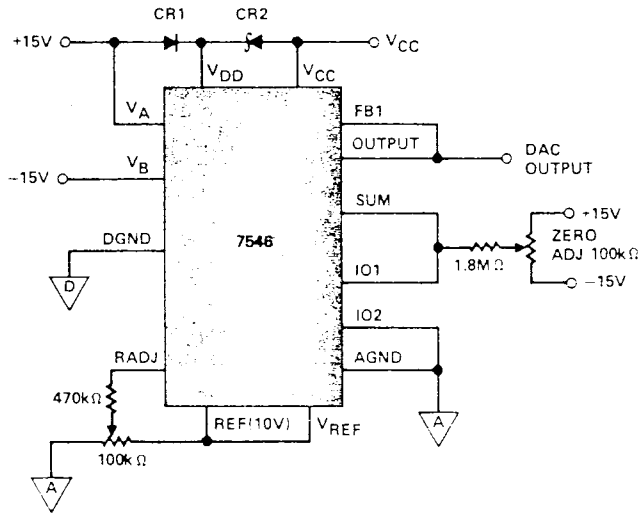


Figure 9. Unipolar Operation Utilizing Internal +10V Reference

Unipolar Two Quadrant Multiplying DAC (7546)

Series 7546 can utilize an external AC reference to accomplish two quadrant multiplication (bipolar reference × unipolar digital input) as shown in Figure 10.

1. Gain Adjustment—Set DB0 to DB11 to all "0's" and set R1 and R2 to zero ohms. If the DAC output voltage is greater than $+V_{REF}$, increase R1 until it reads precisely $+V_{REF}$. If the DAC output is less than $-V_{REF}$, increase R2 until it reads precisely $-V_{REF}$.

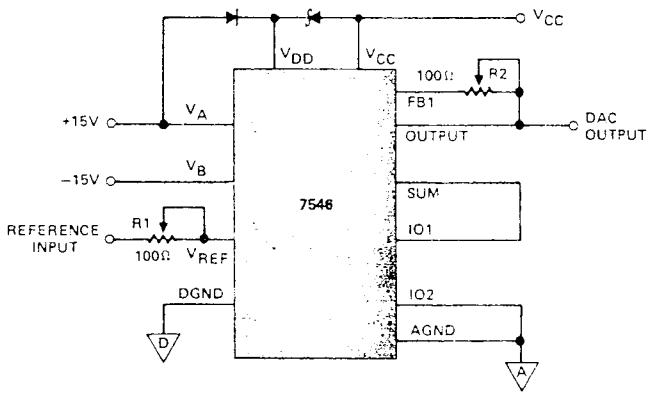


Figure 10. Unipolar Two Quadrant Multiplying DAC

Bipolar Operation (7546)

The circuit configuration for bipolar operation using the internal precision reference is shown in Figure 11.

1. Zero Offset Adjustment—The DAC output can be adjusted to read precisely zero for a code of 100000000000 by adjusting the current into or out of the summing junction (SUM) as shown.
2. Gain Adjustment—Set the DAC to all "0's" and adjust the reference adjust potentiometer until the DAC output reads +10.000V.

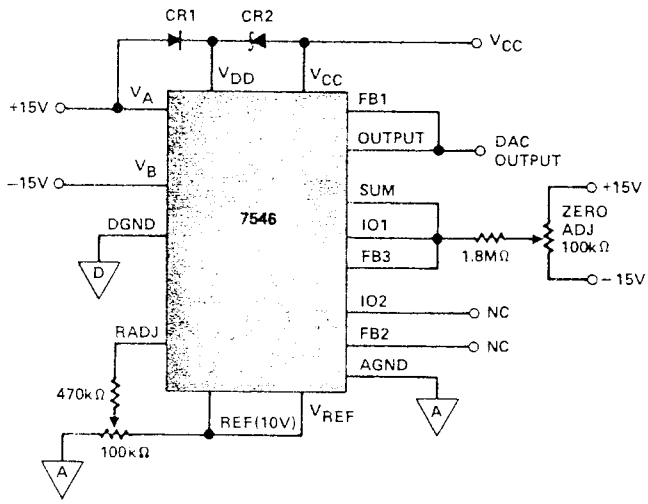


Figure 11. Bipolar Operation Using Internal +10V Reference

Four Quadrant Multiplying DAC (7546)

Series 7546 can operate as a four quadrant multiplier (bipolar digital input × bipolar reference) using an external reference as shown in Figure 12.

1. Gain Adjustment—Set DB0 to DB11 to all "0's" and set R1 and R2 to zero ohms. If the DAC output is greater than $-V_{REF}$, increase R1 until the output reads $+V_{REF}$. If the DAC output is less than $+V_{REF}$, increase R2 until it reads $-V_{REF}$.

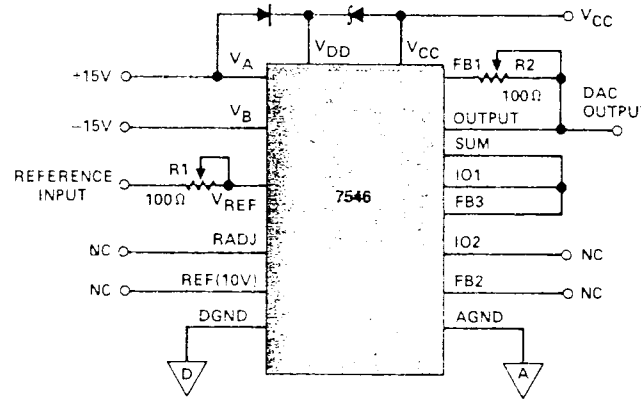
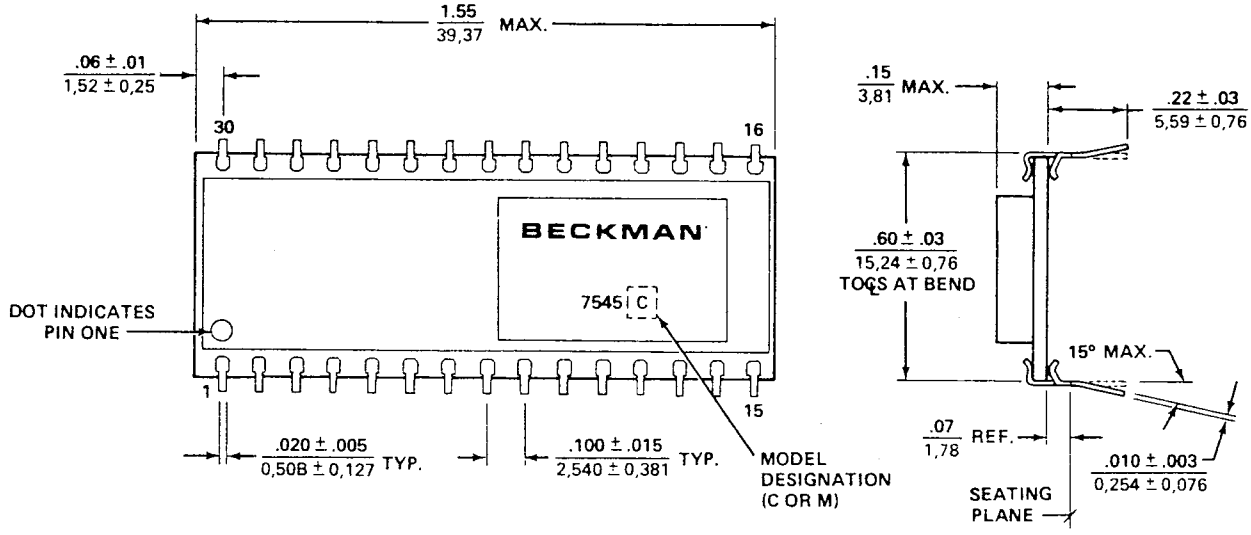
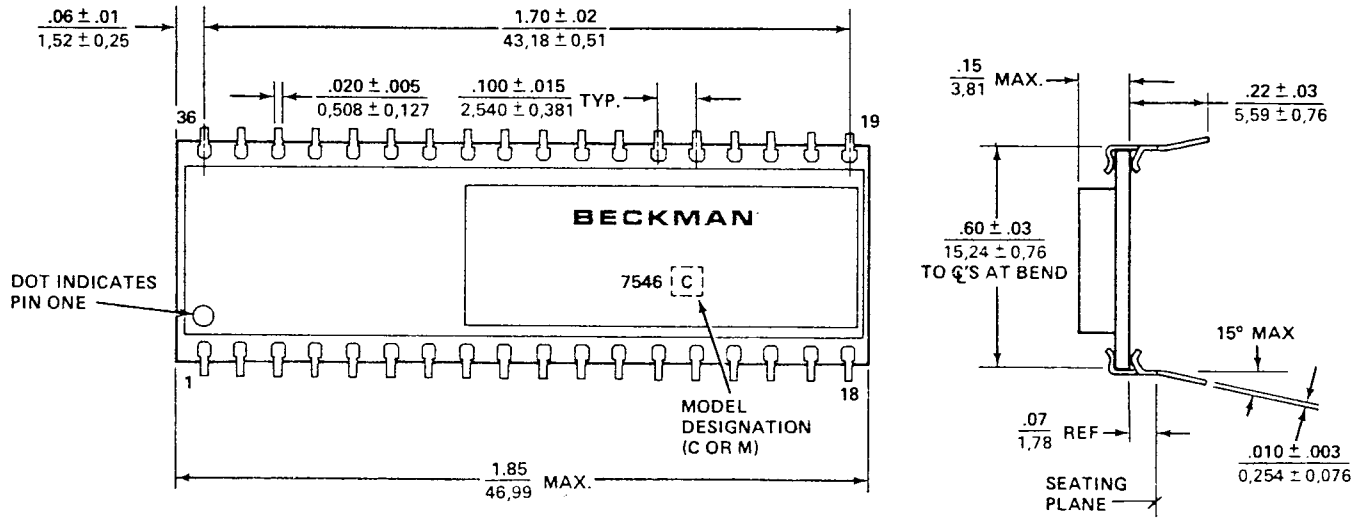


Figure 12. Four Quadrant Multiplying DAC

Outline Drawing—Series 7545



Outline Drawing—Series 7546



DIMENSIONS
INCH
(mm)

THIRD ANGLE
PROJECTION

Tolerances unless otherwise specified
± .005 inch and ±0.127 mm
angular ±2°

Metric equivalents, based upon 1 inch = 25.4 mm are rounded to the same number of decimal places as in the original English units and are provided for general information only

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