- Offers Carry Functions in a Compatible Form for Direct Connections to the ALU
- Cascadable to Perform Look-Ahead Across n-Bit Adders
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

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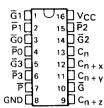
THE DESIGNATIONS							
ALTERNATIVE	DESIGNATIONS [†]	FUNCTION					
GO, G1, G2, G3 GO, G1, G2, G3		Carry Generate Inputs					
PO, P1, P2, P3	P0, P1, P2, P3	Carry Propagate Inputs					
Cn	Ĉ _n	Carry Input					
C _{n+x} , C _{n+y} , C _{n+z}	$\overline{C}_{n+x}, \overline{C}_{n+y}, \overline{C}_{n+z}$	Carry Outputs					
Ğ	Y	Carry Generate Output					
P X		Carry Propagate Output					
٧	Supply Voltage						
G	ND	Ground					

[†] Interpretations are illustrated in connection with the Function Tables for the 'HC181 and 'HC881.

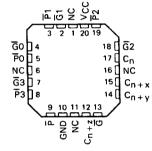
description

The 'HC182 look-ahead carry generators are capable of anticipating a carry across four binary adders or group of adders. They are cascadable to perform full look-ahead across n-bit adders.

SN54HC182 . . . J PACKAGE SN74HC182 . . . J OR N PACKAGE (TOP VIEW)



SN54HC182 . . . FH OR FK PACKAGE SN74HC182 . . . FH OR FN PACKAGE (TOP VIEW)



NC-No internal connection

This generator, when used in conjunction with the 'HC181 or 'HC881 Arithmetic Logic Unit ALU, provides high-speed carry look-ahead capability for any word length. The 'HC182 generates the look-ahead (anticipated carry) across a group of four ALUs. In addition, other carry look-ahead circuits may be employed to anticipate carry-across sections of four look-ahead packages up to n-bits.

The carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connections to the ALU. Reinterpretations of carry functions as explained on the 'HC181 and 'HC881 data sheet are also applicable to and compatible with the look-ahead generator. Logic equations for the 'HC182 are:

$$\begin{array}{ll} C_{n+x} = G0 + P0 \ C_n & \overline{C}_{n+x} = \overline{\frac{Y0 \ (X0 + C_n)}{(X0 + C_n)}} \\ C_{n+y} = G1 + P1 \ G0 + P1 \ P0 \ C_n & \overline{C}_{n+y} = \overline{\frac{Y1 \ [X1 + Y0 \ (X0 + C_n)]}{(X0 + C_n)}} \\ C_{n+z} = G2 + P2 \ G1 + P2 \ P1 \ G0 + P2 \ P1 \ P0 \ C_n & \overline{C}_{n+z} = \overline{\frac{Y2 \ (X2 + Y1 \ [X1 + Y0 \ (X0 + C_n)]}{(X3 + X2 + Y1)}} \\ \overline{C}_{n+z} = \overline{\frac{Y2 \ (X3 + Y2) \ (X3 + X2 + Y1)}{(X3 + X2 + Y1)}} \\ \overline{C}_{n+z} = \overline{\frac{Y2 \ (X3 + Y2) \ (X3 + X2 + Y1)}{(X3 + X2 + Y1)}} \\ \overline{C}_{n+z} = \overline{\frac{Y2 \ (X0 + C_n)}{(X1 + Y0 \ (X0 + C_n))}} \\ \overline{C}_{n+z} = \overline{\frac{Y2 \ (X0 + C_n)}{(X1 + Y0 \ (X0 + C_n))}} \\ \overline{C}_{n+z} = \overline{\frac{Y2 \ (X0 + C_n)}{(X1 + Y0 \ (X0 + C_n))}} \\ \overline{C}_{n+z} = \overline{\frac{Y2 \ (X0 + C_n)}{(X1 + Y0 \ (X0 + C_n))}} \\ \overline{C}_{n+z} = \overline{\frac{Y2 \ (X0 + C_n)}{(X1 + Y0 \ (X0 + C_n))}} \\ \overline{C}_{n+z} = \overline{\frac{Y2 \ (X0 + C_n)}{(X1 + Y0 \ (X0 + C_n))}} \\ \overline{C}_{n+z} = \overline{\frac{Y2 \ (X0 + C_n)}{(X1 + Y0 \ (X0 + C_n))}} \\ \overline{C}_{n+z} = \overline{\frac{Y2 \ (X0 + C_n)}{(X1 + Y0 \ (X0 + C_n))}} \\ \overline{C}_{n+z} = \overline{\frac{Y2 \ (X0 + C_n)}{(X1 + Y0 \ (X0 + C_n))}} \\ \overline{C}_{n+z} = \overline{\frac{Y2 \ (X0 + C_n)}{(X1 + Y0 \ (X0 + C_n))}} \\ \overline{C}_{n+z} = \overline{\frac{Y2 \ (X0 + C_n)}{(X1 + Y0 \ (X0 + C_n))}} \\ \overline{C}_{n+z} = \overline{\frac{Y2 \ (X0 + C_n)}{(X1 + Y0 \ (X0 + C_n))}} \\ \overline{C}_{n+z} = \overline{\frac{Y2 \ (X0 + C_n)}{(X1 + Y0 \ (X0 + C_n))}} \\ \overline{C}_{n+z} = \overline{\frac{Y2 \ (X0 + C_n)}{(X1 + Y0 \ (X0 + C_n))}} \\ \overline{C}_{n+z} = \overline{\frac{Y2 \ (X0 + C_n)}{(X1 + Y0 \ (X0 + C_n))}} \\ \overline{C}_{n+z} = \overline{\frac{Y2 \ (X0 + C_n)}{(X1 + Y0 \ (X0 + C_n))}} \\ \overline{C}_{n+z} = \overline{\frac{Y2 \ (X0 + C_n)}{(X1 + Y0 \ (X0 + C_n))}} \\ \overline{C}_{n+z} = \overline{\frac{Y2 \ (X0 + C_n)}{(X1 + Y0 \ (X0 + C_n))}} \\ \overline{C}_{n+z} = \overline{\frac{Y2 \ (X0 + C_n)}{(X1 + Y0 \ (X0 + C_n))}} \\ \overline{C}_{n+z} = \overline{\frac{Y2 \ (X1 + Y0 \ (X0 + C_n))}{(X1 + Y0 \ (X0 + C_n))}} \\ \overline{C}_{n+z} = \overline{\frac{Y2 \ (X1 + Y0 \ (X0 + C_n)}{(X1 + Y0 \ (X1 + C_n))}} \\ \overline{C}_{n+z} = \overline{\frac{Y2 \ (X1 + Y0 \ (X1 + C_n)}{(X1 + Y0 \ (X1 + C_n))}} \\ \overline{C}_{n+z} = \overline{\frac{Y2 \ (X1 + Y0 \ (X1 + C_n)}{(X1 + Y0 \ (X1 + C_n))}} \\ \overline{C}_{n+z} = \overline{\frac{Y2 \ (X1 + Y0 \ (X1 + C_n)}{(X1 + Y0 \ (X1 + C_n))}} \\ \overline{C}_{n+z} = \overline{\frac{Y2 \ (X1 + Y0 \ (X1 + C_n)}{(X1 + Y0 \ (X1 + C_n)$$

maximum ratings recommended operating conditions, and electrical characteristics

See Table IV, page 2-10.

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	FUNC	TION 1	ABLE	FOR G	OUT	PUT	
	INPUTS						
G3	Ğ2	Ğ1	Ğο	P3	P2	P1	OUTPUT Ĝ
L	X	Х	Х	Х	Х	X	L
Х	Ł	Х	X	L	X	Х	L
Х	Х	L	Х	L	L	х	Ĺ
Х	X	Х	L	L	L	L	L
	All	other	combi	nation	s		н

	FUNCTION TABLE FOR P OUTPUT							
L	INPUT	S		OUTPUT				
P3	P2	P1	PΟ	P				
L	L	L	L	L				
	All oth	er						
co	mbinat	ions		Н				

FUNCTION TABLE FOR C _{n+x} OUTPUT								
	INPUTS OUTPUT							
ĞΟ	Ρo	Cn	C _{n+x}					
L	X	X	Н					
×	L	н	н					
1	All other L							

FUNCTION TABLE C_{n+y} OUTPUT

		OUTPUT			
Ğ1	Ğ0	P1	P0	Cn	Cn+y
L	X	X	X	Х	Н
Х	L	L	X	Х	н
Х	X	L	L	н	Н
		All ot	her		
	cc	mbina	itions		L

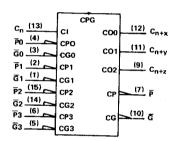
FUNCTION TABLE FOR Cn+2 OUTPUT

	OUTPUT						
G2	Ĝ1	ĞΟ	P2	P1	P0	Cn	Cn+z
L	Х	X	Х	X	Х	X	H
Х	L	X	L	Х	×	X	н
X	X	L	Ł	Ł	x	х	н
X	X	X	L	L	Ł	н	н
		All oth	er con	nbinati	ons		L

H = High-level, L = Low-level, X = irrelevant

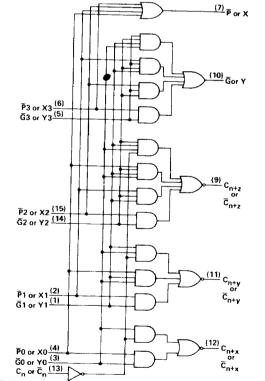
Any inputs not shown in a given table are irrelevant with respect to that output.

logic symbols (alternatives)



OR

logic diagram (positive logic)



CPG (12) C_{n+x} C_n (13) 1,2 Po -(4) 3,4 (11) G2/Z10 5 (3) Ğο **Z**3 1,2,4,6 (9) C_{n+z} P1 (2) 3,4,6 G4 (1) 5,6 Ğ1 **Z**5 (7) P (15) Ē2 G6 10,4,6,8 (14) G2 **Z**7 (10) G (6) P3 5,6,8 7,8 G8 G3_⁽⁵⁾

Pin numbers shown are for J and N packages only.