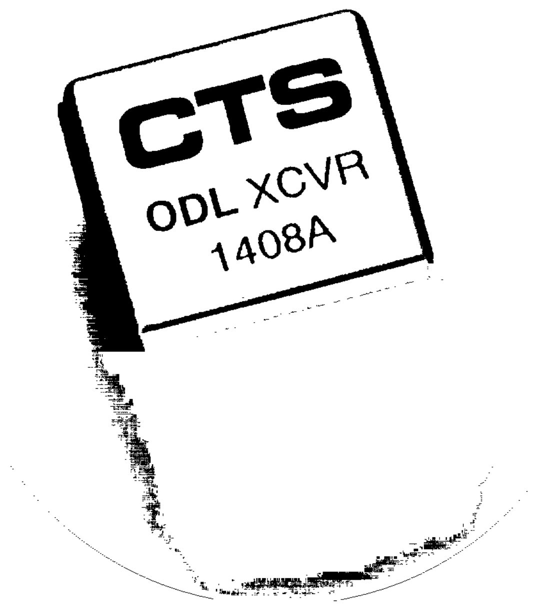
1408-Type ODL® Transceiver
Technical Data

Features

- Compliant LCF (low-cost FDDI) transceiver (1408B)
- Options for full spec FDDI and performance at OC-3 data rate (1408A)
- Flexible, compatible performance
  — ATM, FDDI, SONET (1408A)
  — Low-cost FDDI (LCF), ATM-OC3 (1408B)
  — ATM, *ESCON**, FC, SONET (1408N)
- Conforms to multisourced 9-pin SIP configuration
- SC duplex receptacle
- Low power dissipation
- Single +5 V power supply
- Low EMI/RFI emissions and susceptibility
- 100KH PECL logic
- Operational over temperature range 0°C to 70°C



The 1408-Type *ODL* Transceiver features high-speed performance in a multisourced 9-pin SIP.

Applications

- FDDI networks (1408A and 1408B)
- ATM, SONET OC-3 (1408A/N)
- Fibre channel, *ESCON* (1408N)
- Point-to-point links—CPU to CPU, CPU to disk/disk array, and CPU to peripheral

Description

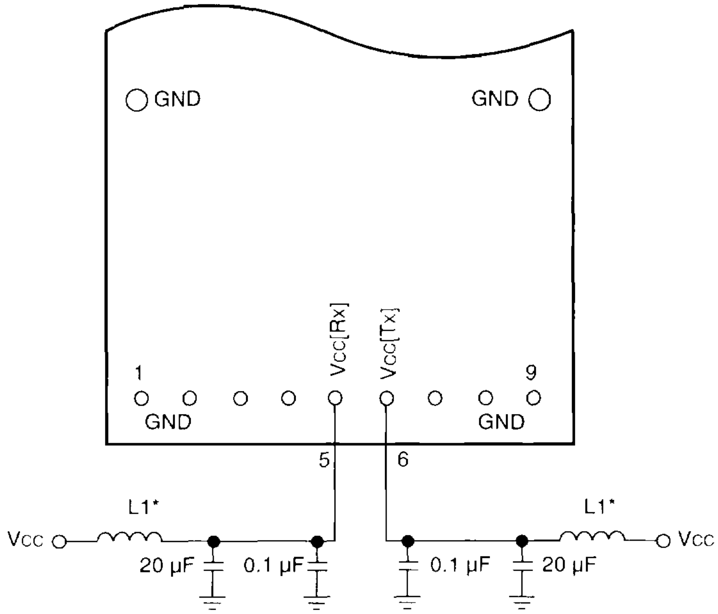
The electrical and optical parameters of the American National Standard Institute's ANSI T1E1 Specification for the asynchronous transfer mode (ATM) OC-3 data rate are met by the 1408A *ODL* Transceiver. The 1408A Transceiver operates at 156 Mbits/s over a typical distance of 2 km. The 1408N *ODL* Transceiver operates over data rates up to 275 Mbits/s. This device meets the ATM User Network Interface (UNI) Version 3.0 Specification for 8B-10B coded application. This flexibility makes the 1408-Type *ODL* Transceiver an ideal low-cost solution for ATM and SONET multimode applications. For short distances, the 1408B can provide a lower-cost solution for ATM OC-3 application. In addition, the 1408A Transceiver meets the ANSI X3T9.5 physical medium dependent (PMD) specification for Fiber Distributed Data Interface (FDDI).

The 1408B Transceiver also meets ANSI specifications for low-cost FDDI (LCF) compliant fiber-optic components. The LCF-PMD specification is a supplement to the original FDDI-PMD specification and provides for an optically interoperable, lower-cost, physically smaller interface for front-end, single attached station applications. The 1408B Transceiver operates at the data rates of 10 Mbits/s to 156 Mbits/s (NRZ) at a typical distance of 500 meters.

In addition to its ATM applications, the 1408N *ODL* Transceiver is suited both to *ESCON* applications and compliant to the 25-M6-LE-I multimode fiber interface specification as stated in the ANSI X3T9.3 Fibre Channel Standard.

**ESCON* is a trademark of International Business Machines Corporation.

Pin Information



* L1 — Ferrite bead; Fair-Rite Products Corp., Part Number 2743002111 or equivalent.

Figure 1. Pin Diagram (Top View)

Printed-Wiring Board Layout

As with any sensitive or high-speed electronic component, to obtain optimum performance from the transceiver, careful attention must be given to the printed-wiring board. Board layout is crucial for achieving rated performance. The routing of sensitive input traces relative to other components and signal lines must be considered in great detail. Data lines must be of controlled impedance and properly terminated to minimize reflections that might degrade performance. Power supply pins must be protected from noisy operating conditions by proper filtering.

Printed-Wiring Board

As a minimum, a double-sided printed-wiring board having a large ground plane on the component side, directly beneath the transceiver, should be utilized. In applications where a large number of other devices are included on the circuit card, a multilayer circuit board is preferred. This allows for the separation of power and ground connections, and provides isolation for sensitive traces from high-level signals that might couple to the sensitive inputs. In either case, the ideal approach is to have the ground plane as close to the transceiver as possible and to cover as much of the printed-wiring board as possible.

When laying out the PWB, note the location of the solder tabs, which attach the metal shield to the transceivers. These solder tabs are at ground potential. Therefore, there should be no topside metal or vias that are not at ground potential within the regions defined by the solder tabs (see Outline Diagram).

Layout Considerations

A fiber-optic receiver employs a very high-gain, wide-bandwidth, transimpedance amplifier. The amplifier detects and amplifies signal levels that are only nanoamperes in amplitude. Any unwanted signals that couple into the receiver circuitry cause a decrease in the receiver's sensitivity and can also degrade the performance of the receiver's signal detect indicators.

To minimize the coupling of unwanted noise into the receiver, route transmitter-input traces and other traces carrying high-level signals as far away as possible from the receiver pins. If wide separation of the receiver pins from other high-level signal lines is not possible, the receiver pins and traces connected to them should be shielded by placing a ground trace between the receiver's pins and connecting traces and other high-level signal paths.

Printed-Wiring Board Layout (continued)

Power Supply Filtering

Noise that couples into the transceiver through the power supply pins can also degrade device performance. Figure 1 shows the recommended power supply filtering for both the transmitter and receiver power supply pins. The 0.1 µF capacitors should be high-quality ceramic devices rated for RF applications. Place the capacitors as close as physically possible to the V_{CC} pins. The ideal situation is surface-mount capacitors mounted up against the power supply pins.

Data Lines

The signals on the data lines typically have rise and fall times on the order of 1 ns to 2 ns. If the data lines are not properly handled, the fast transitions cause EMI problems as well as electrical reflections and excessive ringing, which degrade the performance of the transceiver. When laying out the traces for the data lines, follow high-speed ECL design guidelines as described in the *Motorola MECL System Design Handbook*.

- All high-speed output lines must use controlled-impedance traces and have the termination impedance match the trace impedance. Controlled-impedance interruptions must be avoided (i.e., 90° bends, etc.), and paired lines (i.e., DATA and $\overline{\text{DATA}}$ should be of equal length.
- Each output line should be terminated at the end of the line and must have a bypass capacitor on the voltage side of the resistor for each termination resistor.
- Data and signal detect output lines should be as short and straight as possible and should be isolated from noise sources (and each other) to prevent noise from feeding back into the receiver.

Handling Precautions

Electrostatic Discharge

CAUTION: This device is susceptible to damage as a result of electrostatic discharge. Take proper precautions during both handling and testing. Follow guidelines such as JEDEC Publication No. 108-A (Dec. 1988).

Although protection circuitry is designed into the device, take proper precautions to avoid exposure to ESD.

CTS employs a human-body model (HBM) for ESD-susceptibility testing and protection-design evaluation. ESD voltage thresholds are dependent on the critical parameters used to define the model. A standard HBM (resistance = 1.5 kΩ, capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes. The 1408-Type Transceiver was tested to an ESD threshold of ±2000 V by using these parameters.

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{stg}	–40	100	°C
Lead Soldering Temperature/Time[1]	—	—	240/10	°C/s
Supply Voltage[2]	V_{CC}	0	6.5	V
Output Current[3]	I_O	—	50	mA
Input Voltage[4]	V_I	0	V_{CC} + 0.5	V
Differential Input Voltage	—	—	2.0	V

1. Applies to electrical pins only.
2. Measured from ground to V_{CC}.
3. From DATA and $\overline{\text{DATA}}$ outputs of receiver.
4. Voltage at DATA or $\overline{\text{DATA}}$ input terminals of transmitter measured from V_{CC}.

Optical/Electrical Characteristics

Table 1. 1408A and 1408B Transmitter Performance Specifications

The transceiver meets the below specifications over the following conditions: V_{CC} = 4.5 V to 5.5 V; T_A = 0 °C to 70 °C; complementary inputs.[1, 2]

Parameter	Symbol	Min[2]	Max[2]	Unit
Input Data Voltage:[3]				
Low	V_{IL}	–1.810	–1.475	V
High	V_{IH}	–1.165	–0.880	V
Input Current:				
Low[4]	I_{IL}	–0.1	—	mA
High[5]	I_{IH}	—	0.1	mA
Input Transition Time[6, 7]	t_I	0.5	3.0	ns
Power Supply Current	I_{CC}	—	140	mA
Data Rate (NRZ encoding)	DR	10	156	Mbits/s
Average Optical Power (BOL)[8, 9]				
1408A	P_O	–19.0	–14.0	dBm
1408B	P_O	–21.0	–14.0	dBm
Disable Power (input low)[10]	P_{OL}	—	–45.0	dBm
Dynamic Extinction Ratio[6, 11]	EXT_S	10.0	—	%
Output Rise Time[6, 12, 13]	t_R	—	3.5	ns
Output Fall Time[6, 12, 13]	t_F	—	3.5	ns
Optical Wavelength (center)[13]	λ_C	1270	1380	nm
Power Dissipation[14]	P_{DISS}	—	0.77	W
Data-dependent Jitter[15]	DDJ	—	0.6	ns p-p
Random Jitter[16]	RJ	—	0.7	ns p-p
Duty-cycle Distortion[16]	DCD	—	0.6	ns p-p

1. These specifications assume the use of both inputs with complementary input data. Similar performance can be achieved when driven single-endedly.
2. Minimum and maximum values are guaranteed over specified voltage and temperature ranges.
3. Measured from V_{CC} with a 50 Ω load to (V_{CC} – 2.0 V).
4. Measured at $V_{IL} = V_{IL,\ min}$.
5. Measured at $V_{IH} = V_{IH,\ max}$.
6. Measured with the FDDI-specified, halt-line-state input (12.5 MHz square wave).
7. Between 20% and 80% points.
8. Minimum value given at beginning-of-life (BOL) and from 0 °C to 70 °C ambient; 1 dB allowed for aging over 100,000 hours lifetime.
9. Measured average power coupled into 0.275 NA, 62.5/125 µm fiber.
10. The optical output power with a logic low at the input.
11. Ratio of the optical power in the logic low state to the optical power in the logic high state when the transmitter is transmitting valid data.
12. Between 10% and 90% points.
13. The optical rise time, fall time, center wavelength, and spectral width fit within the boundaries outlined in ANSI X3T9.5 PMD, Figure 5.1.
14. Maximum value specified with a 5.5 V power supply voltage.
15. Measured output jitter by using an input of 125 Mbits/s worst-case data pattern specified in FDDI PMD Appendix A, having negligible DDJ.
16. Measured with an input of 125 Mbits/s 1010 pattern having negligible DCD or random jitter.

Optical/Electrical Characteristics (continued)

Table 2. 1408N Transmitter Performance Specifications

The transceiver meets the below specifications over the following conditions: V_{CC} = 4.5 V to 5.5 V; T_A = 0 °C to 70 °C; complementary inputs.[1, 2]

Parameter	Symbol	Min[2]	Max[2]	Unit
Input Data Voltage:[3]				
Low	V_{IL}	–1.810	–1.475	V
High	V_{IH}	–1.165	–0.880	V
Input Current:				
Low[4]	I_{IL}	–0.1	—	mA
High[5]	I_{IH}	—	0.1	mA
Power Supply Current	I_{CC}	—	140	mA
Data Rate (NRZ encoding)	DR	—	275	Mbits/s
Average Optical Power (BOL)[6, 7]	P_O	–19.0	–14.0	dBm
Dynamic Extinction Ratio[8]	EXT_S	10	—	%
Output Rise Time[9, 10]	t_R	—	2.0	ns
Output Fall Time[9, 10]	t_F	—	2.2	ns
Optical Wavelength (center)[11]	λ_C	1270	1380	nm
Power Dissipation[12]	P_{DISS}	—	0.77	W
Spectral Width[11]	$\Delta\lambda$	—	200	nm
Random Jitter[13]	RJ	—	0.5	ns p-p
Duty-cycle Distortion[13]	DCD	—	0.6	ns p-p
Data-dependent Jitter[13]	DDJ	—	0.5	ns p-p

1. These specifications assume the use of both inputs with complementary input data. Similar performance can be achieved when driven single-endedly.
2. Minimum and maximum values are guaranteed over specified voltage and temperature ranges.
3. Measured from V_{CC} with a 50 Ω load to (V_{CC} – 2.0 V).
4. Measured at $V_{IL} = V_{IL,\,min}$.
5. Measured at $V_{IH} = V_{IH,\,max}$.
6. Minimum value given at beginning-of-life (BOL) and from 0 °C to 70 °C ambient; 1 dB allowed for aging over 100,000 hours lifetime.
7. Measured average power coupled into 0.275 NA, 62.5/125 µm fiber.
8. Ratio of the optical power in the logic low state to the optical power in the logic high state when the transmitter is transmitting valid data.
9. Between 10% and 90% points at 25 °C.
10. Specified at a 53.2 Mbits/s data rate.
11. The spectral width is a function of center wavelength as per Figure 26 in FC-PH.
12. Maximum value specified with a 5.5 V power supply voltage.
13. Measured output jitter as specified in Appendix A of FC-PH.

Optical/Electrical Characteristics (continued)

Table 3. 1408A and 1408B Receiver Performance Specifications

V_{CC} = 4.5 V to 5.5 V; T_A = 0 °C to 70 °C; complementary inputs.[1, 2]

Parameter	Symbol	Min[2]	Max[2]	Unit
Output Data Voltage:[3]				
Low	V_{OL}	−1.810	−1.620	V
High	V_{OH}	−1.025	−0.880	V
Current Drain on V_{CC}[4]	I_{CC}	—	105	mA
Data Rate (NRZ encoding)	DR	10	156	Mbits/s
Eyewidth[5]	EW	2.1	8.0	ns
Average Optical Sensitivity:				
125 Mbits/s[6]	P_I	—	−34.0	dBm
156 Mbits/s[7]	P_I	—	−32.0	dBm
Average Maximum Input Power[8]	P_{MAX}	—	−14.0	dBm
Optical Wavelength for Rated Sensitivity	λ	1270	1380	nm
Output Rise/Fall Time[9, 10]	t_R/t_F	0.5	2.5	ns
Power Dissipation, V_{CC}[11]	P_{DISS}	—	0.72	W
Output Signal Detect Voltage:[4, 12]				
Low	V_{FL}	−1.810	−1.620	V
High	V_{FH}	−1.025	−0.880	V
Signal Detect Assert Level (avg. power):				
Increasing Light Input[12]	S_{DAL}	−39.5	−29.0	dBm
Decreasing Light Input[12]	S_{DDL}	−41.0	−31.5	dBm
Signal Detect — Hysteresis[12]	HYS	1.5	—	dBm
Signal Detect Timing:				
Assert[13]	S_{DTA}	—	100	µs
Deassert[14]	S_{DTD}	—	350	µs
Duty-cycle Distortion[15]	DCD	—	0.4	ns p-p

1. Specifications assume the use of both outputs with complementary data. Similar performance can be achieved by using either output individually.
2. Minimum and maximum values are for the 1408A and are guaranteed over specified voltage and temperature ranges by using the bypass filter network in Figure 1.
3. Measured from V_{CC} with a 50 Ω load to (V_{CC} − 2.0 V).
4. For (V_{CC} − V_{EE}) max. The supply current (I_{CC}) does not include output load drive current.
5. During an 8 ns bit-period, eyewidth is the time span in which the bit error rate (BER) is less than 2.5 x 10^{-10}. Eyewidth is measured with a 125 Mbits/s optical input that uses the data pattern specified in Appendix A of the FDDI PMD. An average optical power of −32.5 dBm is used for the receiver. The input is coupled from a 0.275 NA, 62.5/125 µm fiber.
6. Average optical power coupled from a 0.275 NA, 62.5/125 µm fiber at 125 Mbits/s with a $2^7 - 1$ pseudorandom data pattern with a 50% duty cycle for a BER of 2.5 x 10^{-10} (optimum sensitivity with 0 eyewidth).
7. Average optical power coupled from a 0.275 NA, 62.5/125 µm fiber at 156 Mbits/s with a $2^7 - 1$ pseudorandom data pattern with a 50% duty cycle for a BER of 2.5 x 10^{-10} (see Figure 2 for relative shift in sensitivity over data rate).
8. The maximum average input power corresponds to a minimum output eyewidth of 2.1 ns at 2.5 x 10^{-10} BER.
9. Specified at a 125 Mbits/s data rate.
10. Between the 20% and 80% points with a 50 Ω load to (V_{CC} − 2.0 V).
11. With a +5.5 V power supply, 50% duty cycle, and logic outputs terminated in 50 Ω to (V_{CC} − 2.0 V).
12. Signal detect output is logic 1 for light input levels above the indicated switching level and logic 0 for input levels below the indicated switching level. Whenever the signal detect is asserted, the BER of the data outputs is less than or equal to 0.01.
13. The value specified is the maximum time it takes the signal detect to assert after a step increase in the optical power into the receiver. Measured with the data pattern specified in Appendix A of the FDDI PMD.
14. The value specified is the maximum time it takes the signal detect to deassert after a step decrease in the optical power into the receiver. Measured with the data pattern specified in Appendix A of the FDDI PMD.
15. Measured with an input 1010, 125 Mbits/s data pattern having negligible duty-cycle distortion.

Optical/Electrical Characteristics (continued)

Table 4. 1408N Receiver Performance Specifications

The transceiver meets the below specifications over the following conditions: V_{CC} = 4.5 V to 5.5 V; T_A = 0 °C to 70 °C; complementary outputs.[1, 2]

Parameter	Symbol	Min[2]	Max[2]	Unit
Output Data Voltage:[3]				
Low	V_{OL}	–1.810	–1.620	V
High	V_{OH}	–1.025	–0.880	V
Current Drain on V_{CC}[4]	I_{CC}	—	150	mA
Data Rate (NRZ encoding)	DR	156	275	Mbits/s
Eyewidth[5]	EW	1.88	3.76	ns
Average Optical Sensitivity[6]	P_I	—	–29.0	dBm
Average Maximum Input Power[7]	P_{MAX}	—	–14.0	dBm
Optical Wavelength for Rated Sensitivity	λ	1270	1380	nm
Output Rise Time[8, 9]	t_R	0.5	2.5	ns
Output Fall Time[8, 9]	t_F	0.5	2.5	ns
Power Dissipation, V_{CC}[10]	P_{DISS}	—	0.88	W
Signal Detect Assert Level (avg. power): Increasing Light Input	S_{DAL}	–39.5	–29.0	dBm
Signal Detect Deassert Level (avg. power): Decreasing Light Input[11]	S_{DDL}	–41.0	–31.5	dBm
Signal Detect: Hysteresis[11]	HYS	1.5	—	dBm

1. Specifications assume the use of both outputs with complementary data. Similar performance can be achieved by using either output individually.
2. Minimum and maximum values are guaranteed over specified voltage and temperature ranges using bypass filter network (Figure 1).
3. Measured from V_{CC} with a 50 Ω load to (V_{CC} – 2.0 V).
4. For (V_{CC} – V_{EE}) max. The supply current (I_{CC}) does not include output load drive current.
5. During an 3.76 ns bit-period, eyewidth is the time span in which the bit error rate (BER) is less than 1 x 10^{-12}. Eyewidth is measured with a 266 Mbits/s optical input that uses a $2^7 - 1$ PRBS data pattern. An average input optical power of –29.0 dBm is used for the receiver. The input is coupled from a 0.275 NA, 62.5/125 µm fiber.
6. Average optical power coupled from a 0.275 NA, 62.5/125 µm fiber at 266 Mbits/s with a $2^7 - 1$ pseudorandom data pattern with a 50% duty cycle for a BER of 1.0 x 10^{-12} (see Figure 2 for relative shift in sensitivity vs. data rate).
7. The maximum average input power corresponds to a minimum ouput eyewidth 1.88 ns at 1 x 10^{-12} BER.
8. Specified at a 53.2 Mbits/s data rate.
9. Between the 10% and 90% points with a 50 Ω load to (V_{CC} – 2.0 V).
10. With a +5.5 V power supply, 50% duty cycle, and logic outputs terminated in 50 Ω to (V_{CC} – 2.0 V).
11. Signal detect output is logic 1 for light input levels above the indicated switching level and logic 0 for input levels below the indicated switching level. Whenever the signal detect is asserted, the BER of the data outputs is less than or equal to 0.01.

Characteristic Curve

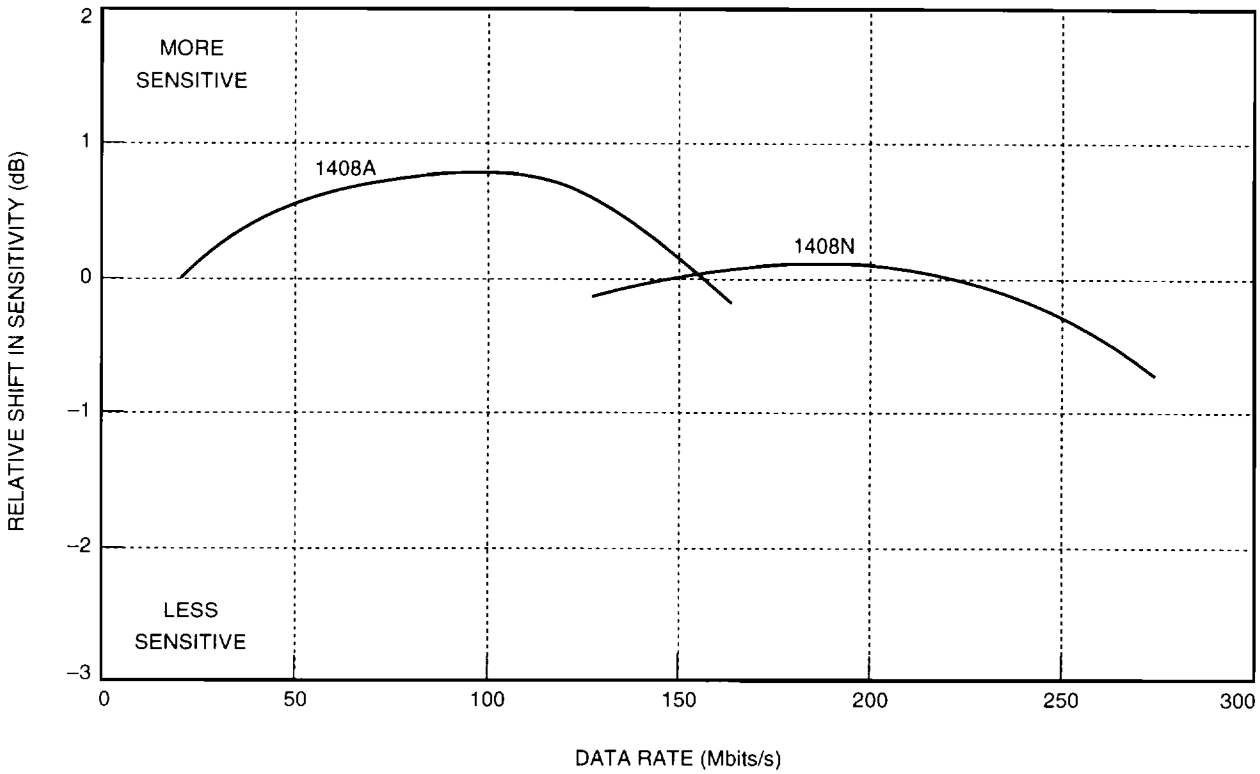


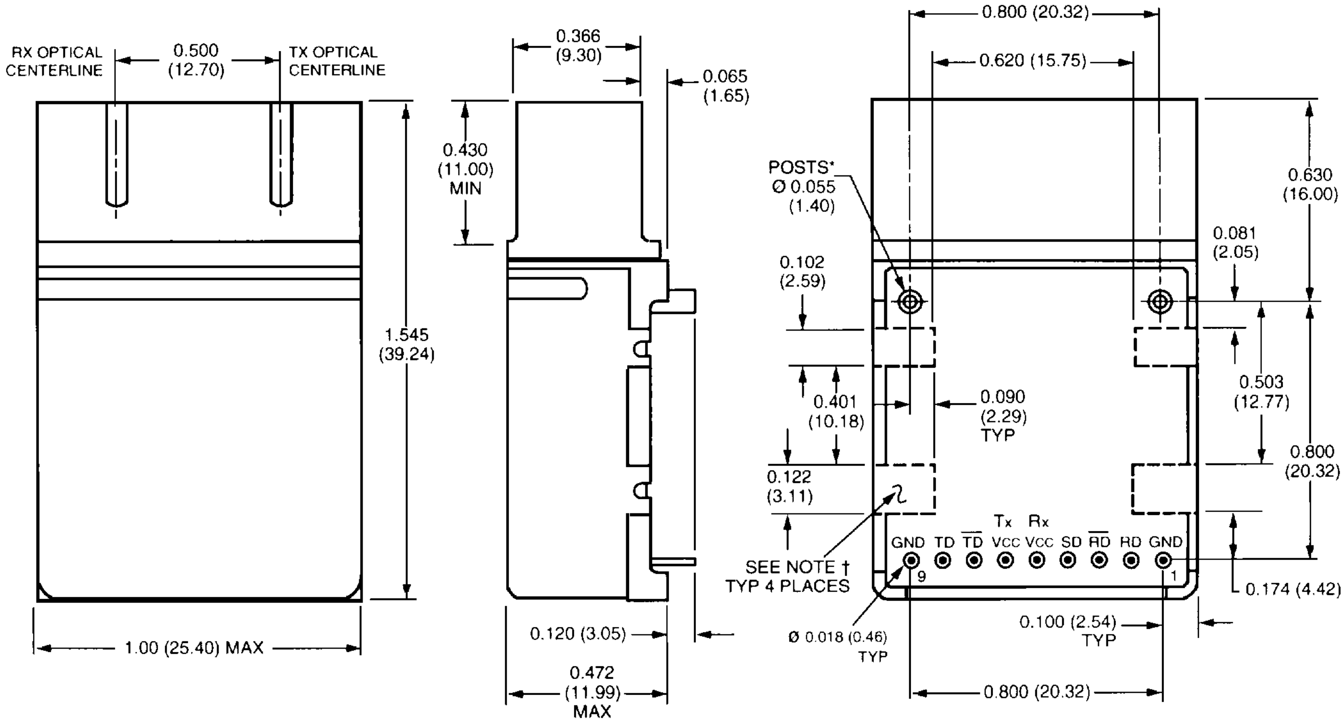
Figure 2. Relative Shift in Sensitivity vs. Data Rate

Outline Diagram

Dimensions are in inches and (millimeters).

All dimensions are reference unless tolerances are specified.

Top View **Side View** **Bottom View**



* Posts should be connected to circuit-board ground plane. The two mounting posts and pins 1 and 9 are internally connected together. The mounting posts and leads have a solder finish.

† There should be no open metallization patterns on the area of the board beneath the outlined transceiver solder tabs.

Ordering Information

Table 5. Device Information

Description	Device Code	Comcode
Full-Spec FDDI Transceiver	1408A	106761810
LCF (low-cost FDDI) Transceiver	1408B	106761828
ODL Transceiver	1408N	106993199

Table 6. Documentation Information

Document Title	Document Number
Power Margin Analysis	TN89-004LWP
Using the *ODL*/FDDI Lightwave Data Link Evaluation Board	TN89-009LWP
Cleaning Fiber-Optic Assemblies	TN92-010LWP
ODL 200 Lightwave Data Link with Flag	DS89-137LWP
ODL 125 Series II Lightwave Data Links	DS92-081LWP
Reliability Assessment: *ODL* 200 Lightwave Data Links	OT89-069LWP

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U.S.A., EUROPE, ASIA PACIFIC:
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JAPAN:
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Tel. 81-3-5472-6201, Fax 81-3-5472-6234

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