YAMAHA LSI

PRELIMINARY
('94.10.18)

YSS238

I²C Bus Converter
(I2CC)

■ OUTLINE

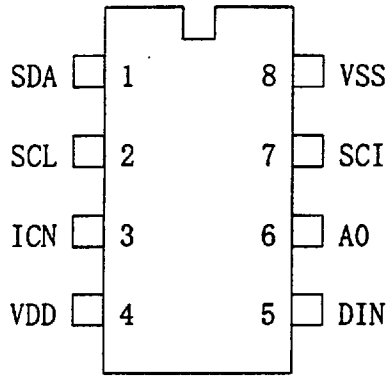
The YSS238 is an I²C bus converter LSI which connects I²C bus to the YAMAHA digital audio signal processor LSIs such as YM3428(SPB), YM7128B(SP2), YM7306C(DPLD), YSS205B (KP), YSS215(AVSP), YSS216B(KP2), YSS220(SP3), YSS231(GE).
The YSS238 converts I²C bus signals to the microprocessor interface signals of above YAMAHA digital audio signal processor LSIs.

■ FEATURES

- Data receiving from I²C bus.
  - starting condition detection
  - slave address and R/W detection
  - stopping condition detection
  - reception data.
- Returns acknowledge bit by one byte to conform receiving data.
- Outputs register address and data of YAMAHA digital audio signal processor LSIs by inputing clock from SCL line of I²C bus.
- Maximum 400kbps reception by high speed mode
- The power supply to the YSS238 and connecting YAMAHA digital audio signal processor LSIs can be stopped, while the master microprocessor is operating.
- 5V single power supply, Si-gate CMOS process.
- 8-pin plastic DIP.

NOTE) Purchase of I²C components of YAMAHA Corporation conveys a license under the Philips I²C patent rights to use these compornents in an I²C system, provided that the system conforms to the I²C standard specification as defined by Philips.

■ PIN CONFIGURATION



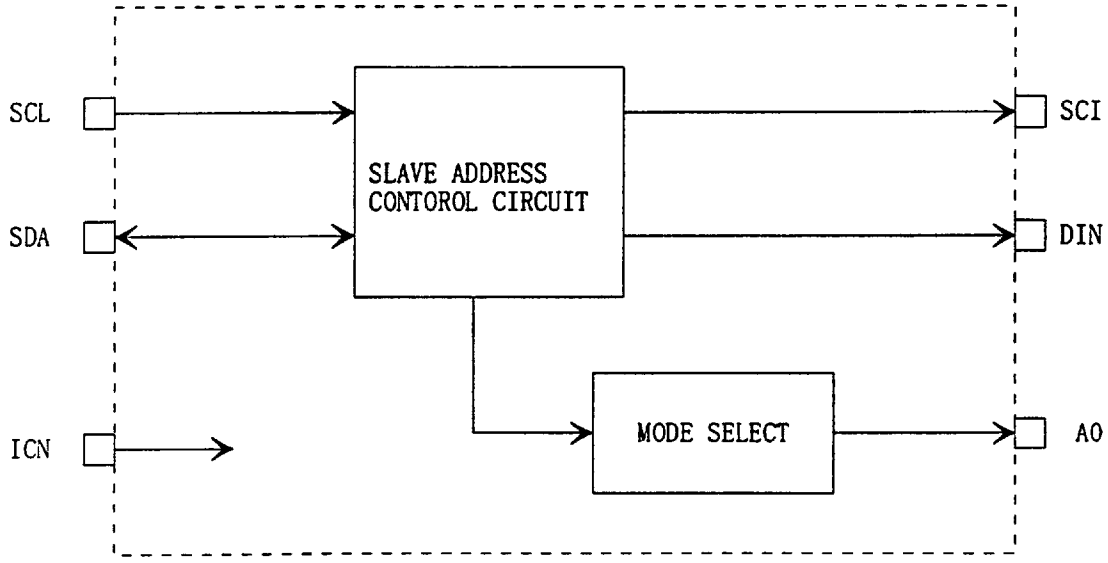
Top View

■ PIN FUNCTION

No.	Name	I/O	Function
1	SDA	Is/OD	I^2C interface SDA line
2	SCL	I	I^2C interface SCL line
3	ICN	I+	Reset input
4	VDD	-	Power supply
5	DIN	O	Microprocessor interface serial data
6	A0	O	Microprocessor interface chip select/word clock
7	SCI	O	Microprocessor interface serial clock
8	VSS	-	Ground

注) I+: Input terminal with pulled-up resistor
OD: Open drain output termimnal
s: Schmidt input terminal

■ BLOCK DIAGRAM

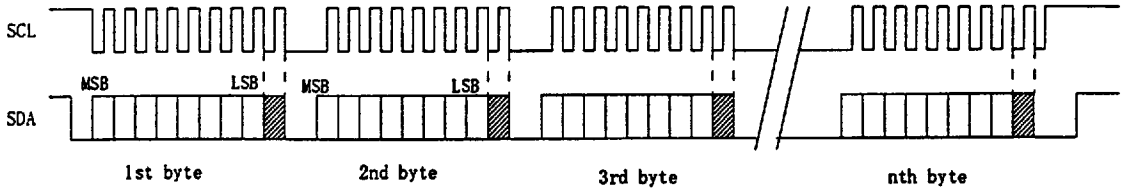


■ FUNCTION DESCRIPTION

1. I^2C interface SCL, SDA

1 – 1. I^2C format signal

Input the data in the following format from I^2C bus.



The acknowledge bit(slant line) is returned to the I^2C bus after each byte data reception.

1 – 2. Data transfer

● 1st byte

MSB	B6	B5	B4	B3	B2	B1	LSB
Slave address							'0'

MSB~B1 : Set the exclusive slave address of YSS238 by '*******'.

● 2nd byte

MSB	B6	B5	B4	B3	B2	B1	LSB
Don't care							MODE

LSB : Mode select
'0' : MODE0
'1' : MODE1

Mode setting is different by microprocessor interface format of the connecting YAMAHA digital audio signal processor LSIs.

MODE	YAMAHA digital audio signal processor LSI
MODE0	YM3428, YM7128B, YM7306C, YSS215
MODE1	YSS205B, YSS216B, YSS220, YSS231

● 3rd and following byte

When the input slave address corresponds with the YSS238's, the data input in 3rd and following bytes are directly output from the DATA terminal.
Set the MSB or LSB first data according to the microprocessor interface format of the connecting YAMAHA digital audio signal processors.

MSB first	YM3428, YM7128B
LSB first	YM7306C, YSS205B, YSS215, YSS216B, YSS220, YSS231

● Dummy data

Mode0 LSIs(YM3428, YM7128B, YM7306C, YSS215) require 1~3 clocks after the last data. Input another one byte (the data is " don't care ") after the last data byte.

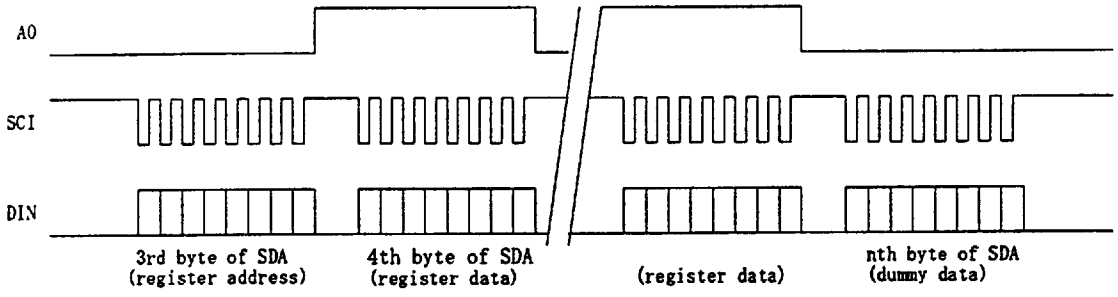
1 – 3. Acknowledge bit

After receiving each byte, acknowledge bit is returned to the I^2C SDA line.

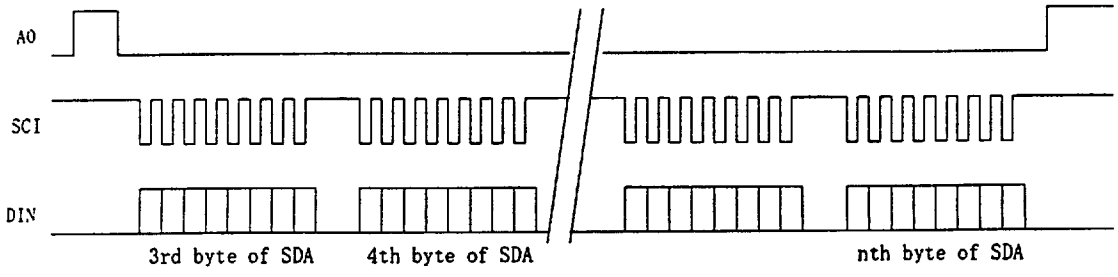
'0' : Receiving data is "Success" (when the YSS238 exclusive slave address is input).
'1' : Receiving data is "Failure".

2. Microprocessor interface signal output AO, SCI, DIN

2 – 1. MODE0



2 – 2. MODE1



3. Initial clear ICN

The YSS238 requires initial clear when turning on the power.

Note) The specifications of this product are subject to improvement change without prior notice.

AGENCY

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