T-51-10-12

October 1989
PRELIMINARY

Micro Linear

ML2233

μP Compatible 12-Bit Plus Sign A/D Converter with Sample and Hold

GENERAL DESCRIPTION

The ML2233 is a member of Micro Linear's 12-bit plus sign CMOS A/D converter family utilizing a self calibrating algorithmic technique. The sample-and-hold, incorporated on the ML2233, has a differential input for noise immunity and power supply rejection. All errors of the sample-and-hold are accounted for in the analog-to-digital converter's accuracy specification.

The ML2233B has a maximum non-linearity error over temperature of 0.012% of full scale, and the ML2233C has a maximum non-linearity error over temperature of 0.024% of full scale.

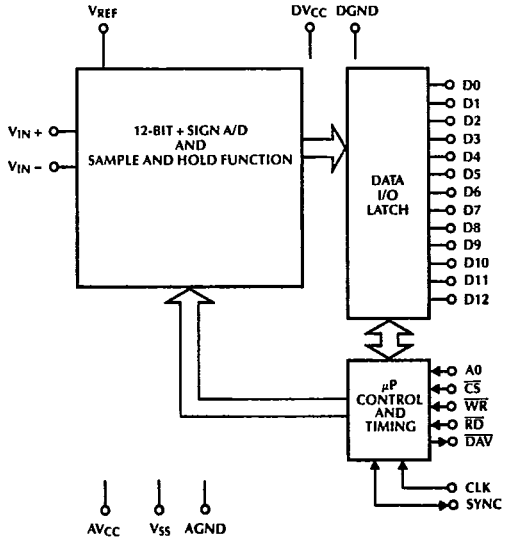
Designed to interface to a 16-bit microprocessor bus without additional components, the ML2233 outputs the 13-bit data result in one word. Data format is 2's complement. All digital signals are fully TTL and CMOS compatible.

For interfacing to an 8-bit microprocessor bus the ML2230 provides a 13-bit data result in two 8-bit bytes.

FEATURES

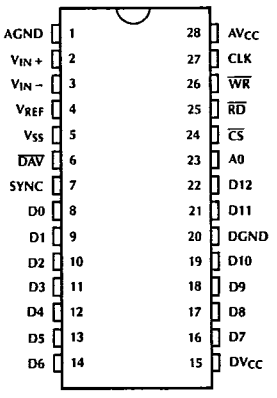
- Resolution 12-bits + sign
- Conversion time (including S/H acquisition) 31.5μs max
- Sample and hold acquisition 2.3μs max
- Non-linearity error ±1/2LSB and ±1LSB max
- Low harmonic distortion 0.01%
- No missing codes
- Self calibrating—maintains accuracy over time and temperature
- Inputs withstand |7V| beyond supplies
- Data transfer options—interrupt, DMA, or polling
- 13-bit result for 16-bit bus interface
- 0°C to 70°C, −40°C to +85°C temperature range
- Standard 28-pin DIP or 28-pin PCC

BLOCK DIAGRAM



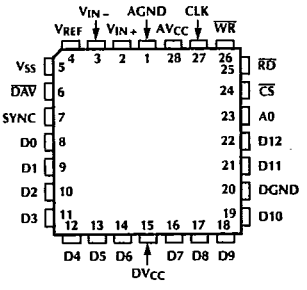
PIN CONNECTIONS

ML2233
28-PIN DIP



TOP VIEW

ML2233
28-PIN PCC



TOP VIEW

T-51-10-12

PIN DESCRIPTION

PIN NO.	NAME	FUNCTION
1	AGND	Analog ground.
2	$V_{IN}+$	Positive differential analog input; range = $V_{SS} \le V_{IN}+ \le AV_{CC}$, $\lvert(V_{IN}+)-(V_{IN}-)\rvert \le V_{REF}$.
3	$V_{IN}-$	Negative differential analog input; range = $V_{SS} \le V_{IN}- \le AV_{CC}$, $\lvert(V_{IN}+)-(V_{IN}-)\rvert \le V_{REF}$.
4	V_{REF}	Voltage reference input; referenced to analog ground.
5	V_{SS}	Negative power supply; decouple to AGND.
6	$\overline{DAV}$	Data available; indicates a conversion has completed and data is available or calibration completed.
7	SYNC	In the slave mode, SYNC is a positive edge triggered input used to start aconversion. In master mode, SYNC is an output and indicates conversion start.
8	D0	Bidirectional data bit.
9	D1	Bidirectional data bit.
10	D2	Bidirectional data bit.
11	D3	Bidirectional data bit.
12	D4	Bidirectional data bit.
13	D5	Bidirectional data bit.
14	D6	Bidirectional data bit.
15	DV_{CC}	Digital power supply.
16	D7	Bidirectional data bit.
17	D8	Bidirectional data bit.
18	D9	Bidirectional data bit.
19	D10	Bidirectional data bit.
20	DGND	Digital ground.
21	D11	Bidirectional data bit.
22	D12	Bidirectional data bit.
23	A0	Address for the microprocessor interface to access registers.
24	$\overline{CS}$	Chip select; enables writing to or reading from.
25	$\overline{RD}$	Read; enables ML2233 to drive data bus.
26	$\overline{WR}$	Write; allows writing into the registers.
27	CLK	Clock input. Driven with an external clock or crystal referenced to DGND. The crystal must be parallel resonant with minimum capacitive loading. (i.e., no bypass caps should be used and leads should be kept short.)
28	AV_{CC}	Positive analog power supply. Decouple to AGND. Tie to DV_{CC} from same power supply.

2

ABSOLUTE MAXIMUM RATINGS
(Note 1)

Supply Voltages (AV_{CC} and DV_{CC}) 6.0V
Negative Supply Voltage (V_{SS}) ..... −6.0V
Voltage at Analog Inputs ..... V_{SS} − 7V to AV_{CC} + 7V
Voltage at V_{REF} ..... V_{SS} − 7V to AV_{CC} + 7V
Input Current per Digital Pin ..... ±10mA
Input Current at Analog Inputs ..... ±20mA
Storage Temperature Range ..... −65°C to +150°C
Package Dissipation @ 25°C 875mW
Lead Temperature (soldering, 10 seconds)
- Dual-In-Line Package (Molded) ..... 260°C
- Dual-In-Line Package (Ceramic) ..... 300°C
- Molded PCC Package
  - Vapor Phase (60 sec.) ..... 215°C
  - Infrared (15 sec.) ..... 220°C

OPERATING CONDITIONS (Note 2)

Temperature Range ..... $T_{MIN} \le T_A \le T_{MAX}$
- ML2233BIJ, ML2233CIJ ..... −40°C to +85°C
- ML2233BCP, ML2233CCP, ML2233BCQ, ML2233CCQ ..... 0°C to 70°C

Supply Voltage (AV_{CC} and DV_{CC}) ..... $4.5V_{DC}$ to $6.0V_{DC}$
Negative Supply Voltage (V_{SS}) ..... $-4.5V_{DC}$ to $-6.0V_{DC}$
Reference Voltage (V_{REF}) 2.60V

ELECTRICAL CHARACTERISTICS

The following specifications apply for $AV_{CC} = DV_{CC} = 5V \pm 5\%$, $V_{SS} = -5V \pm 5\%$, $V_{REF} = 2.500V$, $V_{IN}- = AGND$, $V_{IN+} = -2.5V$ to $+2.5V$, $T_A = T_{MIN}$ to T_{MAX} unless otherwise specified.

PARAMETER	NOTES	CONDITIONS	ML2233BIJ, ML2233CIJ MIN	ML2233BIJ, ML2233CIJ TYP (NOTE 3)	ML2233BIJ, ML2233CIJ MAX	ML2233BCP, ML2233CCP ML2233BCQ, ML2233CCQ MIN	ML2233BCP, ML2233CCP ML2233BCQ, ML2233CCQ TYP (NOTE 3)	ML2233BCP, ML2233CCP ML2233BCQ, ML2233CCQ MAX	UNITS
Converter Characteristics									
Linearity Error ML2233BXX ML2233CXX	4	$f_{CLK} = 1 \le 7MHz$			 ±1/2 ±1			 ±1/2 ±1	 LSB LSB
Unadjusted Zero Error ML2233BXX ML2233CXX	4				 ±1 ±2			 ±1 ±2	 LSB LSB
Unadjusted Positive and Negative Full-Scale Error ML2233BXX ML2233CXX	5				 ±1 ±2			 ±1 ±2	 LSB LSB
Zero Error Temperature Coefficient				0.5			0.5		ppm/°C
Gain Temperature Coefficient				10			10		ppm/°C
Common Mode Rejection	5, 6		80			80			dB
Analog Input Source Resistance	5				2			2	kΩ
Analog Input Range	4	$V_{IN}+$ Referred to $V_{IN}-$	$-V_{REF}$		$+V_{REF}$	$-V_{REF}$		$+V_{REF}$	V
Analog Input Leakage Current	4				100			100	nA
Voltage Reference Input Source Impedance	5				0.5			0.5	kΩ
Reference Input Leakage Current	4				100			100	nA
Digital and DC Characteristics									
Power Supply Current AI_{CC}, Analog V_{CC} DI_{CC}, Digital V_{CC} I_{SS}, V_{SS}	4			 30 10 18	 50 30		 30 10 18	 50 30	 mA μA mA
Power Supply Rejection AV_{CC} V_{SS} 	7	 DC DC to 25kHz DC DC to 25kHz		 80 50 80 50			 80 50 80 50		 dB dB dB dB
V_{ILCLK}, Clock Input Low Voltage	4				0.8			0.8	V
V_{IHCLK}, Clock Input High Voltage	4		3.5		AV_{CC}	3.5		AV_{CC}	V
I_{L1}, Input Leakage Current (CLK)	4	$AGND \le V_{IN} \le AV_{CC}$			±200			±200	μA
V_{IL}, Input Low Voltage	4				0.8			0.8	V
V_{IH}, Input High Voltage	4		2.0		DV_{CC}	2.0		DV_{CC}	V
V_{OL}, Output Low Voltage	4	$I_{OL} = 2.0mA$			0.45			0.45	V
V_{OH}, Output High Voltage	4	$I_{OH} = -400\mu A$	2.4			2.4			V
I_L, Input Leakage Current (except CLK)	4	$AGND \le V_{IN} \le AV_{CC}$			±10			±10	μA
I_{Hi-Z}, Output Leakage Current (D0–D12)	4	$\overline{RD} = \overline{CS} = V_{IH}$			±10			±10	μA
C_i, Input Capacitance (all digital inputs)				10			10		pF
C_o, Output Capacitance (outputs D0 to D12, SYNC, and $\overline{DAV}$)				10			10		pF

T-51-10-12

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	NOTES	CONDITIONS		MIN	TYP (NOTE 3)	MAX	UNITS
AC Electrical Characteristics (Note 8)								
t_C	Conversion Time	4,9	f_{CLK} = 7.0MHz (CLK Mode = 0)		31.5			µs
	Sample and Hold Acquisition	4,9	f_{CLK} = 7.0MHz (CLK Mode = 0)				2.3	µs
f_{CLK0}	Clock Frequency	5,9	Crystal (CLK Mode = 0)		3		7	MHz
			Driven (CLK Mode = 0)		1		7	MHz
t_{CLK0}	Clock Width	5,9	Driven (CLK Mode = 0)	High	50			ns
				Low	50			ns
f_{CLK1}	Clock Frequency	5,10	Driven (CLK Mode = 1)		0.5		(Note 11)	MHz
t_{CLK1}	Clock Width	5,10	Driven (CLK Mode = 1)	High	125			ns
				Low	125			ns
t_{AD}	Address Stable to Valid Data	4			150			ns
t_{AR}	Address Stable Before Read	4			0			ns
t_{RA}	Address Hold After Read	4			0			ns
t_{RR}	Read Pulse Width	4			150			ns
t_{RD}	Read Access	4					150	ns
t_{1Z}, t_{0Z}	Data Read to Hi-Z	4			0		50	ns
t_{RV}	Recovery Between Two Reads or Writes	5			250			ns
t_{RDCK}	Read to Clock Setup Time	5,12			40			ns
t_{AW}	Address Stable Before Write	4			0			ns
t_{WA}	Address Hold After Write	4			0			ns
t_{WW}	Write Pulse Width	4			150			ns
t_{DW}	Data Setup Before Write Trailing Edge	4			100			ns
t_{WD}	Data Hold After Write Trailing Edge	4			0			ns
t_{WRCK}	Write to Clock Setup Time	5,12			40			ns
t_{CKDAV}	Clock to DAV Assert	5,13	C_L = 50pF			120	180	ns
t_{SYNCCK}	SYNC Input to Clock Setup	5,12			40			ns
t_{SYNCN}	SYNC Input Width	5	(CLK Mode = 0)		6			$1/f_{CLK0}$
			(CLK Mode = 1)		3			$1/f_{CLK1}$
t_{CKSYNC}	External Clock to SYNC Output Delay	5,13	C_L = 50pF			150	200	ns
t_{SYNCO}	SYNC Output Pulse Width	5,13	(CLK Mode = 0)				8	$1/f_{CLK0}$
			(CLK Mode = 1)				4	$1/f_{CLK1}$
t_{WRDAV}	Write Reg1 to DAV Rising Edge	5,14	C_L = 50pF				100	ns
t_{RDDAV}	Read Reg0 to DAV Rising Edge	5,15	C_L = 50pF				150	ns
t_r, t_f	Rise and Fall		All Inputs				25	ns

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.
Note 2: 0°C to 70°C and −40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling or by correlation with worst-case test conditions.
Note 3: Typicals are parametric norm at 25°C.
Note 4: Parameter guaranteed and 100% production tested.
Note 5: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.
Note 6: Common mode rejection is the ratio of the change in zero error to the change in common mode input range.
Note 7: Power supply rejection is the ratio of the change in zero error to the change in power supply voltage.
Note 8: All parameters measured from 0.8V to 2.0V, C_L = 100pF.
Note 9: CK1X bit in control register = 0.
Note 10: CK1X bit in control register = 1.
Note 11: Maximum frequency is $1/t_{CLK1}$ (high) + t_{CLK1} (low) + rise + fall times, which must be ≤ 3.5MHz.
Note 12: Setup time required for synchronous start of conversion.
Note 13: In CLK mode = 0 (CK1X bit in control register = 0) start of conversion will occur at specified time; or time plus one f_{CLK0} period (see Figure 5).
Note 14: Writing a control register bit 0 with a one will acknowledge the DAV condition and de-assert DAV output.
Note 15: In start mode = 1, a read from location "0" will start the next conversion and de-assert the DAV output.

TIMING DIAGRAMS

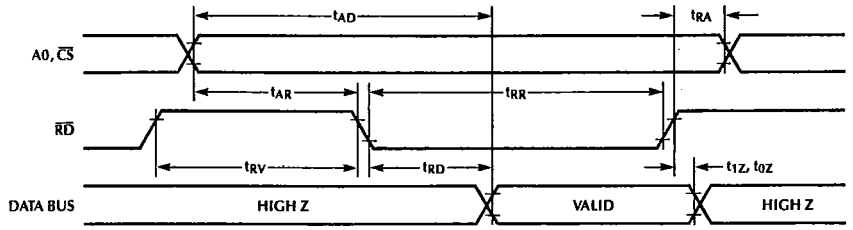


Figure 1. Read Cycle

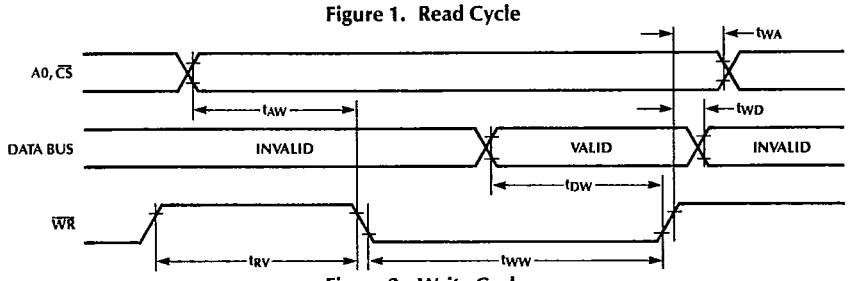
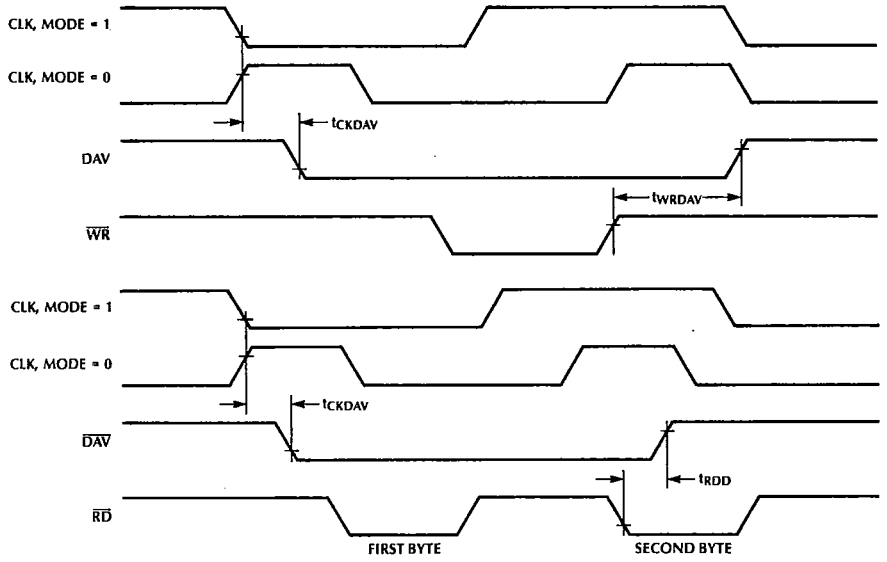


Figure 2. Write Cycle



DAV IS SET AND CLEARED BY INTERNAL CIRCUITRY.
NOTE: DMA BIT IN THE CONTROL REGISTER MUST BE SET FOR THIS OPERATION.

Figure 3. Data Available

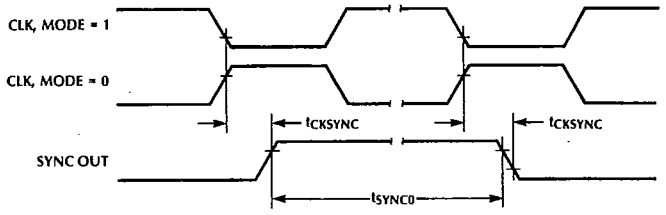
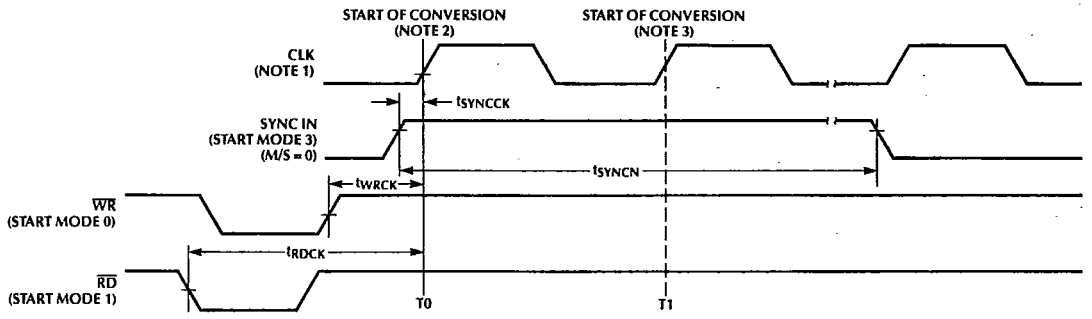


Figure 4. SYNC Output

TIMING DIAGRAMS (Continued)

T-51-10-12



NOTES:
1. CLK IS THE CLOCK DRIVEN AT THE CLOCK PIN.
2. IN CLK MODE 1, WILL ALWAYS OCCUR AT T0 IF SETUP TIMES ARE MET.
3. IN CLK MODE 0, WILL OCCUR EITHER AT T0 OR T1 IF SETUP TIMES ARE MET.

Figure 5. Synchronous Start of Conversion (Start Mode 0,1,3)

BLOCK DIAGRAM

2

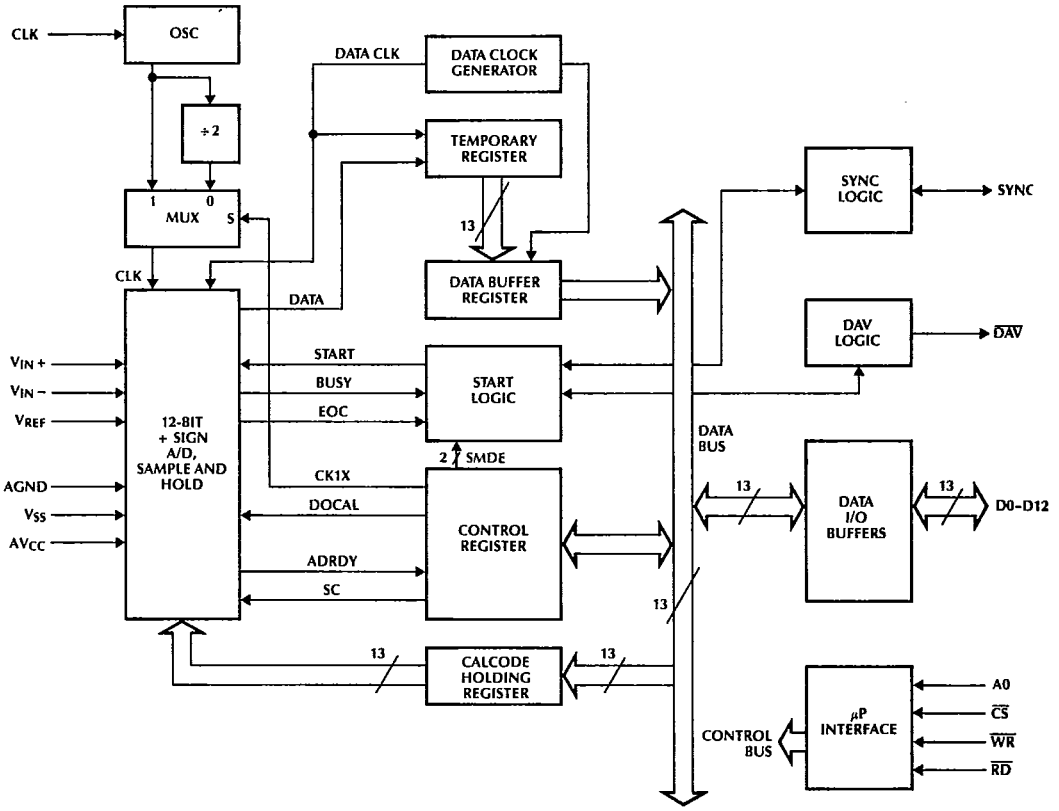


Figure 6. Block Schematic Diagram

FUNCTIONAL DESCRIPTION

ALGORITHMIC A/D CONVERTER

Micro Linear's algorithmic converter uses a successive approximation technique. Most of today's successive approximation converters use a DAC to feedback the approximated signal, however this technique requires more circuitry than algorithmic converters. In addition the values of all of the resistors or capacitors in the DAC must be matched to within the accuracy of the converter. This is difficult to do in silicon beyond 10 bits unless trimming is used. An algorithmic converter uses less circuitry and is more easily trimmed. Micro Linear's algorithmic converter is implemented using a 2x amplifier, a sample/hold amp, and a comparator as shown in Figure 7.

The input sample is first multiplied by two then compared to the reference voltage. If the 2x input voltage is greater than the reference, the MSB is a 1 and the reference voltage is subtracted from the 2x input voltage. The remainder is stored in the sample and hold. If the 2x input voltage is less than the reference, the MSB is a 0 and the 2x input voltage is stored in the sample and hold. This process repeats again, however now the sample and hold voltage is multiplied by 2. (For a more detailed description of an Algorithmic Conversion refer to Mathematical Interpretation of Algorithmic Conversion.)

SELF CALIBRATION

In order to maintain integral and differential linearity to the 1/2 LSB level in an algorithmic converter, two critical parameters need to be controlled, loop offsets and the gain of the loop. Loop offsets are automatically nulled before each conversion using auto-zeroing circuitry on both the sampling amp and the 2x amp. The gain of the loop is adjusted using self calibration.

Self calibrating the algorithmic converter, once the offsets have been nulled, is performed by measuring the 2x gain of the loop and adjusting it. The gain can be measured by converting the reference voltage as the input as well as the reference (V_{REF}/V_{REF}), and examining the output code. Converting V_{REF} should yield plus full scale, since V_{REF}/V_{REF} should equal 1. If the gain of the loop is slightly less than 2, the resulting LSB of the conversion will be "0". If the magnitude bits of the resulting conversion are all "1s", the gain may be too great, therefore the gain is reduced to the point where the threshold of the LSB is reached.

Adjustment of the 2x gain is done with the binary weighted trim capacitor arrays connected to each of the 2C input capacitors. A small value of capacitance is either added to or subtracted from the 2C input caps until the gain of the loop is within 13 bit accuracy of 2.

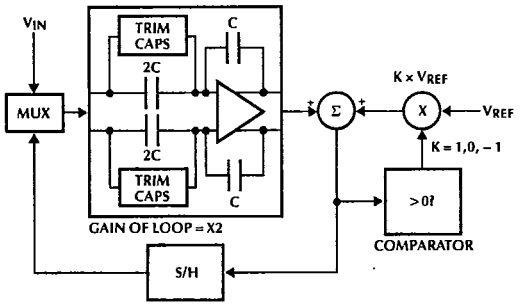


Figure 7. Self Calibrating A/D Converter

FUNCTIONAL DESCRIPTION (Continued)

CONVERSION TIMES

The following table lists the conversion times which include the sample and hold acquisition time. For a CALRD and CALWR no A/D conversion actually takes place.

OPERATION	# OF INTERNAL CLOCKS*
8 bit A/D	80
13 bit A/D	110
CALWR	52
CALRD	80

SAMPLE AND HOLD TIMING

Figure 8 shows the internal timing for the sample and hold circuitry. The relationship between the "Start of Conversion" and the input channel going into sample mode is fixed at 6 internal clocks*, regardless of the Start Mode. Six internal clocks after the Start of Conversion the Sample and Hold is switched into the sample mode, placing two 9pF capacitors in parallel with the inputs pins; one on $V_{IN}+$ and one on $V_{IN}-$. The sample switch is kept in the sample mode for 8 internal clocks (2.3μs at a 7MHz external clock), then placed in the hold mode. During the next 2 internal clocks the charge on the sample and hold is transferred into the A/D, after which the V_{REF} pin is sampled for 8 internal clocks.

Figure 8 also illustrates the timing of the SYNC pin in Master Mode during a conversion (M/S = 1 Control register) and Start Mode 0, 1, or 2. SYNC is activated one internal clock cycle after the Start of Conversion and lasts for four internal clocks.

*For a description of internal clocks see Clock section.

ANALOG INPUTS

DIFFERENTIAL INPUTS AND COMMON MODE REJECTION

The differential inputs of the ML2233 eliminate the effects of common mode input noise (60Hz for example), as $V_{IN}+$ and $V_{IN}-$ are sampled at the same time.

NOISE

The leads to the analog inputs should be kept as short as possible to minimize output noise. Noise as well as digital clocks can couple into the inputs and cause errors. Input filters can be used to reduce the effects of these sources.

POWER SUPPLY DECOUPLING

Low inductance tantalum capacitors of 1μF or greater and 0.01μF disc ceramic capacitors are recommended for bypassing AV_{CC} as well as V_{SS} to AGND. These capacitors should be placed close to the AV_{CC} and V_{SS} pins.

MICROPROCESSOR INTERFACE

2

There are two 13-bit directly addressable registers; a Data Buffer register and a Control register. The data buffer register provides the conversion results. The data register is double buffered, allowing one result to be read while the next sample is being converted. The data register also allows access to the algorithmic converter's calibration code. Normally the ML2233 is operated without ever accessing these registers. (Refer to Diagnostics for more information). The Control register provides complete control and status information. The two registers are addressed by pin A0.

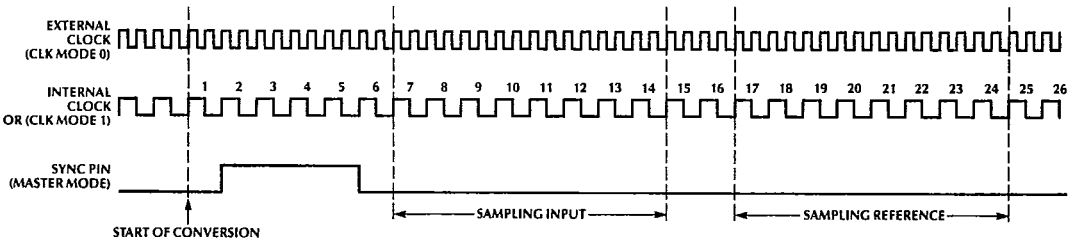


Figure 8. Sample and Hold Timing

FUNCTIONAL DESCRIPTION (Continued)

All data is returned from the converter in two's complement format.

Cycle	+Max	−Min	Zero
13	0FFF	1000	0000
8	007F	1F80	0000

REGISTER DESCRIPTION

Register 0—Data Buffer:
Register 0 contains the results of the latest conversion when read. Depending on the Start Mode selected, reading or writing to this register may start the next conversion.

Register 1—CONTROL Register:

Bit 0 (DAV status when READ/DAVACK acknowledge when a ONE is written):
Reading DAV = 1 indicates that new data is available or a calibration is complete. DAV will be cleared automatically when the data is read. This bit can be explicitly acknowledged by writing a ONE to it; writing a zero has no effect. The $\overline{DAV}$ output pin always reflects the DAV status bit.

Bit 1 (BUSY status when READ/RESET when a ONE is written):
Reading BUSY = 1 indicates that a conversion or calibration is in progress. Writing a ONE will force a chip reset. Writing a zero has no effect.

RESET Default Conditions:

The Control register will automatically be cleared. The Data Buffer register will be unchanged. The Calibration register is not cleared after a reset, however the ADRDY bit is cleared. Since the DAV status bit is cleared, the $\overline{DAV}$ output is inactivated (high). The SYNC pin is forced to be an input as a result of clearing the M/S bit in the Control register.

Bit 2 (ADRDY status when READ/DOCAL request when a ONE is written):
Reading ADRDY = 0 indicates that the converter has not been calibrated since the last reset, and ADRDY = 1 indicates that it has been calibrated since the last reset. Writing a ONE will force the converter to do a calibration; writing a zero has no effect.

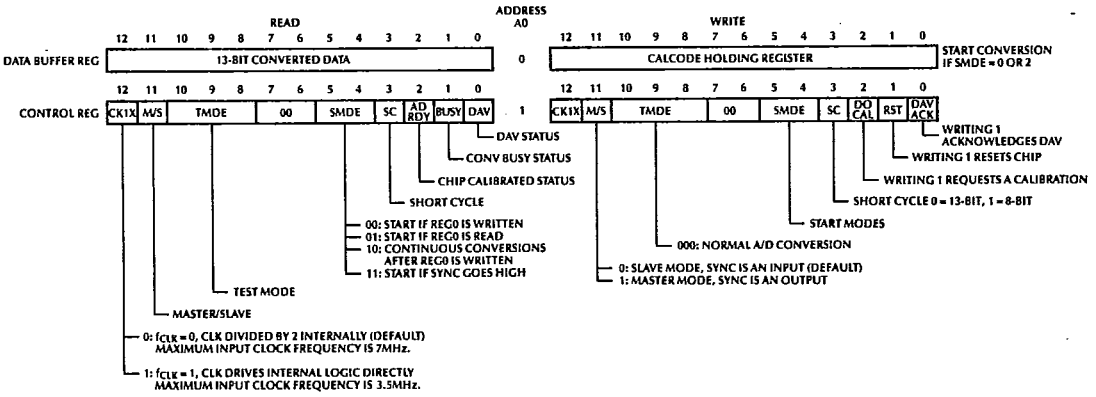


Figure 9. Register Description

FUNCTIONAL DESCRIPTION (Continued)

Bit 3 (SC: Short cycle select):
Selects 8 or 13 bit conversions.

SC = 0: 13-bit conversion (default)
SC = 1: 8-bit conversion (short cycle)

Bits 4,5 (SMDE: Start Mode):
Defines Start Conversion mode.

Bits 5,4

00	Start Conversion upon writing to register 0 (default)
01	Start Conversion upon reading register 0
10	Start Continuous Conversions upon writing to register 0.
11	Start on external SYNC input going high (Requires Slave mode: M/S = 0)

Bits 7,6 (reserved):
These bits are reserved by Micro Linear and must be written as zero.

Bits 10,9,8 (TMDE: test mode select bits)

These bits are used for diagnostic purposes only and normally not accessed during operation. The default value of TMDE is 000 which selects a normal A/D conversion. See Diagnostics for more information.

TMDE	Description
000	Normal A/D Conversion
001	Reserved by Micro Linear (Do Not Use)
010	CALWR Operation
011	CALRD Operation
100	System Offset
101	Common-mode
110	Plus Full Scale
111	Minus Full Scale

Bit 11 (M/S: Master/Slave bit):

Dictates whether the SYNC pin is an input or an output. Upon RESET, this bit is cleared.

M/S = 0: Slave Mode	SYNC is an input which is used to trigger a conversion if SMDE = 11.
M/S = 1: Master Mode	SYNC is an output. At the beginning of every conversion, SYNC is high for 4 internal clocks.

Bit 12 (CK1X: clock select bit):

Selects whether the external clock will be divided by two or used directly as the internal clock. See Clock section for a detailed explanation.

CK1X = 0:	the external clock is divided by two and used as the internal clock. This is referred to as CLK Mode = 0.
CK1X = 1:	the external clock input is used directly as the internal clock. This is referred to as CLK Mode = 1.

2

FUNCTIONAL DESCRIPTION (Continued)

GENERAL OPERATING INFORMATION

CONVERSION-START PROTOCOL

There are four different ways to start a conversion. They are defined by SMDE bits 4 and 5 in the Control Register.

SMDE Bits 5,4

00: A write to register 0 will start a conversion. During a conversion, if another write is issued to register 0, the "Start Conversion" command will be latched and another conversion will immediately follow the current one. To insure that the second write will be latched, it must occur at least 3 internal clocks after the first write. Only one additional write will be latched; multiple writes within a conversion will only yield one more conversion.

01: Reading the data from the previous conversion starts the next conversion.

10: This mode causes continuous conversions; the next conversion begins immediately after the previous conversion ends. Writing to register 0 will start the first conversion; thereafter the converter runs continuously. This mode yields the maximum conversion rate.

11: The SYNC input triggers the start of a conversion. The M/S bit in the Control Register must be cleared, placing the chip in the slave mode.

Note: The external activation signals for Start Modes 0, 1, and 3 are synchronized internally to the system clock. If periodic sampling is required using these Start Modes, the SYNC, $\overline{RD}$, or $\overline{WR}$ pulses must be synchronized to the system clock. Start Mode 2 guarantees periodic sampling.

DOUBLE-BUFFERED DATA REGISTER

The A/D conversion result is double-buffered using the Data Buffer register and the A/D Data register. The actual End-Of-Conversion (EOC) does not correspond with the $\overline{DAV}$ output going low. The $\overline{DAV}$ output goes low 16 internal clocks after the EOC. From the time $\overline{DAV}$ output goes LOW, the user has one full conversion time (80 or 110 internal clocks) minus 16 internal clocks to read the data as shown in Figure 10.

SELF CALIBRATION

Setting the DOCAL bit issues a calibration request to the chip. When calibration is done, the DAV status bit is set and the $\overline{DAV}$ output goes low.

A calibration requires 8,260 internal clocks. Using a 7MHz clock (CLK Mode = 0), this is approximately 2 ms. Power supplies and external voltage reference must be stable before issuing a request for calibration.

The ML2233 should be calibrated before any conversions are attempted. Calibrations must not be performed simultaneously with conversions. Before requesting a calibration, the user may want to read the Busy status bit to make sure that the converter is idle. Polling the chip while the calibration is in progress is not recommended.

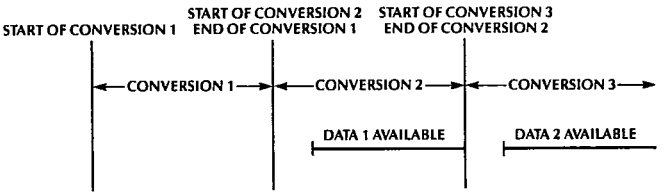


Figure 10

FUNCTIONAL DESCRIPTION (Continued)

CLOCK

The ML2233 has the option of dividing the clock at the CLK pin by 2, or using it directly to drive the internal logic. This option is selected through the CK1X bit in the Control register. When CK1X = 0 the clock is divided by 2. This is referred to as CLK Mode = 0. The clock at the CLK pin is referred to as the External clock, and the Internal Clock is the External clock divided by 2. When CK1X = 1, the clock at the CLK pin drives the internal logic directly, therefore this clock is referred to as the Internal clock. This is also known as CLK Mode = 1. All internally clocked logic is positive edge triggered.

CLK Mode = 0:

There are two advantages to CLK Mode 0. This is the only Mode that allows an external crystal to be used. CLK Mode 1 cannot operate with an external crystal, the CLK pin must be driven. The second advantage of CLK Mode 0 is that the duty cycle for a driven clock is less stringent than in CLK Mode 1. (Refer to t_{CLK0} and t_{CLK1} in AC Electrical Characteristics for CLK Mode 0 and 1 timing requirements, respectively.)

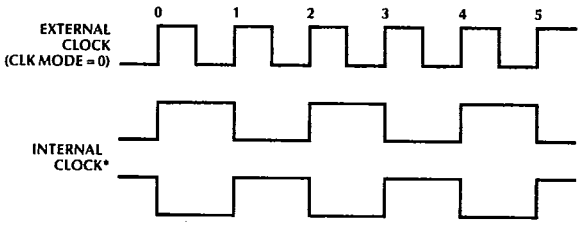
On power up the state of the divide by two flip-flop is indeterminate. Therefore the relationship between the internal clock and the external clock at the CLK pin can have one of two possibilities as shown in Figure 11. As a result the following should be considered.

t_{WRCK}, t_{RDCK}, and t_{SYNCCK} specs, ($\overline{RD}$, $\overline{WR}$, and SYNC set-up times to Start of Conversion), will be as shown in the data sheet, or the data sheet specs plus one external clock period. Since these specifications are with respect to the rising edge of the external clock, it is not known whether this rising edge corresponds to the rising edge or falling edge of the internal clock. Therefore there is an uncertainty of one external clock period.

If periodic sampling is necessary and Start Mode 0,1, or 3 is used, the external start pulse (either $\overline{RD}$, $\overline{WR}$, or SYNC) must be synchronous to the external clock, meet the setup time, and be an even number of external clock periods. If the start pulse were an odd number of external clock periods, half the pulses would correspond with the rising edge of the internal clock, and the other half would correspond with the falling edge of the internal clock. Therefore the sampling period would change by one external clock period every sample. Start Mode 2 guarantees periodic sampling regardless of the CLK mode.

CLK Mode = 1:

This mode eliminates the requirement that external start pulses must be an even number of external clock periods. However periodic sampling still requires that the start pulse be synchronous to the external clock, and the setup time must be met. CLK Mode 1 also eliminates the uncertainty of the t_{WRCK}, t_{RDCK}, and t_{SYNCCK} requirements.



*INTERNAL CLOCK MAY BE ONE OF THE TWO ABOVE IN CLK MODE = 0

Figure 11

FUNCTIONAL DESCRIPTION (Continued)

DIAGNOSTICS

Diagnostic routines may be run after power up or any other time to ensure proper operation. The diagnostic features, which are software selectable, don't require external hardware. Both the analog and digital sections can be tested.

The ML2233 is placed in the diagnostic mode via the TMDE field in the Control Register. Once the ML2233 is placed in one of the diagnostic modes, a conversion must be executed before the results can be read. As with all conversions, $\overline{DAV}$ will be activated upon completion.

ANALOG CONVERSION DIAGNOSTICS

TMDE = 000: Normal Operation
Selects normal A/D conversion. Default condition after a software reset.

TMDE = 001: Reserved by Micro Linear.

TMDE = 010: CALWR operation
The data in Write register 0 (CALCODE Holding Register), is transferred into the converter's Calibration register when a "Start Conversion" is issued. A dummy conversion occurs and the $\overline{DAV}$ output goes LOW to indicate that the operation is complete.

TMDE = 011: CALRD operation
The contents of the Calibration register are transferred through the A/D Data register and loaded into the Data Buffer register. A dummy 8-bit conversion occurs and $\overline{DAV}$ output goes LOW to indicate that the CALRD operation is complete.

TMDE = 100: System Offset
The positive and negative inputs to the Sample and Hold are tied to analog ground. With this setting, converted data will give the offset of the A/D converter and Sample/Hold combination. The $V_{IN}+$ and $V_{IN}-$ pins will remain in a high impedance state while in this mode.

TMDE = 101: Common-mode
Both the positive and negative inputs of the Sample and Hold are tied to V_{REF}. The results of a conversion in this test mode indicates how well the converter is rejecting a common mode signal.

TMDE = 110: Positive Full Scale
This test mode connects the positive input of the Sample and Hold to V_{REF} and the negative input of the Sample and Hold to analog ground. The result of converting in this test mode is a value near positive full scale.

TMDE = 111: Negative Full Scale
This test mode connects the positive input of the Sample and Hold to analog ground and the negative input to V_{REF}. The result of converting in this test mode is a value near negative full scale.

DIGITAL LOOPBACK

The ML2233's architecture provides a way for the microprocessor to indirectly read and write to the A/D converter's calibration register and data register via a CALRD and CALWR. Figure 12 illustrates this architecture. This in effect allows a digital loopback.

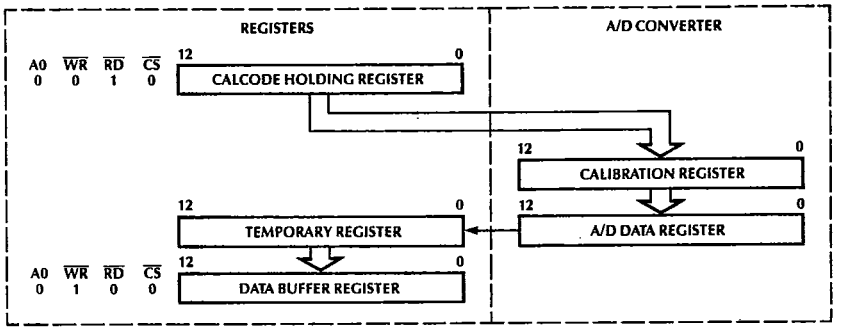


Figure 12. Digital Loopback

FUNCTIONAL DESCRIPTION (Continued)

When the TMDE bits are set to 010 CAL WRITE (CALWR), and a Start Conversion is issued in any one of the four modes, the contents of the CALCODE Holding register is transferred into the A/D converter's Calibration register. When the TMDE bits are set to 011 CAL READ (CALRD), and a Start Conversion is issued, the contents of the Calibration register are transferred through the A/D's Data register into the Data Buffer register. The result of these two operations is a complete loopback from the CALCODE Holding register through the A/D converter and back into the Data buffer register. This loopback provides user assurance that all the paths are clear and there are no stuck bits.

Note: When a CALWR is done, the previous calibration value is lost. The correct calibration value must be restored before the converter is used to convert data.

CALIBRATION PASS/FAIL TEST

The CALRD can be used as a way to verify a successful calibration. After a calibration is completed, the CALRD may be issued in order to read the contents of the Calibration register. If the Low Byte (lower 8 bits) of the data buffer register are ones after executing a CALRD, the calibration failed; otherwise the calibration is successful.

MATHEMATICAL INTERPRETATION OF ALGORITHMIC CONVERSION

The A/D conversion process generates a binary representation of the ratio of the input voltage divided by the reference voltage; V_{IN}/V_{REF}. The following equation illustrates this representation, where Bit(0) is the MSB.

$$V_{IN}/V_{REF} = (Bit(0)/2 + Bit(1)/4 + Bit(2)/8 + \ldots + Bit(n)/2^{n+1}) \quad (1)$$

$$V_{IN} = V_{REF}(Bit(0)/2 + Bit(1)/4 + Bit(2)/8 + \ldots + Bit(n)/2^{n+1}) \quad (2)$$

In the successive approximation conversion, one bit at a time is evaluated, beginning with the MSB, to determine whether it should be a 1 or a 0. The process begins by multiplying both sides of the equation by 2 and determining whether the left side of the equation ($2*V_{IN}$) is greater than or less than the first term of the right side of the equation (V_{REF}).

$$\mathbf{2*V_{IN} = V_{REF}(Bit(0)} + Bit(1)/2 + Bit\ (2)/4 + \ldots + Bit\ (n)/2^{n}) \quad (3)$$

If $2*V_{IN}$ is greater than V_{REF}, Bit(0) should be a one, and this term is moved to the left side of the equation as shown in equation (4). If $2*V_{IN}$ is less than V_{REF}, Bit(0) should be a zero, and this term is now eliminated, as shown in equation (5).

Bit(0) = 1

$$(2*V_{IN}) - V_{REF} = V_{REF}(Bit(1)/2 + Bit\ (2)/4 + \ldots + Bit(n)/2^{n}) \quad (4)$$

Bit(0) = 0

$$(2*V_{IN}) = V_{REF}(Bit(1)/2 + bit\ (2)/4 + \ldots + Bit(n)/2^{n}) \quad (5)$$

Once again both sides of the equation, either (4) or (5), are multiplied by 2. The equation now reads.

Bit(0) = 1

$$\mathbf{2*((2*V_{IN}) - V_{REF}) = V_{REF}(Bit(1)} + Bit\ (2)/2 + \ldots + Bit(n)/2^{n-1}) \quad (6)$$

Bit(0) = 0

$$\mathbf{2*(2*V_{IN}) = V_{REF}(Bit(1)} + Bit(2)/2 + \ldots + Bit(n)/2^{n-1}) \quad (7)$$

Now Bit(1) is evaluated. If the left side of the equation is greater than V_{REF}, Bit (1) is a 1, and this term is moved to the left side of the equation. Else Bit(1) is a zero and the term cancels out.

This algorithm is repeated until all n bits are evaluated.

From the previous example it was shown that the algorithm involves multiplication by 2, comparison, and possibly subtraction. Referring to Figure 7, the algorithm for the circuit can be described as follows:

Step 1 If $(2*V_{IN}) - V_{REF} \geq 0$
then MSB = 1
$(2*V_{IN}) - V_{REF} \rightarrow S/H$
else MSB = 0
$(2*V_{IN}) \rightarrow S/H$

Step 2 If $(2*S/H) - V_{REF} \geq 0$
then next bit = 1
$(2*S/H) - V_{REF} \rightarrow S/H$
else next bit = 0
$(2*S/H) \rightarrow S/H$

Step 3 Repeat Step 2 until done.

Since the A/D converter handles bipolar inputs, negative inputs are handled slightly differently using the same principle.

2

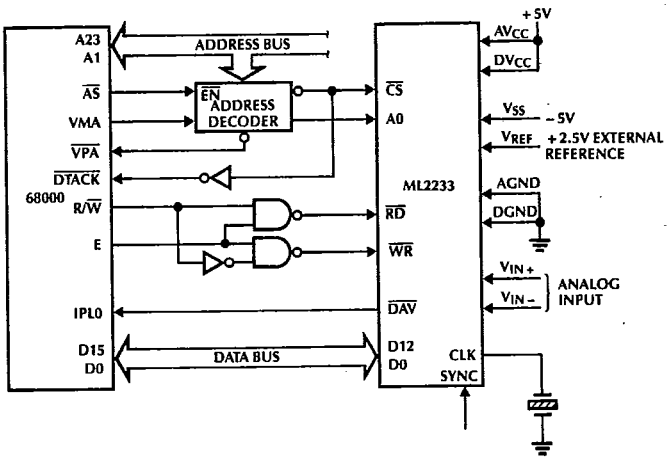


Figure 13. Interfacing to 68000 Microprocessor

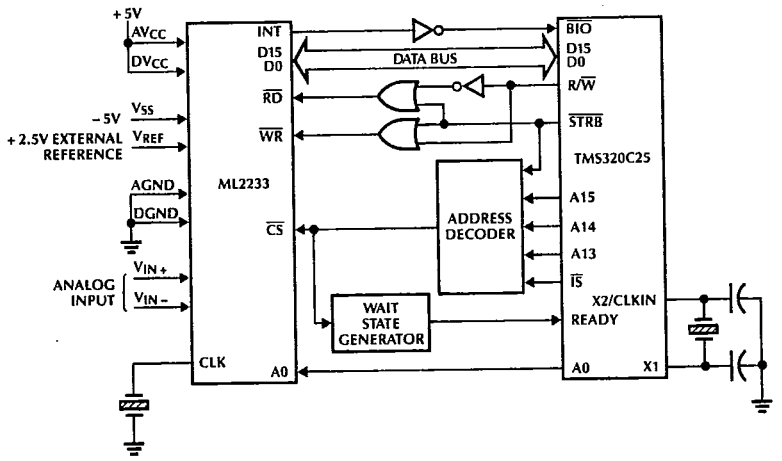


Figure 14. Interfacing to TMS320C25 Digital Signal Processor

T-51-10-12

ORDERING INFORMATION

PART NO.	LINEARITY ERROR	TEMPERATURE RANGE	PACKAGE
ML2233BCP	±1/2LSB	0°C to +70°C	Molded DIP
ML2233CCP	±1LSB	0°C to +70°C	Molded DIP
ML2233BCQ	±1/2LSB	0°C to +70°C	Molded PCC
ML2233CCQ	±1LSB	0°C to +70°C	Molded PCC
ML2233BIJ	±1/2LSB	−40°C to +85°C	Hermetic DIP
ML2233CIJ	±1LSB	−40°C to +85°C	Hermetic DIP

2