MLX80001

4-channel Master LIN Transceiver

Features

- Compliant to LIN Specification Version 1.3, 2.x and J2602
- 4 channel independent enhanced master transceiver function
- Slew rate selection for 10.4kbps (J2602) and 20kbps (LIN 2.x) for optimized radiated emission behavior
- Disable of slew rate control for fast programming or test modes
- High EMC immunity
- Fully integrated receiver filter
- LIN terminals proof against short-circuits and transients in the automotive environment
- High impedance LIN in case of loss of ground , loss of battery and under voltage condition
- LIN short to ground protection
- Control output for voltage regulator
- Only 25µA typical power consumption in sleep mode
- Remote wake up via LIN traffic
- Integrated master termination resistors (1kOhm) and decoupling diodes
- Thermal overload protection
- 5V and 3.3V compatible digital inputs
- 20-pin thermally enhanced QFN 5x5 package
- ±4kV ESD protection pin LIN

Ordering Code

Product Code	Temperature Code	Package Code	Option Code	Packing Form Code
MLX80001	K	LQ	BAA-001	TU
MLX80001	K	LQ	BAA-001	RE

Legend:

Temperature Code: K for Temperature Range -40°C to 125°C
Package Code: LQ for QFN
Packing Form: RE for Reel

Ordering example: MLX80001KLQ-BAA-001-TU

General Description

The MLX80001 is a 4 channel physical layer device for applications of low speed vehicle serial data network communication using the Local Interconnect Network (LIN) protocol. The device is designed in accordance to the physical layer definition of the LIN Protocol Specification Package 2.x and the SAE J2602 standard. The IC furthermore can be used in ISO9141 systems.

Because of the very low current consumption of the MLX80001 in the recessive state it's suitable for ECU applications with hard standby current requirements. An advanced sleep mode capability allows a shutdown of a complete master node. The included wake-up function detects incoming dominant LIN messages and enables the voltage regulator.

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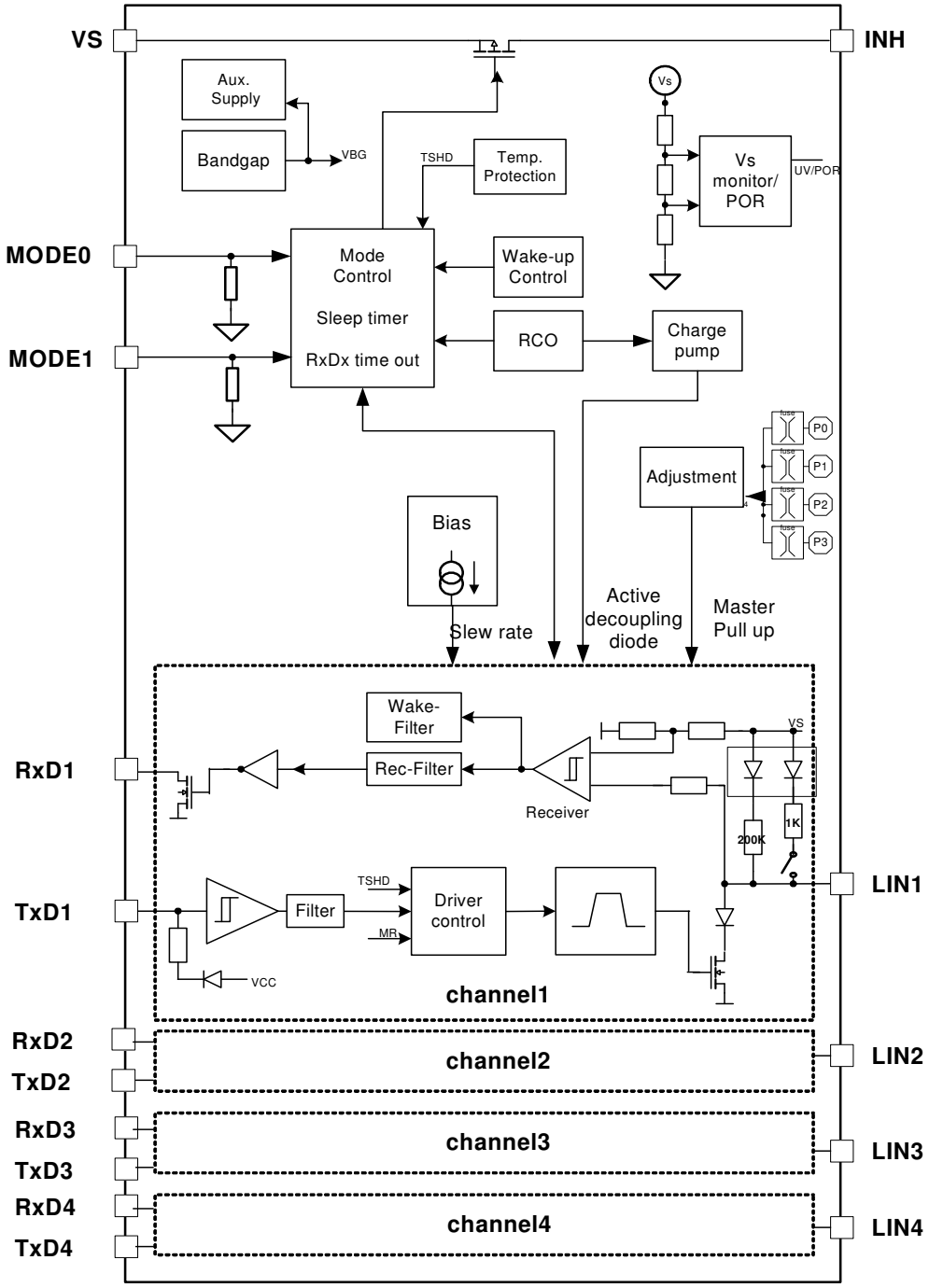


Figure 1 - Block diagram

2. Electrical Specification

All voltages are referenced to ground (GND). Positive currents flow into the IC.
The absolute maximum ratings (in accordance with IEC 60 134) given in the table below are limiting values which do not lead to a permanent damage of the device. Exceeding any of these limits may do so. Long term exposure to limiting values may effect the reliability of the device.

2.1 Operating Conditions

Parameter	Symbol	Min	Max	Unit
Battery supply voltage [1]	V_S	7	18	V
Short time battery supply voltage	V_{S_S}	18	26.5	V
Low battery supply voltage	V_{s_L}	5	7	V
Operating ambient temperature	T_{amb}	-40	+125	°C

[1] Vs is the IC supply voltage including voltage drop of reverse battery protection diode, V_{DROP} = 0.4 to 1V, V_{BAT_ECU} voltage range is 6 to 26.5V

2.2 Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Max	Unit
Battery Supply Voltage	V_S	t < 1 min	-0.3	30	V
		ISO 7637/2 pulse 5, t < 400ms		45	
Transients at battery supply voltage	$V_{VS.tr1}$	ISO 7637/2 pulse 1[1]	-100		V
Transients at battery supply voltage	$V_{VS.tr2}$	ISO 7637/3 pulse 2[1]		+50	V
Transients at high voltage signal pins	$V_{LINx..tr1}$	ISO 7637/3 pulse 1[2]	-30		V
Transients at high voltage signal pins	$V_{LINx..tr2}$	ISO 7637/3 pulse 2[2]		+30	V
Transients at high voltage signal and power supply pins	$V_{HV..tr3}$	ISO 7637/2 pulse 3A, 3B [3]	-200	+200	V
DC voltage LIN	V_{LIN_DC}	t < 500ms , Vs = 18V Vs = 0V	-22 -40	+40	V
DC voltage logic I/O's	V_{logic_DC}		-0.3	+7	V
ESD capability any pins	V_{ESDHB}	Human body model, equivalent to discharge 100pF with 1.5kΩ,	-2	+2	kV
ESD capability LINx	V_{ESDHB_HV}	Human body model, equivalent to discharge 100pF with 1.5kΩ,	-4	+4	kV
Maximum latch – up free current at any Pin	I_{LATCH}		-500	+500	mA
Maximum power dissipation [4]	P_{tot}	Tamb = +125 °C Tamb = +105 °C Tamb = + 95 °C		0.75 1.3 1.6	W
Thermal impedance	Θ_{JA}	in free air		34	K/W
Storage temperature	T_{stg}		-55	+150	°C
Junction temperature	T_{vj}		-40	+150	°C

[1] ISO 7637/2 test pulses are applied to VS via a reverse polarity diode and >10uF blocking capacitor.
[2] ISO 7637/3 test pulses are applied to LIN via a coupling capacitance of 100nF.
[3] ISO 7637/3 test pulses are applied to LIN via a coupling capacitance of 1nF. ISO 7637/2 test pulses are applied to VS via a reverse polarity diode and >10uF blocking capacitor
[4] Simulated values for low conductance board (JEDEC)

2.3 Static Characteristics

Unless otherwise specified all values in the following tables are valid for V_S = 5 to 26.5V and T_{AMB}= -40 to 125°C. All voltages are referenced to ground (GND), positive currents are flow into the IC.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
PIN VS						
Undervoltage lockout	V_{S_UV}	MODE0/1=1, TxDx=0	2		4.5	V
Supply current single channel, dominant	I_{Sd_single}	V_S = 26.5V, TxDx=0 no load current			30 2	mA
Supply current four channel, dominant	I_{Sd_four}	V_S = 26.5V, TxDx=0 No load current			120 4	mA
Supply current, recessive	I_{Sr}	V_S = 18V, TxDx=H		950	1500	µA
Supply current, sleep mode	I_{Ssl}	MODE0/1=0 V_S = 12V, Tamb= 25°		25		µA
Supply current, sleep mode	I_{Ssl}	MODE0/1=0			50	µA
PIN LINx – Transmitter						
Short circuit LIN current	$I_{\_LIN\_LIM}$	V_{LIN} = VS, TxD=0		120	200	mA
Pull up resistor LIN	$R_{\_LIN\_PU}$	V_{LIN} =0, TxD open	900		1100	Ω
Pull up current LIN , sleep mode	$I_{\_LIN\_PU\_SLEEP}$	V_{LIN}=0, V_S=12V, sleep mode	-100	-75		µA
LIN reverse current, recessive	$I_{\_LIN\_rec}$	V_{LIN}> V_S, 5V < V_{LIN} < 26.5V , 5V < V_S < 26.5V, TxD open			20	µA
LIN reverse current loss of battery	$I_{\_LIN\_LOB}$	V_S=0V, 0V < V_{LIN} < 26.5V			20	µA
LIN current during loss of Ground[2]	$I_{\_LIN\_LOG}$	V_S=12V, 0V < V_{LIN} < 26.5V	-150		100	µA
Transmitter dominant voltage	V_{olLIN_3}	V_S=18V, network load =500Ω, TxDx = 0			2	V
Transmitter driving capability low battery	$I_{\_LIN\_dom\_min}$	V_S=7V, V_{LIN}=1.5V, TxDx = 0	40			mA
Recessive output voltage	V_{ohLIN}	TxDx open	0.8*Vs		Vs	V
LIN input capacitance [1]	C_{LIN}	Pulse response via 1KΩ, V_{PULSE} = 12V, VS open		25	35	pF
PIN LINx – Receiver						
Receiver dominant voltage	V_{ilLIN}		0.4 *V_S			V
Receiver recessive voltage	V_{ihLIN}				0.6 *V_S	V
Center point of receiver threshold	V_{iLIN_cnt}	V_{LIN_cnt} = ($V_{ilLIN\_}$ + V_{ihLIN})/2	0.475 *V_S	0.5 *V_S	0.525 *V_S	V
Receiver hysteresis	V_{iLIN_hys}	V_{LIN_cnt} = (V_{ihLIN} -V_{ilLIN})			0.175 *V_S	V
PIN TXD_x, MODE 0/1						
High level input voltage	V_{ih}		2.0			V
Low level input voltage	V_{il}				0.65	V
TxD pull up current	$-I_{IL\_TXD}$	TxD_x =L, MODE0&1=H	10		50	µA
MODE pull down resistor	R_{MODE_pd}		10		50	kΩ

Parameter	Symbol	Condition	Min	Typ	Max	Unit
PIN RXD_x						
Low level output voltage	V_{ol_rxd}	I_{RxD} = 2mA			0.9	V
High level output leakage	I_{ih_rxd}	V_{RxD} = 5.5V	-10		+10	µA
PIN INH						
High level output voltage	V_{oh_INH}	I_{INH} = -180µA	VS -0.8V	VS -0.5V		V
Leakage current INH	I_{INH_lk}	EN = L ,V_{INH} = 0V	-10		10	µA
Thermal Protection						
Thermal shutdown [1]	T_{sd}		160		190	°C
Thermal recovery [1]	T_{hys}		126		150	°C

[1] No production test, guaranteed by design and qualification
[2] The current is determined by the master pull up, to prevent discharge battery the master pull up path will be disconnected under LOG conditions

2.4 Dynamic Characteristics

Unless otherwise specified all values in the following table are valid for V_S = 5 to 26.5V and T_{AMB}= -40 to 125°C.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Propagation delay receiver [1]	t_{rec_pdf}	C_{RxD} =25pF falling edge			6	µs
Propagation delay receiver [1]	t_{rec_pdr}	C_{RxD} =25pF rising edge			6	µs
Propagation delay receiver symmetry [2]	t_{rec_sym}	Calculate ttrans_pdf - ttrans_pdr	-2		2	µs
Receiver debounce time [2]	t_{rec_deb}	LIN rising & falling edge	0.5		4	µs
LIN duty cycle 1 [3] [4]	D1	20kbps operation , normal mode	0.396			
LIN duty cycle 2 [3] [4]	D2	20kbps operation , normal mode			0.581	
LIN duty cycle 3 [3] [4]	D3	10.4kbs operation , low speed mode	0.417			
LIN duty cycle 4 [3] [4]	D4	10.4kbs operation , low speed mode			0.590	
trec(max) – tdom(min)	Δt3	10.4kbs operation , low speed mode			15.9	µs
trec(min) – tdom(max)	Δt4	10.4kbs operation , low speed mode			17.28	µs
Rise time in high speed mode	t_{r_hs}	Network τ < 1µs			2	µs
Fall time in high speed mode	t_{f_hs}	Network τ < 1µs			2	µs
Wake-up filter time	t_{wu}	Sleep mode LIN_x rising & falling edge	15		150	µs
Delay from Standby to Sleep Mode	t_{dsleep}	MODE0/1 = L	100		500	ms
RxD time out	t_{RxD_to}	Active modes, RxD_x = L	25		50	ms
MODE0/1 – debounce time	t_{MODE_deb}	Active <--> standby mode transitions	2	5	20	µs

[1] This parameter is tested by applying a square wave signal to the LIN. The minimum slew rate for the LIN rising and falling edges is 50V/us
[2] See figure 4 - receiver debounce and propagation delay
[3] See figure 5 and 6 – duty cycle measurement & calculation,
[4] Standard loads for duty cycle measurements are 1KΩ/1nF , 660Ω/6.8nF, 500Ω/10nF,internal termination disabled

2.5 Timing Diagrams

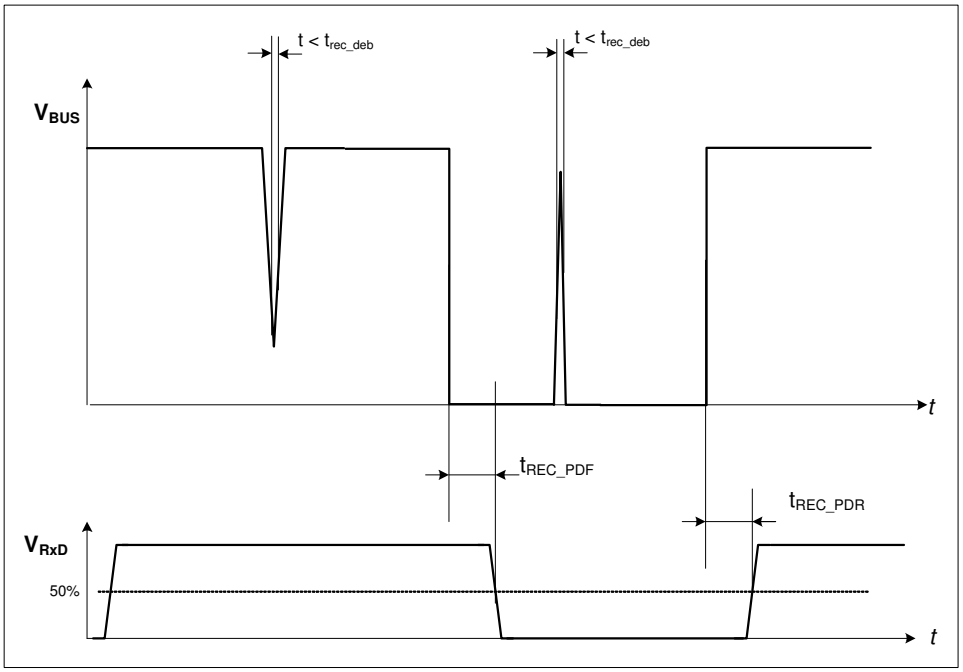


Figure 2 – Receiver debouncing and propagation delay

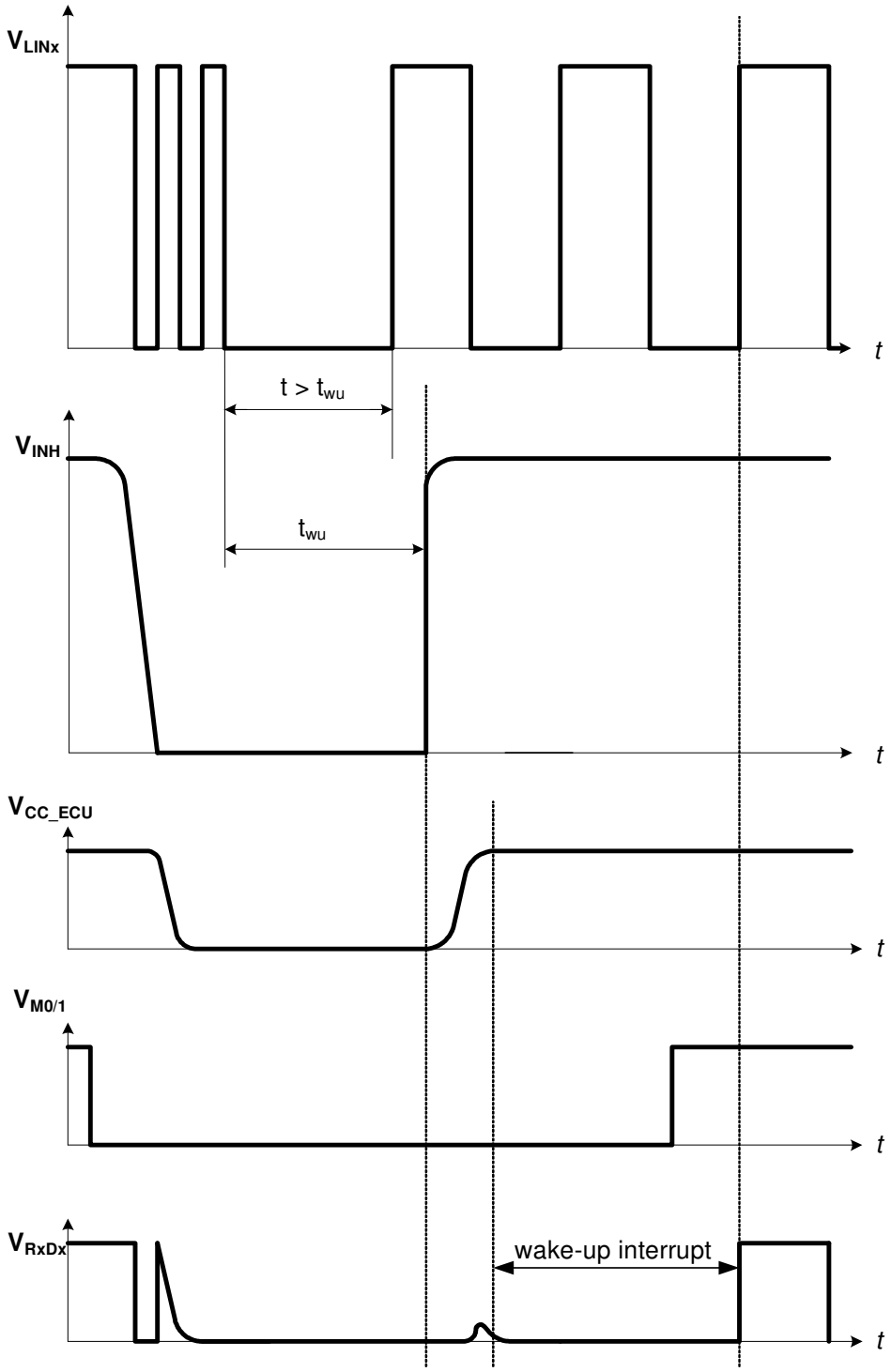


Figure 3 - Sleep mode and wake up procedure

2.6 Test Circuits for Dynamic and Static Characteristics

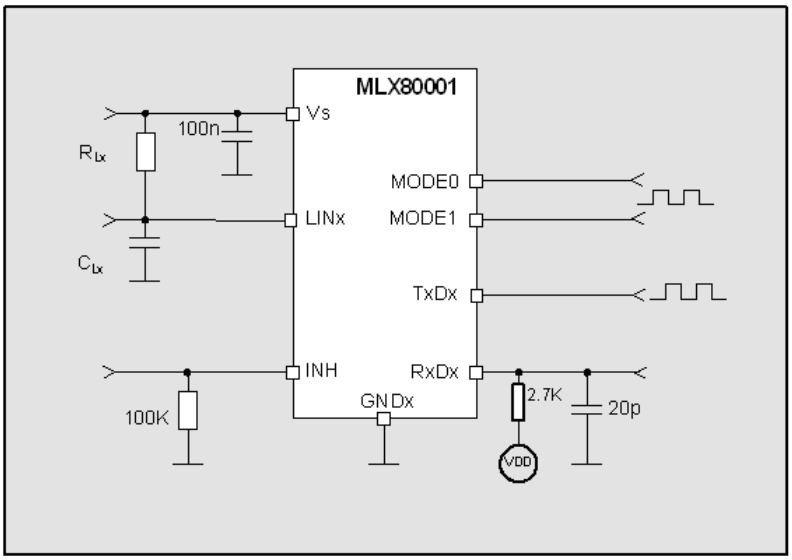


Figure 4 - Test circuit for dynamic characteristics

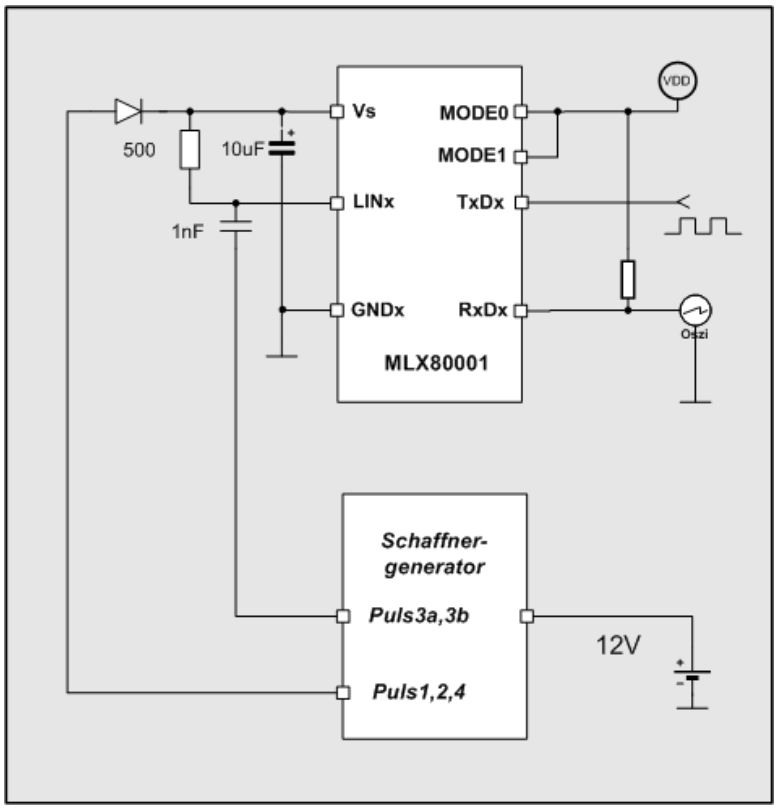


Figure 5 - Test circuit for automotive transients

3. Functional Description

3.1 TxDx Input pin - Logic command to transmit on LINx bus as follows:

TxD Polarity

- TxD = logic 1 (or floating) on this pin applies a recessive bus state (high bus voltage)
- TxD = logic 0 on this pin applies a bus dominant state depending on the transceiver mode state (low bus voltage)

If the TxD pin is driven to a logic low state while the Mode 0,1 pins are in the 0,0 state or open, the transceiver does not drive the LIN pin to the dominant state.
The pin contains an internal pull up to guarantee a recessive LIN behaviour in case of an open TxD pin. For 5V ECU supply systems an external pull up resistor is recommended.
TxD input thresholds are standard CMOS logic levels for 3.3V and 5V supply voltages.

3.2 RxDx Output pin - Logic data as sensed on the LINx bus

RxD polarity

- RxD = logic 1 on this pin indicates a bus recessive state (high bus voltage)
- RxD = logic 0 on this pin indicates a bus dominant state (low bus voltage)

The RxDx output is a low side open drain output. An external pull up resistor is required to realize the level shift of a logic 1 level (high impedance output) to the Vcc_ECU voltage level.

Wake up source recognition

RxDx do not pass signals to the micro processor while in sleep mode until a valid wake up bus voltage level is received or the Mode 0,1 pins are not 0,0 respectively. When the valid wake up bus signal awakens the transceiver, the RxDx pin signalized an active low interrupt. This interrupt is active as long as no MODE pin is switched to logic 1. After the MLX80001 enters an active mode, all valid bus signals will be sent out to the RxD output.
The micro can detect the source of the wake up event and start the transmission only to the network caused the wake up.

RxD time out feature

A dominant RxDx level longer than the specified time indicates a faulty blocked bus caused by a LIN node itself or a short circuit to ground. The master pull up resistor of the LIN channel affected by the short will be disconnected from the network in order to prevent thermal overload conditions or failure currents from the battery without any intervention from the micro. The RxD timeout will be disabled with the next L->H transition.

RxD Typical Load

Resistance: 2.7 kΩ	(recommended pull up resistor)
Capacitance: < 25 pF	(parasitic board capacitance)

Mode 0 and Mode 1 pins respectively are used to select transceiver operating modes:

The MLX80001 provides a weak internal pull down current on each of these pins. In case of open pins or during the micro I/O initialisation procedure after power on or ECU wake up a stable passive behaviour of the MLX80001 is given.
The MODE0/1 input thresholds are standard CMOS logic level for 3.3V and 5V supply voltages.

M0	M1	Mode
L	L	Sleep Mode
H	L	High Speed Mode (slew rate control disabled)
L	H	Low speed mode
H	H	Normal Mode

Mode 0 = 0, Mode 1 = 0 - Sleep mode.

Transceiver is in low power state, waiting for remote wake up via LIN or by mode changes to any state other than 0,0. In this mode, the LINx pin is not in the dominant state regardless of the voltage at the TxDx pin. As long as the MODE0/1 pin are logic 0, the transceiver returns to sleep mode after power on or remote wake up after the specified time.

Mode 0 = 1, Mode 1 = 0. High Speed mode

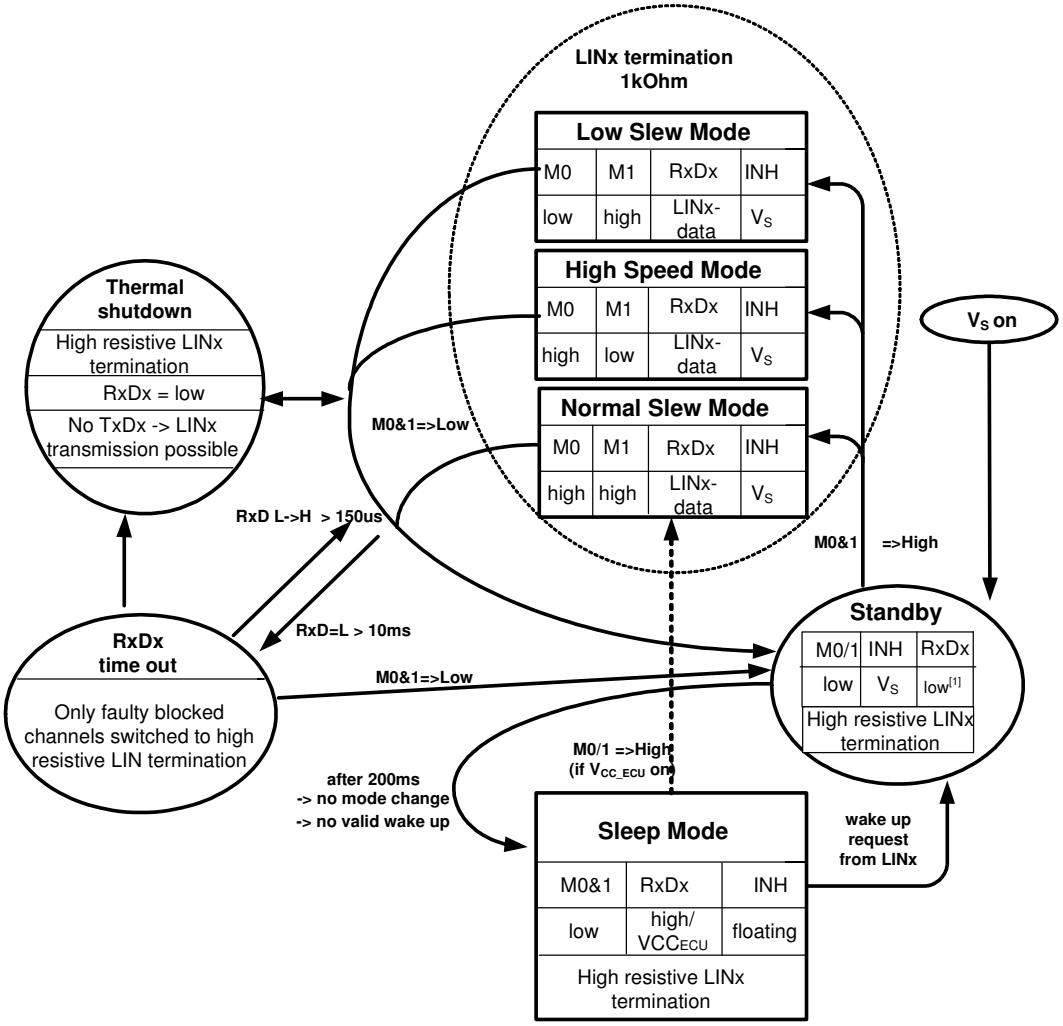
This mode allows high speed data download up to 100Kbit/s. The slew rate control is disabled in this mode all the six transmission channels. The falling edge is the active driven edge, the rising edge additional is determined by the network time constant.

Mode 0 = 0, Mode 1 = 1. Transmit with reduced slew rate for low speed applications with 10.4kbps or below

This mode is the recommended operating mode for J2602 applications. The slew rate control of any channel is optimized for minimum radiated noise, especially in the AM band.

Mode 0 = 1, Mode 1 = 1. Normal speed mode

Transmission bit rate in normal mode is up to 20kbps. The slew rate control of any channel is optimized for maximum allowed bit rate in the LIN specification package 2.x.



[1] active low interrupt, indicates source of wake up after power on all channel RxDx are active low

Figure 6 - State diagram MLX80001

3.3 Power on procedure , INH Pin – INHIBIT

After power on the MLX80001 automatically enters an intermediate standby mode, the INH output becomes HIGH (VBAT) and therefore the external voltage regulator will provide the Vcc supply voltage for the ECU . If there is no mode change within the time stated (typically 350ms), the IC re-enters the sleep mode and the INH output is going to become floating (logic 0).
When the device detects a valid wake up condition (bus traffic on any of the four LIN networks exceeds the wake up filter time delay) the INH output becomes HIGH (VBAT) again and the same procedure starts as described after power on. In case of a mode change to any active mode the sleep timer is stopped and INH keeps HIGH(VBAT). If the transceiver enters the sleep mode (M0/1=0) , INH goes to logic 0 (floating) after typically 350 ms when no valid wake up is detected.

3.4 Pin LIN

The LINx pins are the four physical interfaces to the automotive environment. The related circuitry consists of three parts:

- Transmitter with slew rate control

The slew rate of the transmitter is configurable by the MODE0/1 pins and depends from the application.

- Receiver

The receiver guarantees the specified input threshold levels and a very high robustness to external disturbances.

- Termination

This circuitry contains the master pull up resistor and decoupling diodes. The integrated solution allows a very comfortable control of failure situations, see description below. To guarantee the specified value of +/- 10% and to minimize the power dissipation, this circuitry is adjustable on wafer level. In order to allow a battery current limitation in failure situations, a high resistive termination is placed in parallel to the master pull up resistor.

4. Fail-save Features

Loss of battery

If the ECU is disconnected from the battery, the LIN pin is in high impedance state. There is no impact to the LIN bus traffic nor to the ECU and therefore no damage can occur.

Loss of Ground

In case of an interrupted ECU ground connection the LIN pin is in high impedance state. There is no impact to the LIN bus traffic nor to the ECU and therefore no damage can occur.

Short circuit to battery

The transmitter output current is limited to the specified value in case of short circuit to battery in order to protect the MLX80001 itself against high current densities. Otherwise the micro of the master ECU or the slave nodes will not detect any bus traffic until the failure disappears and will switch into sleep mode.

Ground shift and short circuit to ground

If the LIN wire is shorted to negative shifted ground levels, there is no current flow from the ECU ground to the LIN bus and no distortion of the LIN bus traffic.

A permanent failure current from battery via LIN short to ground can be reduced dramatically by disconnection of the master pull up resistor. The following different situations may occur:

- The master node is in sleep mode, there is no bus traffic at any channel. If a short circuit to ground is applied to a LIN network, the H ->L transition will awakens the shorted LIN network and the master node. Due to the wake up source recognition the master is able to detect the wake up channel and will not awaken the other LIN networks too. If there is no bus traffic possible with the shorted network, the connected nodes will go to sleep mode again and the failure current to ground is limited. If the failure disappears, the high resistive termination is able to drive a recessive voltage level and the master node and the network will wake up due to the L->H transition.
- The master node is busy and there is bus traffic on one or more connected LIN networks. If a short circuit to ground is applied to a LIN network, the integrated RxD timeout circuit will disconnect the master pull up resistor from the shorted LIN network (high resistive termination present now). The failure current to ground is limited and the thermal overload condition of the MLX80001 is removed without any intervention of the micro. If the failure disappears, the RxD L->H transition will reset the RxD timer circuit and the master termination will be reconnected to the LIN network.

Thermal overload

The MLX80001 is protected against thermal overloads.
Independent from the source of a LIN bus transmission (master channel1...4 or any slave node), the most significant part of the power dissipation will be produced in the master pull up resistor(s) during normal operation. Assuming a duty cycle of 50% and all channels are busy by bus traffic, the chip only can exceed the specified trip off temperature if the ambient temperature is higher than the specified maximum of125°C.
Due to failure situations such as short of a LIN channel vs. battery voltage or ground, the power dissipation can become higher than expected in the operating temperature range.
In these situations any transmit path will be interrupted and any master pull up resistor will be disconnected from the LIN interfaces until thermal recovery, independent from the operating mode of the MLX80001 and without any intervention of the micro. The thermal shutdown can be detected by the micro due to the active low interrupt applied to any RxD output.
Usually the short to ground situation is covered by the sleep mode behaviour or the RxD timeout feature for each channel. Thereby very high system availability is guaranteed.

Undervoltage Vs

If the supply voltage is missing or will be decreased under the specified value, the transmitter is switched off to prevent undefined LIN bus traffic. If the supply voltage is in the range of Vs = 5V…7V (low battery operation), the transmitter operates in the mode as indicated by the MODE0/1 pins. Communication can not be guaranteed under all worst case conditions (plug & play specification of LIN2.x and SAE J2602 standard is defined from 7V…18V IC battery supply voltage).

Overvoltage Vs

If the supply voltage is in the range of Vs = 18V…26.5, the transmitter operates in the mode as indicated by the MODE0/1 pins. In case of multi channel bus traffic the power consumption can exceed the expected maximum value for the normal operation voltage range up to Vs = 18V and the thermal overload protection will operate as described above. Communication can not be guaranteed under all worst case conditions (plug & play specification of LIN2.x and SAE J2602 standard is defined from 7V..18V IC battery supply voltage).

5. Application Hints

5.1 Bus loading requirements

Parameter	Symbol	Min	Typ	Max	Unit
Operating voltage range	V_{BAT}	8		18	V
Voltage drop of reverse protection diode	V_{Drop_rev}	0.4	0.7	1	V
Voltage drop at the serial diode in pull up path	$V_{SerDiode}$	0.4	0.7	1	V
Battery shift voltage	V_{Shift_BAT}	0		0.1	V_{BAT}
Ground shift voltage	V_{Shift_GND}	0		0.1	V_{BAT}
Master termination resistor	R_{master}	900	1000	1100	Ω
Slave termination resistor	R_{slave}	20	30	60	kΩ
Number of system nodes	N	2		16	
Total length of bus line	LEN_{BUS}			40	m
Line capacitance	C_{LINE}		100	150	pF/m
Capacitance of master node	C_{Master}		220		pF
Capacitance of slave node	C_{Slave}	195	220	300	pF
Total capacitance of the bus including slave and master capacitance	C_{BUS}	0.47	4	10	nF
Network Total Resistance	$R_{Network}$	500		862	Ω
Time constant of overall system	τ	1		5	µs

Table 1 - Bus loading requirements

5.2 Duty Cycle Calculation

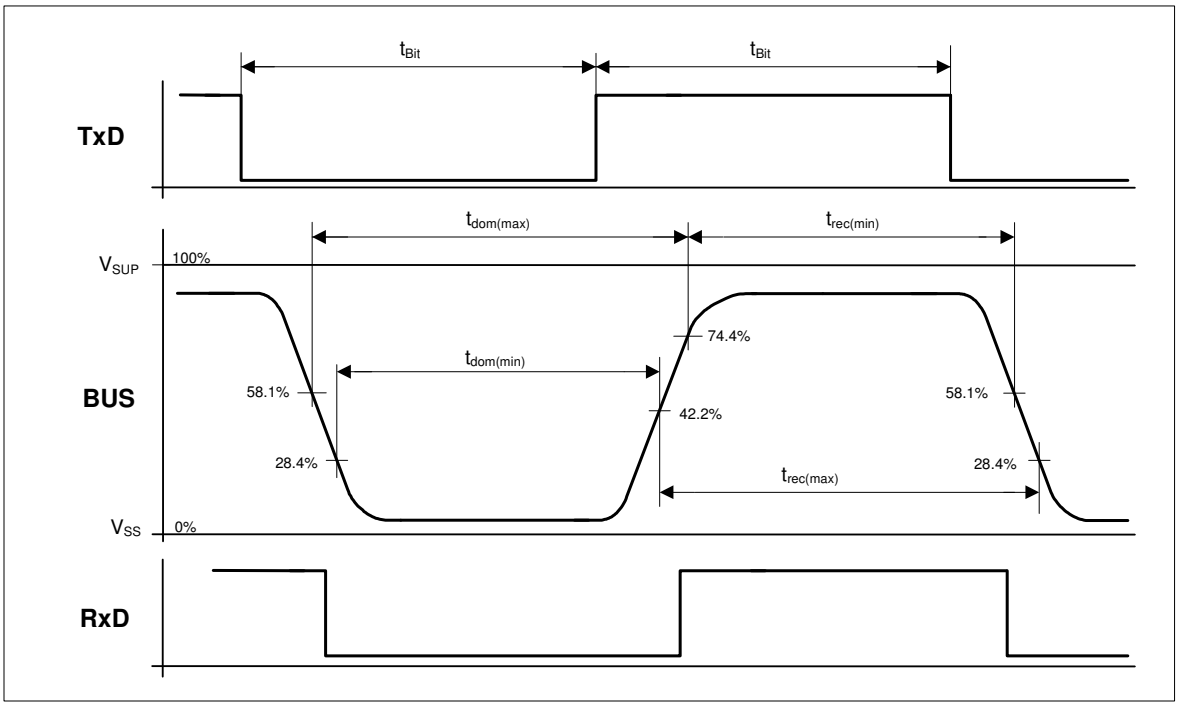


Figure 7 - Duty cycle calculation in accordance to LIN 2.x

With the timing parameters shown in Figure 7 two duty cycles , based on $t_{rec(min)}$ and $t_{rec(max)}$ can be calculated as follows :

$$D1 = t_{rec(min)} / (2 * t_{Bit})$$
$$D2 = t_{rec(max)} / (2 * t_{Bit})$$

For proper operation at 20KBit/s (t_{Bit} = 50µs) the LIN driver has to fulfill the duty cycles specified in chapter 2.4 for supply voltages of 7 to 18V and the defined standard loads .

Due to this simplified definition there is no need to measure slew rates, slope times, transmitter delays and dominant voltage levels as specified in the LIN physical layer specification 1.3.

The device within the D1/D2 duty cycle range operates also in applications with reduced bus speed of 10.4KBit/s or below.

In order to minimize EME, the slew rates of the transmitter can be reduced (approximately by 2 times). Such devices have to fulfill the duty cycle definition D3/D4 in the LIN physical layer specification 2.x. Devices within this duty cycle range cannot operate in 20KBit/s applications.

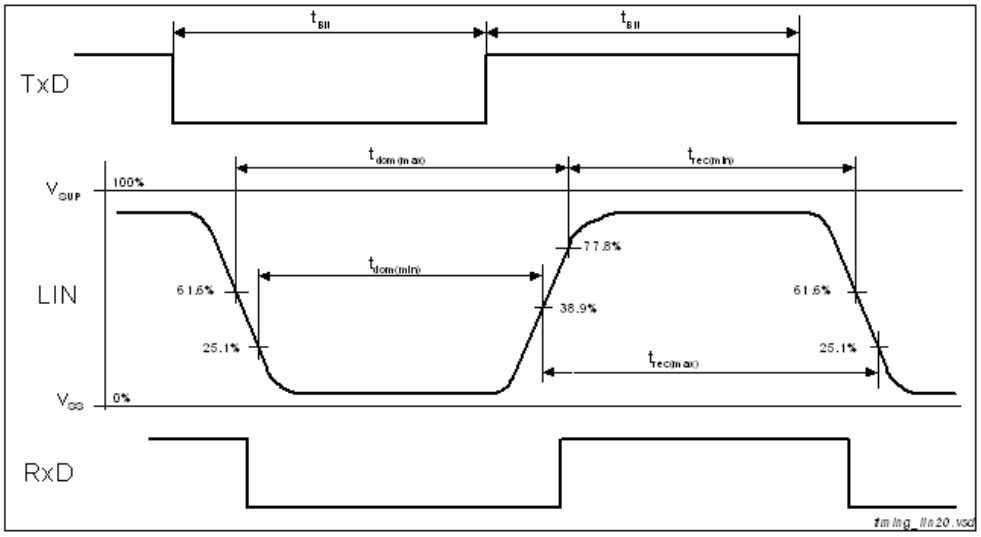


Figure 8 - Duty cycle measurement in accordance to LIN 2.x for baud rates of 10.4Kbps

With the timing parameters shown in the above diagram two duty cycles , based on trec(min) and trec(max) can be calculated as follows : tBit =96µs

D3 = trec(min) / (2 x tBit)

D4 = trec(max) / (2 x tBit)

5.3 Application Circuitry

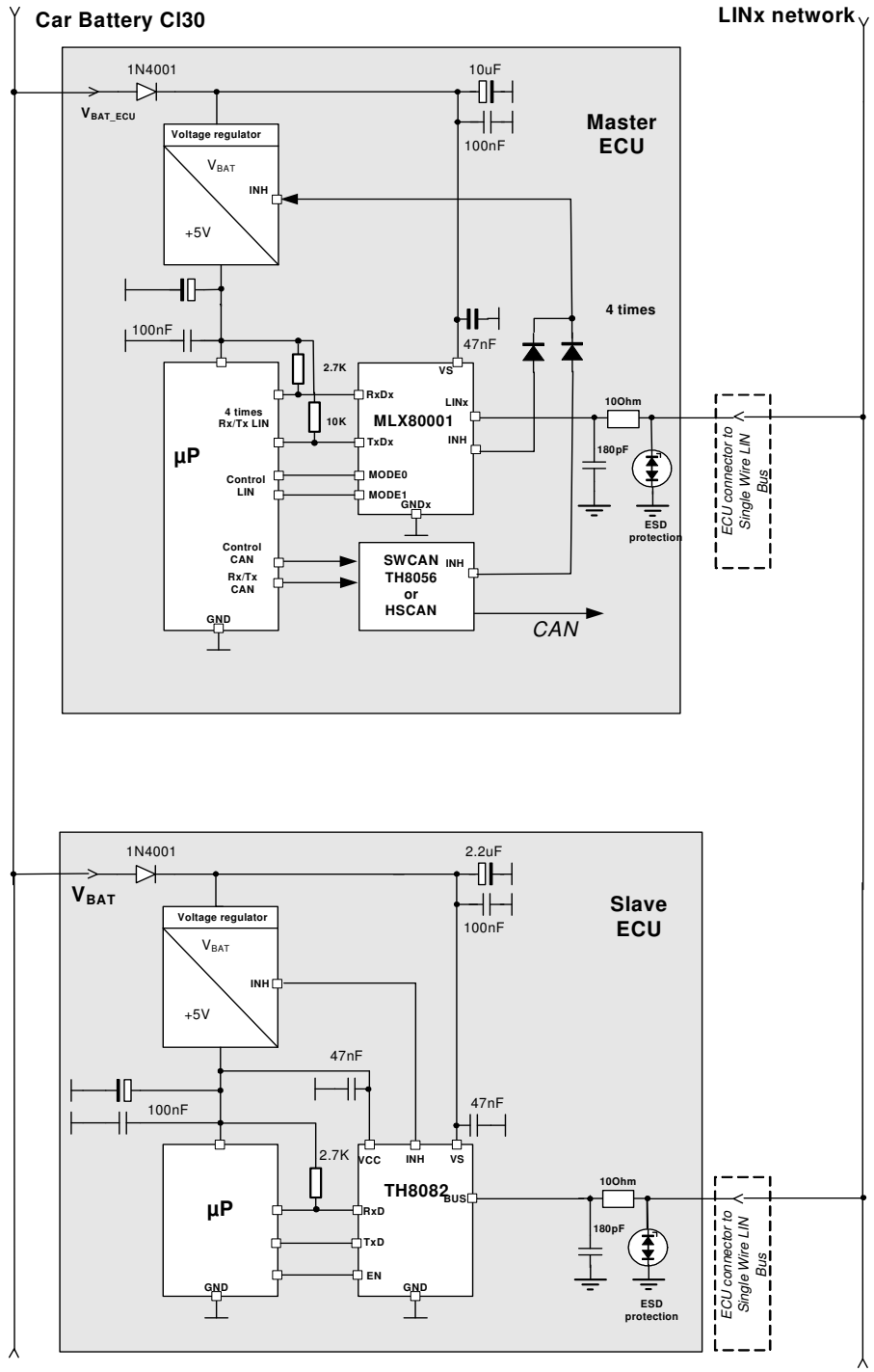


Figure 9 - Typical application circuitry of the MLX80001

6. Pin Description

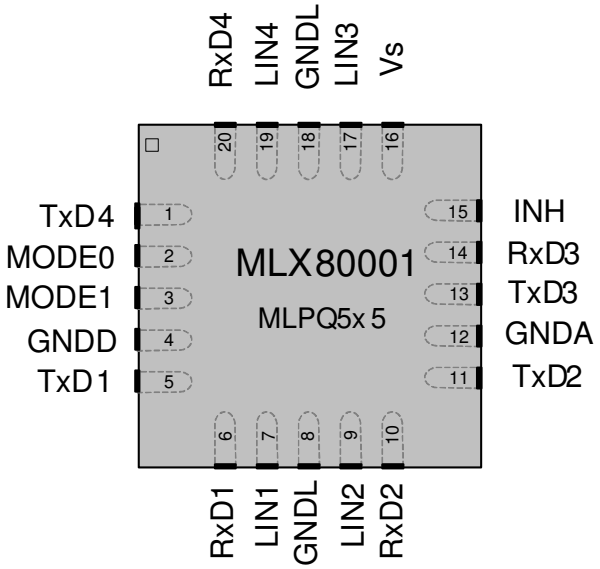
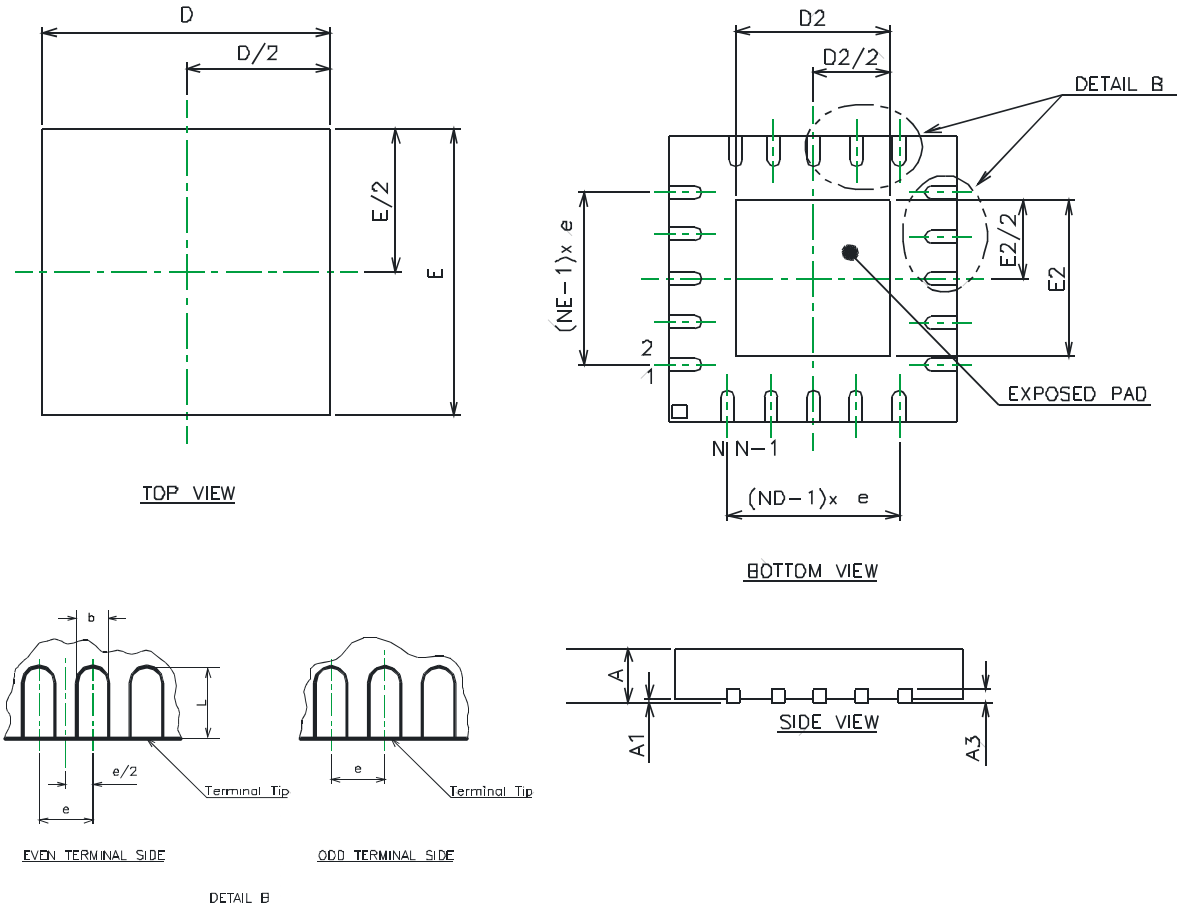


Figure 10 - Pin description MLPQ 20 package

Pin	Name	IO-Typ	Description
1	TxD4	I	Transmit data to LIN4
2	MODE0	I	Mode control pin
3	MODE1	I	Mode control pin
4	GNDD	P	Ground for digital core
5	TxD1	I	Transmit data to LIN1
6	RxD1	O	Receive data from LIN1
7	LIN1	I/O	Interface to LIN bus ,channel 1
8	GNDL	P	Power ground for LIN1&2
9	LIN2	I/O	Interface to LIN bus ,channel 1
10	RxD2	O	Receive data from LIN2
11	TxD2	I	Transmit data to LIN2
12	GNDA	P	Ground for analogue core
13	TxD3	I	Transmit data to LIN3
14	RxD3	O	Receive data from LIN3
15	INH	O	Control output for voltage regulator
16	Vs	P	Battery supply voltage
17	LIN3	I/O	Interface to LIN bus ,channel 3
18	GNDL	P	Power ground for LIN3&4
19	LIN4	I/O	Interface to LIN bus ,channel 4

20	RxD4	O	Receive data from LIN4

7. Mechanical Specification MLPQ5x5 20



	A	A1	A3	b[1]	D	D2	E	E2	e	L	N [6][3]	ND [5]	NE [5]
All Dimension in mm, coplanarity < 0.1 mm													
Min	0.8	0		0.25		3.00		3.00		0.45			
nom	0.90	0.02	0.20	0.30	5.00	3.15	5.00	3.15	0.65	0.55	20	5	5
max	1.00	0.05		0.35		3.25		3.25		0.65			

[1] Dimensions and tolerances conform to ASME Y14.5M-1994
[2] All dimensions are in Millimeters. All angels are in degrees
[3] N is the total number of terminals
[4] Dimension b applies to metallized terminal and is measured between 0.25 and 0.30mm from terminal tip
[5] ND and NE refer to the number of terminals on each D and E side respectively
[6] Depopulation is possible in a symmetrical fashion

8. ESD/EMC Remarks

- The MLX80001 is designed for automotive environments. Typical ESD - and EMC events the device can withstand are defined in chapter 2.2 'Absolute maximum ratings '.

- The application circuit board should be designed related to the board layout requirements in the SAE J2602 chapter 7.6.2. .

- The MLX80001 is an ESD sensitive device and should be handled according to guideline EN100015/ part1 (" The protection of ESD sensitive devices ")

9. Revision History

Version	Changes	Remark	Date
001		1st Release	March 2007
002	Update of order code		June 2011
003	Order code, logo, disclaimer, information regarding solderability		June 2012

10. Standard information regarding manufacturability of Melexis products with different soldering processes

Our products are classified and qualified regarding soldering technology, solderability and moisture sensitivity level according to following test methods:

Reflow Soldering SMD's (Surface Mount Devices)

- IPC/JEDEC J-STD-020
  Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
  (classification reflow profiles according to table 5-2)
- EIA/JEDEC JESD22-A113
  Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing
  (reflow profiles according to table 2)

Wave Soldering SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EN60749-20
  Resistance of plastic- encapsulated SMD's to combined effect of moisture and soldering heat
- EIA/JEDEC JESD22-B106 and EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

Iron Soldering THD's (Through Hole Devices)

- EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

Solderability SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EIA/JEDEC JESD22-B102 and EN60749-21
  Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

Melexis is contributing to global environmental conservation by promoting **lead free** solutions. For more information on qualifications of **RoHS** compliant products (RoHS = European directive on the Restriction Of the use of certain Hazardous Substances) please visit the quality page on our website: http://www.melexis.com/quality.aspx

11. Disclaimer

Devices sold by Melexis are covered by the warranty and patent indemnification provisions appearing in its Term of Sale. Melexis makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. Melexis reserves the right to change specifications and prices at any time and without notice. Therefore, prior to designing this product into a system, it is necessary to check with Melexis for current information. This product is intended for use in normal commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life-sustaining equipment are specifically not recommended without additional processing by Melexis for each application.

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