16Mb LW R-R HSTL High Speed Synchronous SRAMs (512Kb x 36 or 1Mb x 18) **Preliminary**

Description

The CXK77N36R160GB (organized as 524,288 words by 36 bits) and the CXK77N18R160GB (organized as 1,048,576 words by 18 bits) are high speed CMOS synchronous static RAMs with common I/O pins. These synchronous SRAMs integrate input registers, high speed RAM, output registers, and a one-deep write buffer onto a single monolithic IC. Register - Register (R-R) read operations and Late Write (LW) write operations are supported, providing a high-performance user interface.

All address and control input signals except $\overline{G}$ (Output Enable) and ZZ (Sleep Mode) are registered on the rising edge of the K differential input clock.

During read operations, output data is driven valid from the rising edge of K, one full clock cycle after address is registered.

During write operations, input data is registered on the rising edge of K, one full clock cycle after address is registered.

Sleep (power down) capability is provided via the ZZ input signal.

Output drivers are series terminated, and output impedance is programmable via the ZQ input pin. By connecting an external control resistor RQ between ZQ and V_{SS}, the impedance of all data output drivers can be precisely controlled.

333 MHz operation is obtained from a single 1.8V or 2.5V power supply. JTAG boundary scan interface is provided using a subset of IEEE standard 1149.1 protocol.

Features

- 3 Speed Bins

3 Speed Bins	Cycle Time / Access Time
-3	3.0ns / 1.5ns
-33	3.3ns / 1.7ns
-4	4.0ns / 2.0ns

- Single 1.8V or 2.5V power supply (V_{DD}): 1.8V ± 0.1V or 2.5V ± 5%
- Dedicated output supply voltage (V_{DDQ}): 1.5V or 1.8V typical
- HSTL-compatible I/O interface with dedicated input reference voltage (V_{REF}): $V_{DDQ}/2$ typical
- Register - Register (R-R) read protocol
- Late Write (LW) write protocol
- Full read/write coherency
- Byte Write capability
- Differential input clocks (K/$\overline{K}$)
- Asynchronous output enable ($\overline{G}$)
- Sleep (power down) mode via dedicated mode pin (ZZ)
- Programmable output driver impedance
- JTAG boundary scan (subset of IEEE standard 1149.1)
- 119 pin (7x17), 1.27mm pitch, 14mm x 22mm Ball Grid Array (BGA) package

512Kb x 36 Pin Assignment (Top View)

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	SA	SA	NC (32M)	SA	SA	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQc	DQc	V_{SS}	ZQ	V_{SS}	DQb	DQb
E	DQc	DQc	V_{SS}	$\overline{SS}$	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	$\overline{G}$	V_{SS}	DQb	V_{DDQ}
G	DQc	DQc	$\overline{SBW}$c	NC	$\overline{SBW}$b	DQb	DQb
H	DQc	DQc	V_{SS}	NC	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	V_{REF}	V_{DD}	V_{REF}	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	K	V_{SS}	DQa	DQa
L	DQd	DQd	$\overline{SBW}$d	$\overline{K}$	$\overline{SBW}$a	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	$\overline{SW}$	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
P	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
R	NC	SA	M1 (1)	V_{DD}	M2 (2)	SA	NC
T	NC	NC (x18)	SA	SA (x36)	SA	NC (x18)	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	RSVD (3)	V_{DDQ}

Notes:

1. Pad Location 3R is defined as an M1 mode pin in LW SRAMs. However, it must be tied “low” in this device.
2. Pad Location 5R is defined as an M2 mode pin in LW SRAMs. However, it must be tied “high” in this device.
3. Pad Location 6U must be left unconnected. It is used by Sony for internal test purposes.

1Mb x 18 Pin Assignment (Top View)

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	SA	SA	NC (32M)	SA	SA	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQb	NC	V_{SS}	ZQ	V_{SS}	DQa	NC
E	NC	DQb	V_{SS}	$\overline{SS}$	V_{SS}	NC	DQa
F	V_{DDQ}	NC	V_{SS}	$\overline{G}$	V_{SS}	DQa	V_{DDQ}
G	NC	DQb	$\overline{SBW}$b	NC	V_{SS}	NC	DQa
H	DQb	NC	V_{SS}	NC	V_{SS}	DQa	NC
J	V_{DDQ}	V_{DD}	V_{REF}	V_{DD}	V_{REF}	V_{DD}	V_{DDQ}
K	NC	DQb	V_{SS}	K	V_{SS}	NC	DQa
L	DQb	NC	V_{SS}	$\overline{K}$	$\overline{SBW}$a	DQa	NC
M	V_{DDQ}	DQb	V_{SS}	$\overline{SW}$	V_{SS}	NC	V_{DDQ}
N	DQb	NC	V_{SS}	SA	V_{SS}	DQa	NC
P	NC	DQb	V_{SS}	SA	V_{SS}	NC	DQa
R	NC	SA	M1 (1)	V_{DD}	M2 (2)	SA	NC
T	NC	SA (x18)	SA	NC (x36)	SA	SA (x18)	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	RSVD (3)	V_{DDQ}

Notes:

1. Pad Location 3R is defined as an M1 mode pin in LW SRAMs. However, it must be tied “low” in this device.
2. Pad Location 5R is defined as an M2 mode pin in LW SRAMs. However, it must be tied “high” in this device.
3. Pad Location 6U must be left unconnected. It is used by Sony for internal test purposes.

Pin Description

Symbol	Type	Description
SA	Input	Synchronous Address Inputs - Registered on the rising edge of K.
DQa, DQb DQc, DQd	I/O	Synchronous Data Inputs / Outputs - Registered on the rising edge of K during write operations. Driven from the rising edge of K during read operations. DQa - indicates Data Byte a DQb - indicates Data Byte b DQc - indicates Data Byte c DQd - indicates Data Byte d
K, $\overline{K}$	Input	Differential Input Clocks
$\overline{SS}$	Input	Synchronous Select Input - Registered on the rising edge of K. $\overline{SS}$ = 0 enables the device to accept read and write commands $\overline{SS}$ = 1 disables the device
$\overline{SW}$	Input	Synchronous Global Write Enable Input - Registered on the rising edge of K. $\overline{SW}$ = 0 specifies a write operation when the device is enabled $\overline{SW}$ = 1 specifies a read operation when the device is enabled
$\overline{SBW}$a, $\overline{SBW}$b, $\overline{SBW}$c, $\overline{SBW}$d	Input	Synchronous Byte Write Enable Inputs - Registered on the rising edge of K. $\overline{SBW}$a = 0 specifies write Data Byte a during a write operation $\overline{SBW}$b = 0 specifies write Data Byte b during a write operation $\overline{SBW}$c = 0 specifies write Data Byte c during a write operation $\overline{SBW}$d = 0 specifies write Data Byte d during a write operation
$\overline{G}$	Input	Asynchronous Output Enable Input - Deasserted (high) disables the data output drivers.
ZZ	Input	Asynchronous Sleep Mode Input - Asserted (high) forces the SRAM into low-power mode.
M1, M2	Input	Read Operation Protocol Select - These mode pins must be tied “low” and “high” respectively to select Register - Register read operations.
ZQ	Input	Output Driver Impedance Control Resistor Input - This pin must be connected to V_{SS} through an external resistor RQ to program data output driver impedance. See the Programmable Output Driver Impedance section for further information.
V_{DD}		1.8V or 2.5V Core Power Supply - Core supply voltage.
V_{DDQ}		Output Power Supply - Output buffer supply voltage.
V_{REF}		Input Reference Voltage - Input buffer threshold voltage.
V_{SS}		Ground
TCK	Input	JTAG Clock
TMS	Input	JTAG Mode Select - Weakly pulled “high” internally.
TDI	Input	JTAG Data In - Weakly pulled “high” internally.
TDO	Output	JTAG Data Out
RSVD		Reserved - This pin is used for Sony test purposes only. It must be left unconnected.
NC		No Connect - These pins are true no-connects, i.e. there is no internal chip connection to these pins. They can be left unconnected or tied directly to V_{DD}, V_{DDQ}, or V_{SS}.

•Clock Truth Table

K	ZZ	$\overline{SS}$ (t_n)	$\overline{SW}$ (t_n)	$\overline{SBW}x$ (t_n)	$\overline{G}$	Operation	DQ (t_n)	DQ (t_{n+1})
X	1	X	X	X	X	Sleep (Power Down) Mode	Hi - Z	Hi - Z
↑	0	1	X	X	X	Deselect	***	Hi - Z
↑	0	0	1	X	1	Read	Hi - Z	Hi - Z
↑	0	0	1	X	0	Read	***	Q(t_n)
↑	0	0	0	0	X	Write All Bytes	***	D(t_n)
↑	0	0	0	X	X	Write Bytes With $\overline{SBW}x$ = 0	***	D(t_n)
↑	0	0	0	1	X	Abort Write	***	Hi - Z

Notes:

1. “1” = input “high”; “0” = input “low”; “X” = input “don’t care”.
2. “***” indicates that the input requirement or output state is determined by the previous operation.
3. DQs are tri-stated in response to Write and Deselect commands, one cycle after the command is sampled.

•Sleep (Power Down) Mode

Sleep (power down) mode is provided through the asynchronous input signal ZZ. When ZZ is asserted (high), the output drivers are disabled and the SRAM begins to draw standby current. Contents of the memory array are preserved. An enable time (t_{ZZE}) must be met before the SRAM is guaranteed to be in sleep mode, and a recovery time (t_{ZZR}) must be met before the SRAM can resume normal operation.

•Programmable Output Driver Impedance

These devices have programmable impedance output drivers. The output impedance is controlled by an external resistor RQ connected between the SRAM’s ZQ pin and V_{SS}, and is equal to one-fifth the value of this resistor, nominally. See the DC Electrical Characteristics section for further information.

Output Driver Impedance Power-Up Requirements

Output driver impedance will reach the programmed value within 8192 cycles after power-up. Consequently, it is recommended that Read operations not be initiated until after the initial 8192 cycles have elapsed.

Output Driver Impedance Updates

Output driver impedance is updated during Write and Deselect operations when the output driver is disabled.

•Power-Up Sequence

For reliability purposes, Sony recommends that power supplies power up in the following sequence: V_{SS}, V_{DD}, V_{DDQ}, V_{REF}, and Inputs. V_{DDQ} should never exceed V_{DD}. If this power supply sequence cannot be met, a large bypass diode may be required between V_{DD} and V_{DDQ}. Please contact Sony Memory Application Department for further information.

•Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Supply Voltage	V_{DD}	-0.5 to +3.2	V
Output Supply Voltage	V_{DDQ}	-0.5 to +2.3	V
Input Voltage (Address, Control, Data, Clock)	V_{IN}	-0.5 to V_{DDQ} + 0.5 (2.3V max)	V
Input Voltage (M1, M2)	V_{MIN}	-0.5 to V_{DD} + 0.5 (3.2V max)	V
Input Voltage (TCK, TMS, TDI))	V_{TIN}	-0.5 to +3.8	V
Operating Temperature	T_A	0 to 85	°C
Junction Temperature	T_J	0 to 110	°C
Storage Temperature	T_{STG}	-55 to 150	°C

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions other than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

•BGA Package Thermal Characteristics

Parameter	Symbol	Rating	Units
Junction to Case Temperature	Θ_{JC}	3.6	°C/W

•I/O Capacitance

(T_A = 25°C, f = 1 MHz)

Parameter		Symbol	Test Conditions	Min	Max	Units
Input Capacitance	Address	C_{IN}	V_{IN} = 0V	---	4.0	pF
	Control	C_{IN}	V_{IN} = 0V	---	4.0	pF
	Clock	C_{KIN}	V_{KIN} = 0V	---	4.5	pF
Output Capacitance	Data	C_{OUT}	V_{OUT} = 0V	---	5.0	pF

Note: These parameters are sampled and are not 100% tested.

•DC Recommended Operating Conditions

(V_{SS} = 0V, T_A = 0 to 85°C)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Supply Voltage	V_{DD}	1.7	1.8 or 2.5	2.63	V	
Output Supply Voltage	V_{DDQ}	1.4	1.5 or 1.8	1.9	V	
Input Reference Voltage	V_{REF}	V_{DDQ}/2 - 0.1	V_{DDQ}/2	V_{DDQ}/2 + 0.1	V	1
Input High Voltage (Address, Control, Data)	V_{IH}	V_{REF} + 0.1	---	V_{DDQ} + 0.3	V	2
Input Low Voltage (Address, Control, Data)	V_{IL}	-0.3	---	V_{REF} - 0.1	V	3
Input High Voltage (M1, M2)	V_{MIH}	V_{REF} + 0.3	---	V_{DD} + 0.3	V	
Input Low Voltage (M1, M2)	V_{MIL}	-0.3	---	V_{REF} - 0.3	V	
Clock Input Signal Voltage	V_{KIN}	-0.3	---	V_{DDQ} + 0.3	V	
Clock Input Differential Voltage	V_{DIF}	0.2	---	V_{DDQ} + 0.6	V	
Clock Input Common Mode Voltage	V_{CM}	V_{DDQ}/2 - 0.1	V_{DDQ}/2	V_{DDQ}/2 + 0.1	V	

1. The peak-to-peak AC component superimposed on V_{REF} may not exceed 5% of the DC component.
2. V_{IH} (max) AC = V_{DDQ} + 0.9V for pulse widths less than one-quarter of the cycle time (t_{CYC}/4).
3. V_{IL} (min) AC = -0.9V for pulse widths less than one-quarter of the cycle time (t_{CYC}/4).

•DC Electrical Characteristics

(V_{DD} = 1.8V ± 0.1V or 2.5V ± 5%, V_{SS} = 0V, T_A = 0 to 85°C)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units	Notes
Input Leakage Current (Address, Control, Clock)	I_{LI}	$V_{IN} = V_{SS}$ to V_{DDQ}	-5	---	5	uA	
Input Leakage Current (M1, M2)	I_{MLI}	$V_{MIN} = V_{SS}$ to V_{DD}	-10	---	10	uA	
Output Leakage Current	I_{LO}	$V_{OUT} = V_{SS}$ to V_{DDQ} $\overline{G} = V_{IH}$	-10	---	10	uA	
Average Power Supply Operating Current	I_{DD-3} I_{DD-33} I_{DD-4}	I_{OUT} = 0 mA $\overline{SS} = V_{IL}$, $ZZ = V_{IL}$	--- --- ---	--- --- ---	550 500 450	mA	
Power Supply Standby Current	I_{SB}	I_{OUT} = 0 mA $ZZ = V_{IH}$	---	---	160	mA	1
Output High Voltage	V_{OH}	I_{OH} = -6.0 mA RQ = 250Ω	V_{DDQ} - 0.4	---	---	V	
Output Low Voltage	V_{OL}	I_{OL} = 6.0 mA RQ = 250Ω	---	---	0.4	V	
Output Driver Impedance	R_{OUT}	V_{OH}, V_{OL} = V_{DDQ}/2 RQ < 150Ω	---	---	35 (30*1.15)	Ω	2
		V_{OH}, V_{OL} = V_{DDQ}/2 150Ω ≤ RQ ≤ 300Ω	(RQ/5)* 0.85	RQ/5	(RQ/5)* 1.15	Ω	
		V_{OH}, V_{OL} = V_{DDQ}/2 RQ > 300Ω	51 (60*0.85)	---	---	Ω	3

1. This parameter is guaranteed at T_A = 0 to 55°C.
2. For maximum output drive (i.e. minimum impedance), the ZQ pin can be tied directly to V_{SS}.
3. For minimum output drive (i.e. maximum impedance), the ZQ pin can be left unconnected or tied to V_{DDQ}.

•AC Electrical Characteristics

(V_{DD} = 1.8V ± 0.1V or 2.5V ± 5%, V_{SS} = 0V, T_A = 0 to 85°C)

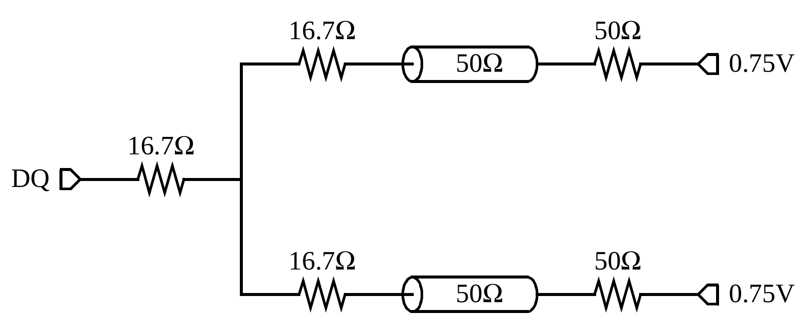
Parameter	Symbol	-3		-33		-4		Units	Notes
		Min	Max	Min	Max	Min	Max		
Input Clock Cycle Time	t_{KHKH}	3.0	---	3.3	---	4.0	---	ns	
Input Clock High Pulse Width	t_{KHKL}	1.2	---	1.3	---	1.5	---	ns	
Input Clock Low Pulse Width	t_{KLKH}	1.2	---	1.3	---	1.5	---	ns	
Address Input Setup Time	t_{AVKH}	0.5	---	0.5	---	0.5	---	ns	
Address Input Hold Time	t_{KHAX}	0.5	---	0.5	---	0.5	---	ns	
Write Enable Input Setup Time	t_{WVKH}	0.5	---	0.5	---	0.5	---	ns	
Write Enable Input Hold Time	t_{KHWX}	0.5	---	0.5	---	0.5	---	ns	
Sync Select Input Setup Time	t_{SVKH}	0.5	---	0.5	---	0.5	---	ns	
Sync Select Input Hold Time	t_{KHSX}	0.5	---	0.5	---	0.5	---	ns	
Data Input Setup Time	t_{DVKH}	0.5	---	0.5	---	0.5	---	ns	
Data Input Hold Time	t_{KHDX}	0.5	---	0.5	---	0.5	---	ns	
Input Clock High to Output Data Valid	t_{KHQV}	---	1.5	---	1.7	---	2.0	ns	
Input Clock High to Output Data Hold	t_{KHQX}	0.5	---	0.5	---	0.5	---	ns	1
Input Clock High to Output Data Low-Z	t_{KHQX1}	0.5	---	0.5	---	0.5	---	ns	1,2
Input Clock High to Output Data High-Z	t_{KHQZ}	---	1.7	---	1.9	---	2.2	ns	1,2
Output Enable Low to Output Data Valid	t_{GLQV}	---	1.7	---	1.9	---	2.2	ns	
Output Enable Low to Output Data Low-Z	t_{GLQX}	0.3	---	0.3	---	0.3	---	ns	1,2
Output Enable High to Output Data High-Z	t_{GHQZ}	---	1.7	---	1.9	---	2.2	ns	1,2
Sleep Mode Enable Time	t_{ZZE}	---	15	---	15	---	15	ns	1
Sleep Mode Recovery Time	t_{ZZR}	20	---	20	---	20	---	ns	1

1. These parameters are guaranteed by design through extensive corner-lot characterization.
2. These parameters are measured at ± 50mV from steady state voltage.

•AC Test Conditions (V_{DDQ} = 1.5V) (V_{DD} = 1.8V ± 0.1V or 2.5V ± 5%, V_{DDQ} = 1.5V ± 0.1V, T_A = 0 to 85°C)

Parameter	Symbol	Conditions	Units	Notes
Input Reference Voltage	V_{REF}	0.75	V	
Input High Level	V_{IH}	1.25	V	
Input Low Level	V_{IL}	0.25	V	
Input Rise & Fall Time		2.0	V/ns	
Input Reference Level		0.75	V	
Clock Input High Voltage	V_{KIH}	1.25	V	V_{DIF} = 1.0V
Clock Input Low Voltage	V_{KIL}	0.25	V	V_{DIF} = 1.0V
Clock Input Common Mode Voltage	V_{CM}	0.75	V	
Clock Input Rise & Fall Time		2.0	V/ns	
Clock Input Reference Level		K/$\overline{K}$ cross	V	
Output Reference Level		0.75	V	
Output Load Conditions		RQ = 250Ω		See Figure 1 below

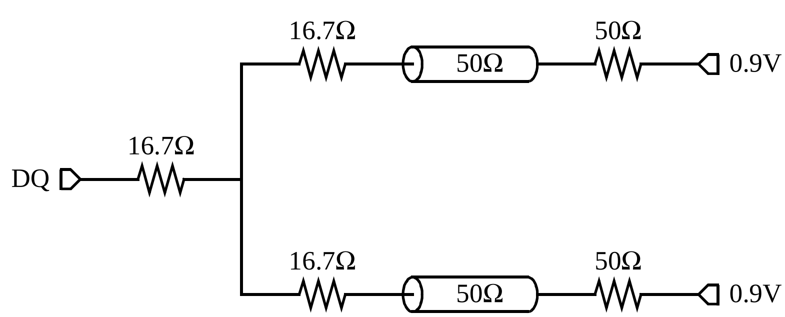
Figure 1: AC Test Output Load (V_{DDQ} = 1.5V)



•AC Test Conditions (V_{DDQ} = 1.8V) (V_{DD} = 1.8V ± 0.1V or 2.5V ± 5%, V_{DDQ} = 1.8V ± 0.1V, T_A = 0 to 85°C)

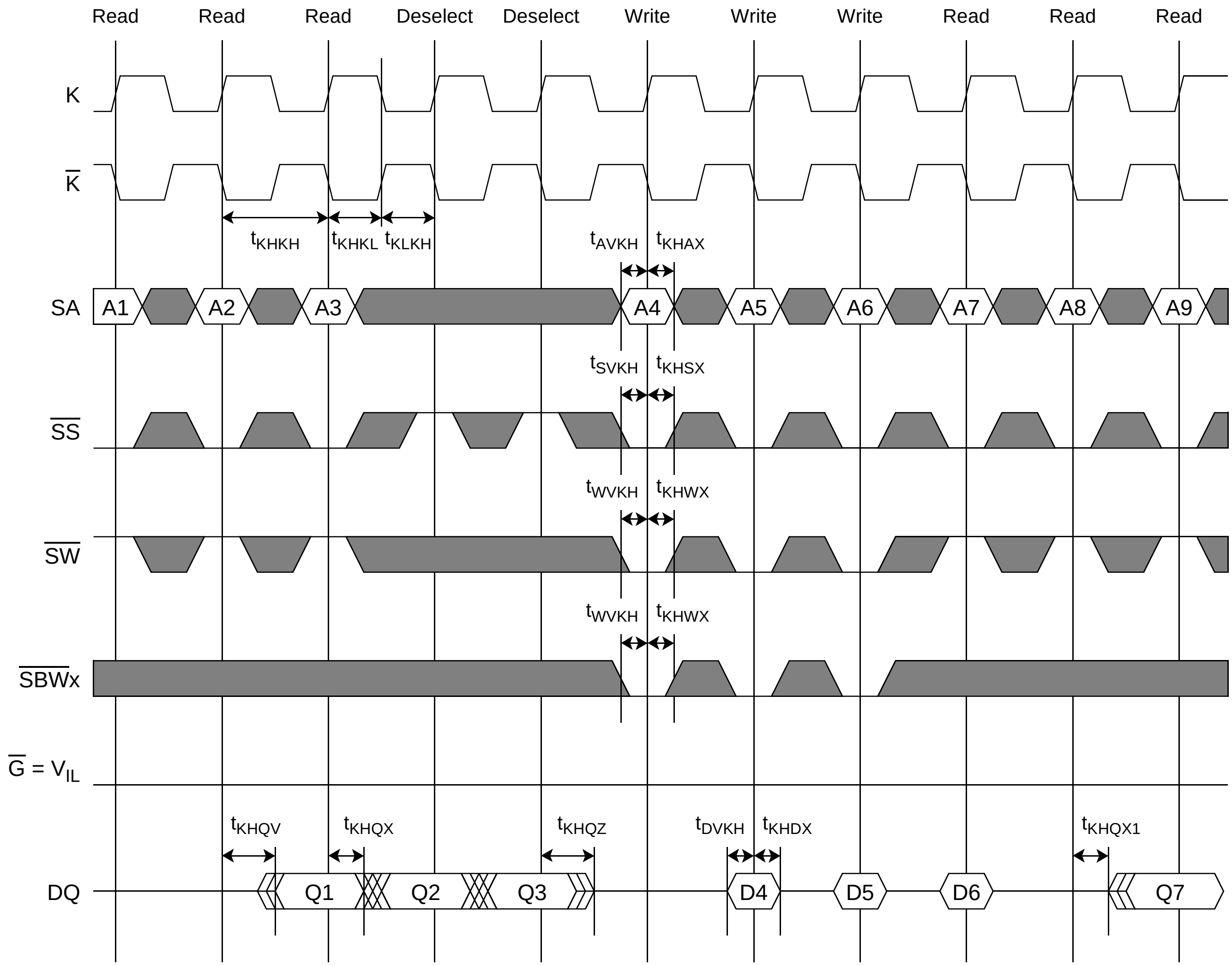
Parameter	Symbol	Conditions	Units	Notes
Input Reference Voltage	V_{REF}	0.9	V	
Input High Level	V_{IH}	1.4	V	
Input Low Level	V_{IL}	0.4	V	
Input Rise & Fall Time		2.0	V/ns	
Input Reference Level		0.9	V	
Clock Input High Voltage	V_{KIH}	1.4	V	V_{DIF} = 1.0V
Clock Input Low Voltage	V_{KIL}	0.4	V	V_{DIF} = 1.0V
Clock Input Common Mode Voltage	V_{CM}	0.9	V	
Clock Input Rise & Fall Time		2.0	V/ns	
Clock Input Reference Level		K/$\overline{K}$ cross	V	
Output Reference Level		0.9	V	
Output Load Conditions		RQ = 250Ω		See Figure 2 below

Figure 2: AC Test Output Load (V_{DDQ} = 1.8V)



Read-Write-Read Timing Diagram
Synchronously Controlled via $\overline{SS}$ and Deselect Operations ($\overline{G}$ = Low)

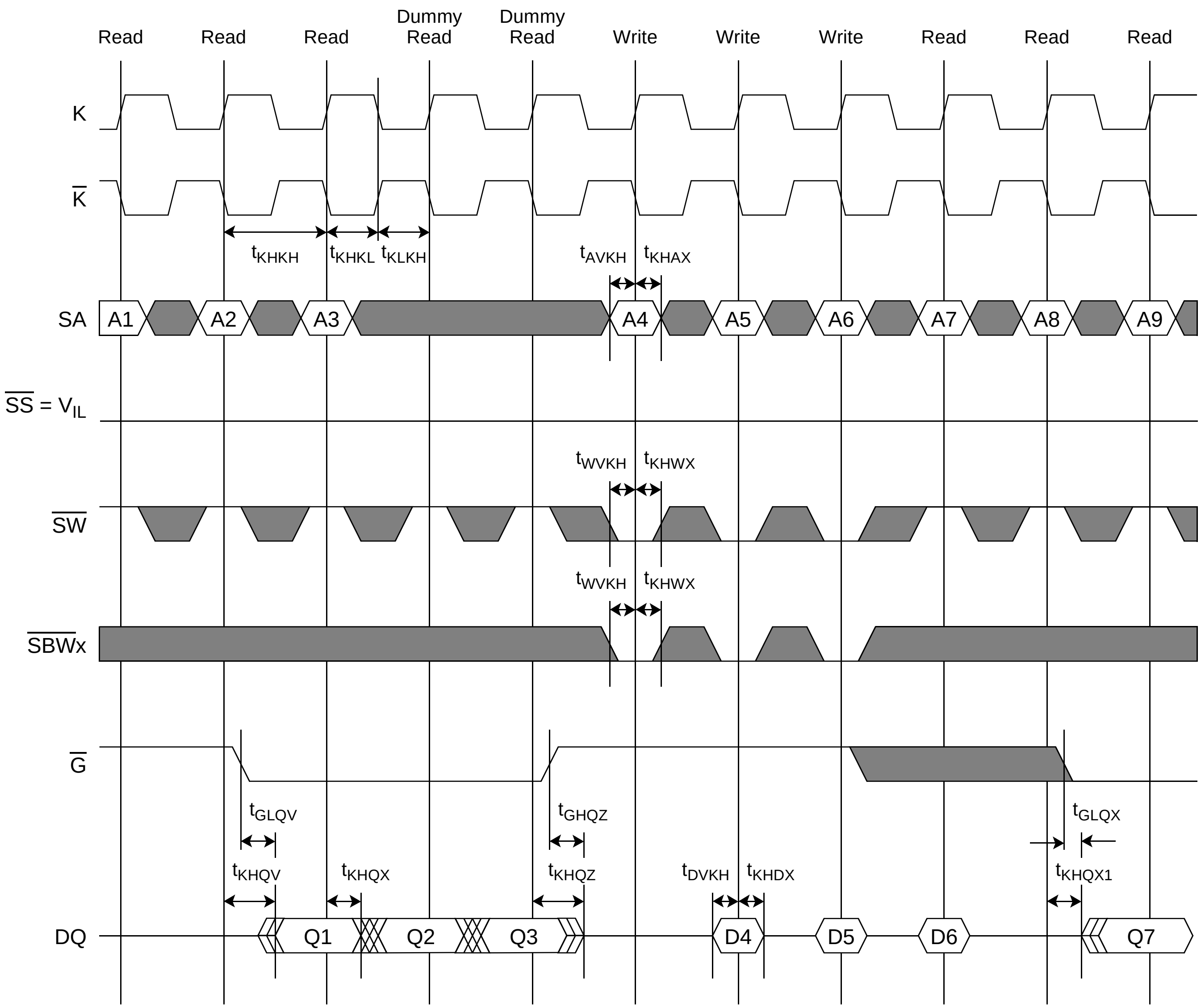
Figure 3



Note: In the diagram above, two Deselect operations are inserted between Read and Write operations to control the data bus transition from output to input. This depiction is for clarity purposes only. It is NOT a requirement. Depending on the application, one Deselect operation may be sufficient.

Read-Write-Read Timing Diagram
Asynchronously Controlled via $\overline{G}$ and Dummy Read Operations ($\overline{SS}$ = Low)

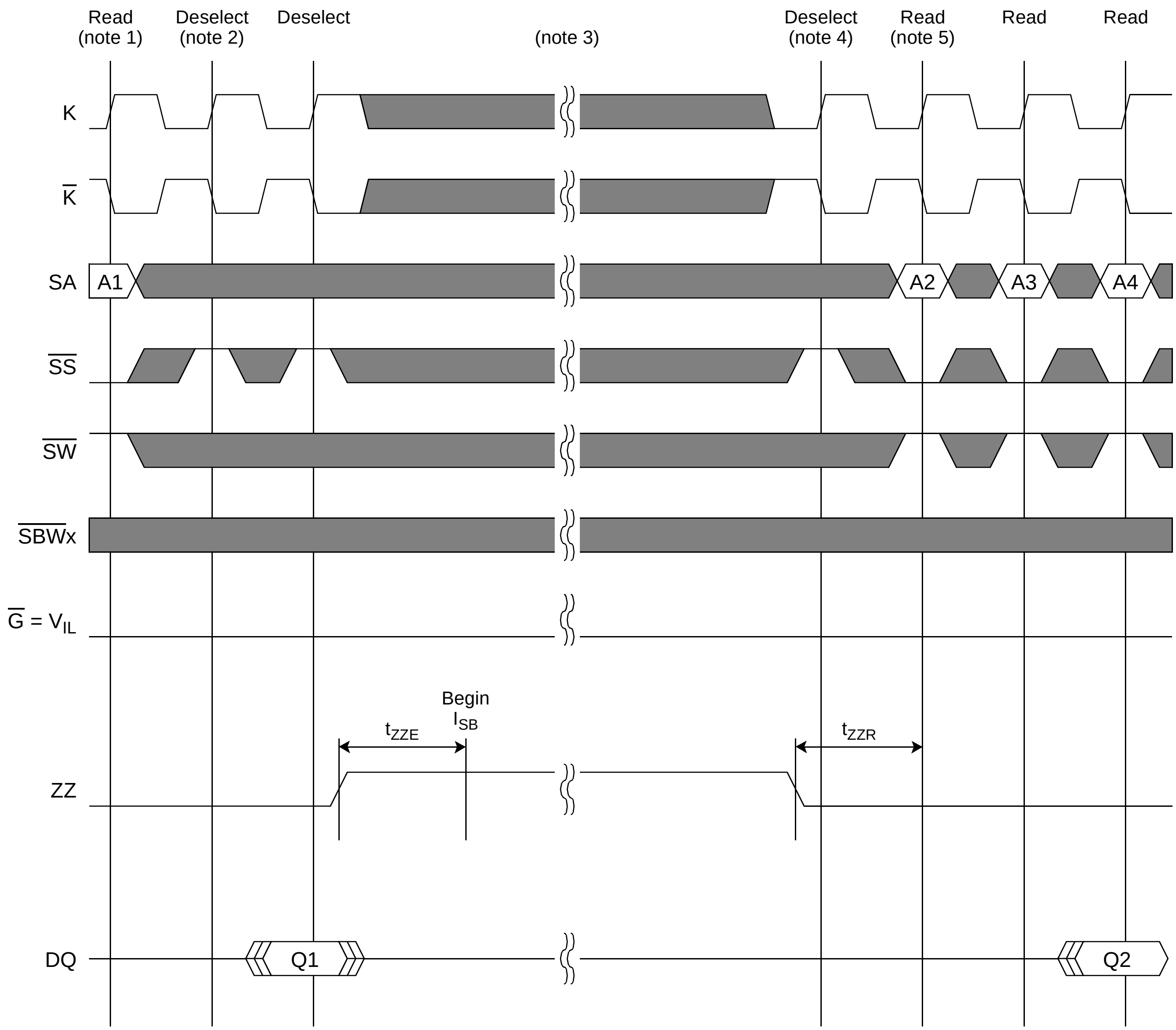
Figure 4



Note: In the diagram above, two Dummy Read operations are inserted between Read and Write operations to control the data bus transition from output to input. This depiction is for clarity purposes only. It is NOT a requirement. Depending on the application, one Dummy Read operation may be sufficient.

Sleep (Power-Down) Mode Timing Diagram

Figure 5



Notes:

1: This can be any operation. The depiction of a Read operation here is provided only as an example.

2: Before ZZ is asserted, at least two (2) Deselect operations must be initiated after the last Read or Write operation is initiated, in order to ensure the successful completion of the last Read or Write operation.

3: While ZZ is asserted, all of the SRAM's address, control, data, and clock inputs are ignored.

4: After ZZ is deasserted, Deselect operations must be initiated until the specified recovery time (t_{ZZR}) has been met. Read and Write operations may NOT be initiated during this time.

5: This can be any operation. The depiction of a Read operation here is provided only as an example.

•Test Mode Description

These devices provide a JTAG Test Access Port (TAP) and Boundary Scan interface using a limited set of IEEE std. 1149.1 functions. This test mode is intended to provide a mechanism for testing the interconnect between master (processor, controller, etc.), SRAMs, other components, and the printed circuit board.

In conformance with a subset of IEEE std. 1149.1, these devices contain a TAP Controller and four TAP Registers. The TAP Registers consist of one Instruction Register and three Data Registers (ID, Bypass, and Boundary Scan Registers).

The TAP consists of the following four signals:

TCK:	Test Clock	Induces (clocks) TAP Controller state transitions.
TMS:	Test Mode Select	Inputs commands to the TAP Controller. Sampled on the rising edge of TCK.
TDI:	Test Data In	Inputs data serially to the TAP Registers. Sampled on the rising edge of TCK.
TDO:	Test Data Out	Outputs data serially from the TAP Registers. Driven from the falling edge of TCK.

Disabling the TAP

When JTAG is not used, TCK should be tied "low" to prevent clocking the SRAM. TMS and TDI should either be tied "high" through a pull-up resistor or left unconnected. TDO should be left unconnected.

Note: Operation of the TAP does not interfere with normal SRAM operation except when the SAMPLE-Z instruction is selected. Consequently, TCK, TMS, and TDI can be controlled any number of ways without adversely affecting the functionality of the device.

JTAG DC Recommended Operating Conditions (V_{DD} = 1.8V ± 0.1V or 2.5V ± 5%, V_{SS} = 0V, T_A = 0 to 85°C)

Parameter	Symbol	Test Conditions	Min	Max	Units
JTAG Input High Voltage	V_{TIH}	---	1.4	3.6	V
JTAG Input Low Voltage	V_{TIL}	---	-0.3	0.8	V
JTAG Output High Voltage (CMOS)	V_{TOH}	I_{TOH} = -100uA	V_{DD} - 0.1	---	V
JTAG Output Low Voltage (CMOS)	V_{TOL}	I_{TOL} = 100uA	---	0.1	V
JTAG Output High Voltage (TTL)	V_{TOH}	I_{TOH} = -8.0mA	V_{DD} - 0.4	---	V
JTAG Output Low Voltage (TTL)	V_{TOL}	I_{TOL} = 8.0mA	---	0.4	V
JTAG Input Leakage Current	I_{TLI}	V_{TIN} = V_{SS} to 3.3V	-10	10	uA

JTAG AC Test Conditions

(V_{DD} = 1.8V ± 0.1V, V_{SS} = 0V, T_A = 0 to 85°C)

Parameter	Symbol	Conditions	Units	Notes
JTAG Input High Level	V_{TIH}	1.8	V	
JTAG Input Low Level	V_{TIL}	0.0	V	
JTAG Input Rise & Fall Time		1.0	V/ns	
JTAG Input Reference Level		0.9	V	
JTAG Output Reference Level		0.9	V	
JTAG Output Load Condition				See Fig.1 (page 10)

JTAG AC Test Conditions

(V_{DD} = 2.5V ± 5%, V_{SS} = 0V, T_A = 0 to 85°C)

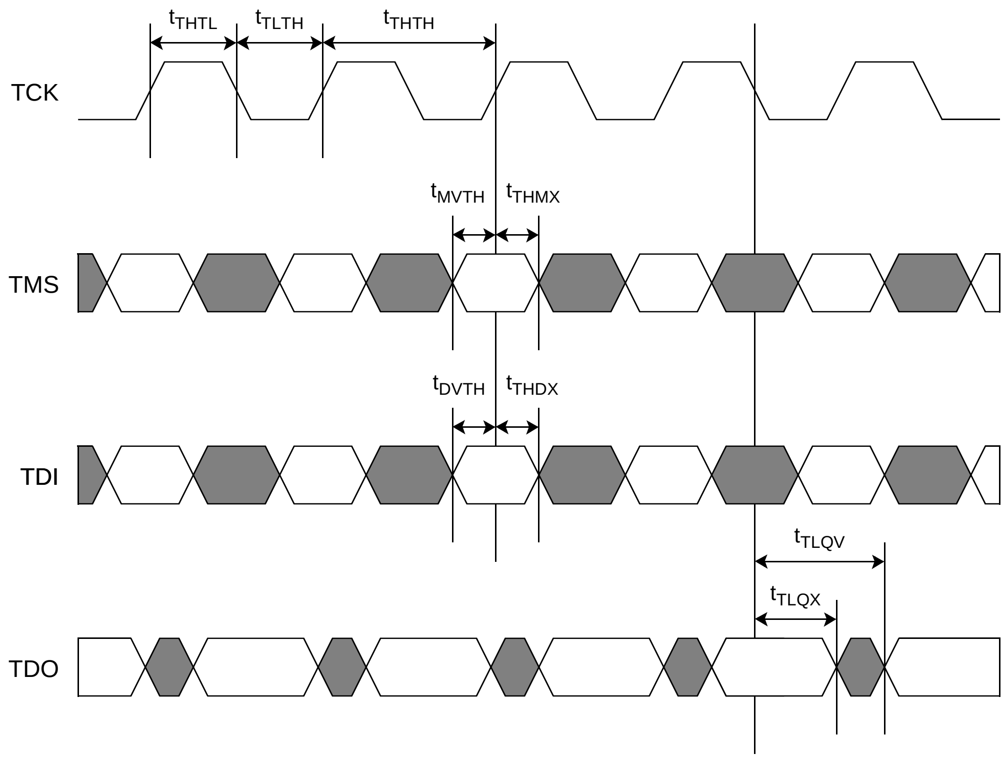
Parameter	Symbol	Conditions	Units	Notes
JTAG Input High Level	V_{TIH}	2.5	V	
JTAG Input Low Level	V_{TIL}	0.0	V	
JTAG Input Rise & Fall Time		1.0	V/ns	
JTAG Input Reference Level		1.25	V	
JTAG Output Reference Level		1.25	V	
JTAG Output Load Condition				See Fig.2 (page 11)

JTAG AC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
TCK Cycle Time	t_{THTH}	100		ns
TCK High Pulse Width	t_{THTL}	40		ns
TCK Low Pulse Width	t_{TLTH}	40		ns
TMS Setup Time	t_{MVTH}	10		ns
TMS Hold Time	t_{THMX}	10		ns
TDI Setup Time	t_{DVTH}	10		ns
TDI Hold Time	t_{THDX}	10		ns
TCK Low to TDO Valid	t_{TLQV}		20	ns
TCK Low to TDO Hold	t_{TLQX}	0		ns

JTAG Timing Diagram

Figure 6



TAP Controller

The TAP Controller is a 16-state state machine that controls access to the various TAP Registers and executes the operations associated with each TAP Instruction. State transitions are controlled by TMS and occur on the rising edge of TCK.

The TAP Controller enters the "Test-Logic Reset" state in one of two ways:

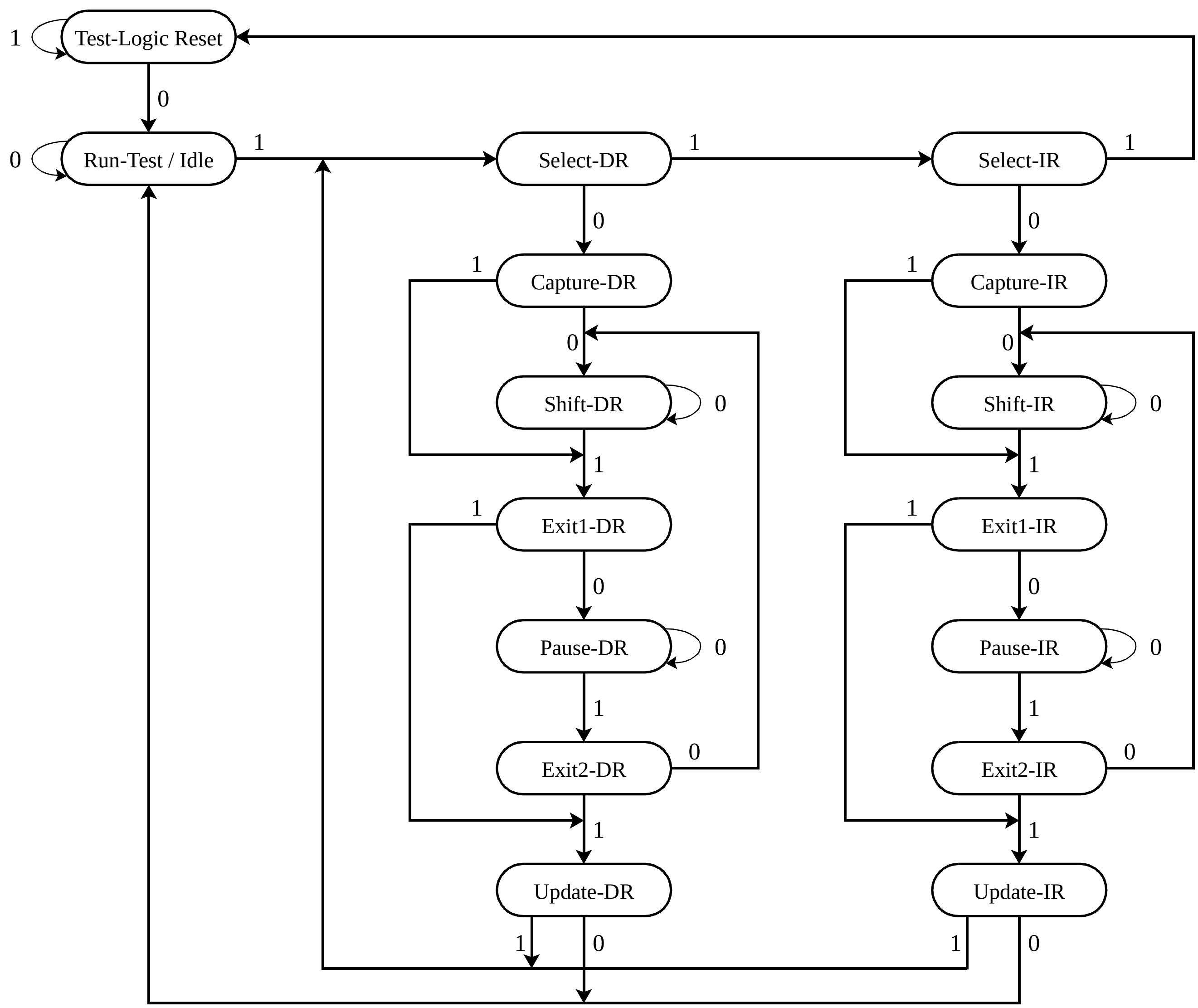
1. At power up.
2. When a logic "1" is applied to TMS for at least 5 consecutive rising edges of TCK.

The TDI input receiver is sampled only when the TAP Controller is in either the "Shift-IR" state or the "Shift-DR" state.

The TDO output driver is active only when the TAP Controller is in either the "Shift-IR" state or the "Shift-DR" state.

TAP Controller State Diagram

Figure 7



TAP Registers

TAP Registers are serial shift registers that capture serial input data (from TDI) on the rising edge of TCK, and drive serial output data (to TDO) from the falling edge of TCK. They are divided into two groups: “Instruction Registers” (IR), which are manipulated via the “IR” states in the TAP Controller, and “Data Registers” (DR), which are manipulated via the “DR” states in the TAP Controller.

Instruction Register (IR - 3 Bits)

The Instruction Register stores the various TAP Instructions supported by these devices. It is loaded with the IDCODE instruction at power-up, and when the TAP Controller is in the “Test-Logic Reset” and “Capture-IR” states. It is inserted between TDI and TDO when the TAP Controller is in the “Shift-IR” state, at which time it can be loaded with a new instruction. However, newly loaded instructions are not executed until the TAP Controller has reached the “Update-IR” state.

The Instruction Register is 3 bits wide, and is encoded as follows:

Code (2:0)	Instruction	Description
000	BYPASS	See code “111”.
001	IDCODE	Loads a predefined device- and manufacturer-specific identification code into the ID Register when the TAP Controller is in the “Capture-DR” state, and inserts the ID Register between TDI and TDO when the TAP Controller is in the “Shift-DR” state. See the ID Register description for more information.
010	SAMPLE-Z	Loads the individual logic states of all signals composing the SRAM’s I/O ring into the Boundary Scan Register when the TAP Controller is in the “Capture-DR” state, and inserts the Boundary Scan Register between TDI and TDO when the TAP Controller is in the “Shift-DR” state. Also disables the SRAM’s data output drivers. See the Boundary Scan Register description for more information.
011	PRIVATE	Do not use. Reserved for manufacturer use only.
100	SAMPLE	Loads the individual logic states of all signals composing the SRAM’s I/O ring into the Boundary Scan Register when the TAP Controller is in the “Capture-DR” state, and inserts the Boundary Scan Register between TDI and TDO when the TAP Controller is in the “Shift-DR” state. See the Boundary Scan Register description for more information.
101	PRIVATE	Do not use. Reserved for manufacturer use only.
110	PRIVATE	Do not use. Reserved for manufacturer use only.
111	BYPASS	Loads a logic “0” into the Bypass Register when the TAP Controller is in the “Capture-DR” state, and inserts the Bypass Register between TDI and TDO when the TAP Controller is in the “Shift-DR” state. See the Bypass Register description for more information.

Bit 0 is the LSB and Bit 2 is the MSB. When the Instruction Register is selected, TDI serially shifts data into the MSB, and the LSB serially shifts data out through TDO.

Bypass Register (DR - 1 Bit)

The Bypass Register is one bit wide, and provides the minimum length serial path between TDI and TDO. It is loaded with a logic “0” when the BYPASS instruction has been loaded in the Instruction Register and the TAP Controller is in the “Capture-DR” state. It is inserted between TDI and TDO when the BYPASS instruction has been loaded into the Instruction Register and the TAP Controller is in the “Shift-DR” state.

ID Register (DR - 32 Bits)

The ID Register is loaded with a predetermined device- and manufacturer-specific identification code when the IDCODE instruction has been loaded into the Instruction Register and the TAP Controller is in the “Capture-DR” state. It is inserted between TDI and TDO when the IDCODE instruction has been loaded into the Instruction Register and the TAP Controller is in the “Shift-DR” state.

The ID Register is 32 bits wide, and contains the following information:

Device	Revision Number (31:28)	Part Number (27:12)	Sony ID (11:1)	Start Bit (0)
512Kb x 36	xxxx	0000 0000 0110 1110	0000 1110 001	1
1Mb x 18	xxxx	0000 0000 0110 1111	0000 1110 001	1

Bit 0 is the LSB and Bit 31 is the MSB. When the ID Register is selected, TDI serially shifts data into the MSB, and the LSB serially shifts data out through TDO.

Boundary Scan Registers (DR - 70 Bits for x36, 51 Bits for x18)

The Boundary Scan Register is equal in length to the number of active signal connections to the SRAM (excluding the TAP pins) plus a number of place holder locations reserved for functional and/or density upgrades. It is loaded with the individual logic states of all signals composing the SRAM’s I/O ring when the SAMPLE or SAMPLE-Z instruction has been loaded into the Instruction Register and the TAP Controller is in the “Capture-DR” state. It is inserted between TDI and TDO when the SAMPLE or SAMPLE-Z instruction has been loaded into the Instruction Register and the TAP Controller is in the “Shift-DR” state.

The Boundary Scan Register contains the following bits:

512Kb x 36		1Mb x 18	
DQ	36	DQ	18
SA	19	SA	20
K, $\overline{K}$	2	K, $\overline{K}$	2
$\overline{SS}$, $\overline{SW}$, $\overline{SBW}$x	6	$\overline{SS}$, $\overline{SW}$, $\overline{SBW}$x	4
$\overline{G}$, ZZ	2	$\overline{G}$, ZZ	2
ZQ, M1, M2	3	ZQ, M1, M2	3
Place Holder	2	Place Holder	2

Note: For deterministic results, all signals composing the SRAM’s I/O ring must meet setup and hold times with respect to TCK (same as TDI and TMS) when sampled.

Note: K and $\overline{K}$ are connected to a differential input receiver that generates a single-ended input clock signal to the device. Therefore, in order to capture deterministic values for these signals in the Boundary Scan Register, they must be at opposite logic levels when sampled.

Note: When an external resistor RQ is connected between the ZQ pin and V_{SS}, the value of the ZQ signal captured in the Boundary Scan Register is non-deterministic.

Boundary Scan Register Bit Order Assignments

The table below depicts the order in which the bits are arranged in the Boundary Scan Register. Bit 1 is the LSB and bit 70 (for x36) or bit 51 (for x18) is the MSB. When the Boundary Scan Register is selected, TDI serially shifts data into the MSB, and the LSB serially shifts data out through TDO.

512Kb x 36					
Bit	Signal	Pad	Bit	Signal	Pad
1	M2	5R	36	SA	3B
2	SA	4P	37	SA	2B
3	SA	4T	38	SA	3A
4	SA	6R	39	SA	3C
5	SA	5T	40	SA	2C
6	ZZ	7T	41	SA	2A
7	DQa	6P	42	DQc	2D
8	DQa	7P	43	DQc	1D
9	DQa	6N	44	DQc	2E
10	DQa	7N	45	DQc	1E
11	DQa	6M	46	DQc	2F
12	DQa	6L	47	DQc	2G
13	DQa	7L	48	DQc	1G
14	DQa	6K	49	DQc	2H
15	DQa	7K	50	DQc	1H
16	$\overline{\text{SBW}}$a	5L	51	$\overline{\text{SBW}}$c	3G
17	$\overline{\text{K}}$	4L	52	ZQ	4D
18	K	4K	53	$\overline{\text{SS}}$	4E
19	$\overline{\text{G}}$	4F	54	NC (1)	4G
20	$\overline{\text{SBW}}$b	5G	55	NC (1)	4H
21	DQb	7H	56	$\overline{\text{SW}}$	4M
22	DQb	6H	57	$\overline{\text{SBW}}$d	3L
22	DQb	7G	58	DQd	1K
24	DQb	6G	59	DQd	2K
25	DQb	6F	60	DQd	1L
26	DQb	7E	61	DQd	2L
27	DQb	6E	62	DQd	2M
28	DQb	7D	63	DQd	1N
29	DQb	6D	64	DQd	2N
30	SA	6A	65	DQd	1P
31	SA	6C	66	DQd	2P
32	SA	5C	67	SA	3T
33	SA	5A	68	SA	2R
34	SA	6B	69	SA	4N
35	SA	5B	70	M1	3R

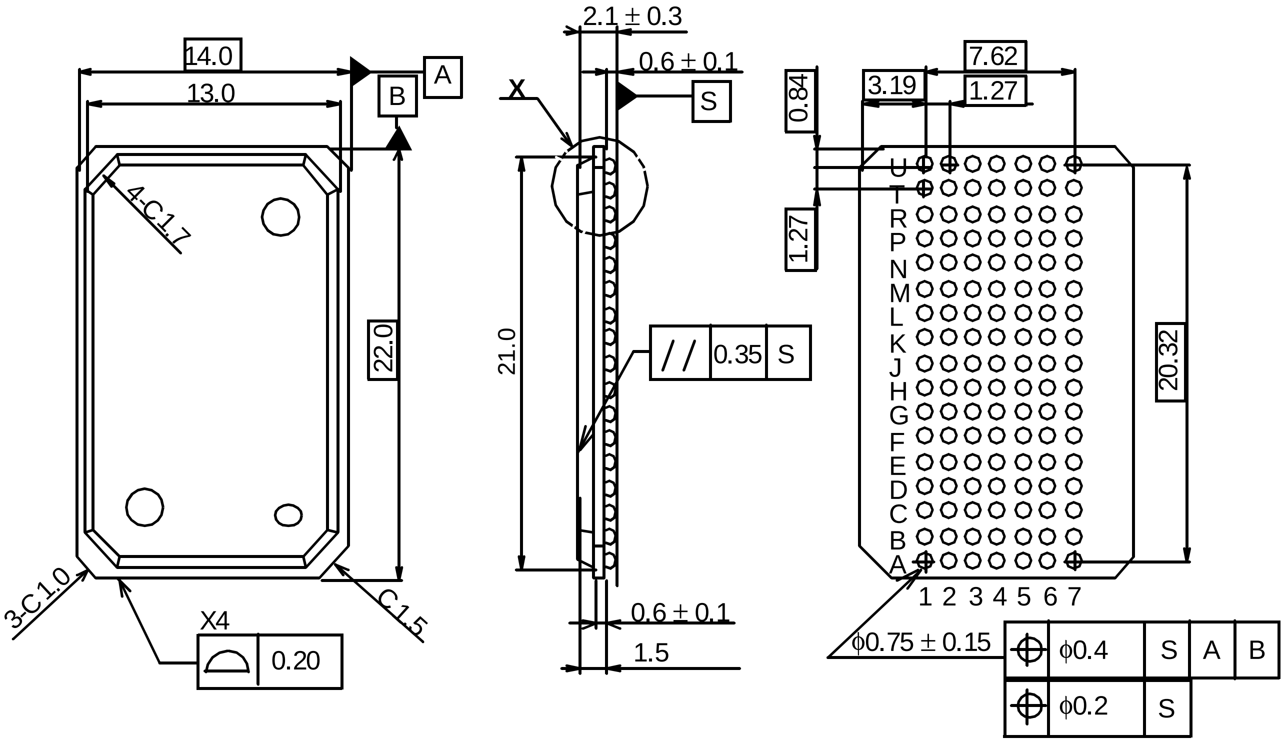
1Mb x 18					
Bit	Signal	Pad	Bit	Signal	Pad
1	M2	5R	36	$\overline{\text{SBW}}$b	3G
2	SA	6T	37	ZQ	4D
3	SA	4P	38	$\overline{\text{SS}}$	4E
4	SA	6R	39	NC (1)	4G
5	SA	5T	40	NC (1)	4H
6	ZZ	7T	41	$\overline{\text{SW}}$	4M
7	DQa	7P	42	DQb	2K
8	DQa	6N	43	DQb	1L
9	DQa	6L	44	DQb	2M
10	DQa	7K	45	DQb	1N
11	$\overline{\text{SBW}}$a	5L	46	DQb	2P
12	$\overline{\text{K}}$	4L	47	SA	3T
13	K	4K	48	SA	2R
14	$\overline{\text{G}}$	4F	49	SA	4N
15	DQa	6H	50	SA	2T
16	DQa	7G	51	M1	3R
17	DQa	6F			
18	DQa	7E			
19	DQa	6D			
20	SA	6A			
21	SA	6C			
22	SA	5C			
22	SA	5A			
24	SA	6B			
25	SA	5B			
26	SA	3B			
27	SA	2B			
28	SA	3A			
29	SA	3C			
30	SA	2C			
31	SA	2A			
32	DQb	1D			
33	DQb	2E			
34	DQb	2G			
35	DQb	1H			

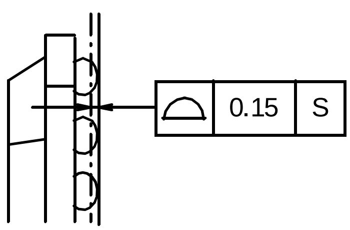
Note 1: NC pins at pad locations 4G and 4H are connected to V_{SS} internally, regardless of pin connection externally.

•Ordering Information

Part Number	V_{DD}	I/O Type	Size	Speed (Cycle Time / Data Access Time)
CXK77N36R160GB-3	1.8V or 2.5V	HSTL	512Kb x 36	3.0ns / 1.5ns
CXK77N36R160GB-33	1.8V or 2.5V	HSTL	512Kb x 36	3.3ns / 1.7ns
CXK77N36R160GB-4	1.8V or 2.5V	HSTL	512Kb x 36	4.0ns / 2.0ns
CXK77N18R160GB-3	1.8V or 2.5V	HSTL	1Mb x 18	3.0ns / 1.5ns
CXK77N18R160GB-33	1.8V or 2.5V	HSTL	1Mb x 18	3.3ns / 1.7ns
CXK77N18R160GB-4	1.8V or 2.5V	HSTL	1Mb x 18	4.0ns / 2.0ns

119 Pin BGA Package Dimensions





DETAIL A

PACKAGE STRUCTURE

SONY CODE	BGA-119P-021
EIAJ CODE	BGA119-P-1422
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
BORAD TREATMENT	COPPER-CLAD LAMINATE
LEAD MATERIAL	SOLDER
PACKAGE MASS	1.1g

•Revision History

Rev. #	Rev. Date	Description of Modification
rev 0.0	02/15/02	Initial Version
rev 0.1	03/13/02	1. Changed nominal V_{DD} from 2.5V to 1.8V. Updated parameters associated with V_{DD} accordingly. 2. Changed nominal V_{DDQ} from 1.8V to 1.5V. Updated parameters associated with V_{DDQ} accordingly.
rev 0.2	11/01/02	1. Added 2.5V nominal V_{DD}. Updated parameters associated with V_{DD} accordingly. 2. Added 1.8V nominal V_{DDQ}. Updated parameters associated with V_{DDQ} accordingly.
rev 0.3	11/26/02	1. Modified I/O Capacitance section (p. 6). C_{IN} 3.5pF to 4.0pF C_{KIN} 3.5pF to 4.5pF C_{OUT} 4.5pF to 5.0pF 2. Modified DC Electrical Characteristics section (p. 8). I_{DD-3} 660mA to 550mA I_{DD-33} 600mA to 500mA I_{DD-4} 500mA to 450mA I_{SB} 130mA to 160mA Removed I_{DD2} specification.